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Thermal Modeling and Design Optimization of PCB Vias and Pads

Yanfeng Shen, *Member, IEEE*, Huai Wang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, Hui Zhao, *Member, IEEE*, and Teng Long, *Member, IEEE*

***Abstract*— Miniature power semiconductor devices mounted on printed circuit boards (PCBs) are normally cooled by means of PCB vias, copper pads, and/or heatsinks. Various reference PCB thermal designs have been provided by semiconductor manufacturers and researchers. However, the recommendations are not optimal, and there are some discrepancies among them, which may confuse electrical engineers. This paper aims to develop analytical thermal resistance models for PCB vias and pads, and further to obtain the optimal design for thermal resistance minimization. Firstly, the PCB via array is thermally modeled in terms of multiple design parameters. A systematic parametric analysis leads to an optimal trajectory for the via diameter at different PCB specifications. Then an axisymmetric thermal resistance model is developed for PCB thermal pads where the heat conduction, convection and radiation all exist; due to the interdependence between the conductive/radiative heat transfer coefficients and the board temperatures, an algorithm is proposed to fast obtain the board-ambient thermal resistance and to predict the semiconductor junction temperature. Finally, the proposed thermal models and design optimization algorithms are verified by computational fluid dynamics (CFD) simulations and experimental measurements.**

***Index terms*— thermal resistance model, thermal management, printed circuit board (PCB), PCB via, thermal pad.**

NOMENCLATURE

Bi	*Biot number*
h	Heat transfer coefficient (W/(m^2·K))
h_{conv}	Convective heat transfer coefficient (W/(m^2·K))
h_{radi}	Radiative heat transfer coefficient (W/(m^2·K))
k	Thermal conductivity of a material (W/(m·K))
k_1	Lateral thermal conductivity of the copper zone (W/(m^2·K))
k_2	Lateral thermal conductivity of the FR4 zone (W/(m^2·K))
k_{Cu}	Thermal conductivity of copper (W/(m^2·K))
k_{FR4}	Thermal conductivity of FR4 (W/(m^2·K))
k_{filler}	Thermal conductivity of via filling material (W/(m^2·K))
l	Length of a via array (m)
L_c	Characteristic length of a hot plate (m)
m_1	Number of rows of a via array in *Pattern I*
m_2	Number of rows of a via array in *Pattern II*
n_1	Number of columns of a via array in *Pattern I*
n_2	Number of columns of a via array in *Pattern II*
N_{Cu}	Number of copper layers in a PCB
P	Power loss generated by a heat source (W)
q	Heat flux (W/m^2)
r_b	Radius of heat source (package) (m)
r_s	Radius of middle (copper) zone (m)
r_e	Radius of outer (FR4) zone (m)
s	Via-to-via spacing (m)
t	PCB thickness(m)
t_{Cu}	Thickness of a PCB copper layer (m)
t_{PTH}	Plating thickness of PCB vias (m)
T_b	PCB board ($r = r_b$) temperature (°C)
T_c	Case temperature of a package (chip) (°C)
T_j	Junction temperature of a chip (°C)
T_t	Top case temperature of a package (chip) (°C)
T_a	Ambient temperature (°C)
w	Width of a via array (m)
ε	Emissivity of PCB surface
Θ_{ba}	Thermal resistance from the inner zone edge ($r = r_b$) to the ambient (°C/W)
Θ_{barrel}	Vertical thermal resistance of the copper barrel in a via unit (°C/W)
Θ_{cb}	Thermal resistance from the case to the PCB ($r = r_b$) (°C/W)
Θ_{unit}	Vertical thermal resistance of a via unit (°C/W)
Θ_{Cu}	Vertical thermal resistance of the copper layers in a via unit (°C/W)
Θ_{filler}	Vertical thermal resistance of the filler in a via unit (°C/W)
Θ_{FR4}	Vertical thermal resistance of the FR4 layers in a via unit (°C/W)
Θ_{jc}	Thermal resistance from the junction to the case (°C/W)
Θ_{jt}	Thermal resistance from the junction to the top case (°C/W)
$\Theta_{r,ij}$	Radial thermal resistance between outer-zone via layers (°C/W)
Θ_{sa}	Thermal resistance from the copper zone edge ($r = r_s$) to the ambient (°C/W)

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Θ_{ta} Thermal resistance from the top case of the chip to the ambient (°C/W)
Θ_{via} Vertical thermal resistance of a via array (°C/W)
$\Theta_{via,n}$ Normalized vertical thermal resistance of a via array
$\Theta_{v,ij}$ Vertical thermal resistance between copper layers of outer-zone vias (°C/W)
λ Convective heat transfer parameter depending on PCB geometry and orientation
σ Stefan-Boltzmann constant $\sigma = 5.670367\times10^{-8}$ ($W\cdot m^{-2}\cdot K^{-4}$)
τ Time (s)
ϕ Via diameter (m)
ϕ_{opt} Optimal via diameter (m)
ψ_{ea} Equivalent thermal resistance from the FR4 zone edge ($r = r_e$) to the ambient (°C/W)
ψ_{sa} Equivalent thermal resistance from the copper zone edge ($r = r_s$) to the ambient (°C/W)
ψ_{ta} Equivalent thermal resistance from the top case of a package to the ambient (°C/W)

I. Introduction

The volume of modern power semiconductor devices (e.g., GaN transistors) are continuingly shrinking in order to achieve higher power densities, lower parasitic inductances, and lower power losses [1]-[3]. However, thermal management has been identified as the main barrier for further power density increase [4]. The heat generated inside the miniaturized semiconductors must be effectively dissipated to the ambient; otherwise, the high junction and board temperatures may cause serious reliability issues to the semiconductor, solder, thermal grease, and printed circuit board (PCB) [5]-[8]. In addition, suitable heat dissipation measures should be considered as early as in the design and development phase, because subsequent modifications are generally more costly and involve increased engineering effort [9], [10].

In medium power applications, the surface-mounted devices (SMDs) are normally cooled by a heatsink attached to the PCB, where the thermal via array provides an effective thermal path for the heat transfer [11]-[13]. In low power scenarios, a PCB copper pad is typically used for heat spreading, and the SMD can be cooled by natural convection [14]. Many reference thermal designs can be found from device manufacturers' websites [14]-[18]. However, several problems remain:

1) the thermal design guidelines recommended by manufacturers are not optimal, and they are applicable for specific packages only [15], [16];
2) inconsistent guidelines; for instance, the thermal via diameter should be designed as large to reduce the thermal resistance according to [16]; however, [15], [17] and [18] recommend smaller via diameters and adopt different via pitches.

Although the computational fluid dynamics (CFD) simulations feature high accuracy, the model generation time and computational cost could be fairly high [14]. Moreover, CFD simulators are expensive and they are not always available for electrical engineers. Therefore, it is necessary to develop analytical models which enable fast and accurate design optimization for thermal vias and pads.

In the literature, many efforts have been devoted to the optimization of PCB thermal vias. The research in [19]-[21] is based on either experimental results or CFD simulations; thus, not all design scenarios are explored, but only some general design guidelines are provided for specific applications. Analytical thermal models of vias are built in [11], [22]-[25]; unfortunately, only partial parameters are analyzed, and no optimal via design is derived.

For the PCB heat transfer characteristics, the heat conduction, convection and radiation all exist, which makes the thermal analysis complicated. Texas Instruments have developed an online PCB thermal calculation tool based on CFD thermal resistance data of different package sizes and pad dimensions [26]. However, some important factors (e.g., the PCB thickness, number of copper layers, and copper thickness) are not taken into account, and also the online tool does not support design optimization. In addition to the CFD simulations, some other numerical calculation methods are developed [27], [28]. The study in [28] deals with a substrate for a ball grid array package, where a belt of densely populated vias and two continuous copper layers are placed; however, the model is complicated and no CFD or experimental verifications are provided. For electrical engineers, it is more desirable to have an analytical thermal model such that the temperatures of devices with different designs and cooling methods can be fast predicted [29], [30]. In [14] and [31], an analytical thermal resistance model is developed for PCB thermal pads; however, the heat transfer boundary and the convective heat transfer coefficient variation over the temperature difference are not included, causing potential errors between calculations and measurements.

This paper proposed two new analytical thermal models for PCB vias and thermal pads, respectively. For the thermal model of PCB vias, a systematic parametric analysis is firstly conducted, which leads to a simplified thermal resistance model. An optimal design trajectory is then obtained for PCB vias with different specifications. After that, an analytical axisymmetric thermal resistance model is proposed for PCB thermal pads. Taking into account the interdependence between the convection/radiative heat transfer coefficients and board temperatures, a simple algorithm is developed to size thermal pads at different PCB parameters, power losses, ambient temperatures, and allowed maximum junction temperatures. Finally, CFD simulations and experimental measurements verify the developed analytical thermal models. The proposed models enable electrical engineers to optimize their PCB via design and thermal pad sizing at lower cost and less time effort.

II. Thermal Modeling and Design Optimization of PCB Vias

A. Thermal Modeling of PCB Vias

A cluster of PCB plated through holes (PTHs), i.e., vias, can provide an effective thermal path, which helps to transfer heat from an SMD (chip) to a heatsink. The vertical structure of a multilayer PCB with vias is shown in Fig. 1(a). The via diameter, via-to-via spacing, and via plating thickness are denoted as ϕ, s, and t_{PTH}, respectively. The number of copper layers and the copper layer thickness are represented by N_{Cu} and t_{Cu}, respectively.

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For the layout of vias, there are various uniform and non-uniform design options. For the sake of simplicity, this paper focuses on two simple uniform patterns, denoted as *Pattern I* and *Pattern II*, as illustrated in Fig. 1(b) and (c), respectively. However, the derived method can be applied to other vias layout with minor modifications. The length, width, and thickness of the PCB via array are denoted as l, w, and t, respectively. Normally, the PCB thickness is much smaller than its length and width. Also, the attached heatsink has a large heat dissipation capability. Therefore, it is assumed that the heat generated inside the SMD is transferred in the vertical direction only. Accordingly, the PCB via array in each pattern can be divided into multiple via units, as indicated by the dashed box in Fig. 1. It is seen from the horizontal cross-sections of the via array that the basic via unit in *Pattern I* is a square of $(\phi + s) \times (\phi + s)$, whereas that in *Pattern II* is rectangular with $[\sqrt{3}(\phi + s)/2] \times (\phi + s)$. If the PCB via array size (l and w) and via parameters (ϕ and s) are fixed, and the array parameters (l and w) are much larger than the via unit parameters (ϕ and s), then the numbers of vias that *Patterns I* and *II* can accommodate are calculated as

$$\begin{cases} m_1 \times n_1 = \text{floor}[l/(\phi+s)] \times \text{floor}[w/(\phi+s)] \\ \qquad \approx lw/[(\phi+s)^2], & \text{Pattern I} \\ m_2 \times n_2 = \text{floor}[l/(\phi+s)] \times \text{floor}\{2w/[\sqrt{3}(\phi+s)]\} \\ \qquad \approx 2lw/[\sqrt{3}(\phi+s)^2], & \text{Pattern II} \end{cases} \tag{1}$$

It is seen from (1) that *Pattern II* can accommodate approximately $2/\sqrt{3} - 1 = 15.5\%$ more vias than *Pattern I*.

As can be seen from Fig. 1, there are three vertical thermal paths for each via unit, i.e., the via filler, the via barrel, and the copper and flame retardant 4 (FR4) layers, whose vertical thermal resistances are represented by Θ_{barrel}, Θ_{filler}, and $\Theta_{Cu} + \Theta_{FR4}$, respectively, as below

$$\begin{aligned} \Theta_{filler} &= \frac{t}{k_{filler}\pi(\phi/2 - t_{PTH})^2}, \\ \Theta_{barrel} &= \frac{t}{k_{Cu}\pi t_{PTH}(\phi - t_{PTH})}, \\ \Theta_{Cu} + \Theta_{FR4} &= \left(\frac{N_{Cu}t_{Cu}}{k_{Cu}} + \frac{t - N_{Cu}t_{Cu}}{k_{FR4}}\right) \\ &\quad \times \begin{cases} \dfrac{1}{(\phi+s)^2 - \pi\phi^2/4}, & \text{Pattern I} \\ \dfrac{1}{\sqrt{3}(\phi+s)^2/2 - \pi\phi^2/4}, & \text{Pattern II} \end{cases} \end{aligned} \tag{2}$$

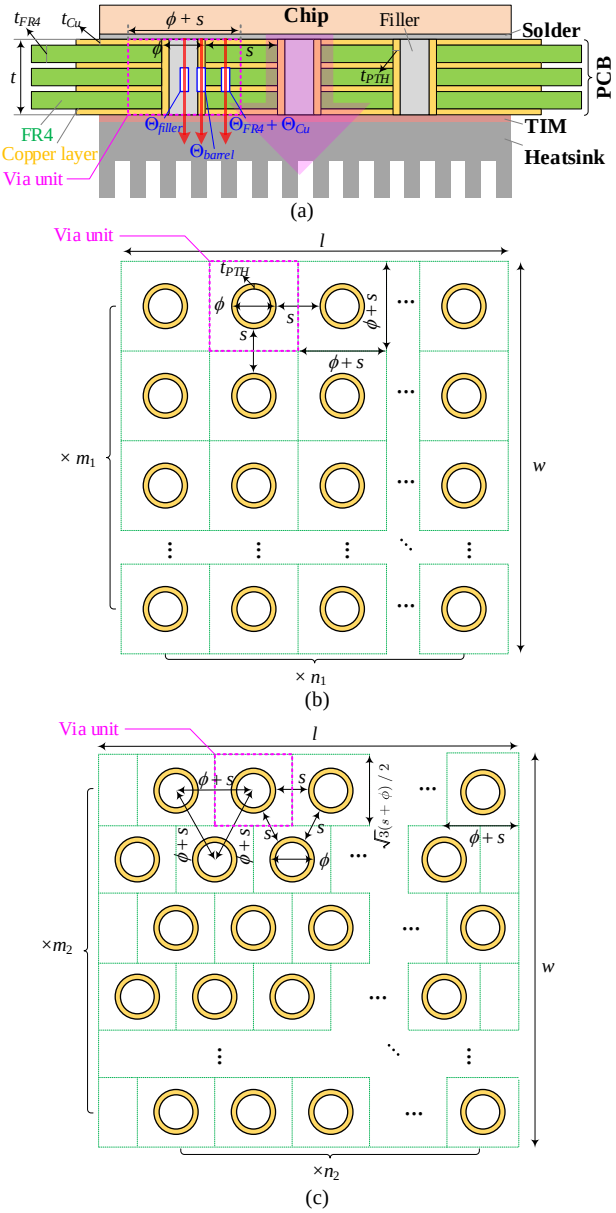

Fig. 1. Structure and layout of PCB via array. (a) Vertical structure of a multilayer PCB with vias. Top view of via array in (b) *Pattern I* and (c) *Pattern II*.

where k_{filler}, k_{Cu} and k_{FR4} represent the thermal conductivities of via filling material, copper, and FR4, respectively. Thus, the vertical thermal resistance of a via unit can be calculated as

$$\begin{aligned} \Theta_{unit} &= \Theta_{filler} \,||\, \Theta_{barrel} \,||\, (\Theta_{Cu} + \Theta_{FR4}) \\ &\Rightarrow \begin{cases} \Theta_{unit,I} = \dfrac{1}{\underbrace{\dfrac{k_{filler}\pi(\phi/2 - t_{PTH})^2}{t}}_{1/\Theta_{filler}} + \underbrace{\dfrac{k_{Cu}\pi t_{PTH}(\phi - t_{PTH})}{t}}_{1/\Theta_{barrel}} + \underbrace{\dfrac{(\phi+s)^2 - \pi\phi^2/4}{N_{Cu}t_{Cu}/k_{Cu} + (t - N_{Cu}t_{Cu})/k_{FR4}}}_{1/(\Theta_{Cu}+\Theta_{FR4})}}, & \text{Pattern I} \\ \Theta_{unit,II} = \dfrac{1}{\underbrace{\dfrac{k_{filler}\pi(\phi/2 - t_{PTH})^2}{t}}_{1/\Theta_{filler}} + \underbrace{\dfrac{k_{Cu}\pi t_{PTH}(\phi - t_{PTH})}{t}}_{1/\Theta_{barrel}} + \underbrace{\dfrac{\sqrt{3}(\phi+s)^2/2 - \pi\phi^2/4}{N_{Cu}t_{Cu}/k_{Cu} + (t - N_{Cu}t_{Cu})/k_{FR4}}}_{1/(\Theta_{Cu}+\Theta_{FR4})}}, & \text{Pattern II} \end{cases} \end{aligned} \tag{3}$$

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From the perspective of vertical heat transfer, the via units are equivalently connected in parallel, and therefore the total vertical thermal resistances of a via array of $l \times w \times t$ can be obtained as

$$\Theta_{via} = \begin{cases} \dfrac{\Theta_{unit,I}}{m_1 \times n_1}, & \text{Pattern I} \\ \dfrac{\Theta_{unit,II}}{m_2 \times n_2}, & \text{Pattern II} \end{cases} \tag{4}$$

To simplify the following theoretical analysis, the thermal resistance of a via array is normalized based on the thermal resistance of an FR4 pad with the same size ($l \times w \times t$), yielding (5).

$$\Theta_{via,n} = \frac{\Theta_{via}}{\dfrac{t}{k_{FR4} l w}} = \begin{cases} \dfrac{4(s+\phi)^2 k_{FR4}}{\underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{filler} + \underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{barrel} + \underbrace{\dfrac{t[4s^2 + 8s\phi + (4-\pi)\phi^2]}{N_{Cu}t_{Cu} / k_{Cu} + (t - N_{Cu}t_{Cu}) / k_{FR4}}}_{copper\ and\ FR4\ layers}}, & \text{Pattern I} \\ \dfrac{2\sqrt{3}(s+\phi)^2 k_{FR4}}{\underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{filler} + \underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{barrel} + \underbrace{\dfrac{t[2\sqrt{3}(s+\phi)^2 - \pi\phi^2]}{N_{Cu}t_{Cu} / k_{Cu} + (t - N_{Cu}t_{Cu}) / k_{FR4}}}_{copper\ and\ FR4\ layers}}, & \text{Pattern II} \end{cases} \tag{5}$$

B. Parametric Analysis and Design Optimization of PCB Vias

TABLE I
THERMAL CONDUCTIVITIES OF MATERIALS AT 25 °C [33]-[36]

Material	Copper	SnAgCu solder	FR4		Air at atmospheric pressure
			Through-plan	In-plane	
Thermal conductivity	393 W/(m·K)	57.3 W/(m·K)	0.29 W/(m·K)	0.81 W/(m·K)	0.026 W/(m·K)

Since multiple design variables are included in the thermal resistance model, it is difficult to directly apply (5) in practical design optimization. Hence, it is necessary to conduct a parametric analysis on (5).

The thermal conductivity of a material is a measure of its ability to conduct heat. It is evaluated primarily in terms of the Fourier's law for heat conduction. The general equation for thermal conductivity is [32] $k = -q / \nabla T$, where q is the heat flux (W/m^2) and ∇T represents the temperature gradient (K/m). The thermal conductivities of the materials used in this paper are listed in Table I. The standard IPC-6012 specifies a minimum copper plating thickness of 20 μm for Class 1 PCBs, and 25 μm is a standard via plating thickness [37]. Thus, t_{PTH} = 25 μm is used in the following analysis.

1) Via-to-Via Spacing s

Based on (5), the curves of the normalized via thermal resistance with respect to the via-to-via spacing s can be depicted for different filler materials, PCB thicknesses, and via diameters, as shown in Fig. 2. It is seen that the normalized via thermal resistance $\Theta_{via,n}$ always rises when the via-to-via spacing s increases, regardless of the PCB thickness, via filling material and via diameter. Therefore, s should be designed as small as possible in order to reduce the thermal resistance of PCB via array. In practice, however, the allowed minimum via-to-via spacing depends on PCB manufacturing capability and is cost sensitive. Generally, 8 mil (0.2 mm) is a commonly-specified minimum via-to-via spacing by most PCB manufacturers, and therefore, s = 0.2 mm is used in the following analysis and experiments.

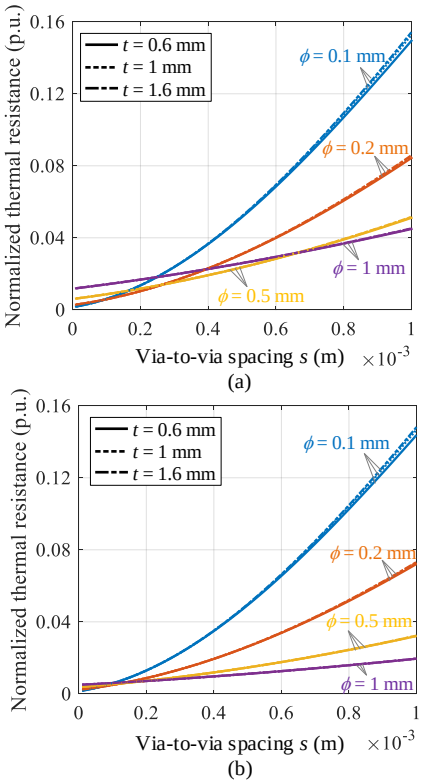

Fig. 2. Dependence of the normalized thermal resistance of via array in *Pattern I* on the via-to-via spacing s with two via filling materials: (a) air with a thermal conductivity of 0.026 W/(m·K), and (b) solder with a thermal conductivity of 57.3 W/(m·K).

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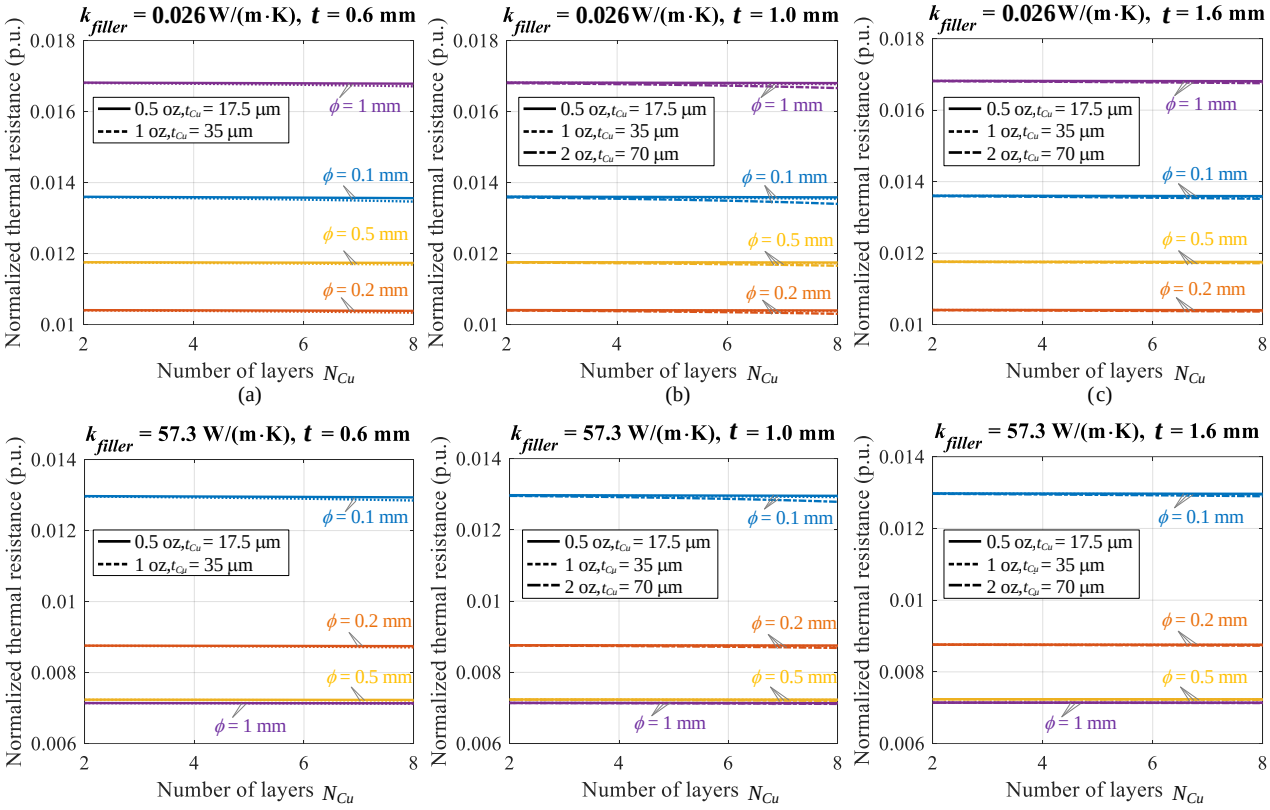

Fig. 3. Dependence of the normalized thermal resistance of via array in *Pattern I* on the number of copper layers N_{Cu}, copper thickness t_{Cu}, and PCB thickness t with different via filling materials. (a) Air with thermal conductivity k_{filler} = 0.026 W(m·K) and PCB thickness t = 0.6 mm; (b) Air with thermal conductivity k_{filler} = 0.026 W(m·K), PCB thickness t = 1.0 mm; (c) Air with thermal conductivity k_{filler} = 0.026 W(m·K), PCB thickness t = 1.6 mm; (d) Solder with thermal conductivity k_{filler} = 57.3 W(m·K), PCB thickness t = 0.6 mm; (e) Solder with thermal conductivity k_{filler} = 57.3 W(m·K), PCB thickness t = 1.0 mm; (f) Solder with thermal conductivity k_{filler} = 57.3 W(m·K), PCB thickness t = 1.6 mm.

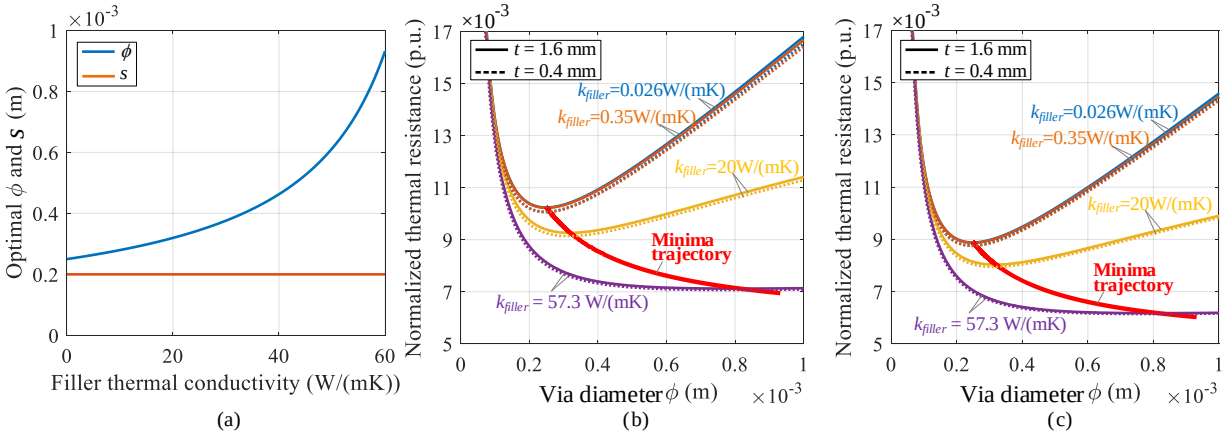

Fig. 4. (a) Optimal trajectories of via diameter ϕ and via-to-via spacing s with respect to the filler thermal conductivity. Dependence of the normalized thermal resistance of via array on the diameter ϕ at different PCB thicknesses and filler thermal conductivities for (b) *Pattern I* and (c) *Pattern II*.

2) Number of layers N_{Cu}, PCB Thickness t, and Copper Layer Thickness t_{Cu}

The dependence of the normalized thermal resistance of a PCB via array, $\Theta_{via,n}$, on the number of copper layers N_{Cu}, copper thickness t_{Cu}, and PCB thickness t is shown in Fig. 3. As can be seen, the parameters N_{Cu}, t_{Cu} and t, have a negligible impact on the normalized thermal resistance, implying that the copper and FR4 layers have a much higher thermal resistance compared to the vias. Thus the heat is mainly transferred through the vias, and (5) can be simplified as

$$\Theta_{via,n} \approx \begin{cases} \dfrac{4(s+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & Pattern\ I \\ \dfrac{2\sqrt{3}(s+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & Pattern\ II \end{cases} \quad (6)$$

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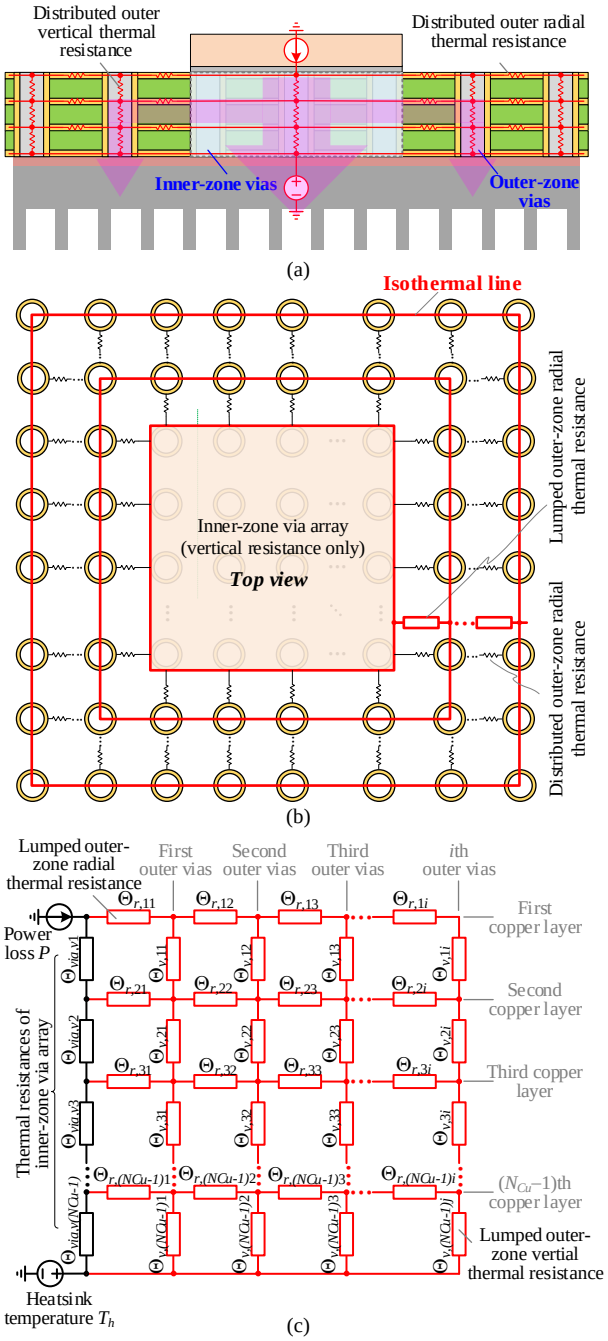

Fig. 5. Thermal resistances of outer-zone vias. (a) Vertical structure of a multilayer PCB with both inner- and outer-zone vias and a large heatsink. (b) Top view of inner- and outer-zone vias. The red lines represents the isothermal lines, and the distributed outer-zone radial thermal resistances are lumped together. (c) Equivalent thermal resistance network of the PCB with both inner- and outer-zone vias.

With the same area for the via array, the thermal resistance of *Pattern II* is about $\sqrt{3}/2 = 86.6\%$ of that in *Pattern I*. From (6), we can also obtain the optimal via diameter for both patterns, which can achieve the minimum thermal resistance, i.e.,

$$\phi_{opt} = \frac{2t_{PTH}(s+2t_{PTH})(k_{Cu}-k_{filler})}{2t_{PTH}(k_{Cu}-k_{filler})-k_{filler}s}, \text{ Patterns I \& II} \quad (7)$$

According to (7), the optimal trajectory of the via diameter ϕ with respect to the filler thermal conductivity can be depicted, as shown in Fig. 4(a). Then, the dependence of the normalized thermal resistance on the via diameter ϕ and the filler material is illustrated in Fig. 4(b) and (c). For each filler material, there is an optimal via diameter which can achieve the minimum thermal resistance; the minima trajectories are also depicted in Fig. 4. When the vias are not filled, the optimal via diameter is about 0.25 mm; if ϕ = 0.8 mm is chosen, then there will be a 44% increase in the thermal resistance. When the vias are filled up with SnAgCu solder (k_{filler} = 57.3 W/mK), then the optimal via diameter is about 0.8 mm; if ϕ = 0.2 mm is chosen, then there will be a 23% increase in the thermal resistance.

Ref [16] uses SnAgCu solder as the filler material of vias, and therefore recommends large via diameters. By contrast, [15], [17] and [18] recommend smaller via diameters (0.3 mm, 0.2 mm, and 0.33 mm, respectively) for unfilled vias. Also, the via-to-via spacing values in [15], [17] and [18] are designed as 0.34 mm, 1 mm, and 0.34 mm, respectively. Compared with the recommended designs in [15], [17] and [18], the thermal resistance of a via array with the proposed optimal trajectories (see Fig. 4) can be reduced by 47%, 89.5%, and 46.4%, respectively.

C. Modeling of Outer-Zone Vias

In some cases, the heatsink is larger than the chip, and thus the outer-zone vias can be added around the inner via array to further decrease the equivalent thermal resistance between the case and the heatsink, as shown in Fig. 5. For the sake of simplicity, only via *Pattern I* is considered herein. The PCB vias can be divided into two zones, i.e., the inner-zone via array directly beneath the chip, and the outer-zone vias around the inner-zone via array, as illustrated in Fig. 5(a) and (b).

1) Lumped Thermal Resistance Model

Since there is a uniform heat source on the inner via array, and a powerful heatsink beneath the PCB, the radial-direction heat transfer of the inner-zone via array is not pronounced compared with the vertical direction. Therefore, only the vertical thermal resistance is considered for the inner-zone via array, and it is divided into N_{Cu}–1 parts which represent the thermal resistances between the N_{Cu} copper layers. As for the outer-zone vias, the radial and vertical heat transfers are equally pronounced. Hence, both the distributed radial and vertical thermal resistances are taken into account, as shown in Fig. 5(a).

It is assumed that the lateral boundary of the inner-zone via array is isothermal. Also, multilayer outer-zone vias are evenly placed around the inner-zone via array, as shown in Fig. 5(b). It implies that each layer (in the radial direction) of the outer-zone vias can be also regarded isothermal, as indicated by the red lines in Fig. 5(b). Then the distributed outer radial and vertical thermal resistances can be lumped together, yielding an equivalent thermal resistance network, as shown in Fig. 5(c).

By applying the similar principle as in Section II-A, the lumped outer-zone radial and vertical thermal resistances, i.e., $\Theta_{r,ij}$ and $\Theta_{v,ij}$, can be obtained as

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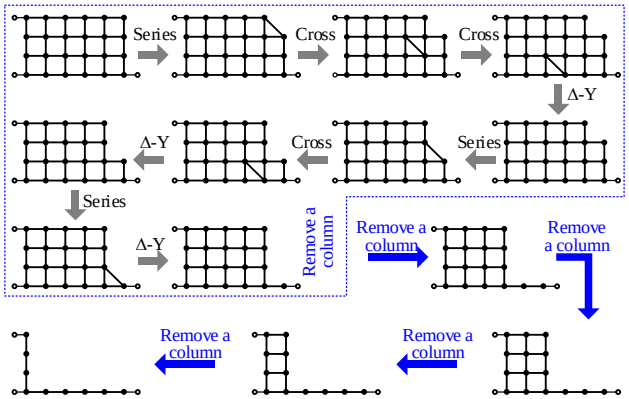

Fig. 6. Simplification of a three-terminal thermal resistance grid network. Each thick solid line represents a resistor. The terms "Series", "Δ-Y" and "Cross" represent the series transformation, Δ-Y transformation, and cross transformation of resistor network, respectively.

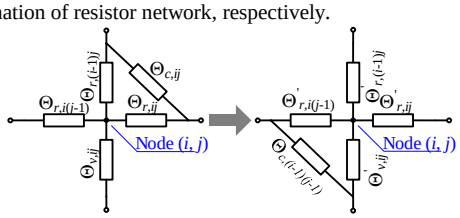

Fig. 7. Schematic of the cross transformation of a four-terminal resistor network unit. The cross transformation can be decoupled into a Δ-Y transformation and a Y-Δ transformation. $\Theta_{r,i(j-1)}$, $\Theta_{r,ij}$, $\Theta_{v,(i-1)j}$, $\Theta_{v,ij}$ and $\Theta_{c,ij}$ represent the original thermal resistance, whereas $\Theta'_{r,i(j-1)}$, $\Theta'_{r,ij}$, $\Theta'_{v,(i-1)j}$, $\Theta'_{v,ij}$ and $\Theta_{c,(i-1)(j-1)}$ denote the corresponding thermal resistances after the cross transformation.

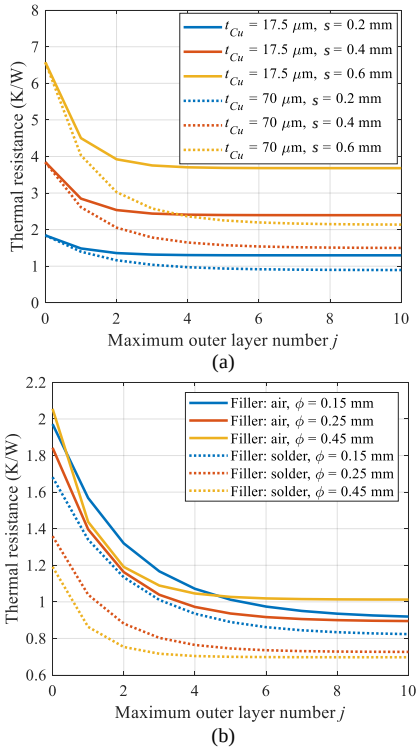

Fig. 8. Characteristics of thermal resistance of PCB vias with respect to the maximum layer number j of outer-zone vias at different parameters. The PCB length l = 5.6 mm, width w = 5.6 mm, thickness t = 1.6 mm, and the number of copper layers N_{Cu} = 4. (a) Fixed parameters: via diameter ϕ = 0.25 mm, and filler material is air; variables: copper layer thickness t_{Cu}, via-to-via spacing s, and the maximum outer layer number j. (b) Fixed parameters: t_{Cu} = 70 μm, s = 0.2 mm; variables: filler material, via diameter ϕ, and the maximum outer layer number j.

$$\begin{cases} \Theta_{r,ij} = \dfrac{\phi + s}{k_{Cu} t_{Cu}[2(l+w) + 4(2j-1)(\phi+s)]} \\ \Theta_{v,ij} = \dfrac{4(t_{Cu} + t_{FR4})\left(\dfrac{2(l+w)}{\phi+s} + 4(2j-1)\right)^{-1}}{\pi \;\; k_{filler}(\phi - 2t_{PTH})^2 + 4k_{Cu} t_{PTH}(\phi - t_{PTH})} \end{cases} \quad (8)$$

where i represents the copper layer order, and j denotes the outer via layer order.

Meanwhile, it is observed from (8) that both the radial and vertical outer-zone thermal resistances are functions of j, implying the two types of thermal resistances vary with respect to the outer via layer number. Therefore, the thermal resistances of the network shown in Fig. 5(c) are not identical.

2) *Derivation of Equivalent Thermal Resistance*

The equivalent thermal resistance of the complicated network shown in Fig. 5(c) can be derived by performing analog circuit simulations with given radial and vertical thermal resistance values as (8). However, there are multiple design variables (e.g., ϕ, s, j) and system parameters (l, w, t_{Cu}, k_{filler}, t_{PTH}, N_{Cu}, t), which implies that the method of circuit simulation does not support systematical parametric analysis. Hence, a simplification method consisting of various steps of network transformations is proposed to derive the equivalent thermal resistance of Fig. 5(c), as illustrated in Fig. 6. Apart from the basic series and Δ-Y transformations, a new transformation termed as *cross transformation* is introduced in this paper, as shown in Fig. 7. The cross transformation can be decoupled into a Δ-Y transformation and a Y-Δ transformation. As shown in Fig. 7, the resulting resistances after a cross transformation can be expressed by

$$\begin{cases} \Theta'_{r,ij} = \dfrac{\Theta_{r,ij}\Theta_{c,ij}}{\Theta_{r,ij} + \Theta_{v,ij} + \Theta_{c,ij}}, \\ \Theta'_{v,ij} = \dfrac{\Theta_{v,ij}\Theta_{c,ij}}{\Theta_{r,ij} + \Theta_{v,ij} + \Theta_{c,ij}} \\ \Theta'_{r,i(j-1)} = \Theta_{r,i(j-1)} + \Theta_o(1 + \Theta_{r,i(j-1)} / \Theta_{v,(i-1)j}) \\ \Theta'_{v,(i-1)j} = \Theta_{v,(i-1)j} + \Theta_o(1 + \Theta_{v,(i-1)j} / \Theta_{r,i(j-1)}) \\ \Theta_{c,(i-1)(j-1)} = \Theta_{v,(i-1)j} + \Theta_{r,i(j-1)}(1 + \Theta_{v,(i-1)j} / \Theta_o) \end{cases} \quad (9)$$

where $\Theta_o = \Theta_{v,ij}\Theta_{r,ij} / (\Theta_{r,ij} + \Theta_{v,ij} + \Theta_{c,ij})$.

Multiple transformations of a thermal resistance grid network give rise to lengthy and unwieldy expressions. Therefore, a simple algorithm is developed in MATLAB to obtain the final equivalent thermal resistance of the complicated network (Fig. 5(c)) with any values.

3) *Parametric Analysis*

Based on the proposed thermal resistance model for outer-zone vias, the dependence of the ultimate thermal resistance of PCB vias on multiple design variables and parameter is plotted in Fig. 8. If the maximum outer via layer number equals 0, then it means that there are only inner-zone vias. It is seen from Fig. 8 that the thermal resistance decreases with the increase of the outer via layer number. However, the thermal resistance reduction becomes insignificant when the outer via layer number exceeds a certain range, e.g., [2, 4]. It is also observed that the thermal resistance is always

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inversely proportional to the via-to-via spacing *s*; thus, *s* should be designed possibly small. According to Fig. 8(b), one can conclude that the filler material and via diameter affect the thermal resistance as well. In the case of air filling, the optimal diameter is 0.25 mm. In the case of solder as filler material, the via diameter should be designed larger to decrease the thermal resistance.

III. Thermal Modeling and Sizing of PCB Pads

For the natural convection in the air, the flow remains laminar when the temperature difference involved is less than 100 °C and the characteristic length of the body is less than 0.5 m [38], which is almost always the case in electronic systems. Therefore, the airflow in the following analysis is assumed to be laminar. The natural convection heat transfer coefficient for laminar flow of air at atmospheric pressure, h_{conv}, and the radiation heat transfer coefficient h_{radi} are [38]

$$\begin{cases} h_{conv} = \lambda[(T_x - T_a)/L_c]^{0.25} \\ h_{radi} = \varepsilon\sigma[(T_x + 273)^2 + (T_a + 273)^2] \\ \qquad \times [(T_x + 273) + (T_a + 273)] \\ h = h_{conv} + h_{radi} \end{cases} \tag{10}$$

where T_x is the PCB surface temperature, T_a is the ambient temperature, and h is the total heat transfer coefficient. The PCB mask is an epoxy-based lacquer, which is an organic material and has a high emissivity of about 0.9 [39].

A. Model Simplification

Fig. 9(a) shows the vertical cut plane of a multilayer PCB with a chip soldered. As can be seen, multiple vias are normally used to provide an efficient thermal propagation path from the chip to the PCB. Then the heat spreads radially inside the PCB which is further vertically cooled by convection. For the heat transferred inside the PCB, it is obvious that the source originates from the center area.

In addition to the heat source, there are two heat transfer zones, i.e., the middle zone (copper zone) within $[r_b, r_s]$ and the outer zone (FR4 zone) within $[r_s, r_e]$. For the radial heat conduction, the equivalent thermal conductivities in the two zones can be calculated by [25]

$$\begin{cases} k_1 = k_{Cu}N_{Cu}t_{Cu}/t + k_{FR4}(1 - N_{Cu}t_{Cu}/t) \\ k_2 = k_{FR4} \end{cases} \tag{11}$$

If the convective resistance is much larger than the conductive resistance, then the temperature drop over the thickness of a pad is negligible [40]. Thus, the pad can be considered thin, and heat conduction occurs in the radial direction. This assumption holds true when the *Biot number* *Bi* is small, i.e., [41]

$$Bi = \frac{ht}{k} < 0.1 \tag{12}$$

Substituting (11) into (12) yields

$$N_{Cu}t_{Cu} > \frac{t(10ht - k_{FR4})}{k_{Cu} - k_{FR4}} \tag{13}$$

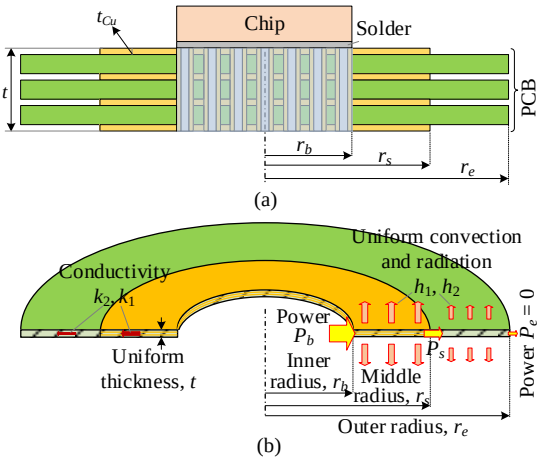

Fig. 9. Simplified PCB model. (a) Vertical cut plane of a multilayer PCB; (b) Heat transfer in a circular PCB: heat conduction in the radial direction, convection and radiation in the axial direction.

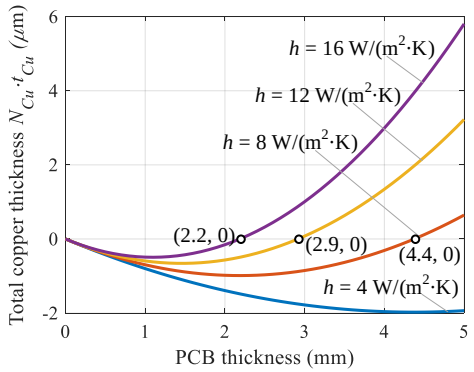

Fig. 10. Lower boundaries of $N_{Cu}t_{Cu}$ at different PCB thicknesses and heat transfer coefficients in order to satisfy $Bi < 0.1$.

Based on (13), the lower boundary of $N_{Cu}t_{Cu}$ with respect to the PCB thickness is depicted at different heat transfer coefficients. With the natural convection, the heat transfer coefficient is normally smaller than 16 W/(m^2 K) [42].

When the PCB is composed of FR4 only (i.e., $N_{Cu}t_{Cu} = 0$), its in-plane thermal conductivity reaches the minimum k_{FR4}. In order to satisfy $Bi < 0.1$, the maximum PCB thickness is 2.2 mm when h = 16 W/(m^2 K). As the decrease of h, the allowed maximum PCB thickness increases.

In most cases, there is at least one-layer 0.5-oz copper in a PCB, yielding a total copper thickness of $N_{Cu}t_{Cu}$ = 17.5 μm. As can be seen from Fig. 10, the lower boundary of $N_{Cu}t_{Cu}$ is far below 17.5 μm even when the PCB thickness reaches 5 mm. Hence, PCBs can be considered thin, and the temperature drop over their thicknesses can be neglected.

Actual semiconductor chips and PCBs are typically rectangular. Due to the phenomena of radial heat conduction and vertical heat convection in the PCB thermal system shown in Fig. 9(a), it is much easier to analyze the thermal resistance in the cylindrical coordinates. Hence, the rectangular heat source and PCB pad are transformed to axisymmetric circular ones based on ensuring that the total area remains the same, as shown in Fig. 9(b). An axisymmetric heat source (package) is located at the inner radius, and the outer edge is assumed to be isothermal.

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B. Heat Transfer in a Circular PCB

The general three-dimensional heat-conduction equation in cylindrical coordinates is [43]

$$\frac{\partial^2 T}{\partial r^2}+\frac{1}{r}\frac{\partial T}{\partial r}+\frac{1}{r^2}\frac{\partial^2 T}{\partial \theta^2}+\frac{\partial^2 T}{\partial z^2}+\frac{\dot{P}}{k}=\frac{k}{\rho c}\frac{\partial T}{\partial \tau} \quad (14)$$

where r, θ, and z denote the radial, azimuthal, and vertical coordinates, respectively, T represents the temperature, τ denotes time, $\dot{P}$ denotes the power generated per unit volume, k represent the thermal conductivity of a material, ρ is the density, and c is the specific heat.

As discussed in Section III-A, PCB pads can be regarded thin due to the negligible temperature drop over the vertical direction. Assume that the thermal pad is of central symmetry, and thus, the heat transfer in the azimuthal direction can be neglected as well. When the steady state of the thermal system is reached, the temperature does not change with time τ, and thus, (14) can be simplified as

$$\frac{\mathrm{d}^2 T}{\mathrm{d}r^2}+\frac{1}{r}\frac{\mathrm{d}T}{\mathrm{d}r}+\frac{\dot{P}}{k}=0 \quad (15)$$

The PCB is cooled by means of natural convection and radiation. Based on Newton's Law, we have

$$P=-hA_z(T-T_a) \quad (16)$$

where the temperature-dependent parameter h represents the sum of convective and radiative heat transfer coefficients, and A_z denotes the PCB cooling area.

Substituting (16) into (15) yields

$$\frac{\mathrm{d}^2 T}{\mathrm{d}r^2}+\frac{1}{r}\frac{\mathrm{d}T}{\mathrm{d}r}-\frac{h}{kt}(T-T_a)=0 \quad (17)$$

where t denotes the PCB thickness.

According to Fourier's law, the transferred power can be expressed by

$$P=-kA_r\frac{\mathrm{d}T}{\mathrm{d}r}=-2k\pi rt\frac{\mathrm{d}T}{\mathrm{d}r} \quad (18)$$

where A_r is the PCB area in the radial direction when the radius equals r.

The general solutions of (17) and (18) can be obtained as

$$\begin{cases}\Delta T=aI_0(z)+bK_0(z)\\ P=-2\pi ktz[aI_1(z)+bK_1(z)]\end{cases} \quad (19)$$

where $\Delta T = T - T_a$, $z=r\sqrt{h/(kt)}$, I_0 is the modified Bessel function of the first kind and order 0, I_1 is the modified Bessel function of the first kind and order 1, K_0 is the modified Bessel function of the second kind and order 0, K_1 is the modified Bessel function of the second kind and order 1, and a and b are arbitrary constants. Eliminating a and b, and applying the two-port theory yield

$$\begin{bmatrix}\Delta T_i\\ P_i\end{bmatrix}=\mathbf{T}_{ij}\begin{bmatrix}\Delta T_j\\ P_j\end{bmatrix}=\begin{bmatrix}A_{ij} & B_{ij}\\ C_{ij} & D_{ij}\end{bmatrix}\begin{bmatrix}\Delta T_j\\ P_j\end{bmatrix} \quad (20)$$

where the subscript i and j represent the sending and receiving ports at any locations, $\mathbf{T}_{ij}$ is the transmission matrix,

$z_i=r_i\sqrt{h/(kt)}$, $A_{ij}=z_j[I_1(z_j)K_0(z_i)+I_0(z_i)K_1(z_j)]$,

$z_j=r_j\sqrt{h/(kt)}$,

$B_{ij}=[I_0(z_j)K_0(z_i)-I_0(z_i)K_0(z_j)]/(2\pi kt)$,

$C_{ij}=2\pi ktz_iz_j[I_1(z_j)K_1(z_i)-I_1(z_i)K_1(z_j)]$, and

$D_{ij}=z_i[I_0(z_j)K_1(z_i)+I_1(z_i)K_0(z_j)]$.

The heat transfer from r_s to r_e (including radial conduction and axial convection and radiation) can be illustrated with a two-port system, i.e., the temperature potential ΔT_s and heat flow P_s can be obtained as (20). Assume that the outer edge of $r = r_e$ is adiabatic in the horizontal direction, i.e., $P_e = 0$, then the thermal resistance from r_s to the ambient, Θ_{sa}, can be derived as

$$\begin{bmatrix}\Delta T_s\\ P_s\end{bmatrix}=\mathbf{T}_{se}\begin{bmatrix}\Delta T_e\\ 0\end{bmatrix}=\begin{bmatrix}A_{se} & B_{se}\\ C_{se} & D_{se}\end{bmatrix}\begin{bmatrix}\Delta T_e\\ 0\end{bmatrix} \quad (21)$$

$$\Theta_{sa}=\frac{\Delta T_s}{P_s}=\frac{A_{se}}{C_{se}} \quad (22)$$

As for the two-port system from r_b to r_s, we have

$$\begin{bmatrix}\Delta T_b\\ P_b\end{bmatrix}=\mathbf{T}_{bs}\begin{bmatrix}\Delta T_s\\ P_s\end{bmatrix}=\begin{bmatrix}A_{bs} & B_{bs}\\ C_{bs} & D_{bs}\end{bmatrix}\begin{bmatrix}\Delta T_s\\ P_s\end{bmatrix}=\mathbf{T}_{bs}\mathbf{T}_{se}\begin{bmatrix}\Delta T_e\\ 0\end{bmatrix}=\begin{bmatrix}A_{bs}A_{se}+B_{bs}C_{se} & A_{bs}B_{se}+B_{bs}D_{se}\\ C_{bs}A_{se}+D_{bs}C_{se} & C_{bs}B_{se}+D_{bs}D_{se}\end{bmatrix}\begin{bmatrix}\Delta T_e\\ 0\end{bmatrix} \quad (23)$$

Then the thermal resistance from r_b to the ambient, and the temperature at r_b can be obtained

$$\Theta_{ba}=\frac{\Delta T_b}{P_b}=\frac{A_{bs}A_{se}+B_{bs}C_{se}}{C_{bs}A_{se}+D_{bs}C_{se}} \quad (24)$$

$$T_b=T_a+P_b\Theta_{ba} \quad (25)$$

where P_b represents the power injected to the board.

Manipulating (21) and (23) yields the equivalent thermal resistance from r_s to the ambient and the thermal resistance from r_e to the ambient when an axisymmetric heat source is located at r_b

$$\psi_{sa}=\frac{\Delta T_s}{P_b}=\frac{A_{se}}{C_{bs}A_{se}+D_{bs}C_{se}}\Rightarrow T_s=T_a+P_b\psi_{sa} \quad (26)$$

$$\psi_{ea}=\frac{\Delta T_e}{P_b}=\frac{1}{C_{bs}A_{se}+D_{bs}C_{se}}\Rightarrow T_e=T_a+P_b\psi_{ea} \quad (27)$$

It should be noted that ψ_{sa} and ψ_{ea} are defined similarly to the thermal metric ψ_{JT} adopted by the industry (JEDEC Standard: JESD51-2 [44]). They are not true thermal resistances but can be used to calculate the temperatures at r_s and r_e.

The analysis above is carried out by assuming the heat source, copper pad and PCB are circular. The equivalent radius of a rectangular pad can be approximated by $r_x=\sqrt{a_xb_x/\pi}$ where a_x and b_x are the rectangular side lengths, and the subscript 'x' denotes 'b', 's', and 'e'.

C. Heat Transfer Boundary

In order to satisfy the boundary condition that there is no conductive heat flow at r_e, the thermal resistance Θ_{sa} (22) is investigated with respect to different parameters, i.e., r_e, t, and h, as shown in Fig. 11(a). When r_s is specified, the

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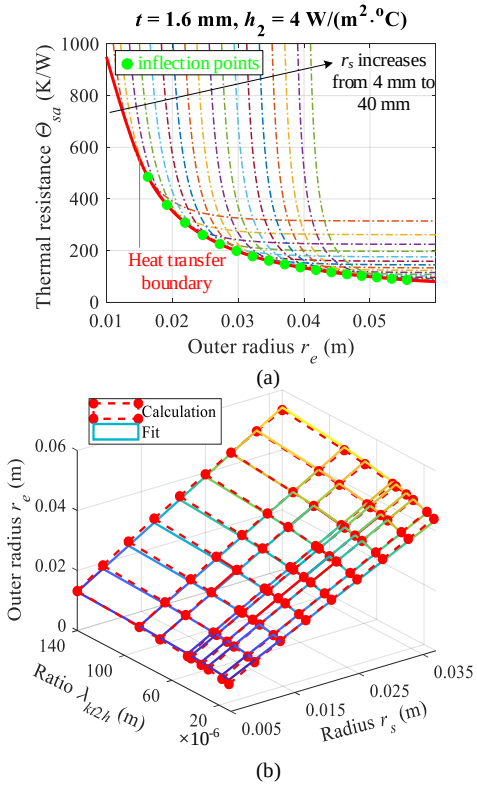

Fig. 11. (a) Curves of the thermal resistance Θ_{sa} with respect to r_s and r_e. (b) The heat transfer boundary r_e versus the copper radius r_s and the ratio λ_{kt2h}.

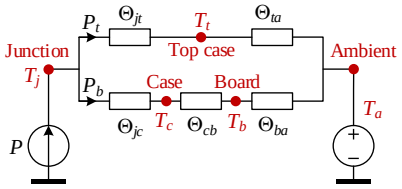

Fig. 12. Equivalent thermal resistance diagram for a DPAK package mounted on a PCB. The thermal resistance of the thin solder between the package and the PCB is small and therefore is neglected [45].

thermal resistance Θ_{sa} decreases with respect to the increase of r_e; however, the decrease of Θ_{sa} becomes insignificant when r_e exceeds the inflection point r_{ec}, which means that the heat flow beyond r_{ec} can be negligible and the inflection points can be chosen as the heat transfer boundary. It should be noted that r_{ec} depends on both the copper radius r_s and the ratio of $k{\cdot}t$ to h_2, i.e., $\lambda_{kt2h} = kt / h_2$. It is quite difficult to directly obtain the analytical expression of r_{ec}. Therefore, curve fitting is carried out, as shown in Fig. 11(b). It is found that the outer radius r_e can be determined by

$$r_e = 3\lambda_{kt2h}^{0.095}(r_s + 0.005) \tag{28}$$

D. Algorithm for Copper Pad Sizing

When an SMD is mounted on a PCB, the heat generated inside the device will dissipate in two parallel pathways: one is from the junction, then to the top case, and finally to the ambient; the other is from the junction to the bottom case, then to the board, and finally to the ambient. The heat flow rates in the two paths are termed as P_t and P_b, respectively. Obviously, we have $P = P_t + P_b$. Fig. 12 shows the equivalent thermal resistance diagram for a DPAK package mounted on a PCB.

If all the thermal resistances are known, then the top-case and junction temperatures can be predicted by

$$T_t = \frac{P(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}}\Theta_{ta} + T_a = P_b\psi_{ta} + T_a \tag{29}$$

where the equivalent top-case-ambient thermal resistance

$$\psi_{ta} = \frac{(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})\Theta_{ta}}{\Theta_{jt} + \Theta_{ta}} \tag{30}$$

$$T_j = \frac{P(\Theta_{jt} + \Theta_{ta})(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}} + T_a \tag{31}$$

If the top-case temperature T_t and other thermal resistances are determined, then the board-ambient thermal resistance Θ_{ba} can be expressed as

$$\Theta_{ba} = \frac{P\Theta_{ta}(\Theta_{jt} + \Theta_{ta})}{P\Theta_{ta} + T_a - T_t} - \Theta_{jc} - \Theta_{cb} - \Theta_{jt} - \Theta_{ta} \tag{32}$$

For the heat transfers from the junction to the top case, from the junction to the case, and from the case to the board, there is only heat conduction, and therefore the corresponding thermal resistances Θ_{jt}, Θ_{jc}, and Θ_{cb} are constant if neglecting the relatively small material property variation over temperature. However, the heat transfers from the top case to the ambient and from the board to the ambient involve convection and radiation. Hence, the thermal resistances Θ_{ta} and Θ_{ba} are temperature dependent.

As seen from (25)-(27), and (29), a temperature T_x can be obtained by

$$T_x = P_b\Theta_x + T_a \tag{33}$$

where T_x denotes the temperature T_b, T_s, T_e or T_t, and Θ_x represents the thermal resistance Θ_{ba}, ψ_{sa}, ψ_{ea} or ψ_{ea}. It is concluded from (10) that Θ_x is a monotonically decreasing function of T_x:

$$\Theta_x = f_x(T_x) \tag{34}$$

The higher the temperature T_x, the lower the thermal resistance Θ_x. Substituting (34) into (33) yields

$$T_x = P_b f_x(T_x) + T_a = \varphi_x(T_x) \tag{35}$$

Due to the fact that both P_b and Θ_x are positive, $\varphi_x(T_x) = P_b\Theta_x + T_a$ is always larger than T_a. The thermal resistance Θ_x is a monotonically decreasing function of T_x, and therefore $\varphi_x(T_x)$ is also monotonically decreasing with respect to T_x. The full expression of (35) can be obtained by substituting (10), (24), (26), (27) and (29) into (33). However, the final transcendental equations do not have analytical solutions. Therefore, the fixed-point iteration method [46] is used to obtain the solution of (35). The iterative scheme with the recursive relation is

$$T_{x,c+1} = \varphi_x(T_{x,c}) \tag{36}$$

where the subscript "c" represents the iteration order. Fig. 13. shows the fixed-point iterative trajectories of $T_x = \varphi_x(T_x)$ at different initial points. The solution, i.e., temperature

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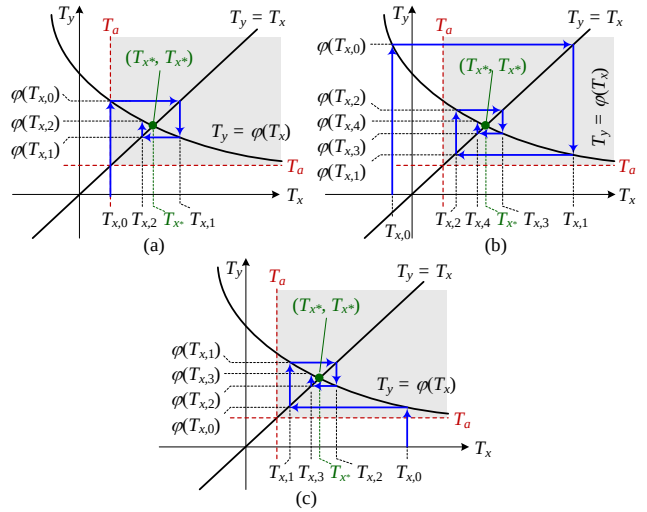

Fig. 13. Fixed-point iterative schemes at different initial points. (a) The initial point equals the ambient temperature, i.e., $T_{x,0} = T_a$; (b) the initial point is lower than the ambient temperature, i.e., $T_{x,0} < T_a$; (c) The initial point is higher than the ambient temperature, i.e., $T_{x,0} > T_a$.

point (T_{x*}, T_{x*}) locates in the shaded region, i.e., $T_x > T_a$ and $T_y > T_a$. Therefore, the initial iteration value of $T_{x,0} \geq T_a$ enables fewer iteration times, as illustrated in Fig. 13. However, it is noted that when the initial value $T_{x,0}$ is smaller than T_a, it takes only one iteration before the iterative value enters the shaded region. This is because that $\varphi_x(T_x) = P_b\Theta_x + T_a$ is always larger than T_a. Hence, the iteration speed does not vary much with respect to the initial value $T_{x,0}$.

A fixed-point iteration based algorithm taking into account all the five thermal resistances shown in Fig. 12 is developed to design the copper pad size, as shown in Fig. 14.

Before the design, the system parameters, e.g., the ambient temperature T_a, total Power loss P, PCB thickness t, copper thickness t_{Cu}, number of copper layers N_{Cu}, package radius r_b, junction-top-case thermal resistance Θ_{jt}, junction-case thermal resistance Θ_{jc}, case-board thermal resistance Θ_{cb}, allowed maximum junction temperature T_{jmax}, should be determined. Then, a small initial value is given to the copper pad radius r_s before the four initial given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$, are initialized as $T_{t,0}$, $T_{e,0}$, $T_{s,0}$, and $T_{b,0}$, respectively. Then the heat transfer coefficients h_1 and h_2 can be calculated based on (10), and the thermal resistances Θ_{ta}, Θ_{ba}, ψ_{sa}, and ψ_{ea} can be obtained accordingly. After that, the calculated temperatures $T_{t,c}$, $T_{e,c}$, $T_{s,c}$ and $T_{b,c}$ are compared with the given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$; also the errors can be obtained, i.e., $\varepsilon_t = T_{t,c} - T_{t,g}$, $\varepsilon_e = T_{e,c} - T_{e,g}$, $\varepsilon_s = T_{s,c} - T_{s,g}$, and $\varepsilon_b = T_{b,c} - T_{b,g}$. If the absolute error ε_x is greater than the preset limit ε_{lmt}, then the given temperature $T_{x,g}$ will be updated by the calculated temperature $T_{x,c}$ and the subscript x represents 't', 'e', 's', or 'b'. If all four temperatures errors are smaller than ε_{lmt}, then the algorithm proceeds to calculate the junction temperature T_j according to (31). If the calculated T_j is higher than the allowed maximum junction temperature, then the copper pad radius r_e will be increased. Otherwise, it implies that current copper pad radius r_e is large enough for cooling. In this way, we can find the minimum r_e which helps to achieve the maximum power density while meeting the thermal specifications.

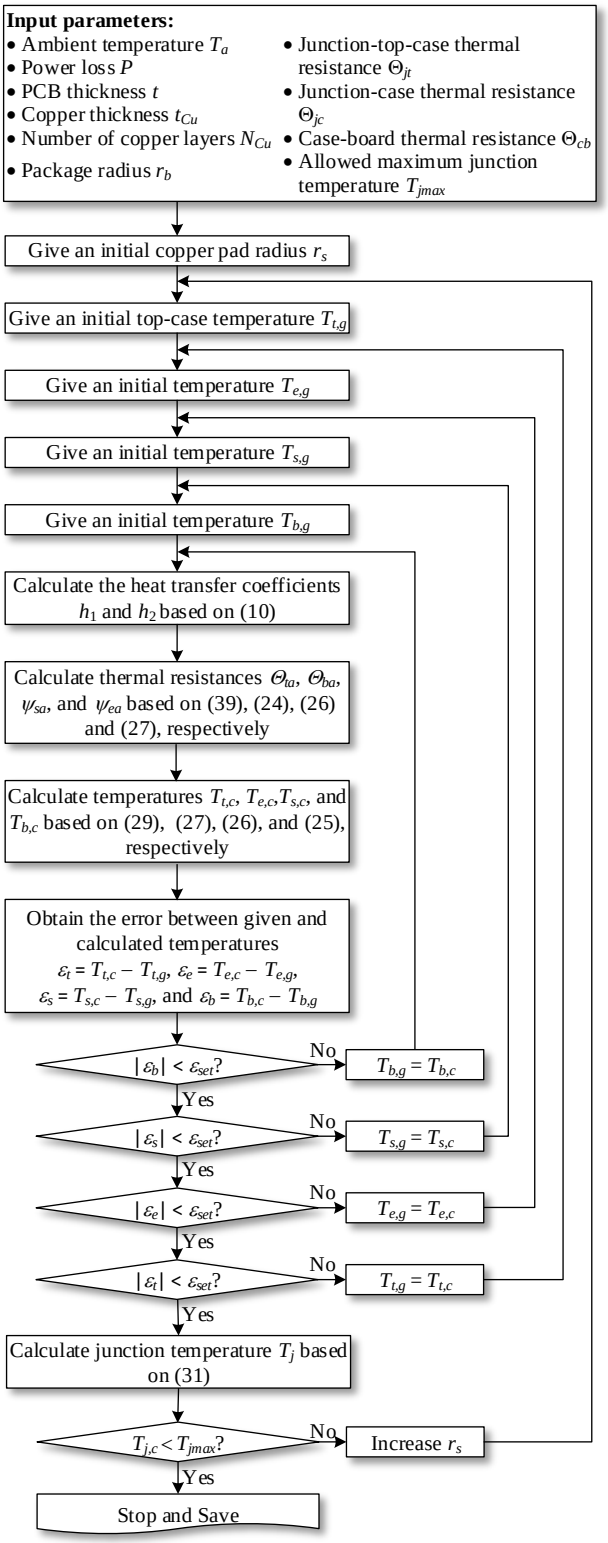

Fig. 14. Flowchart of sizing a PCB thermal pad to satisfy the requirement of below the specified maximum junction temperature.

Fig. 15 shows the elapsed time to run the algorithm shown in Fig. 14 with MATLAB 2018b. Although a small temperature error limit 0.01 °C is set, the average elapsed times are as short as approximately 30 ms. Also, it is seen that the average times do not vary significantly for the three

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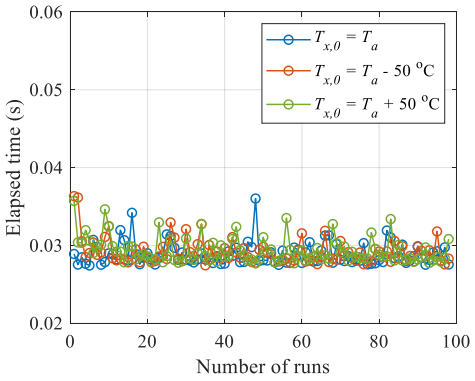

Fig. 15. Elapsed time to run the algorithm in Fig. 14 with MATLAB R2018b.

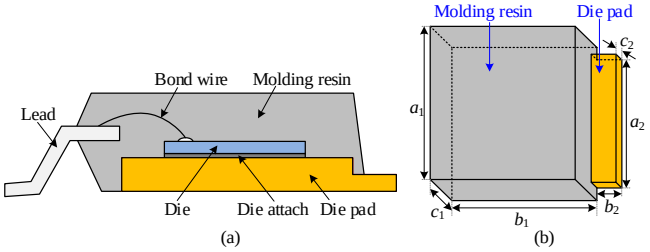

Fig. 16. (a) DPAK package structure; (b) Simplified package outline dimensions of diode VS-6EWL06FN-M3 [49].

selected initial iteration values, which agrees well with previous analysis. Nevertheless, the iteration can be further accelerated by using advanced methods, e.g., the Aitken's delta-squared process [47] and the Steffensen's method [48].

E. Thermal Modeling of DPAK Package

As mentioned before, when an SMD is mounted on a PCB, the equivalent thermal resistance diagram is shown in Fig. 12. Apart from the board to ambient thermal resistance Θ_{ba}, the realization of the proposed algorithm shown in Fig. 14 also requires the knowledge of the other four thermal resistances Θ_{cb}, Θ_{jt}, Θ_{ta}, and Θ_{jc}. The case-board thermal resistance Θ_{cb} can be obtained from the analysis in Section II. For the other three thermal resistances Θ_{jt}, Θ_{ta}, and Θ_{jc}, however, they are package dependent and are usually not available in datasheets. Therefore, the detailed structure model and simplified package outline dimensions of DPAK package are derived, as shown in Fig. 16.

An analytical model of the thermal resistance Θ_{ta} is firstly developed. Its side and top surfaces are cooled by natural convection and radiation. Thus, the heat transfer from the surfaces of the diode to the ambient involves the heat conduction, convection and radiation, and the heat transfer coefficient depends on both the ambient temperature and the temperature difference between the surfaces and the ambient.

Assume that the package is placed horizontally, and its surfaces share the same temperature T_t. For the horizontal top surfaces of the molding resin and die pad (see Fig. 16(b)), their areas are $A_{hor1} = a_1 b_1$ and $A_{hor2} = a_2 b_2$, respectively. Based on [38], the characteristic lengths of the two rectangular surfaces under natural convection can be calculated as $L_{c,hor1} = a_1 b_1 / [(a_1 + b_1)/2]$ and $L_{c,hor2} = a_2 b_2 / [(a_2 + b_2)/2]$, respectively. Then, we can obtain the convective heat transfer coefficients of the two top surfaces [38], i.e.,

$$\begin{cases} h_{hor,conv1} = \lambda_{hor}[(T_t - T_a)/L_{c,hor1}]^{0.25} \\ \qquad\qquad = \lambda_{hor}[(a_1 + b_1)(T_t - T_a)/(2a_1 b_1)]^{0.25} \\ h_{hor,conv2} = \lambda_{hor}[(T_t - T_a)/L_{c,hor2}]^{0.25} \\ \qquad\qquad = \lambda_{hor}[(a_2 + b_2)(T_t - T_a)/(2a_2 b_2)]^{0.25} \end{cases} \tag{37}$$

where λ_{hor} = 1.32 is a constant for horizontal plates [38].

Similarly, the convective heat transfer coefficients of the vertical surfaces of the molding resin and die pad with areas of $A_{ver1} = 2c_1(a_1 + b_1) - a_2 c_2$ and $A_{ver2} = c_2(a_2 + 2b_2)$ can be obtained as

$$\begin{cases} h_{ver,conv1} = \lambda_{ver}[(T_t - T_a)/L_{c,ver1}]^{0.25} \\ \qquad\qquad = \lambda_{ver}[(T_t - T_a)/c_1]^{0.25} \\ h_{ver,conv2} = \lambda_{ver}[(T_t - T_a)/L_{c,ver2}]^{0.25} \\ \qquad\qquad = \lambda_{ver}[(T_t - T_a)/c_2]^{0.25} \end{cases} \tag{38}$$

where λ_{ver} = 0.59 is a constant for vertical plates [38].

Considering both the convection and radiation, the thermal resistance from the package surface to the ambient can be obtained as

$$\begin{aligned} \Theta_{ta} &= \frac{1}{A_{hor1}(h_{hor,conv1} + h_{radi1}) + A_{hor2}(h_{hor,conv2} + h_{radi2}) + A_{ver1}(h_{ver,conv1} + h_{radi1}) + A_{ver2}(h_{ver,conv2} + h_{radi2})} \\ &= \frac{1}{\begin{pmatrix} 2c_1(a_1 + b_1)(\lambda_{ver}[(T_t - T_a)/c_1]^{0.25} + h_{radi1}) + c_2(a_2 + 2b_2)(\lambda_{ver}[(T_t - T_a)/c_2]^{0.25} + h_{radi2}) \\ + a_1 b_1(\lambda_{hor}[(a_1 + b_1)(T_t - T_a)/(2a_1 b_1)]^{0.25} + h_{radi1}) + a_2 b_2(\lambda_{hor}[(a_2 + b_2)(T_t - T_a)/(2a_2 b_2)]^{0.25} + h_{radi2}) \end{pmatrix}} \end{aligned} \tag{39}$$

where the radiative heat transfer coefficients $h_{radi1} = \varepsilon_1 \sigma(T_a + 273 + T_t + 273)[(T_a + 273)^2 + (T_t + 273)^2]$ and $h_{radi2} = \varepsilon_2 \sigma(T_a + 273 + T_t + 273)[(T_a + 273)^2 + (T_t + 273)^2]$ are for the molding resin surface and the tab surface, respectively; ε_1 and ε_2 are the emissivities of the molding resin and tab surfaces, respectively.

As for the other two thermal resistances Θ_{jc} and Θ_{jt}, their values relate to the conductive heat transfer inside the DPAK package, and therefore CFD simulations with ANSYS Icepak 18.0 are conducted, as discussed in Section IV-A.

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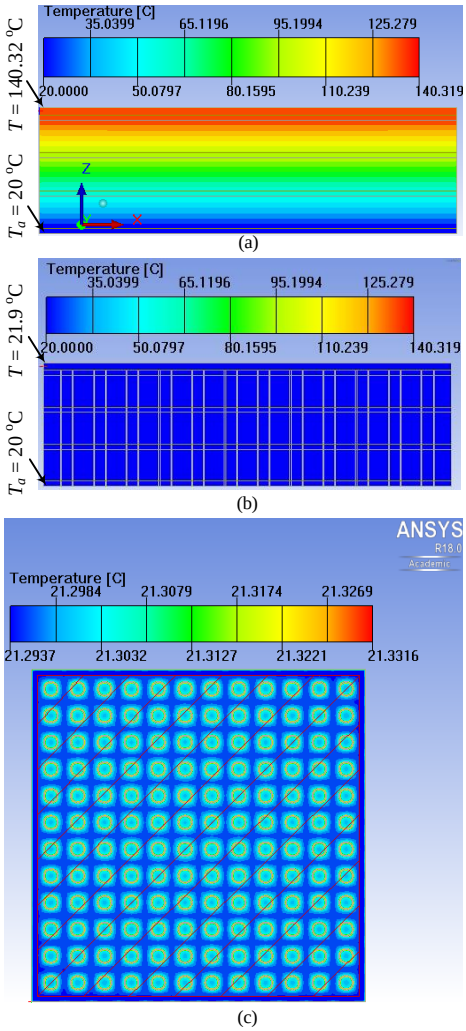

Fig. 17 CFD simulations of PCBs with the simulation tool ANSYS Icepak™ 18.0. The top surface of each PCB generates 1-W power loss, whereas the bottom surface is fixed at the ambient temperature T_a = 20 °C. PCB parameters in common: 5.6-mm length × 5.6-mm width ×1.6-mm thickness, 4 copper layers, and 2 oz for each layer. (a) Temperature contour on a vertical cut plane of the PCB without vias; (b) Temperature contour on a vertical cut plane of the PCB with unfilled vias of 0.25-mm diameter; (c) Temperature contour on a horizontal cut plane of the PCB with unfilled vias of 0.25-mm diameter.

IV. CFD Simulation and Experimental Verifications of Proposed Thermal Models

A. CFD Simulations

ANSYS Icepak provides powerful electronic cooling solutions which utilize the ANSYS Fluent CFD solver for thermal and fluid flow analyses. In order to verify the proposed thermal models of PCBs, CFD simulations are conducted in ANSYS Icepak 18.0 with the pressure-based ANSYS Fluent solver [50], [51].

The CFD simulation results of a PCB via array for the DPAK package are shown in Fig. 17. As can be seen, the thermal resistance of the PCB pad is significantly reduced from 120.3 K/W (no via, see Fig. 17(a)) to 1.86 K/W (via diameter ϕ = 0.25 mm, see Fig. 17(b)).

The calculated and simulated results for different via patterns, diameters and filler materials are shown in Fig. 18.

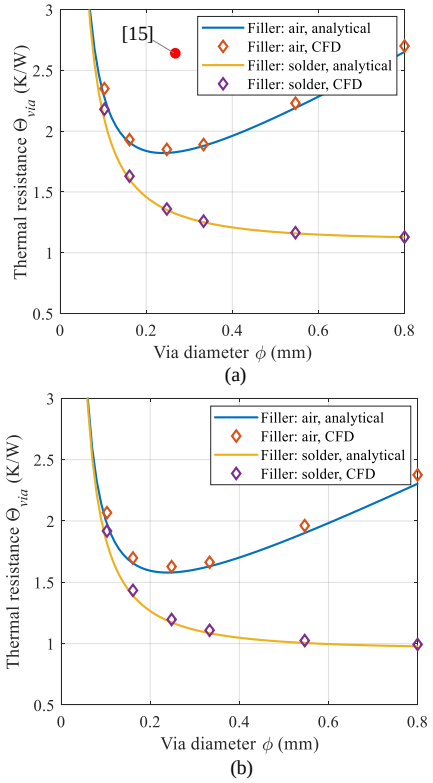

Fig. 18. Comparison between the calculated and simulated thermal resistance of DPAK (TO252) via array with different parameters: (a) *Pattern I* and (b) *Pattern II*.

It is seen that there is a good agreement between calculations and simulations. Also, it indicates that a proper design of the vias (i.e., the pattern, diameter, filler material, *etc*) enables a remarkable reduction for the thermal resistance. Compared to the reference design provided in [15], the thermal resistance can be reduced up to 62%, i.e., from 2.63 K/W (see Fig. 18(a)) based on [15] to 0.98 K/W with the proposed optimal design trajectory (*Pattern II*, ϕ = 0.8 mm, solder filling, see Fig. 18(b)).

As mentioned in Section III-E, a detailed structural model has been built for the DPAK package based on real dimensions. Thermal simulations are then performed in ANSYS Icepak 18.0 to obtain the junction-case and junction-top-case thermal resistances Θ_{jc} and Θ_{jt}, as shown in Fig. 19(a) and (b). It is found that the two thermal resistances are Θ_{jc} = 2.47 °C/W and Θ_{jc} = 44.12 °C/W, respectively.

To verify the built analytical thermal resistance model of Θ_{ta}, multiple CFD simulations are also conducted in ANSYS Icepak 18.0, as shown in Fig. 19(c) and Fig. 20. It is seen that there is a negligible error (maximum error = 3.2 %) between the simulations and the analytical results (39).

B. Experimental Verifications

A curve tracer B1506A from Keysight Technologies is used to measure the *I-V* characteristics of a batch of VS-6EWL06FN-M3 diodes, as shown in Fig. 21(a). It is seen that the voltage drop difference is small. For instance, when the forward current I_F = 3 A, the maximum forward voltage difference is 0.944 V – 0.93 V = 0.014 V, which represents only 1.5% of the average forward voltage 0.934 V.

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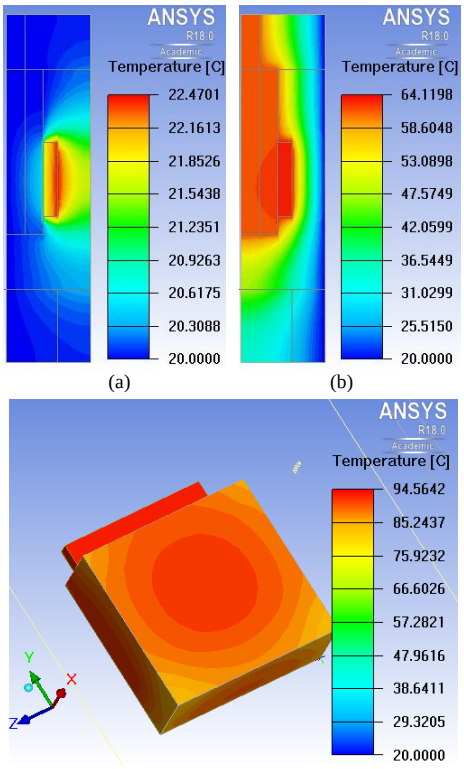


Fig. 19. CFD simulation results of diode VS-6EWL06FN-M3 in ANSYS Icepak 18.0. (a) Simulation results for the junction-case thermal resistance Θ_{jc}; boundary conditions: 1-W power loss is generated on the top surface of the die, the case temperature is fixed at the ambient temperature 20 ºC, and other surfaces of the diode are adiabatic. (b) Simulation results for the junction-top-case thermal resistance Θ_{jt}; boundary conditions: 1-W power loss is generated on the top surface of the die, the top-case temperature is fixed at the ambient temperature 20 ºC, and other surfaces of the diode are adiabatic. (c) Simulation results for the top-case-ambient thermal resistance Θ_{ta}; boundary conditions: 0.2-W power loss is injected on the top surface of the die, and the surfaces of the diode are opening to the ambient.

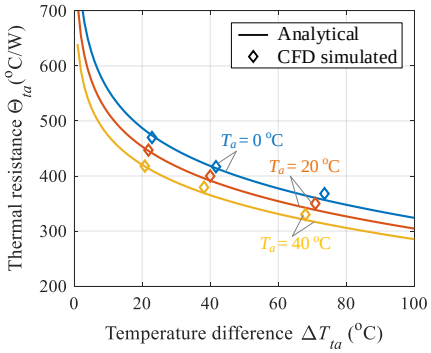
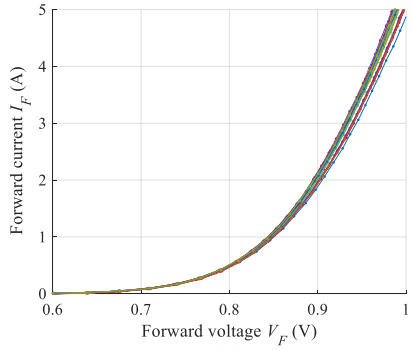
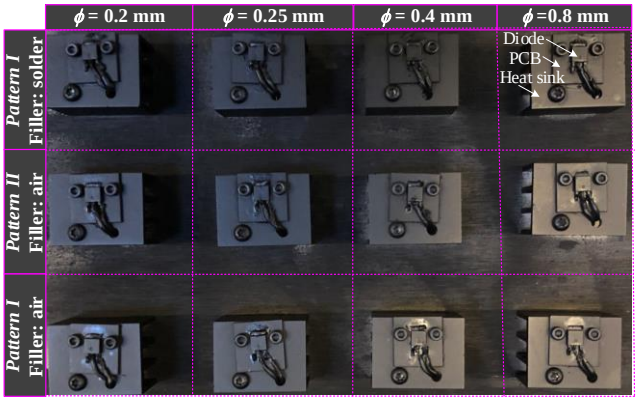


Fig. 20. Comparison between CFD simulations and the analytical model (39) for the top-case-ambient thermal resistance of the DPAK diode VS-6EWL06FN-M3.

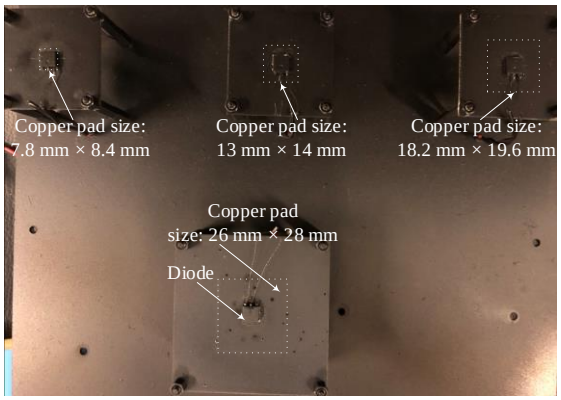
Nevertheless, the 16 diodes with close *I-V* characteristics (maximum forward voltage difference = 0.08% at I_F = 3 A) are used to build the experimental setups for PCB thermal measurements, as shown in Fig. 21(b) and (c). Nevertheless, the *I-V* characteristic of a diode varies significantly with the junction temperature. In order to make sure that all the diodes generate the same power loss, each diode is connected to a separate dc power source. Also, a voltage meter and a current meter are used to monitor the consumed power by each diode.



(a)



(b)



(c)

Fig. 21. Experimental setups. (a) Measured I_F-V_F curves of 50 VS-6EWL06FN-M3 diodes at 25 ºC by using a curve tracer B1506A from Keysight Technologies. (b) Photo of the experimental setup for PCB vias. Each diode is soldered on a heatsink-cooled PCB with a specified via design. (c) Photo of the built PCB thermal pads with different copper areas.

The vertical structure of a diode mounted on a heatsink-cooled PCB is shown in Fig. 22(a). For the power loss generated inside the diode and dissipated to the ambient, two heat transfer paths exist, i.e., the one through the diode's top case, and the other one through the diode's bottom case, PCB vias, and heatsink. The equivalent thermal resistance diagram is shown in Fig. 22(b). In addition to the thermal resistance of PCB via Θ_{via}, other thermal resistances (e.g., Θ_{jc}, Θ_{jt}, Θ_{ha}, Θ_{ta}, Θ_{solder}, and Θ_{TIM}) also affect the cooling of the diode. In contrast to the junction temperature of a diode, the top-case temperature T_t can be more easily measured with an infrared camera, and also T_t can be calculated with (40) if all thermal resistances are known.

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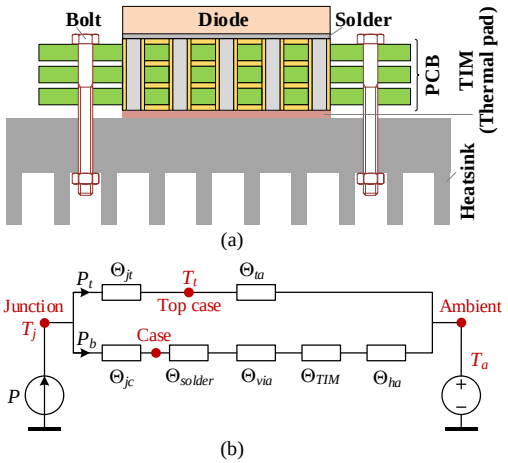

Fig. 22. (a) Vertical structure and (b) equivalent thermal resistance diagram when a DPAK diode VS-6EWL06FN-M3 is mounted on a heatsink-cooled PCB. Θ_{jc}, Θ_{jt}, Θ_{ha}, and Θ_{ta} represent the junction-case, junction-top-case, heatsink-ambient, and top-case-ambient thermal resistances, respectively. Θ_{solder} and Θ_{TIM} denote the thermal resistances of the solder and thermal interface material (TIM) layers, respectively.

$$T_t = \frac{P\Theta_{ta}(\Theta_{jc}+\Theta_{solder}+\Theta_{via}+\Theta_{TIM}+\Theta_{ha})}{\Theta_{jt}+\Theta_{ta}+\Theta_{jc}+\Theta_{solder}+\Theta_{via}+\Theta_{TIM}+\Theta_{ha}} + T_a \tag{40}$$

The thermal resistances from the top-case to the ambient and from the heatsink to the ambient, Θ_{ta} and Θ_{ha}, are temperature-dependent, and thus, it is difficult to directly obtain their values. Hence, an equivalent top-case to ambient thermal resistance ψ_{ta} is introduced, which is defined as

$$\psi_{ta} = \frac{T_t - T_a}{P} \tag{41}$$

where P represents the total power loss generated inside the chip. Substituting (40) to (41) yields

$$\begin{aligned}\psi_{ta} &= \frac{\Theta_{ta}(\Theta_{jc}+\Theta_{solder}+\Theta_{via}+\Theta_{TIM}+\Theta_{ha})}{\Theta_{jt}+\Theta_{ta}+\Theta_{jc}+\Theta_{solder}+\Theta_{via}+\Theta_{TIM}+\Theta_{ha}} \\ &= \left(\frac{\Theta_{jt}/\Theta_{ta}+1}{\Theta_{jc}+\Theta_{solder}+\Theta_{via}+\Theta_{TIM}+\Theta_{ha}} + \frac{1}{\Theta_{ta}}\right)^{-1} \\ \Rightarrow \Theta_{via} &= \psi_{ta}(1+\Theta_{jt}/\Theta_{ta}) - \Theta_{jc} - \Theta_{solder} - \Theta_{TIM} - \Theta_{ha}\end{aligned} \tag{42}$$

It is seen from (42) that the thermal resistance of a PCB via array is proportional to the equivalent top-case-ambient thermal resistance ψ_{ta}. If other thermal resistances stay the same, then ψ_{ta} can be used to reflect the thermal resistance of PCB vias with different designs.

Each diode in Fig. 21(b) is controlled to generate a 2.8-W power loss. When the steady state is reached, the temperature contour of the experimental setup is captured by an infrared camera, as shown in Fig. 23. Then, the top-case temperature and the equivalent top-case-ambient thermal resistance of each diode can be obtained, as listed in Table II. Without solder filled, the via diameter of 0.25 mm helps the diode achieve the lowest top-case temperature and the smallest equivalent top-case-ambient thermal resistance. When the vias are filled up with high-thermal-conductivity solder, then the via array with ϕ = 0.8 mm has the minimum thermal resistance. Furthermore, it is seen that the via array in *Pattern II* has a lower thermal resistance than *Pattern I* when other parameters remain the same. These trends agree pretty well with the theoretical analysis done in Section II.

The experimental setup for the thermal measurements of PCB pads is shown in Fig. 21(c). As can be seen, the diodes are mounted on four 2-layer PCBs (70-μm copper thickness for each layer) with different sizes of copper pads. Each diode is connected to a dc power source, and thus the diode is able to generate power losses, which are further conducted to the thermal pad and dissipated to the ambient by natural convection. A voltage meter and a current meter are used to measure the power loss generated by each diode. For each measurement, the power losses of the four diodes are controlled to the same value. The steady-state thermal images of the diodes are captured for different power losses (i.e., P = 0.5 W and P = 1 W) and different sizes of copper pads, as shown in Fig. 24.

Fig. 25 (a) and (b) presents the measured and calculated junction and top-case temperatures in the two cases of P = 0.5 W and P = 1 W. As can be seen, there is a significant top-case temperature difference between the existing model [14], [31] and the measurements, especially when the copper pad radius is small. In contrast, the proposed model in Section III is able to more accurately predict the top-case temperature.

The maximum operating junction temperature of the selected diode VS-6EWL06FN-M3 is 175 °C [49]. For reliability reasons, the maximum junction temperature T_{jmax} should be smaller than a lower value, e.g., T_{jmax} = 125 °C. In this case, the required minimum copper radius can be found, as illustrated in Fig. 25 (a) and (b). If the maximum power loss of the diode is 0.5 W, then the minimum copper radius r_e is 2.8 mm based on the proposed model. In contrast, the existing model provides a minimum copper radius of 6.1 mm, which corresponds to an around 375% increase for the copper pad area compared to the design of r_e = 2.8 mm. If the maximum power loss of the diode is 1 W, then the minimum copper radius r_e is 5.9 mm according to the proposed model. However, the existing model shows the minimum r_s is 9.7 mm. That means a 170 % increase for the copper pad area.

Substitute the measured top-case temperatures into (32), and then the thermal resistance from the board to the ambient can be derived, as shown in Fig. 25(c). To make a comparison, the results from the existing model and the proposed model (24) are shown in Fig. 25(c) as well. It can be seen that there is a remarkable error between the measurements and the results from the existing model. However, a good agreement can be achieved between the measurements and the results from the proposed model.

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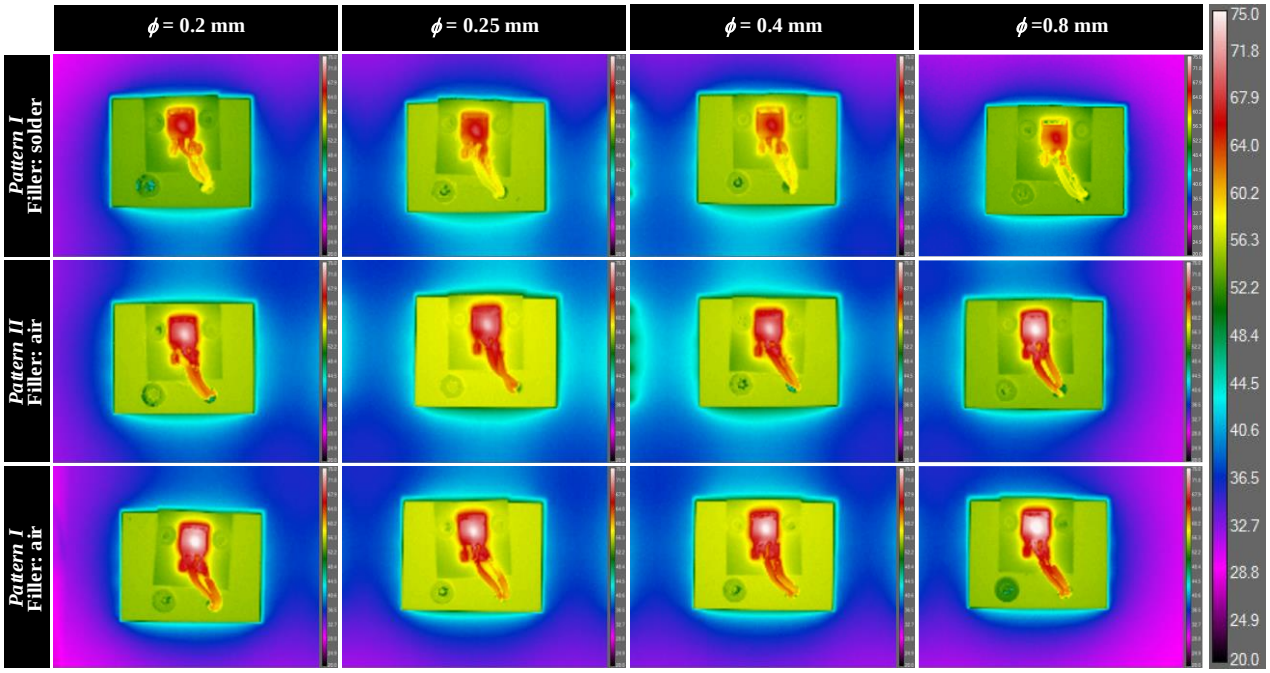

Fig. 23. Thermal image of the experimental setup when each diode generates a power loss of 2.8 W.

TABLE II
MEASURED TOP-CASE TEMPERATURE AND EQUIVALENT TOP-CASE-AMBIENT THERMAL RESISTANCE OF DPAK DIODES VS-6EWL06FN-M3 WHEN THE COOLING CONDITIONS, POWER LOSS AND AMBIENT TEMPERATURE ARE SPECIFIED AS FIG. 22.

Pattern	Filler material	ϕ = 0.2 mm		ϕ = 0.25 mm		ϕ = 0.4 mm		ϕ = 0.8 mm	
		T_t	ψ_{ta}	T_t	ψ_{ta}	T_t	ψ_{ta}	T_t	ψ_{ta}
Pattern I	Solder	68.2 ºC	15.43 ºC/W	67.3 ºC	15.1 ºC/W	66.4 ºC	14.8 ºC/W	65.7 ºC	14.5 ºC/W
Pattern II	Air	72.9 ºC	17.1 ºC/W	72.4 ºC	16.9 ºC/W	72.6 ºC	17.0 ºC/W	74.8 ºC	17.8 ºC/W
Pattern I	Air	75.2 ºC	17.9 ºC/W	74.1 ºC	17.5 ºC/W	74.6 ºC	17.7 ºC/W	76.5 ºC	18.4 ºC/W

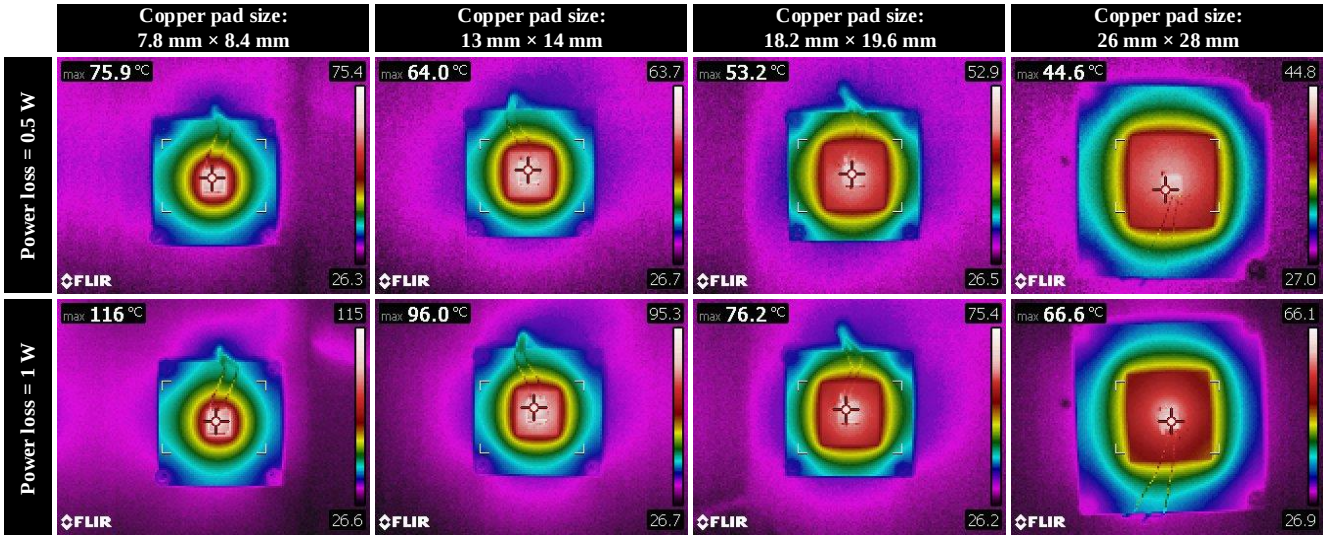

Fig. 24. Thermal images of diodes mounted on PCBs with different power losses and different sizes of copper pads.

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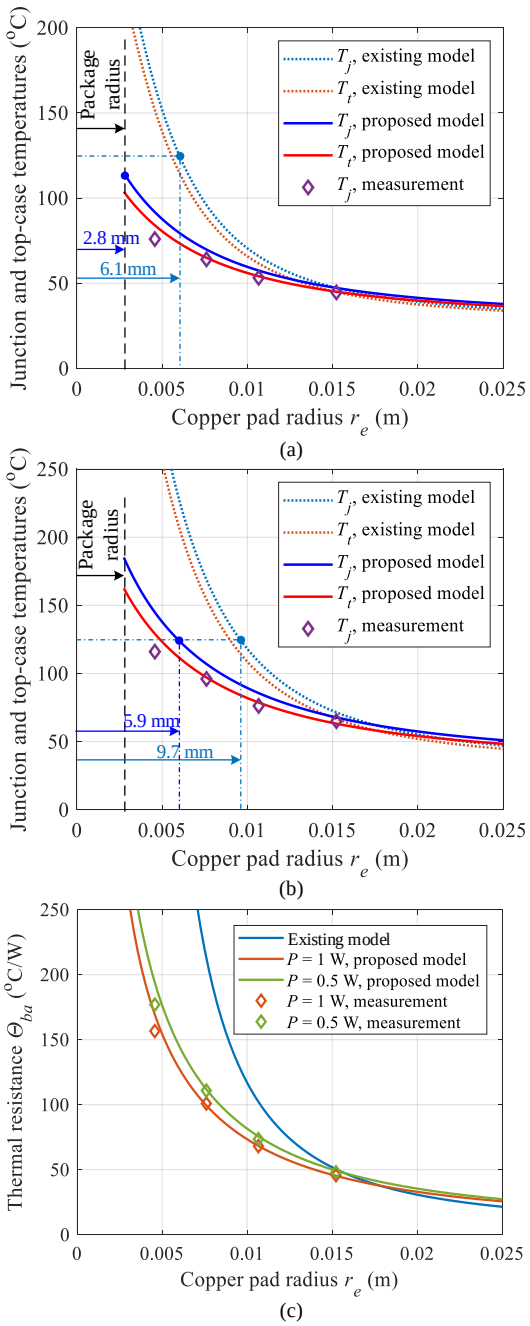

Fig. 25. Comparison of the junction and top-case temperatures between measurements and calculations when (a) 0.5-W and (b) 1-W power losses are generated inside the diode. (c) Comparison of the board-ambient thermal resistances obtained from the measurements, the existing model [14], [31] and the proposed model.

V. Conclusions

This paper proposes two analytical thermal resistance models and two design optimization methods for PCB vias and thermal pads. CFD simulations and experimental measurements verify the developed thermal models and optimal designs.

1) When other PCB parameters are determined, the via-to-via spacing should be designed possibly small, and there exists an optimal via diameter which can help to achieve the minimum thermal resistance for PCB vias;
2) Both the via layout of *Pattern II* and solder filling contribute to further reductions to the thermal resistance of PCB vias;
3) The existing analytical thermal resistance model for PCB pads overestimates the junction temperatures of SMDs, whereas the proposed model enables a more accurate junction temperature prediction.

Therefore, the proposed thermal models enable engineers to fast and easily optimize the design of PCB vias and thermal pads.

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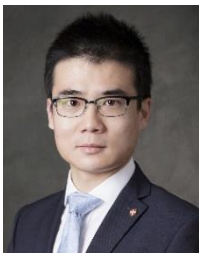

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