Lifetime Evaluation of Three-Level Inverters for 1500-V Photovoltaic Systems

He, Jinkui; Sangwongwanich, Ariya; Yang, Yongheng; Iannuzzo, Francesco

Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3008246

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Lifetime Evaluation of Three-Level Inverters for 1500-V Photovoltaic Systems

Jinkui He, *Student Member, IEEE,* Ariya Sangwongwanich, *Member, IEEE,*
Yongheng Yang, *Senior Member, IEEE,* and Francesco Iannuzzo, *Senior Member, IEEE*

***Abstract*—The installation cost of Photovoltaic (PV) plants can be reduced considerably by extending the maximum DC voltage from 1000 V to 1500 V (e.g., with more PV arrays connected in series). However, the increased DC voltage also presents challenges on the design and operation of PV inverters in terms of efficiency and reliability. To ensure an efficient and reliable PV power conversion, an early-stage reliability assessment is of importance in the design phase of the inverter and then the entire system. This paper, thus, evaluates the lifetime of three-level 1500-V PV inverters with respect to their thermal cycling capabilities both at the component level and system level. The evaluation is carried out through a case study on a 160-kW PV system considering the impact of voltage stress, switching frequency, and mission profile. The evaluation reveals that these factors have a significant impact on the inverter reliability, and thus affect the topology selection and the final cost of the entire PV system. More importantly, the exploration provides insights on the design of 1500-V PV systems seen from the reliability perspective.**

***Index Terms*—Photovoltaic (PV) inverters, multi-level inverters, mission profile, lifetime, reliability.**

I. Introduction

Solar Photovoltaic (PV) is becoming the world's fastest-growing energy technology [1]. Nevertheless, PV-based power plants are, in many cases, still relatively expensive when compared with other conventional solutions like fossil fuels and nuclear power. In order to increase the PV penetration level, the cost of PV energy should be reduced further to a comparable level [2]. The cost of energy for a power generation system is usually referred to as the Levelized Cost of Energy (LCOE) [3], which can be expressed as

$$\text{LCOE} = \frac{C_{\text{Int}} + C_{\text{Cap}} + C_{\text{O\&M}}}{E_{\text{Annual}}} \tag{1}$$

where C_{Int} is the initial development cost, C_{Cap} represents the capital cost, $C_{\text{O\&M}}$ indicates the operational and maintenance cost, and E_{Annual} denotes the average annual energy production. It can be seen from (1) that a highly efficient and reliable system will contribute to a lower LCOE, as the operational and maintenance cost is reduced, while the energy yield is increased. Additionally, a proper design of the entire system can reduce the initial outlays, and in turn, further lowering the LCOE. Recent studies have shown that the technology shift to 1500-V PV arrays offers opportunities to reduce the installation cost to a large extent [4]–[7], and then, the initial development cost becomes lower. The PV system with such a technology also has the potential to increase its efficiency due to the reduced ohmic losses on the DC wires. However, the increased DC voltage (compared to the conventional 1000-V technology) presents a challenge to the PV inverters in terms of design and control. More specifically, the efficiency and reliability may be affected (also, the energy generation), and eventually, the LCOE, according to (1).

For PV systems, an efficient and reliable power interfacing converter (i.e., the core of the PV power generation) will contribute to more energy yield and reduce the cost in maintenance, eventually, achieving a lower LCOE of PV energy, as aforementioned. One of the most expensive and vulnerable components in PV inverters are the semiconductor power devices. In most cases, the lifetime of power devices is limited by the thermal stress that occurs among their different materials [8], where failures due to cumulative bond-wire and solder-joint fatigue will occur after a certain number of power cycles. The lifetime of power devices for PV inverters can be significantly affected by their operating conditions, which include not only the different control strategies (e.g., maximum power point tracking (MPPT) [9] and constant power generation [10]) and the operational conditions (e.g., the 1500-V application environment and the topologies), but also the mission profiles. For the PV inverter, the solar irradiance and the ambient temperature are normally considered as the mission profile parameters, since they strongly influence the electrical and thermal loading condition of the PV inverter.

Accordingly, several attempts have been made to the reliability analysis of the power interfacing converters with the consideration of mission profiles [10]–[14]. Those studies provide lifetime evaluation at the component- or system-level, in which the main concerns are PV array sizing and panel degradation [11], [12], active and reactive power control [10], [13], and battery energy storage integration [14]. Nevertheless, the design for reliability (DfR) of power converters for PV application is still limited in the literature, and the prior-art discussions focused on single-phase PV inverters [15], [16], as well as the application of the wide bandgap (WBG) power devices [17]. These studies provide guidelines for the DfR of PV inverters with lower DC-link voltages (i.e., $<$ 1000 V). However, when it comes to 1500-V PV inverters, different insights may be offered, e.g., due to the multi-level topologies. This aspect, however, has not been discussed in the literature. Another challenge is due to the uneven distribution of loading among the power devices in the inverter. Thus, it is important to identify the critical lifetime limiting components to ensure

Manuscript received December 12, 2019; revised April 10, 2020 and June 6, 2020; accepted July 4, 2020. This work was supported under the research project – Reliable Power Electronic based Power Systems (REPEPS) by The Velux Foundations under Award No.: 00016591. *(Corresponding author: Yongheng Yang.)*

The authors are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: jhe@et.aau.dk; ars@et.aau.dk; yoy@et.aau.dk; fia@et.aau.dk).

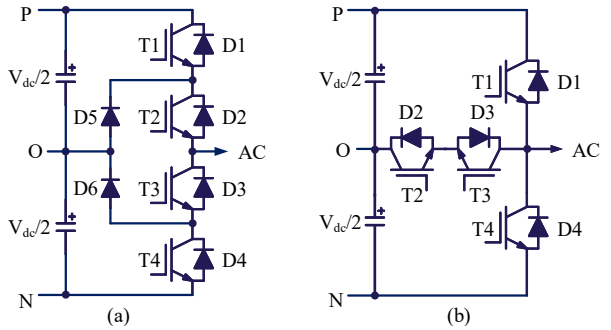

Fig. 1. Promising three-level topologies for the 1500-V PV applications: (a) I-type and (b) T-type, where the three switching states "P" (T1, T2: ON, T3, T4: OFF), "O" (T2, T3: ON, T1, T4: OFF), and "N" (T3, T4: ON, T1, T2: OFF), respectively produce the three output voltage levels, i.e., $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$.

a reliable power conversion, following which, a proper design of 1500-V PV systems can possibly be achieved.

Seen from the design perspective, the conventional two-level topology, which has been widely employed in 1000-V PV systems, may not be suitable for 1500-V PV systems, as the power losses and filtering efforts will be increased significantly [18], [19]. The industry standard three-level neutral point-clamped (NPC) topologies, namely, the I-type and the T-type topologies, as shown in Fig. 1, are promising candidates till present for the 1500-V PV systems. Furthermore, according to the comparisons of two- and three-level inverters in [20], for applications with lower DC-link voltages (i.e., $<$ 1000 V) and switching frequencies of 8 kHz to 20 kHz, the T-type inverter is a more suitable option due to its superior features in terms of efficiency and power quality. However, for 1500-V PV systems, due to the increased voltage stress, the T-type topology may not outperform the I-type topology in respect to efficiency and thermal performance. Hence, it is necessary to explore and benchmark the converter topologies for 1500-V PV applications. In [19] and [21], the comparisons of 1500-V inverters focused on the impact of switching frequency and module selection on the inverter efficiencies, respectively. Also, the thermal performance of the 1500-V PV inverters has been compared in [18], considering constant power generation. This paper extends these comparisons to include the lifetime performance of the three-level 1500-V PV inverters, which thus contributes to a systematic comparison with the aim to assist the design of 1500-V PV systems. Notably, the five-level topologies and the modular multilevel converters are also applicable to the 1500-V PV systems at the cost of an increased component count and control complexity [22].

With the above concerns, this paper thus evaluates the lifetime of three-level 1500-V PV inverters, i.e., the I-type and T-type topologies. A 160-kW PV system is considered as a case study, in which the impact of the DC-link voltage stress (i.e., up to 1500 V), the switching frequencies (2−6 kHz), and the mission profiles (Aalborg, Denmark, and Sacramento, California) on the lifetime of three-level inverter candidates is analyzed. The lifetime evaluation is firstly performed at the component level. Then, a system-level reliability assessment is carried out by using the reliability block diagram (RBD) and the Monte Carlo simulations. The results of the case study indicate that these factors have a considerable impact on the inverter lifetime. The T-type 1500-V PV inverter may be challenged in thermal performance even with switching frequencies between 4 kHz and 6 kHz. Furthermore, the mission profiles may also affect the topology selection. According to the results from the case study, the I-type inverter should be installed in Sacramento, while the T-type inverter is more suitable for the mission profiles from Aalborg.

TABLE I
PV SYSTEM SPECIFICATIONS.

Parameter	Value
Nominal power $P_{\rm nom}$	160 kW
Power factor $\cos(\varphi)$	1.0
Grid line-to-line RMS[1] voltage $V_{\rm LL}$	600 V
Grid frequency $f_{\rm g}$	50 Hz
Switching frequency $f_{\rm sw}$	2 − 6 kHz
Heatsink thermal impedance per module $R_{\rm th(s\text{-}a)}$	0.088 K/W

[1]Root Mean Square.

The rest of this paper is organized as follows: the description of the case study is provided in detail in Section II. The lifetime evaluation method is presented in Section III. Then, the lifetime evaluation for the case study is carried out in Section IV, followed by the Monte Carlo-based reliability assessment, which is provided in Section V. Finally, the concluding remarks are given in Section VI.

II. SYSTEM MODELING

A. System Description

In this paper, the JKM360M-72-V PV modules are employed to assemble the 1500-V PV arrays [23], with 432 PV modules (16 strings, 27 modules in each string). The rated power is around 160 kW with the DC-link voltage up to 1300 V. The three-level I-type or T-type inverter with a proper MPPT control is then employed as the interface between the PV array and the AC grid, as shown in Fig. 2. The system specifications are given in Table I, which are similar to the operation conditions in [19], where the efficiency of three-level 1500-V PV inverters are compared. The same power modules in [19] are selected for this case study, as shown in Table II. In addition, to evaluate the lifetime of the PV inverters under real operating conditions, two mission profiles in Aalborg (cold climate) and Sacramento (hot climate) are used in this case study, which are recorded by field data loggers [24] with a sampling rate of 1 min/sample. The mission profiles are shown in Fig. 3. As shown in Fig. 3(a), both the solar irradiance and ambient temperature in Aalborg vary in a wide range, where the average annual temperature is 9.88 °C. In contrast, the solar irradiance in Sacramento is relatively stable and higher than that in Aalborg, as shown in Fig. 3(b), and its average annual temperature is 16.56 °C.

With these operation conditions, the lifetime evaluation in this paper focuses on the power devices of the inverter candidates with a conventional space vector modulation (SVM)

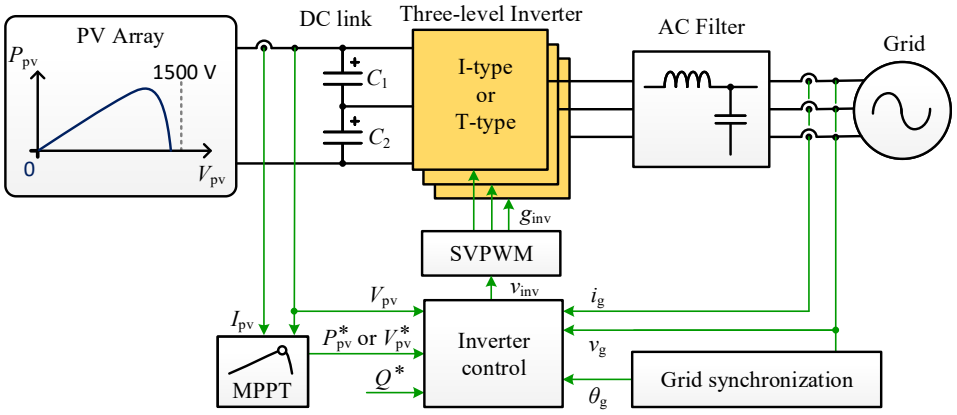

Fig. 2. General configuration and control structure of the 1500-V PV system based on the considered three-level topologies: P_{pv} – PV power, V_{pv} – PV voltage, I_{pv} – PV current, P^*_{pv} – active power reference, V^*_{pv} – DC-link voltage reference, Q^* – reactive power reference, i_g – grid current, v_g – grid voltage, θ_g – phase angle of the grid voltage, v_{inv} – output voltage of the inverter, g_{inv} – gate signals, MPPT – maximum power point tracking, and SVPWM – space vector pulse width modulation.

TABLE II
SELECTED IGBT MODULES FOR THE 1500-V PV INVERTERS.

Parameter	SEMiX305MLI12E4	SEMiX305TMLI17E4
Module type	I-type	T-type
Voltage rating (V)	1200	1700 / 1200
Current rating (A)	300	300
Junction temp. (°C)	-40 to 150	-40 to 150

strategy. For the I-type topology, all power devices need to withstand only half of the DC-link voltage during the blocking operation. On the other hand, the power devices T1 and T4 in the T-type topology (see Fig. 1(b)) must block the entire DC-link voltage. As a consequence, the I-type power module is equipped with 1200-V power devices, while the T-type power module employs a combination of 1700-V and 1200-V power devices for T1, T4, and T2, T3, respectively [25], as summarized in Table II. This difference in voltage stress can potentially affect the entire system performance, which will be explored in this paper. It should be pointed out that the lifetime of DC-link capacitors can also affect the reliability performance of the PV inverters [26], which is not included in this paper to simplify the analysis since the main difference of the inverter candidates is within the power devices.

B. Power Loss Analysis Considering Voltage Stress

To achieve the thermal modeling of the selected inverters, a power loss analysis should be performed. The conduction losses and switching losses of power devices can be modeled based on the forward voltage drop v_{CE} during conduction and the turn-on/-off energy E_{sw} during switching [27], [28]. The forward voltage drop of the device (e.g., IGBT or diode) can be expressed as

$$v_{CE} = V_{CE0} + \frac{V_{CEN} - V_{CE0}}{I_{CN}} i_C \tag{2}$$

where V_{CE0} represents the initial voltage drop, V_{CEN} is the voltage drop at the rated current I_{CN}, and i_C is the collector current. Then, the average conduction losses over one fundamental cycle can be obtained by integrating the product of the forward voltage drop and device current as [29]

$$P_{con} = \frac{1}{T_0} \cdot \int_0^{T_0} v_{CE}(t) \cdot i_C(t) dt \tag{3}$$

in which P_{con} is the average conduction losses and T_0 is the fundamental cycle.

The switching energy of power device can be obtained through experimental tests, and it is also provided in the device datasheet, which can be regarded as a reference of switching energy under specific gate driving parameters. Based on this reference, the switching energy E_{sw} during operation can be modeled as

$$E_{sw} = E_{sw(ref)} \left(\frac{i_C}{I_{C(ref)}} \right)^{k_i} \left(\frac{v_{CC}}{V_{CC(ref)}} \right)^{k_v} \tag{4}$$

where $E_{sw(ref)}$ is the reference value of the switching energy, $I_{C(ref)}$ and $V_{CC(ref)}$ are the reference conditions for the switching loss measurement (i.e., the collect current and collector-emitter supply voltage, respectively), v_{CC} is the actual collector-emitter supply voltage, k_i and k_v are the exponents for the current and voltage dependency of switching losses, respectively. According to [28], the typical values of k_i and k_v for the selected modules are summarized in Table III. The average instantaneous switching loss can then be obtained as [28]

$$P_{sw} = f_{sw} \cdot E_{sw(ref)} \left(\frac{i_C}{I_{C(ref)}} \right)^{k_i} \left(\frac{v_{CC}}{V_{CC(ref)}} \right)^{k_v} \tag{5}$$

with P_{sw} denoting the average instantaneous switching loss and f_{sw} being the switching frequency.

To further explain the power losses, Fig. 4 shows the variation of the voltage drop V_{CE} and switching energy E_{sw} of the IGBT T1 in both power modules under different collector currents I_C, which are based on the corresponding characteristic curves in the datasheets. It can be seen in Fig. 4 that the IGBT T1 in the I-type power module has smaller voltage drops and consumes lower switching energy. It should be mentioned that the switching energy reference $E_{sw(ref)}$ given

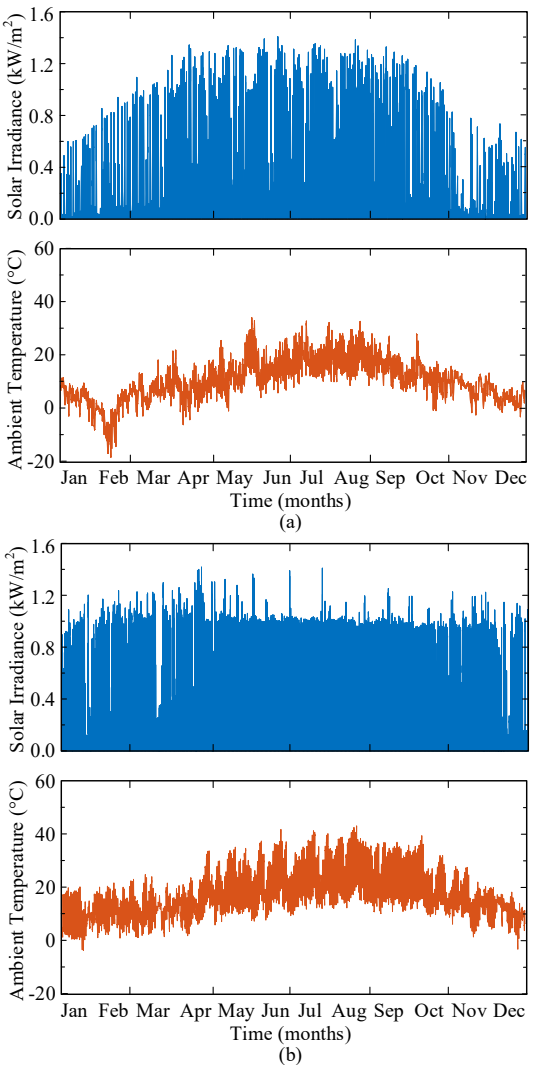

Fig. 3. One-year mission profiles (i.e., solar irradiance and ambient temperature) recorded in: (a) Aalborg and (b) Sacramento.

TABLE III
PARAMETERS OF THE CURRENT AND VOLTAGE DEPENDENCY OF SWITCHING LOSSES [28].

Parameter	IGBT	Diode
k_v	1.4	0.6
k_i	1.0	0.6

in the datasheet is measured when using the minimum permissible gate resistor [30]. In addition, the switching behaviors of both IGBT and diode are also affected by the gate resistor. Thus, the minimum value of the gate resistance should be designed. The relationship between the gate resistor, switching speed, and switching energy is illustrated in Fig. 5. As can be observed in Fig. 5, a smaller gate resistor means less switching energy losses, at the same time, it also means a faster switching speed. Nevertheless, the T-type inverter with 1700-V devices has a limited voltage blocking margin when compared with the I-type inverter with 1200-V devices. As a consequence, the switching speed (di/dt) of the T-type power module should

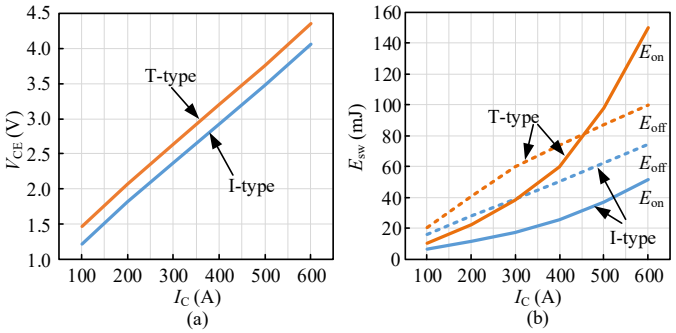

Fig. 4. Voltage drop V_{CE} and switching energy E_{sw} of the IGBT T1 in the selected power modules under different collector currents, when the junction temperature is 150 °C.

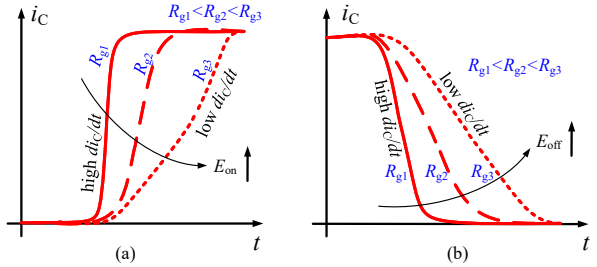

Fig. 5. Relationship between the gate resistor R_g, the switching speed di_C/dt, and the switching energy E_{on} and E_{off} of an IGBT during: (a) turn-on and (b) turn-off, where the subscript number (1, 2, 3) indicates different values of the gate resistor R_g.

be slowed down (by increasing the gate resistors) to reduce the switching overshoot due to the stray inductance in the commutation loops. In that case, the switching losses of the power devices in the T-type inverter may be considerably higher than those in the I-type inverter (when operating under the same conditions), which may cause higher power losses even at low switching frequencies (e.g., $\leq$ 8 kHz) [19].

The efficiency comparison for 1500-V three-level PV inverters under different switching frequencies is further carried out to show the impact of increased voltage stresses. The efficiencies of 1500-V three-level PV inverters with different gate driver parameters under various switching frequencies are shown in Fig. 6. It can be observed in Fig. 6 that the efficiency of the three-level T-type inverter with practical gate driver parameters are significantly lower than that with the gate driver parameters given in datasheets. In contrast, for the efficiencies of the three-level I-type inverter, there is almost no difference. Hence, a correction coefficient should be considered in (4) to scale the switching energy $E_{sw(ref)}$ of power modules for the three-level T-type inverter. In this study, the gate driver parameters of the T-type module are assumed to be the same as in [19]. Correspondingly, a correction coefficient of 1.4 is estimated (through the relationship between the switching losses and gate resistance in the device datasheet) to calibrate the switching energy of the T-type power module.

C. Thermal Modeling of I-type and T-type Inverters

To analyze the reliability, the thermal loading of the devices should be obtained first. In this regard, the thermal modeling

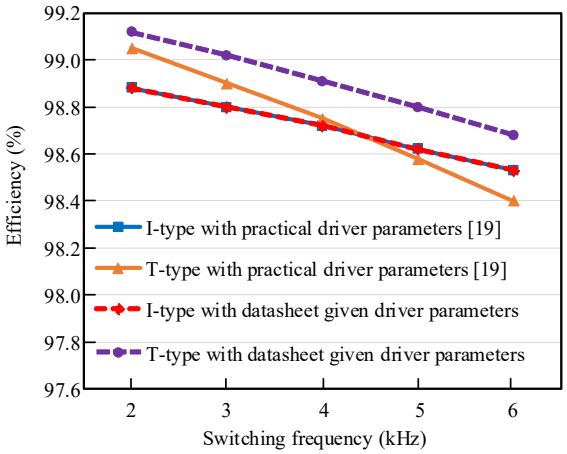

Fig. 6. Efficiencies of the 1500-V three-level PV inverters with different gate driver parameters under various switching frequencies.

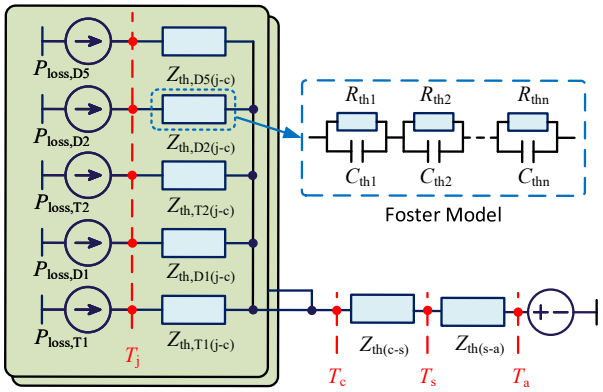

Fig. 7. Thermal model for the three-level I-type inverter: $Z_{th(j\text{-}c)}$ – junction-to-case thermal impedance, $Z_{th(c\text{-}s)}$ – case-to-heatsink thermal impedance, $Z_{th(s\text{-}a)}$ – heatsink-to-ambient thermal impedance, T_j – junction temperature, T_c – case temperature, T_s – heatsink temperature, T_a – ambient temperature, R_{th} – thermal resistance, and C_{th} – thermal capacitance. Notably, the thermal model for the three-level T-type inverter can be obtained by removing the model for diode D5.

of the corresponding power device should be performed. Fig. 7 shows the thermal model of the I-type power module. The thermal model for the T-type inverter can be obtained by removing the model for the diode D5. Notably, referring to Fig. 1, the thermal model of the lower arm is not shown in Fig. 7 due to the symmetrical structure (i.e., the upper and lower arms in one-phase of the three-level topology are symmetrical). The junction temperature of IGBTs or diodes can be modeled according to the method in [31], where the Foster thermal RC network is used to model the thermal impedance from junction to case (i.e., $Z_{th(j\text{-}c)}$), as shown in Fig. 7. The instantaneous value of the junction temperature can then be expressed as [31]

$$T_j(t) = P_{tot(T/D)}\,(t) \cdot Z_{th(j\text{-}c)}(t) + T_c(t) \tag{6}$$

$$T_c(t) = P_{tot(s)}(t) \cdot [Z_{th(c\text{-}s)}(t) + Z_{th(s\text{-}a)}(t)] + T_a(t) \tag{7}$$

where T_c and T_a are the case temperature and ambient temperature, respectively, $Z_{th(j\text{-}c)}$ is the junction-to-case thermal impedance, $Z_{th(c\text{-}s)}$ and $Z_{th(s\text{-}a)}$ are the thermal impedances of case-to-heatsink and heatsink-to-ambient, respectively, $P_{tot(T/D)}$ is the total power losses of a single IGBT or diode inside the power module, and $P_{tot(s)}$ represents the total power losses transferred to the heatsink. The RC parameters of the Foster model (i.e., R_{th} and C_{th} in Fig. 7) can be obtained by using the curve-fitting technique on the transient thermal impedance curves in the datasheets [32]. The Foster model parameters for the selected IGBT modules are summarized in Table IV, where all the thermal impedance is modeled as a three-layer RC network. The thermal resistance (R_{thi}) and capacitance parameters (time constant τ_i) in the Foster model determine the steady-state mean value and transient responses of the junction temperature, respectively.

TABLE IV
FOSTER THERMAL PARAMETERS FOR THE SELECTED IGBT MODULES.

Power Module	Impedance		$Z_{th(j\text{-}c)}$		
	Order(i)		1	2	3
I-type	T1-4	R_{thi} (K/W)	0.0240	0.0461	0.0305
		τ_i (s)	0.0087	0.0443	0.1473
	D1-6	R_{thi} (K/W)	0.0193	0.0540	0.1059
		τ_i (s)	0.0064	0.0176	0.0911
T-type	T1,4	R_{thi} (K/W)	0.0453	0.0255	0.0091
		τ_i (s)	0.0960	0.0195	0.0065
	D1,4	R_{thi} (K/W)	0.0751	0.0537	0.0409
		τ_i (s)	0.1107	0.0359	0.0090
	T2,3	R_{thi} (K/W)	0.0367	0.0665	0.0165
		τ_i (s)	0.0213	0.0962	0.0069
	D2,3	R_{thi} (K/W)	0.1426	0.0234	0.0447
		τ_i (s)	0.0711	0.3774	0.0106

A detailed thermal stress analysis is carried out through simulations in the MATLAB-PLECS co-simulation environment, where the impact of the junction temperature on the conduction and switching losses has also been considered [28]. Fig. 8 shows the loss distributions of the selected power modules under the steady-state operation (i.e., f_{sw} = 6 kHz, P_{in} = 160 kW, unit power factor, and T_a = 25 °C), which is similar to those in [20]. For both the I-type and T-type topologies, the IGBT T1/T4 experiences the highest losses. This is mainly due to their straightforward switching mode [33], which means that each level of the inverter output voltage only has one corresponding switching state (referring to Fig. 1). When the switching state changes between P and O in the positive half-cycle of the AC output voltage, the IGBT T1 operates under the switching frequency while keeping the IGBT T2 in ON state. Moreover, the current path will change between following through T1 and the clamping diode D5 in the I-type topology (or the series connection of T2 and D3 in the T-type topology). Hence, the switching losses in T1 are much larger than those in T2, especially in the T-type topology, which suffers from higher switching losses due to its higher voltage rating. A similar mechanism is also applied to the IGBT T3 and T4 during the negative half-cycle. A comparison of the thermal loadings is shown in Fig. 9. The

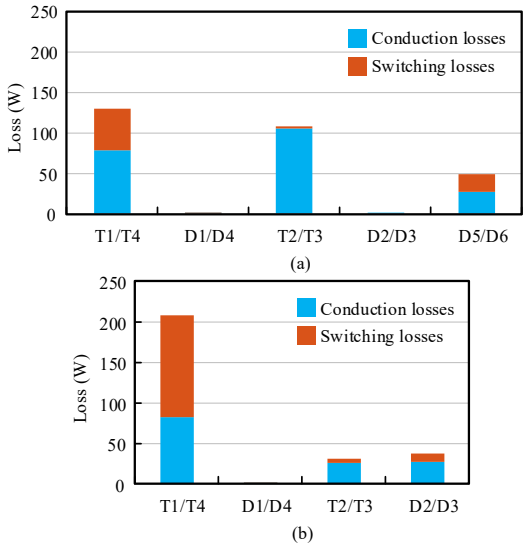

Fig. 8. Loss distribution on the individual devices (referring to Fig. 1, f_{sw} = 6 kHz, P_{in} = 160 kW, and T_a = 25 °C): (a) I-type and (b) T-type.

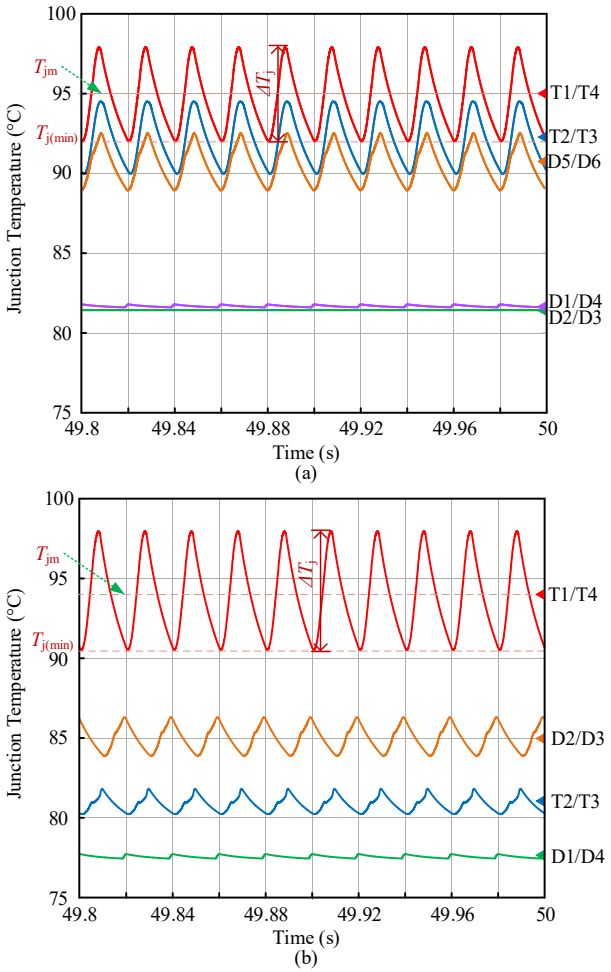

Fig. 9. Thermal loading of the power modules in the considered inverters (seeing in Fig. 1) with f_{sw} = 6 kHz, P_{in} = 160 kW, and T_a = 25 °C: (a) I-type and (b) T-type, where $T_{j(min)}$ and T_{jm} are the minimum and mean junction temperature, respectively, and ΔT_j is the cycle amplitude of the junction temperature.

thermal response of the power devices is proportional to their losses. For the I-type topology, the IGBT T1/T4 are the most stressed devices, followed by IGBT T2/T4, diode D5/D6, and diode D1/D2, as observed in Fig. 9(a). For the T-type topology, the thermal stress in descending order is IGBT T1/T4, diode D2/D3, IGBT T2/T3, and diode D1/D4, as seen in Fig. 9(b). The thermal distributions (especially inside the T-type power module) are clearly unequal in the inverter. As the maximum output power is limited by the most stressed devices, the entire converter or system performance is then dependent on the thermal performance. Moreover, the system-level reliability of the inverters will be affected, which will be discussed in Section V.

III. Lifetime Evaluation

The general steps to estimate the lifetime of the 1500-V PV inverters under mission profiles are shown in Fig. 10. First, the thermal stress of the power modules in PV inverters should be acquired for a certain set of operating conditions (the voltage and current inputs of the loss model should be based on the MPPT operation of PV arrays) to build lookup tables for long-term mission profile translation [31]. Then, the thermal loading of the power modules can be obtained. Afterward, an appropriate lifetime model for the power modules can be applied, and their lifetime can be estimated.

Several empirical lifetime models for the power modules are available in the previous studies [34]–[36]. The LESIT lifetime model in [34] does not cover the factor of heating time t_{on}, and the SEMIKRON model in [35] is specific for the SKiM63 IGBT module. The CIPS2008 model in [36] is one of the recent refined lifetime models, which is based on a large number of power cycling data from different IGBT module generations and test conditions (CIPS2008 project). It contains multiple variables for lifetime evaluation, and the ratings and technology of the power modules in the CIPS2008 project are comparable to the ones in our case study. Hence, the CIPS2008 lifetime model [36] is used in this paper. The CIPS2008 lifetime model provides a simple relationship between the number of cycles to failure N_f under a certain thermal stress (i.e., minimum junction temperature $T_{j(min)}$ and cycle amplitude ΔT_j), which is expressed as

$$N_f = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j(min)} + 273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{8}$$

where the technology fact A, heating time t_{on}, current per bond wire I, blocking voltage V, and bond wire diameter D are considered, as presented in Table V. Additionally, in (8), β_1-β_6 are the model parameters, which are also given in Table V. More details of the model are discussed in [36]. Fig. 11 shows the graph of the function N_f for the selected 1200-V and 1700-V IGBTs under certain heating time and different thermal stresses. It can be observed in Fig. 11 that the logarithm of N_f is proportional to the logarithm of ΔT_j, and the 1700-V device will withstand less power cycles than the 1200-V device, which potentially affect the reliability performance of 1500-V PV inverter with the 1700-V T-type power module.

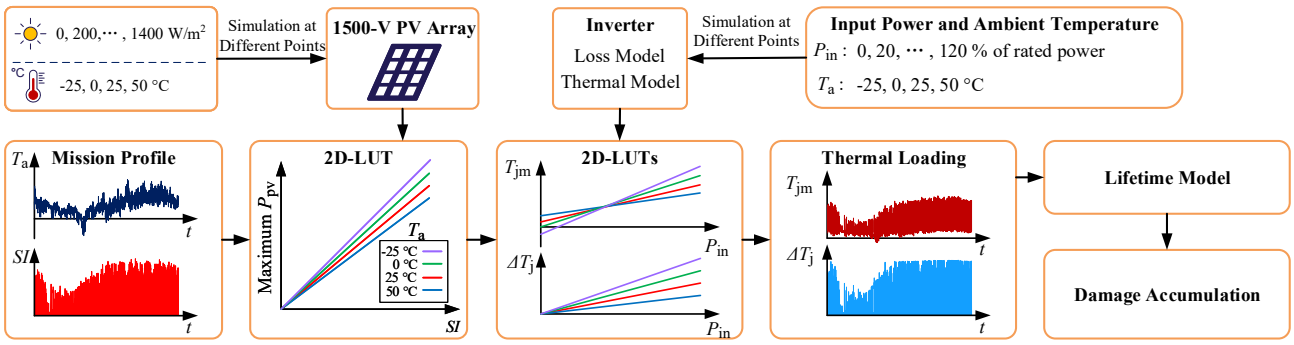

Fig. 10. Block diagram of the reliability evaluation process for the power devices: T_a – ambient temperature, SI – solar irradiance, P_{pv} – PV output power, LUT – lookup table, T_{jm} – mean junction temperature, and ΔT_j – cycle amplitude of the junction temperature.

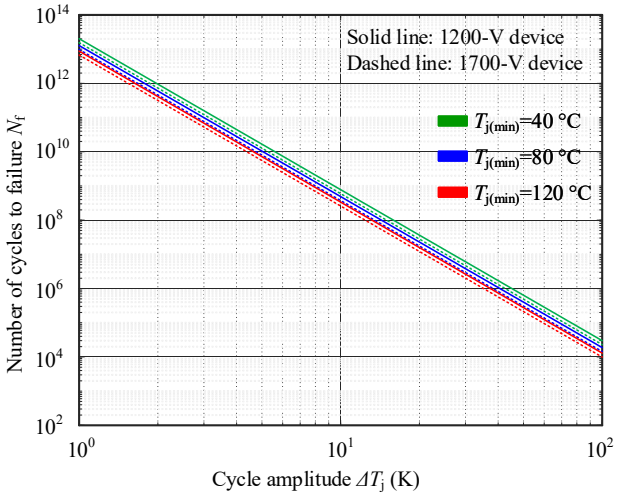

Fig. 11. Number of cycles to failure N_f for 1200-V and 1700-V IGBTs under different thermal stresses: T_{jm} – minimum junction temperature, and ΔT_j – cycle amplitude of the junction temperature.

It should be mentioned that the power cycling tests in the CIPS2008 project were performed with the heating time of 1 s to 15 s. In order to further extend the validity of t_{on} to 0.1 - 60 s, as an approximation, a derating factor is considered, which is given as [37]

$$\frac{N_f(t_{on})}{N_f(1.5\text{ s})} = \left(\frac{t_{on}}{1.5\text{ s}}\right)^{-0.3} \tag{9}$$

in which $N_f(t_{on})$ represents the number of cycles to failure under the real heating time t_{on}, and $N_f(1.5\text{ s})$ denotes the reference number of cycles to failure under the heating time being 1.5 s.

Normally, the lifetime of the power device is expressed in terms of lifetime consumption (LC), which indicates how much lifetime has been consumed during the operation. In this study, a widely-used damage model, i.e., according to the Miner's rule [38], is adopted for the LC calculation, which is expressed as

$$LC = \sum_i \frac{n_i}{(N_f)_i} \tag{10}$$

TABLE V
PARAMETERS OF THE CIPS2008 LIFETIME MODEL [36].

Parameter	Value / Test condition
Technology factor A	9.34×10^{14}
Minimum junction temperature $T_{j(min)}$	20 °C $\leq T_{j(min)} \leq$ 120 °C
Cycle amplitude ΔT_j	45 K $\leq \Delta T_j \leq$ 150 K
Heating time t_{on}	1 s $\leq t_{on} \leq$ 15 s
Current per bond wire I	3 A to 23 A
Voltage class/100 V	6 V to 33 V
Bond wire diameter D	75 μm to 500 μm
Coefficient β_1-β_3	{-4.416, 1285, -0.463}
Coefficient β_4-β_6	{-0.716, -0.761, -0.5}

in which n_i is the number of cycles under certain thermal stress, and $(N_f)_i$ is the corresponding number of cycles to failure according to the lifetime model. The damage model in (10) assumes that various thermal loading events are independent, and the impact of the damage can be linearly accumulated [3], [38]. When the LC exceeds one, the component is considered to reach its end of life.

IV. CASE STUDY

As discussed in Section III, before the lifetime evaluation, the thermal loadings of the power devices should be obtained from the mission profiles. Considering the lifetime of IGBT modules is limited by the most stressed device, only the thermal loading and LC of the IGBT T1/T4 in both topologies have been analyzed in this section. The analysis of the other IGBTs and diodes will be considered within the system-level reliability assessment in the next section. The one-year thermal loadings of the IGBT T1/T4 in the two topologies for the switching frequency of 6 kHz are shown in Fig. 12. As it can be seen in Fig. 12, the IGBT T1/T4 in Sacramento suffers from higher thermal stresses than that in Aalborg due to its average higher solar irradiance and ambient temperature. Furthermore, as observed in Fig 12, the cycle amplitude of the IGBT T1/T4 in the T-type topology is higher than that in the I-type topology. It can be expected that the LC of the IGBT T1/T4 within the T-type inverter will be higher than that in the I-type inverter.

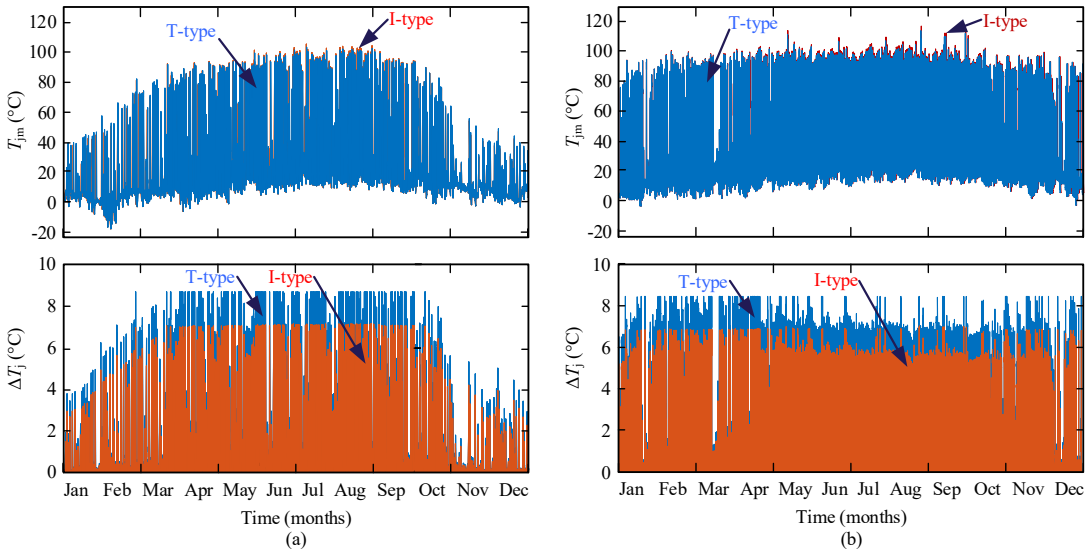

Fig. 12. Thermal loadings (i.e., mean junction temperature T_{jm} and cycle amplitude ΔT_j referring to Fig. 9) of the IGBT T1/T4 in the two topologies for a switching frequency of 6 kHz under a yearly mission profile in: (a) Aalborg and (b) Sacramento.

1) Damage Caused by the Line-Frequency Power Cycling: Since the mission profiles have been recorded with a sampling rate of 1 min/sample. The LC in every minute, due to line-frequency power cyclings (i.e., 50 Hz), can be regarded as a fraction of the total one-year LC. Hence, based on the Miner's rule, the accumulated LC is calculated as

$$LC = \sum_i \frac{n_i}{(N_f)_i} = \sum_i \frac{50 \times 60}{(N_f)_i} \tag{11}$$

where n_i equals to the number of 50-Hz power cyclings in one minute (i.e., 50×60). Notably, similar to [8], it is assumed that the cycle period extension with (9) can also be applied here, i.e., t_{on} = 0.01 s (50% of the fundamental period), and then, $(N_f)_i$ can be calculated according to (8) and (9). The heating time is fixed at 0.01 s, while the minimum junction temperature and its cycle amplitude can be obtained by extracting the sampling points on the thermal loading profiles. The obtained results are summarized in Table VI.

2) Damage Caused by the Low-Frequency Thermal Cycling: Since the mean junction temperature profiles under mission profiles, as shown in Fig. 12, are irregular. In order to categorize the irregular thermal cycles into several regular cycles, a rainflow counting analysis [39] is performed to obtain the number of cycles n_i at a certain cycle amplitude, mean junction temperature, and cycle period t_{cyc} (i.e., $2t_{on}$). The rainflow counting results of the mean junction temperature profiles in Fig. 12 are shown in Fig. 13. The period of each thermal cycle is also obtained from the rainflow analysis, as shown in Fig. 13(c) and (f), where a total of 121,699 and 62,890 cycles have been identified, respectively, and the period of these cycles can vary from minutes to tens of days. Nevertheless, since the CIPS2008 model does not cover the lifetime of the soldered joints (between substrate and base plate) and focuses on the bond wire fatigue only, the maximum heating time t_{on} is limited to 60 s (i.e., if $t_{on} > 60$ s, then $t_{on} = 60$ s). This approximation is based on the assumption that the viscoplastic deformation saturates when $t_{on} > 60$ s [37]. Similarly, the rainflow counting results are applied to the linear damage model in (10) to calculate the accumulated damage caused by the low-frequency thermal cyclings. The obtained results are summarized in Table VI.

Applying the above LC calculation, the total one-year LC of the selected power devices can be compared under the considered mission profiles and operating switching frequencies. The results are shown in Fig. 14. Under the mission profile of Sacramento, for the switching frequencies between 4 and 6 kHz, the IGBT T1/T4 in the I-type inverter has lower LC. In the case of Aalborg, the IGBT T1/T4 in the I-type inverter also has lower LC for the 6 kHz switching frequency. However, for the switching frequencies between 2 and 4 kHz, the T-type inverter in Aalborg is a better choice due to its lower LC of the IGBT T1/T4.

Two conclusions can be drawn from the above LC comparison: 1) for 1500-V PV systems, due to the increased voltage stress, the I-type topology is better than the T-type topology in terms of lifetime performance even in low switching frequencies (e.g., 4 kHz to 6 kHz) and 2) the operation conditions, i.e., switching frequency and mission profile, have a considerable impact on the lifetime of power modules for three-level 1500-V PV inverters. It should be noted that the estimated LC is obtained under a number of assumptions (e.g., MPPT control, unit power factor, and linear cumulative damage) for a qualitative comparison.

V. Reliability Assessment

With the one-year LC of the power devices calculated in the previous section, the corresponding time-to-failure of the power devices can be obtained as certain fixed values. This is typically far from reality since the variations (uncertainties) in device parameters and experienced thermal stresses are not considered. In practice, the time-to-failure of power devices may vary within a range due to these uncertainties. Therefore, the lifetime prediction is usually expressed in terms of a statistical value rather than a fixed value. In this section, a statistical

TABLE VI
ONE-YEAR LIFETIME CONSUMPTION.

Mission profile	Power module	t_{on}	Switching frequency		
			2 kHz	4 kHz	6 kHz
Aalborg	I-type	0.01 s	0.0002 (0.02%)	0.0005 (0.05%)	0.0009 (0.09%)
		60 s	0.0027 (0.27%)	0.0044 (0.44%)	0.0070 (0.70%)
	T-type	0.01 s	0.0003 (0.03%)	0.0009 (0.09%)	0.0032 (0.32%)
		60 s	0.0012 (0.12%)	0.0035 (0.35%)	0.0087 (0.87%)
Sacramento	I-type	0.01 s	0.0014 (0.14%)	0.0025 (0.25%)	0.0051 (0.51%)
		60 s	0.0026 (0.26%)	0.0041 (0.41%)	0.0063 (0.63%)
	T-type	0.01 s	0.0014 (0.14%)	0.0050 (0.50%)	0.0164 (1.64%)
		60 s	0.0013 (0.13%)	0.0033 (0.33%)	0.0078 (0.78%)

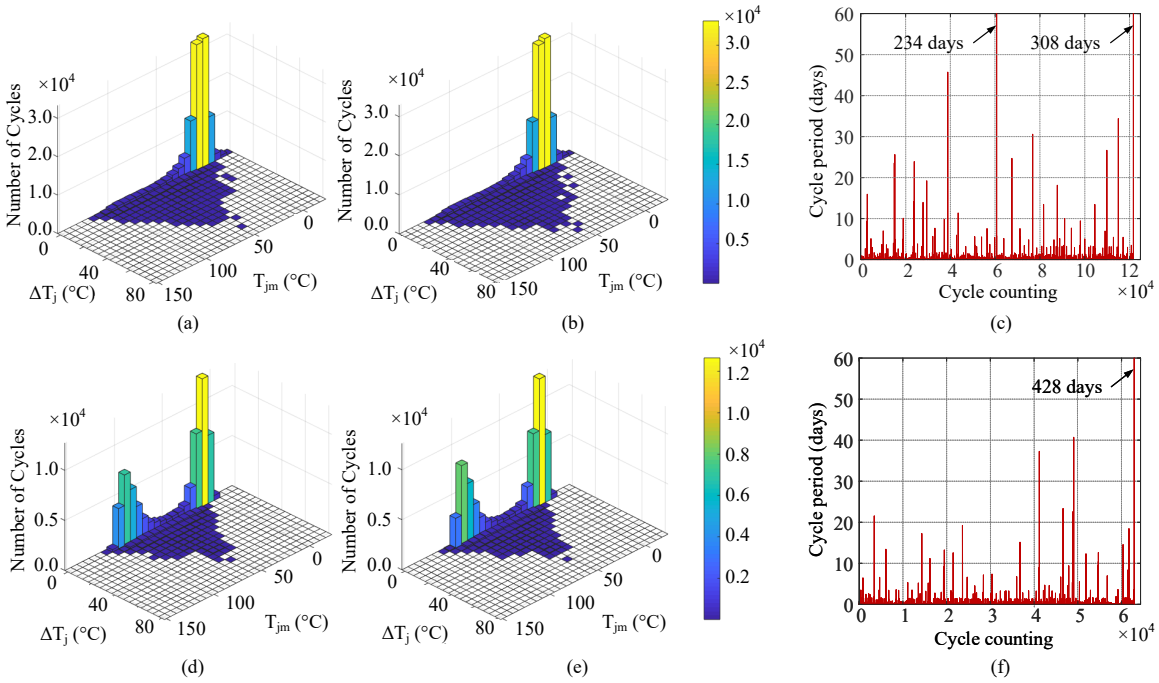

Fig. 13. Rainflow counting results of the thermal loadings of the IGBT T1/T4 in the two topologies for a switching frequency of 6 kHz under yearly mission profiles: (a) I-type in Aalborg, (b) T-type in Aalborg, (c) cycle period in Aalborg, (d) I-type in Sacramento, (e) T-type in Sacramento, and (f) cycle period in Sacramento.

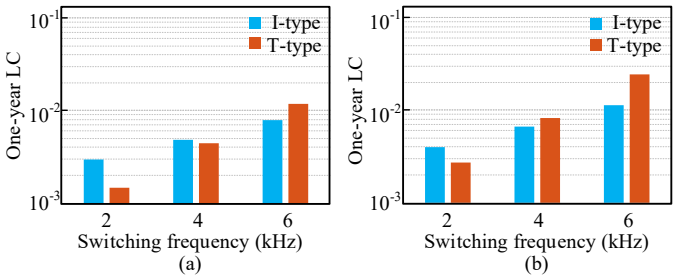

Fig. 14. Impact of the switching frequency on the one-year lifetime consumption under mission profiles in: (a) Aalborg and (b) Sacramento, where the inverters shown in Fig. 1 are employed.

approach based on the Monte Carlo analysis [8], [40], [41] is applied, as shown in Fig. 15. By doing so, the variations in model parameters and thermal stresses can be introduced to represent the uncertainties. Then, the distribution of power device lifetime can be obtained. Moreover, the system-level reliability assessment can be performed by using the reliability block diagram (RBD) [3], [40], [42]. The obtained lifetime results can be used in a comparative way to evaluate the impact of PV inverter topologies on the lifetime expectation of PV inverter systems.

A. Determination of Variations in Thermal Stresses and Lifetime Model

In order to apply the Monte Carlo analysis, two types of variations have been introduced: 1) parameter variations in the selected lifetime model (i.e., the parameters in Table V), and 2) thermal stress variations (i.e., $T_{j(min)}$, ΔT_j, and t_{on}). Regarding the first type of variations, in this study, all the parameters in Table V are assumed to have a 5% variation with a 99%-confidence level. While for the second type of variations, since the thermal stresses change dynamically over the whole year,

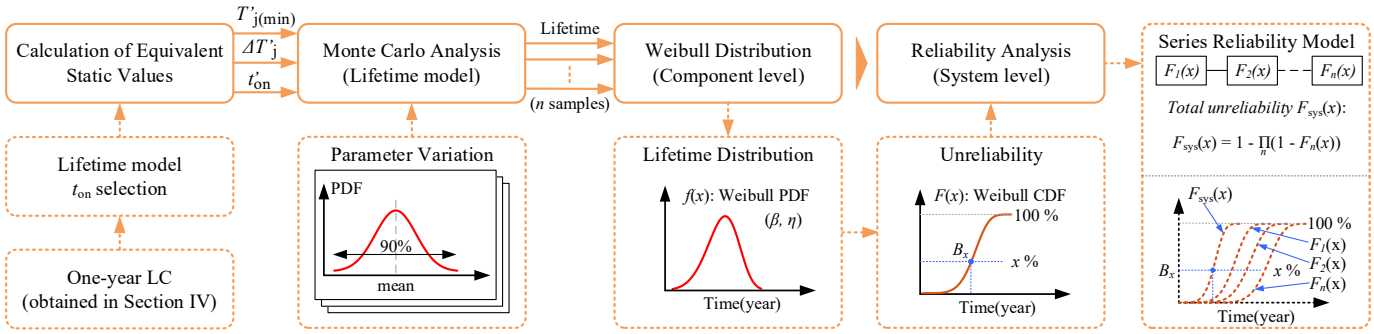

Fig. 15. Flow diagram of the reliability assessment of PV inverters with the Monte Carlo analysis and reliability block diagram: LC – lifetime consumption, t_{on} – heating time, $T'_{j(min)}$ – equivalent minimum junction temperature, $\Delta T'_j$ – equivalent cycle amplitude, t'_{on} – equivalent heating time, $f(x)$ – Weibull probability density function (PDF), β – sharp parameter, η – scale parameter, $F(x)$ – cumulative density function (CDF), $F_i(x)$ – unreliability function of the i^{th} device in the system, $F_{sys}(x)$ – total unreliability of the system, and B_x – operation time when x % of the populations fail.

these dynamic parameters (i.e., $T_{j(min)}$, ΔT_j, and t_{on}) have been converted into equivalent static ones (i.e., $T'_{j(min)}$, $\Delta T'_j$, and t'_{on}), which can produce the same one-year LC when applying them to the LC calculation process in Section IV. There are several possible combinations of equivalent static stress parameters that can be applied to the lifetime model and produce the same LC. In this study, only the line-frequency (i.e., t'_{on} = 0.01 s) thermal cycling is considered for simplicity. Then, the equivalent minimum junction temperature $T'_{j(min)}$ can be obtained by simply averaging the yearly thermal loadings in Fig. 12, which is one simple solution to represent a yearly dynamic temperature. After that, the corresponding static value of $\Delta T'_j$ can be calculated by solving (8)-(10). The obtained results with the switching frequency of 6 kHz are summarized in Table VII. It should be mentioned that the devices with relatively low thermal stresses (i.e., diode D1/D4 and D2/D3 in the I-type topology, and D1/D4 in the T-type topology) are neglected since they have a negligible impact on the system-level reliability assessment. Once the equivalent static stress parameters are determined, their variations can be modeled with a normal distribution function [40], [41], which are the same as the variations introduced to the lifetime model parameters.

B. Lifetime Distribution (Component Level)

With the variations obtained in the previous section, the lifetime distribution of the power devices in Table VII is analyzed individually based on the Monte Carlo simulations with a population of 10,000 samples (a typical number of samples to obtain accurate simulation results). The lifetime distributions for the switching frequency of 6 kHz with the mission profile in Aalborg and Sacramento are shown in Figs. 16 and 17, following the Weibull distribution [43]. It can be observed in Figs. 16 and 17 that the lifetime distributions of power devices within the I-type topology have larger overlapped areas than those of the power devices within the T-type topology, in which the lifetime of the IGBT T1 is much lower than that of the IGBT T2 and diode D2. The relatively serious uneven lifetime distributions of the T-type topology, especially under the more severe mission profile of Sacramento as shown in Figs. 16 (b) and 17 (b), can make it in an inferior position when comparing the reliability of these two topologies both at the component level and system level (will be discussed in the next subsection). This is mainly caused by the high stressed 1700-V IGBTs within the T-type topology. It is worth to mention that the T-type inverter may achieve better thermal performance by replacing the 1700-V IGBTs with 1700-V silicon carbide (SiC) MOSFETs, while the total hardware cost will inevitably be increased [44]. In such a case, as the SiC-based devices/modules follow different failure modes and mechanisms compared with the Si counterparts, new lifetime models are needed to properly analyze their reliability [45], [46]. In addition, for the I-type inverter, the IGBT T1 may not always be the most fragile device. As shown in Fig 16, i.e., the I-type inverter with the Aalborg mission profile, the average lifetime of the diode D5 is even lower than that of the IGBT T1 (while the thermal stress of the former is lower than that of the latter as shown in Fig. 9). The main reason behind this is that a derating factor of 0.59 has been considered in the lifetime model for the 1200-V diodes, since their chip thickness is much higher than that of the 1200-V IGBTs, resulting in a considerable reduction in their lifetime performance [35].

C. Reliability Analysis

From the lifetime distribution of the power devices, the reliability of the I-type and T-type inverters can be evaluated both at the component level and system level by using the cumulative density function (CDF) of the Weibull distribution. This is usually referred to as the unreliability function (the proportion of failures as a function of operation time) and it can be expressed as

$$F(x) = \int_0^x f(x)dx, \quad f(x) = \frac{\beta}{\eta}\left(\frac{x}{\eta}\right)^{\beta-1} e^{-\left(\frac{x}{\eta}\right)^{\beta}} \tag{12}$$

in which $F(x)$ and $f(x)$, respectively, represent the unreliability function and the probability density function (PDF) of the Weibull distribution with x, η, and β being the operation time, the scale parameter, and the shape parameter. Then, the power device lifetime or the system lifetime can be predicted in terms of B_x lifetime, which represents the operation time

TABLE VII
EQUIVALENT STATIC VALUES OF THE STRESS PARAMETERS WITH 6 KHZ SWITCHING FREQUENCY.

Parameters	Aalborg						Sacramento					
	I-type			T-type			I-type			T-type		
	T1	T2	D5	T1	T2	D2	T1	T2	D5	T1	T2	D2
Junction temperature $T'_{j(min)}$ (°C)	16.95	16.73	16.70	17.11	16.00	16.40	36.58	36.00	35.76	36.43	33.36	34.51
Cycle amplitude $\Delta T'_j$ (°C)	5.49	5.23	5.07	5.66	4.64	4.67	5.59	5.02	4.77	6.25	4.33	4.34
Heating time t'_{on} (s)	0.01											
Number of cycles per year n_i	$(365 \times 24 \times 60 \times 60) \times 50$											
One-year LC	0.0079	0.0064	0.0094	0.0119	0.0037	0.0065	0.0114	0.0070	0.0095	0.0242	0.0035	0.0061
Lifetime prediction (year)	127	157	106	84	270	153	88	143	105	41	284	164

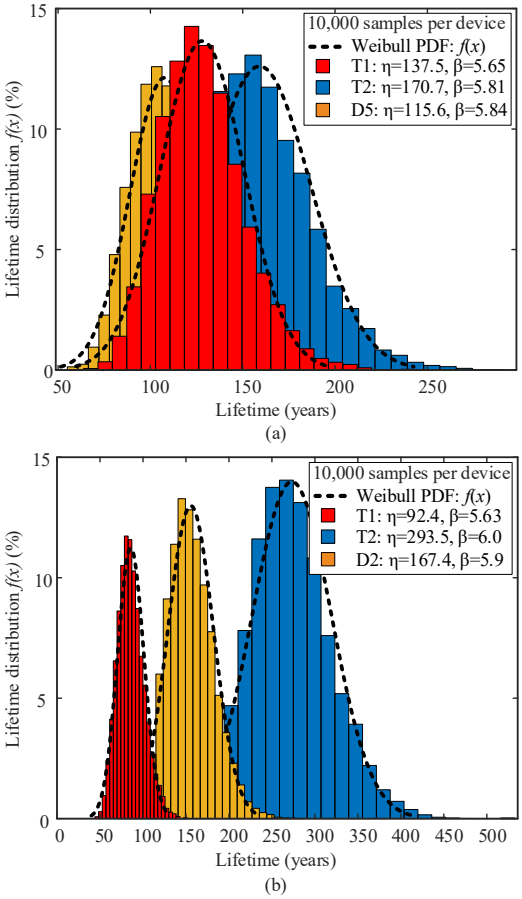

Fig. 16. Lifetime distribution of the power devices in the two topologies under the Aalborg mission profile: (a) I-type and (b) T-type.

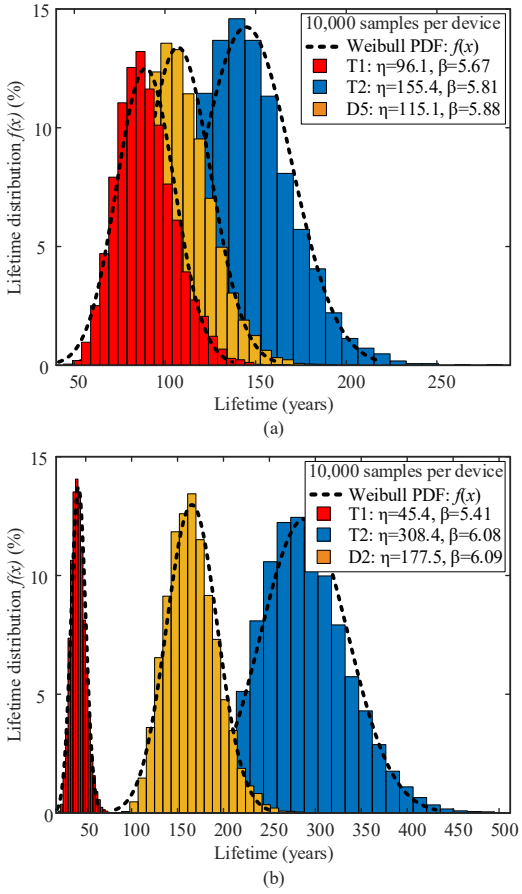

Fig. 17. Lifetime distribution of the power devices in the two topologies under the Sacramento mission profile: (a) I-type and (b) T-type.

when $x\%$ of the populations fail. Regarding the system-level reliability assessment, as mentioned previously, the RBD can be employed, which describes the reliability interaction between each device in the system [42]. For the I-type and T-type inverters, if any of the IGBTs or diodes fails, it would result in the inverters not being able to operate with the designed ratings (e.g., the output voltage/power will be reduced [47], [48]) and expected performance. Thus, the fault-tolerant operation of three-phase three-level inverters was discussed in [49], which is not considered in this paper, and the system-level reliability analysis is done with a series connection of the component-level RBDs, as illustrated in Fig. 18. The total unreliability of the system $F_{\text{sys}}(x)$ can be expressed as

$$F_{\text{sys}}(x) = 1 - \prod_{i=1}^{n} (1 - F_i(x)) \tag{13}$$

in which $F_i(x)$ represents the unreliability function of the i^{th} device in the inverters.

The component-level and system-level unreliability functions of the three-level inverters with the switching frequency of 6 kHz under the mission profiles are shown as the dashed and solid lines, respectively, in Figs. 19 and 20. The system-

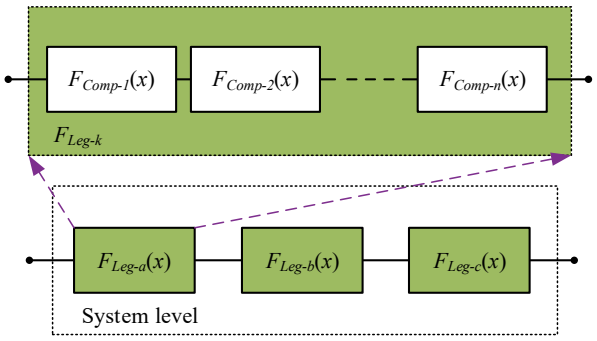

Fig. 18. Series connection of the reliability block diagram of a three-phase three-level inverter, where $F_{Comp\text{-}i}(x)$ represents the unreliability function of the i^{th} device in the inverter leg and the subscript *Leg-k* denotes the a, b, or c phase.

TABLE VIII
RESULTS OF SYSTEM-LEVEL RELIABILITY ASSESSMENT.

Mission profile	Topology	B_x lifetime (year)	switching frequency 2 kHz	4 kHz	6 kHz
Aalborg	I-type	B_{10}	142	86	54
		B_1	97	58	35
	T-type	B_{10}	381	123	44
		B_1	264	83	29
Sacramento	I-type	B_{10}	118	77	45
		B_1	80	52	30
	T-type	B_{10}	210	66	22
		B_1	144	44	14

level B_x (i.e., B_1 and B_{10}) lifetime is also indicated in Figs. 19 and 20 and summarized in Table VIII. As can be observed in Figs. 19 and 20, and Table VIII, the B_x lifetime can vary within a wide range reflecting the impact of mission profiles on the three-level inverter candidates. For the switching frequency of 6 kHz, the three-level I-type inverter is a better choice for both mission profiles, especially in Sacramento. In such a case, the T-type inverter is not recommended for the given heatsink condition in Table I, due to its relatively low B_x lifetime.

The B_1 and B_{10} lifetime for the switching frequency of 2 kHz and 4 kHz are also summarized in Table VIII. The results are in accordance with the LC comparison in Section IV. For the switching frequency of 2 kHz, both three-level inverter candidates can achieve high B_x lifetime under the two mission profiles, especially for the T-type inverter. In contrast, the I-type inverter is the promising candidate with better system-level reliability for the switching frequency of 6 kHz, especially for the mission profile of Sacramento, where the B_x lifetime is more than twice that of the T-type inverter. While for a switching frequency in-between (e.g., 4 kHz), the topology selection for a better reliability performance may be dependent on the mission profiles. For the case study in this paper, the T-type inverter is more suitable for Aalborg, while the I-type inverter should be considered for Sacramento in this case. It should be noted that the verification of the actual lifetime is still an open challenge [50]. However, the estimated lifetime results in this paper can still be used for a qualitative comparison among different topologies. In order words, it is still beneficial for the design of 1500-V PV systems.

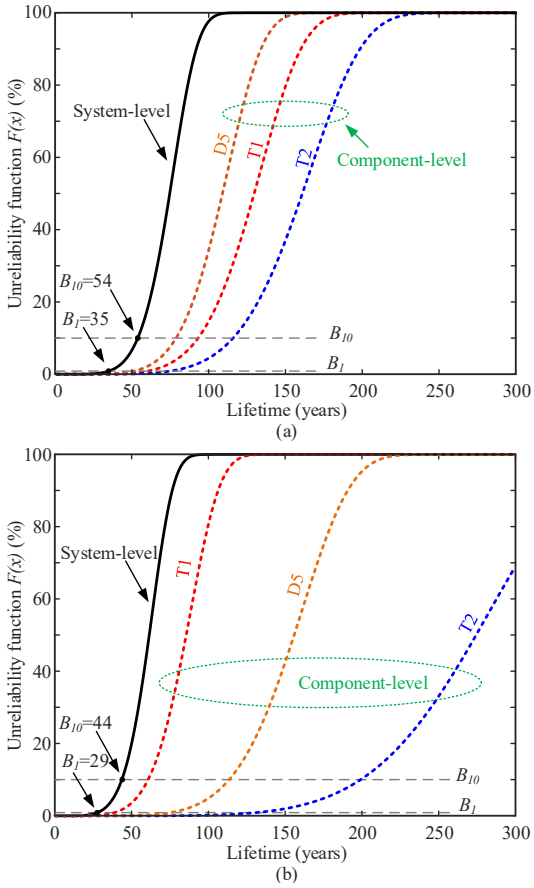

Fig. 19. Unreliability function of the PV inverters under the Aalborg mission profile: (a) I-type and (b) T-type.

VI. CONCLUSION

In this paper, the lifetime of the three-level 1500-V PV inverters was evaluated under two different mission profiles and various switching frequencies at the component level and system level. The evaluation is based on the thermal stress analysis of the two three-level topologies (i.e., I-type and T-type) considering the high voltage stress in 1500-V PV applications. The results reveal that these factors have a considerable impact on the inverter lifetime and reliability. The obtained evaluation results can be used to justify the selection of power modules as well as topologies for the three-level 1500-V PV inverters. It has also been identified in this paper that the most fragile power device in terms of the unreliability probability will determine the reliability performance of the entire system. The lifetime of three-level inverter candidates was estimated based on an analytical lifetime model focusing on the semiconductor devices, which may induce certain uncertainties compared to the real-field experiments. However, the outcomes provide an indication of the lifetime performance of three-level 1500-V PV inverters, and thus, the exploration is beneficial for the design of the corresponding systems, e.g., to choose the most suitable topology for a given mission profile. It should be noted that the reliability performance is also related to the control of the system, which will be the future work.

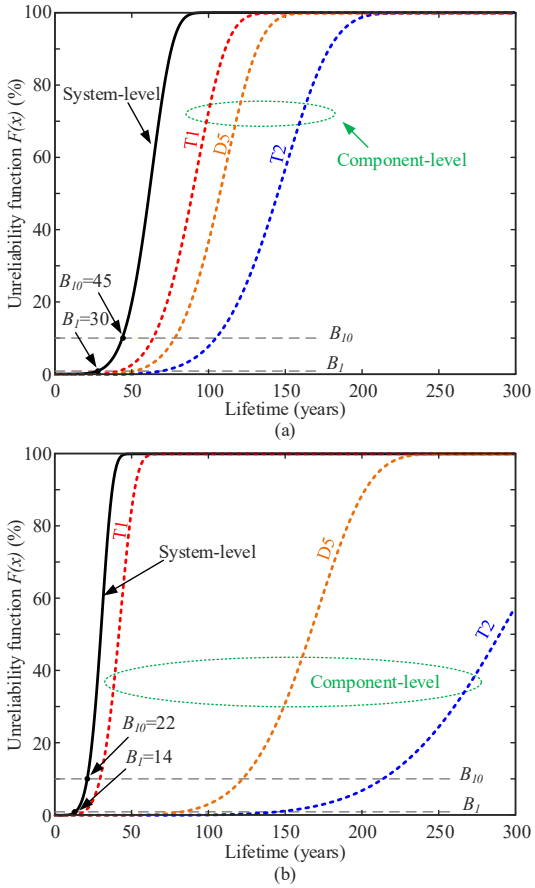

Fig. 20. Unreliability function of the PV inverters under the Sacramento mission profile: (a) I-type and (b) T-type.

REFERENCES

[1] REN21. Renewables 2019: Global Status Report (GRS). (2019). [Online]. Available: https://www.ren21.net/gsr-2019/

[2] Sungrow. The world's most powerful 1500V string inverter. (2019). [Online]. Available: https://www.sungrowpower.com/

[3] Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Design for reliability of power electronics for grid-connected photovoltaic systems," *CPSS Trans. Power Electron. Applicat.*, vol. 1, no. 1, pp. 92–103, Dec. 2016.

[4] B. Stevanović, D. Serrano, M. Vasić, P. Alou, J. A. Oliver, and J. A. Cobos, "Highly efficient, full ZVS, hybrid, multilevel DC/DC topology for two-stage grid-connected 1500-V PV system with employed 900-V SiC devices," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 811–832, Jun. 2019.

[5] R. Inzunza, R. Okuyama, T. Tanaka, and M. Kinoshita, "Development of a 1500VDC photovoltaic inverter for utility-scale PV power plants," in *Proc. IFEEC*, pp. 1–4, Nov. 2015.

[6] E. Serban, M. Ordonez, and C. Pondiche, "DC-bus voltage range extension in 1500 V photovoltaic inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 4, pp. 901–917, Dec. 2015.

[7] SMA. Whitepaper 1500 V. (2019). [Online]. Available: https://www.sma.de/en/

[8] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171–7182, Oct. 2016.

[9] M. Andresen, G. Buticchi, and M. Liserre, "Thermal stress analysis and MPPT optimization of photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4889–4898, 2016.

[10] Y. Yang, H. Wang, F. Blaabjerg, and T. Kerekes, "A hybrid power control concept for PV inverters with reduced thermal loading," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6271–6275, 2014.

[11] A. Sangwongwanich, Y. Yang, D. Sera, F. Blaabjerg, and D. Zhou, "On the impacts of PV array sizing on the inverter reliability and lifetime," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3656–3667, 2018.

[12] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, "Lifetime evaluation of grid-connected PV inverters considering panel degradation rates and installation sites," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1225–1236, Feb. 2018.

[13] A. Anurag, Y. Yang, and F. Blaabjerg, "Thermal performance and reliability analysis of single-phase PV inverters with reactive power injection outside feed-in operating hours," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 4, pp. 870–880, Dec. 2015.

[14] A. Sangwongwanich, G. Angenendt, S. Zurmühlen, Y. Yang, D. Sera, D. U. Sauer, and F. Blaabjerg, "Enhancing PV inverter reliability with battery system control strategy," *CPSS Trans. Power Electron. Applicat.*, vol. 3, no. 2, pp. 93–101, 2018.

[15] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimal design of modern transformerless PV inverter topologies," *IEEE Trans. Energy Conversion*, vol. 28, no. 2, pp. 394–404, 2013.

[16] E. Koutroulis and F. Blaabjerg, "Design optimization of transformerless grid-connected PV inverters including reliability," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 325–335, 2013.

[17] E. Gurpinar, Y. Yang, F. Iannuzzo, A. Castellazzi, and F. Blaabjerg, "Reliability-driven assessment of GaN HEMTs and Si IGBTs in 3L-ANPC PV inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 956–969, Sep. 2016.

[18] J. He, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Thermal performance evaluation of 1500-VDC photovoltaic inverters under constant power generation operation," in *Proc. IEEE CPERE*, pp. 579–583, 2019.

[19] Semikron. Module solutions for 1500V solar inverters. (2017). [Online]. Available: https://www.semikron.com

[20] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[21] K. Lenz, T. Franke, and H. Stroebel-Maier, "IGBT power module solution in three-level topologies for 1MW 1500VOC solar applications," in *Proc. PCIM Asia*, pp. 1–8, 2016.

[22] X. Zhang, T. Zhao, W. Mao, D. Tan, and L. Chang, "Multi-level inverters for grid-connected photovoltaic applications: Examining emerging trends," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 32–41, 2018.

[23] Jinko. JKM360M-72-V. (2019). [Online]. Available: https://www.http://www.jinkosolar.com/

[24] S. K. Chaudhary, P. Ghimire, F. Blaabjerg, P. B. Thøgersen, and P. de Place Rimmen, "Development of field data logger for recording mission profile of power converters," in *Proc. ECCE-Europe*, pp. 1–10, 2015.

[25] T. B. Soeiro, K. Park, and F. Canales, "High voltage photovoltaic system implementing Si/SiC-based active neutral-point-clamped converter," in *Proc. IECON*, pp. 1220–1225, Oct. 2017.

[26] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, "Mission profile-oriented control for reliability and lifetime of photovoltaic inverters," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 601–610, 2020.

[27] E. Serban, C. Pondiche, and M. Ordonez, "Modulation effects on power-loss and leakage current in three-phase solar inverters," *IEEE Trans. Energy Conversion*, vol. 34, no. 1, pp. 339–350, Mar. 2019.

[28] Semikron. Application manual – Power semiconductors. (2015). [Online]. Available: https://www.semikron.com

[29] X. Yuan, "Analytical averaged loss model of a three-level T-type converter," in *Proc. IET PEMD*, pp. 1–6, 2014.

[30] Semikron. Gate resistor – Principles and applications. (2007). [Online]. Available: https://www.semikron.com

[31] Y. Yang, H. Wang, F. Blaabjerg, and K. Ma, "Mission profile based multi-disciplinary analysis of power modules in single-phase transformerless photovoltaic inverters," in *Proc. EPE*, pp. 1–10, Sep. 2013.

[32] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power IGBT modules considering heat coupling effects," in *Proc. PEAC*, pp. 1382–1387, Nov. 2014.

[33] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, 2017.

[34] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. PEDS*, vol. 1, pp. 425–430 vol.1, 1997.

[35] U. Scheuermann, R. Schmidt, and P. Newman, "Power cycling testing with different load pulse durations," in *Proc. PEMD*, pp. 1–6, Apr. 2014.

[36] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules - various factors influencing lifetime," in *Proc. CIPS*, pp. 1–6, Mar. 2008.

[37] Infineon. PC and TC diagrams. (2019). [Online]. Available: https://www.infineon.com/dgdl/Infineon-AN2019-05_PC_and_TC_Diagrams-ApplicationNotes-v01_00-EN.pdf?fileId=5546d46269e1c019016a594443e4396b
[38] M. Miner, "Cumulative damage in fatigue," *J. Appl. Mech.*, vol. 12, pp. 159–164, 1945.
[39] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4113–4119, Aug. 2013.
[40] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of DC/DC converters for a backup power application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8030–8039, 2018.
[41] Y. Shen, H. Wang, Y. Yang, P. D. Reigosa, and F. Blaabjerg, "Mission profile based sizing of IGBT chip area for PV inverter applications," in *Proc. IEEE PEDG*, pp. 1–8, 2016.
[42] D. Smith, *Reliability, maintainability and risk: practical methods for engineers*. Elsevier Science, 2017. [Online]. Available: https://books.google.dk/books?id=zLgxDQAAQBAJ
[43] ZVEI, "How to measure lifetime for robustnesss validation–step by step," *Berlin, Germany, rev. 1.9*, Nov. 2012.
[44] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, 2017.
[45] L. Ceccarelli, R. M. Kotecha, A. S. Bahman, F. Iannuzzo, and H. A. Mantooth, "Mission-profile-based lifetime prediction for a SiC MOSFET power module using a multi-step condition-mapping simulation strategy," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9698–9708, 2019.
[46] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, 2020.
[47] S. Li and L. Xu, "Strategies of fault tolerant operation for three-level PWM inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 933–940, 2006.
[48] U. Choi, F. Blaabjerg, and K. Lee, "Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2660–2673, 2015.
[49] Y. Ding, P. C. Loh, K. K. Tan, P. Wang, and F. Gao, "Reliability evaluation of three-level inverters," in *Proc. APEC*, pp. 1555–1560, 2010.
[50] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765–776, Jan. 2018.

Jinkui He (S'19) received the B.S. degree in electrical engineering and automation and the M.S. degree in control engineering from China University of Petroleum (East China), Qingdao, China, in 2010 and 2012, respectively. He is currently working toward the Ph.D. degree with the Department of Energy Technology, Aalborg University, Aalborg, Denmark.

He was an Experimental Lecturer with the College of Information and Control Engineering, China University of Petroleum (East China), from 2012 to 2018. His research interests include grid-connected converter design and control, reliability in power electronics, and photovoltaic systems.

Ariya Sangwongwanich (S'15-M'19) received the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. Currently, he is working as a Postdoc Fellow at the Department of Energy Technology, Aalborg University.

He was a Visiting Researcher with RWTH Aachen, Aachen, Germany from September to December 2017. His research interests include control of grid-connected converter, photovoltaic systems, reliability in power electronics and multilevel converters. He has co-authored the book – Advanced in Grid-Connected Photovoltaic Power Conversion Systems. In 2019, he received the Danish Academy of Natural Sciences' Ph.D. prize and the Spar Nord Foundation Research Award for his Ph.D. thesis.

Yongheng Yang (SM'17) received the B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, Shaanxi, China, in 2009 and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2014.

He was a postgraduate student with Southeast University, China, from 2009 to 2011. In 2013, he spent three months as a Visiting Scholar at Texas A&M University, USA. Currently, he is an Associate Professor with the Department of Energy Technology, Aalborg University, where he also serves as the Vice Program Leader for the research program on photovoltaic systems. His current research is on the integration of grid-friendly photovoltaic systems with an emphasis on the power electronics converter design, control, and reliability.

Dr. Yang is the Chair of the IEEE Denmark Section. He serves as an Associate Editor for several prestigious journals, including the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the IEEE Industry Applications Society (IAS) Publications. He is a Subject Editor of the *IET Renewable Power Generation* for Solar Photovoltaic Systems, including the Maximum Power Point Tracking. He was the recipient of the 2018 *IET Renewable Power Generation* Premium Award and was an Outstanding Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2018.

Francesco Iannuzzo (M'04-SM'12) received the M.Sc. degree in Electronic Engineering and the Ph.D. degree in Electronic and Information Engineering from the University of Naples, Italy, in 1997 and 2002, respectively. He is primarily specialized in power device modelling.

He is currently a professor of reliable power electronics at the Aalborg University, Denmark, where he is also part of CORPE, the Center of Reliable Power Electronics. His research interests are in the field of reliability of power devices, including mission-profile based life estimation, condition monitoring, failure modelling and testing up to MW-scale modules under extreme conditions. He is author or co-author of more than 230 publications on journals and international conferences, three book chapters and four patents. Besides publication activity, over the past years he has been contributing 17 technical seminars about reliability at first conferences as ISPSD, EPE, ECCE, PCIM and APEC.

Prof. Iannuzzo is a senior member of the IEEE (Industry Application Society, Reliability Society, Power Electronic Society, and Industrial Electronic Society). He currently serves as Associate Editor for Transactions on Industry Applications, and is vice-chair of the IAS Power Electronic Devices and Components Committee. In 2018 he was the general chair of the 29th ESREF, the first European conference on reliability of electronics.