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A Reference Submodule Based Capacitor Condition Monitoring Method for Modular Multilevel Converters

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***Abstract*—This paper proposes a novel capacitor condition monitoring method for modular multilevel converters (MMCs) based on reference submodules (SMs). It significantly enhances the capacitor monitoring accuracy by making full use of the SM voltage sensor measurement range. Accuracy comparison between the existing method and the proposed method is conducted to quantify the improvement of accuracy. Moreover, its operation principle and practical implementation considerations are presented. Finally, a three-phase MMC platform is built to experimentally verify the effectiveness of the proposed method.**

I. Introduction

In modular multilevel converters (MMCs), submodule (SM) capacitors are significant for the reliability of the system. Typically, metalized polypropylene film (MPPF) capacitors are utilized in MMCs due to their high voltage rating and self-healing capability [1]. However, MPPF capacitor failures might occur in practice due to a series of intrinsic and extrinsic factors [2], which may lower the availability of the MMC. These failures can even lead to explosions with potential human casualties and expensive equipment losses [3]. It is therefore of great necessity to monitor these components to avoid the possibility of grievous consequences.

Condition monitoring (CM) is a promising technique to detect the health status of the capacitors in the MMC [4]. Prior to the occurrence of failures, preventive maintenances can thus be scheduled with lower maintenance cost and longer reliable operational time of the MMC system. One of the major challenges is how to accurately monitor the changing of aging precursors. The capacitance and equivalent series resistance (ESR) are two critical aging precursors for capacitors [5], [6]. Although the ESR is commonly used in the CM of electrolytic capacitors (E-caps), it is difficult to be applied for MPPF capacitors, whose ESR is typically very small (on the order of 10^{-2} mΩ [3]) compared to E-caps on the order of 10^{-2} Ω [7]. Thus, the capacitance is widely used as the criteria of end-of-life for MPPF capacitors [8]. Notably, MPPF capacitors typically see a smaller capacitance drop (e.g., 5% of its initial value) compared to 20% of the E-Caps at the end-of-life. As a results, the CM of MPPF capacitors has to fulfill more stringent requirements for the monitoring accuracy.

The CM methods designed for capacitors in the MMC have been reported in the literature. Reference [9] monitors the SM capacitance by utilizing an RC discharging circuit formed by internal bleeding resistors. However, the impact of auxiliary power supply on the monitoring accuracy is not considered when the SM is self-powered by its local capacitor. Several advanced algorithm based methods are proposed for the MMC,

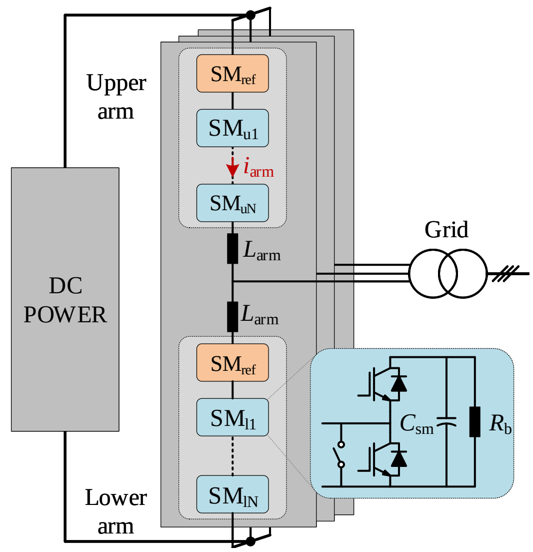

Fig. 1. Three-phase MMC with one reference SM in each arm.

such as Kalman filter [10], band-pass filter [11], and recursive least square algorithm [12]) and reference SM based method [13]. These methods utilize capacitor voltage ripples to achieve the purpose of CM without the aid of additional hardwares. However, this feature poses a great challenge on the accuracy of sensors. Considering a typical 10% voltage ripple and 5% capacitance drop of MPPF capacitors at the end-of-life, the maximum voltage ripple change caused by capacitance drop is merely 0.5% of the voltage sensor range. Given the accuracy level of commonly used voltage senors (e.g., 0.3% or 0.5% [14]) in the market, it is a great challenge for the aforementioned methods to conduct accurate condition monitoring without increasing the accuracy of voltage sensors. Moreover, light loading condition further impairs the monitoring accuracy due to the reduced voltage ripple [15].

When it comes to conventional power converters, many prior-art studies have been done with regards to condition monitoring of capacitors. The offline method has been proposed for applications with frequent interruptions, e.g., PV, motor drive, etc [7], [16], [17]. The health status of capacitors are obtained during the shutdown period. For the MMC without frequent interruptions, few amount of data sampling is difficult to provide sufficient and reliable health history profiles. Furthermore, extra hardware based CM methods (e.g., voltage or current sensor) are applied to applications with simple topologies, e.g., two-level converters [18]. It might be

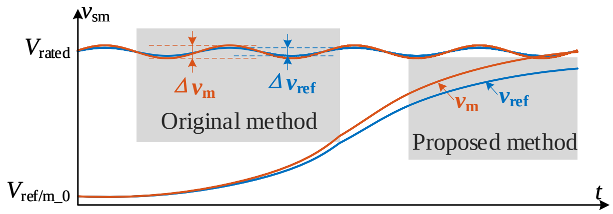

Fig. 2. Voltages used by the original method in [13] and proposed method for CM. (Δv_{ref}, Δv_{m}, v_{ref}, v_{m}, $V_{\mathrm{ref\_0}}$ and $V_{\mathrm{m\_0}}$ are the peak-to-peak voltages, real voltages and initial voltages of the reference SM and monitored SM.)

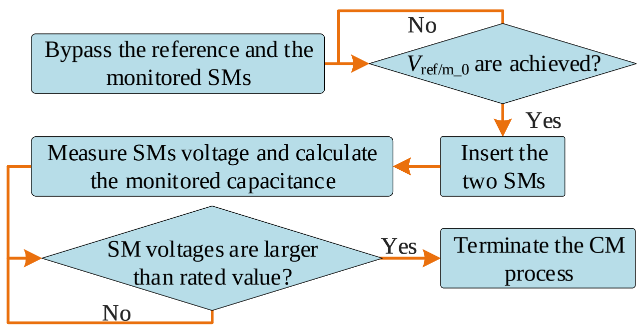

Fig. 3. Flowchart of the proposed condition monitoring method.

feasible for simple circuit structures with a limited number of components. However, due to the large number of SMs, integrating additional hardware in each SM will introduce considerable costs and reliability issues to the MMC system. From this perspective, non-extra-hardware based online condition monitoring method is a feasible research direction to go for SM capacitors in the MMC.

This paper proposes a novel reference SM based capacitor condition monitoring method with enhanced accuracy. The contribution of the method is to take full advantage of the SM voltage sensor range ensuring the monitoring error reduction and to be load-independent of the MMC.

II. New Reference SM Based CM Method

The idea of reference SM based CM method [13] is that the monitored SM shares the same gate signal with the reference SM, whose capacitance is already known beforehand. In this case, series connection of two SMs means their voltage difference is only caused by their capacitance difference. In [13], the capacitance can thus be estimated by

$$C_{\mathrm{m}} = \frac{\Delta v_{\mathrm{ref}}}{\Delta v_{\mathrm{m}}} C_{\mathrm{ref}}, \tag{1}$$

where C_{ref}, C_{m}, Δv_{ref} and Δv_{m} are the capacitances and the peak-to-peak voltages of the reference SM and monitored SM.

Instead of SM voltage ripples, as shown in Fig. 2, the proposed method utilizes a wider SM voltage range to achieve the objective of CM by

$$v_{\mathrm{ref/m}} = \frac{1}{C_{\mathrm{ref/m}}} \int S_{\mathrm{m}} i_{\mathrm{arm}} dt + V_{\mathrm{ref/m\_0}}, \tag{2}$$

where v_{ref}, v_{m}, $V_{\mathrm{ref\_0}}$ and $V_{\mathrm{m\_0}}$ are the instantaneous voltages and initial voltages of the reference SM and monitored SM; i_{arm} is the arm current; S_{m} is the gate signal. The monitored capacitance can be estimated by instantaneous voltages as

$$C_{\mathrm{m}} = \frac{v_{\mathrm{ref}} - V_{\mathrm{ref\_0}}}{v_{\mathrm{m}} - V_{\mathrm{m\_0}}} C_{\mathrm{ref}}. \tag{3}$$

A flowchart is given in Fig. 3 to illustrate how the proposed method is implemented.

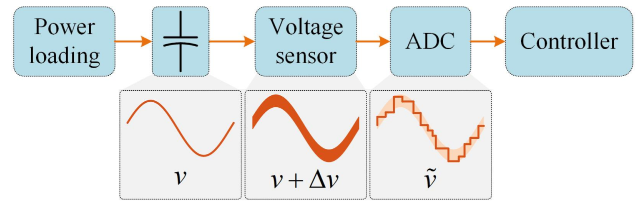

Fig. 4. Impact of the voltage sensor and ADC on the voltage measurement for the capacitance detection (v is the actual SM voltage, Δv is the voltage error caused by the sensor, and $\tilde{v}$ is the measured voltage used for CM).

III. Accuracy Analysis

Monitoring accuracy analysis is conducted in this section in order to illustrate how the monitoring accuracy is improved by the proposed method. The accuracy of measurement system, namely the voltage sensor and analog-to-digital converter (ADC), plays a key role in the CM process shown in Fig. 4. Its impact is quantified as

$$\tilde{v} = \mathrm{floor}\left(\frac{v + \Delta v}{dv}\right) dv, \tag{4}$$

where v and $\tilde{v}$ are the actual voltage and measured voltage, respectively, which correspond to $\Delta v_{\mathrm{ref/m}}$ and $\Delta \tilde{v}_{\mathrm{ref/m}}$ for the original method in [13], and $v_{\mathrm{ref/m}}$ and $\tilde{v}_{\mathrm{ref/m}}$ for the proposed method; $\mathrm{floor}\,(x)$ is the function that gives the largest integer less than or equal to its input; Δv is the voltage measurement error introduced by the sensor with a range of $[-\varepsilon_{\mathrm{s}} V_{\mathrm{s}}, +\varepsilon_{\mathrm{s}} V_{\mathrm{s}}]$ where ε_{s} and V_{s} are the accuracy and rated voltage of the voltage sensor. dv is the minimum voltage that the ADC can detect. Assuming that the voltage range of the sensor is equal to the SM rated voltage with $V_{\mathrm{rated}} = V_{\mathrm{s}}$ and the SM voltage ripple is 10% of its rated voltage, then we have

$$\begin{cases} v_{\mathrm{ref}} = v_{\mathrm{sm}}, v_{\mathrm{m}} = \dfrac{v_{\mathrm{ref}}}{1 - d_{\mathrm{cap}}} \\ \Delta v_{\mathrm{ref}} = 0.1 V_{\mathrm{rated}}, \Delta v_{\mathrm{m}} = \dfrac{\Delta v_{\mathrm{ref}}}{1 - d_{\mathrm{cap}}} \\ V_{\mathrm{ref/m\_0}} = (1 - p_{\mathrm{v}})\, V_{\mathrm{rated}}, dv = \dfrac{V_{\mathrm{rated}}}{2^B} \end{cases} \tag{5}$$

where v_{sm} is the SM voltage; d_{cap} is the capacitance drop percentage; p_{v} is the SM voltage sensor utilization rate; B is the ADC resolution bit. Note that initial voltages of the reference SM and monitored SM are assumed to be the same.

The SM capacitance estimation error e_{cap} is defined as

$$e_{\mathrm{cap}} = \left(\frac{\tilde{C}_{\mathrm{m}}}{C_{\mathrm{m}}} - 1\right) \times 100\%, \tag{6}$$

where C_{m} and $\tilde{C}_{\mathrm{m}}$ are the actual capacitance and estimated capacitance of the monitored SM, respectively.

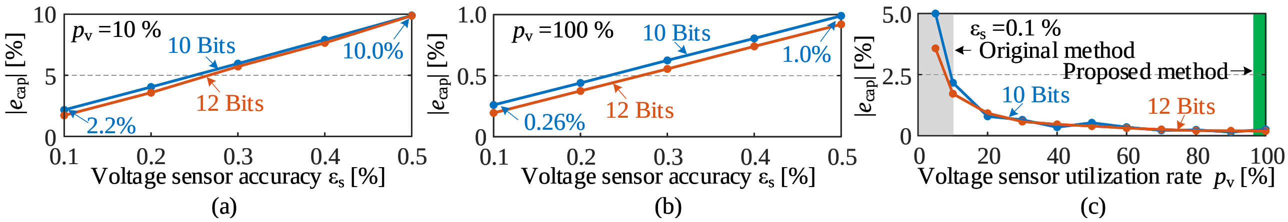

Fig. 5. Capacitance monitoring accuracy comparison between the original method in [13] and the proposed method with different voltage sensor accuracy, ADC resolution, and SM voltage sensor utilization rate: (a) original method, (b) proposed method, and (c) voltage sensor utilization rate.

Combining (1)-(6), the accuracy comparison between the method in [13] and the proposed method is shown in Fig. 5 regarding different accuracies of voltage sensors and ADCs (two commonly used 10-bit and 12-bit ADCs are considered). It can be seen from Fig. 5(a) and (b) that the monitoring error almost shows a linear relationship with the accuracy of the voltage sensor. In the meantime, a higher ADC resolution can contribute to a better capacitance estimation result. Nevertheless, the improvement is insignificant since the bottleneck of the whole measurement system is the accuracy of available voltage sensors in the market (e.g., generally higher than 0.1%) rather than ADCs.

Furthermore, for the original method in [13] considering a typical 10% voltage ripple and 10-bit ADC, an error of about 2.2% and 10% can be observed in Fig. 5(a) for voltage sensor accuracies of 0.1% and 0.5% respectively. By contrast, as it can be seen from Fig. 5(b), the error is merely 0.26% and 1.0% for the proposed method when considering a 100% SM voltage sensor utilization rate (i.e., $V_{\mathrm{ref/m\_0}} = 0$). In this case, almost ten times accuracy improvement can be achieved by the proposed method over the original method.

When the initial voltages for both SMs are between zero and the rated SM voltage, the monitoring accuracy may decrease compared with the case of $p_{\mathrm{v}} = 100\%$ as shown in Fig. 5(c). The capacitance estimation error is almost inversely proportional to the voltage sensor utilization rate. It means that zero initial voltages are the best option in terms of the monitoring accuracy. However, when it comes to the total time required for one round of CM of all SMs in the MMC, a trade-off might need to be made in terms of initial voltages or p_{v}. Detailed explanations are given in the following Section.

IV. Condition Monitoring Speed

The reference SM and monitored SM need to be discharged to their initial voltages ($V_{\mathrm{ref/m\_0}}$) in advance for the CM. This process can be achieved with the aid of bleeding resistor R_{b} and auxiliary power supply P_{aux} [19] inside the SM as shown in Fig. 6. The auxiliary power supply starts to work only when its input voltage exceeds a threshold V_{aux}. Meanwhile, its power dissipation is assumed to be a constant P_{aux} taken from the SM capacitor. When the SM is bypassed, its discharging voltage curve during the CM is shown in Fig. 7. At the very beginning, the SM voltage v_{sm} is at its rated value V_{rated}. Both the bleeding resistor and auxiliary power supply dissipate the energy stored in the SM capacitor, whose voltage drops quickly at stage I. When the SM capacitor voltage is lower

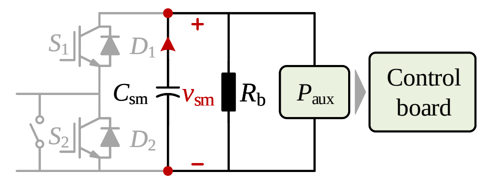

Fig. 6. One typical SM with a bleeding resistor and an auxiliary power supply.

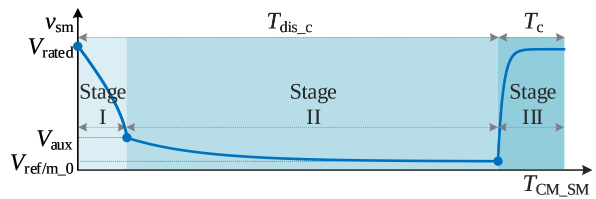

Fig. 7. A typical discharging and charing curve of SM capacitor during the proposed CM process. Stage I: both auxiliary power supply and bleeding resistor discharge the SM capacitor, Stage II: only the bleeding resistor discharges the SM capacitor, and Stage III: charging for capacitance estimation. $T_{\mathrm{dis\_c}}$: discharging time, T_{c}: charging time, and $T_{\mathrm{CM\_SM}}$: monitoring time required for one SM.

than the input voltage threshold V_{aux} of the auxiliary power supply at stage II, only the bleeding resistor itself discharges the SM capacitor and this process takes a much longer time due to a larger discharging time constant. Once one of pre-set initial voltages (i.e., $V_{\mathrm{ref/m\_0}}$) is achieved, Stage III starts to estimate the SM capacitance.

When $v_{\mathrm{sm}} > V_{\mathrm{aux}}$, the discharging time $T_{\mathrm{dis\_c}}$ is

$$T_{\mathrm{dis\_c}} = \frac{R_{\mathrm{b}} C_{\mathrm{sm}}}{2} \ln \left| \frac{V_{\mathrm{rated}}^2 + R_{\mathrm{b}} P_{\mathrm{aux}}}{v_{\mathrm{sm}}^2 + R_{\mathrm{b}} P_{\mathrm{aux}}} \right| . \quad (7)$$

When $v_{\mathrm{sm}} < V_{\mathrm{aux}}$, the discharging time $T_{\mathrm{dis\_c}}$ is

$$T_{\mathrm{dis\_c}} = \frac{R_{\mathrm{b}} C_{\mathrm{sm}}}{2} \left(\ln \left| \frac{V_{\mathrm{rated}}^2 + R_{\mathrm{b}} P_{\mathrm{aux}}}{V_{\mathrm{aux}}^2 + R_{\mathrm{b}} P_{\mathrm{aux}}} \right| + \ln \left| \frac{V_{\mathrm{aux}}^2}{v_{\mathrm{sm}}^2} \right| \right) . \quad (8)$$

The discharging time $T_{\mathrm{dis\_c}}$ of capacitors at stage I and stage II takes about several tens of minutes in practice. It is much longer than the charging time T_{c} for the purpose of the CM at stage III, which ends in a few seconds due to the large arm current. Since the proposed CM method can monitor six SMs simultaneously (i.e., one SM in each arm), the total monitoring time $T_{\mathrm{CM\_MMC}}$ for the whole MMC can be estimated by

$$T_{\mathrm{CM\_MMC}} = N T_{\mathrm{CM\_SM}} = N \left(T_{\mathrm{dis\_c}} + T_{\mathrm{c}} \right) \approx N T_{\mathrm{dis\_c}}, \quad (9)$$

where $T_{\mathrm{CM\_SM}}$ and $T_{\mathrm{CM\_MMC}}$ are the condition monitoring time required for one SM and the whole MMC system.

TABLE I
SYSTEM PARAMETERS OF THE MMC USED FOR CASE STUDY.

Parameter	Value
Power rating S_{rated}	300 MVA
DC bus voltage V_{dc}	300 kV
SM number per arm N	150
SM rated voltage V_{rated}	2 kV
SM capacitor C_{sm}	5 mF
Bleeding resistor R_{b}	100 kΩ
Output power of SM power supply P_{aux}	60 W
Input voltage threshold of SM power supply V_{aux}	300 V

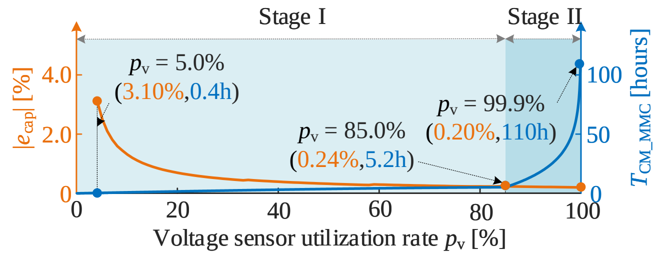

Fig. 8. The impact of the voltage sensor utilization rate p_{v} on the monitoring error e_{cap} and monitoring time $T_{\text{CM\_MMC}}$ required for the whole MMC.

In order to investigate the CM speed of the proposed method, a case study is given based on a 300 MVA MMC system as listed in Table I. The value of bleeding resistor is 100 kΩ which is selected according to requirements of its power dissipation and SM discharging time. The parameters of the auxiliary power supply is selected according to [20].

The relationship among the voltage sensor utilization rate p_{v} (or initial voltages), capacitance monitoring error $|e_{\text{cap}}|$ and monitoring time $T_{\text{CM\_MMC}}$ is shown in Fig. 8 with the accuracies of voltage sensor and ADC being 0.1% and 12 bits. It can be seen that the lower the monitoring error is, the longer the monitoring time will be. It means that a trade-off has to be made between the monitoring accuracy and CM speed. More specifically, when p_{v} increases from 5% to 85%, the monitoring error drops dramatically from 3.1% to 0.24% and $T_{\text{CM\_MMC}}$ rises from 0.4 hours to 5.2 hours. However, if the initial voltages are less than the input voltage threshold of auxiliary power supply (i.e., Stage II), the monitoring time $T_{\text{CM\_MMC}}$ can increase noticeably from 5.2 hours to 110 hours with the monitoring accuracy improvement being merely 0.04% (i.e., from 0.24% to 0.20%). A turning point appears at $p_{\text{v}} = 85\%$ when the initial voltage is equal to the input voltage threshold V_{aux}.

Overall, if a weekly condition monitoring of the whole MMC system is acceptable, then zero initial voltages, namely $p_{\text{v}} = 100\%$, is recommended to achieve the best monitoring accuracy. The monitoring time is thus roughly 4.6 days (110 hours) for the whole MMC. If SM initial voltages for CM are kept higher than the input voltage threshold (e.g., 300 V in this case study), then an hourly condition monitoring can be implemented with a slight monitoring accuracy loss. The monitoring accuracy can still be about eight times that of the method in [13] in this case. Considering a typically long lifetime (e.g., ten years) of MPPF capacitors, the monitoring speed of the proposed method is fast enough to obtain sufficient health status information.

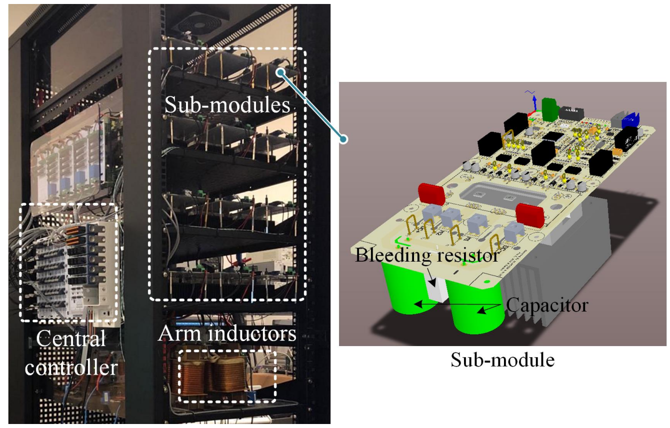

Fig. 9. Experimental setup of three-phase MMC (left) with a 3D SM (right).

V. Practical Considerations

Before the experimental validation of the proposed method, two practical issues are first explained in the following.

1) Reference Submodule Capacitance Estimation: Obtaining the capacitance of the reference SM is a key precondition for the proposed method. The original method in [13] recommends to employ advanced algorithm based methods, such as [10] and [12] to achieve the objective. However, its accuracy (e.g., 1%) is a major concern and might introduce extra large error. Apart from the above solution, it is also applicable to use more accurate sensors or extra measurement circuit in the reference SMs to detect the capacitance since only six reference SMs (one per arm) are required. The additional circuit will not introduce much cost or reliability issue to the whole MMC system.

2) Impact on the Operation of MMC: The missing of the reference and monitored SMs prior to the CM, and the inclusion of two increasing SM voltages during the CM might have an impact on the operation of the MMC, such as the voltage of remaining SMs and the harmonics of output currents and voltages. However, since the above process is the same as putting a cold-reserve redundant SM into service, the transition control strategy proposed in [21] can be applied to mitigate the impact of the proposed CM. In addition, the impact will be, as mentioned in [21], ignorable in practical MMC applications when the SM number is high.

VI. Experimental Validation

The proposed CM method is validated based on a 15 kVA three-phase MMC platform as shown in Fig. 9. The DC bus voltage is 600 V. Each arm has four SMs. The upper arm of phase C is chosen to demonstrate the performance of the proposed method with two lower SMs (SM_3 and SM_4) being the reference SM and monitored SM, respectively. The other two SMs (SM_1 and SM_2) function to track the arm voltage reference. Moreover, to emulate the capacitance drop due to the degradation, several small capacitors (i.e., C_1, C_2, and C_3

TABLE II
COMBINATION OF CAPACITORS TO EMULATE CAPACITANCE DROP.

[uF]	C_{sm}	C_1	C_2	C_3	C_{m}	Capacitance drop
C_{rated}	1640	22	22	10	-	-
C_{cap1}	*	*	*	*	1694	0%
C_{cap2}	*	*		*	1672	1.30%
C_{cap3}	*	*			1662	1.90%
C_{cap4}	*				1640	3.20%

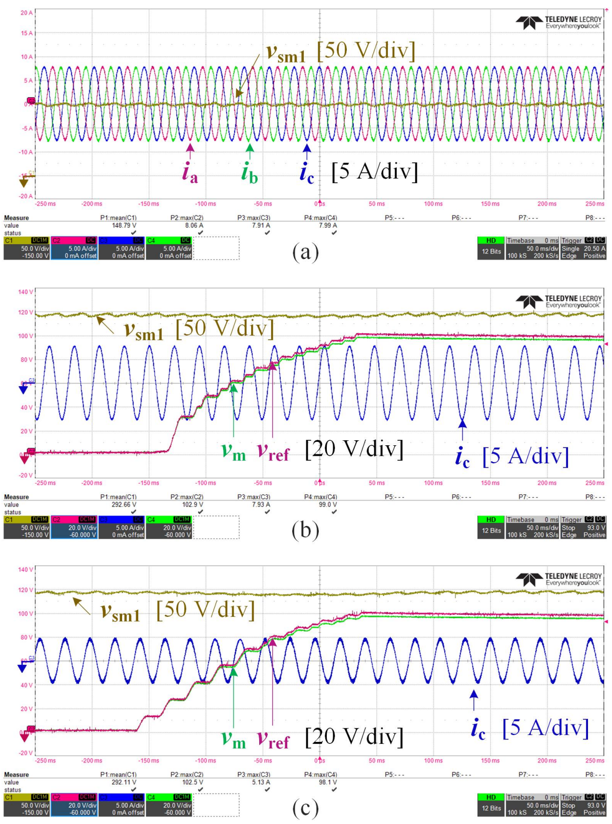

Fig. 10. Experimental waveforms: (a) three-phase output current and the voltage of SM_1 at 3 kW prior to CM, (b) and (c) the output current of phase C, and voltages of the reference and monitored SMs and SM_1 during the CM, (b) 3 kW and (c) 1 kW.

as listed in Table II) are connected in parallel with the SM capacitor C_{sm}. By removing one or several of them, the SM with reduced capacitance can be mimicked. The reference SM capacitance is 1.64 mF. The voltage measurement accuracy is adjusted to 0.1% by applying a low-pass filter and the rated SM voltage for the CM purpose is defined as 100 V. The initial voltages for both SMs are zero in the experiments.

Fig. 10 shows the experimental waveforms. Prior to the CM, it can be seen from Fig. 10(a) that the output current of three phases are 50 Hz sinusoidal waveforms. The voltage of SM_1 is 150 V since all four SMs in the arm are working. When the CM process begins, as can be observed from Fig. 10(b) and (c), the voltage of SM_1 grows to 300 V with only SM_1 and SM_2 functioning to support the 600 V DC bus voltage. Meanwhile, the voltages of the reference SM and monitored SM are gradually rising from 0 V to 100 V under two loading conditions (i.e., 3 kW and 1 kW). It confirms the proposed

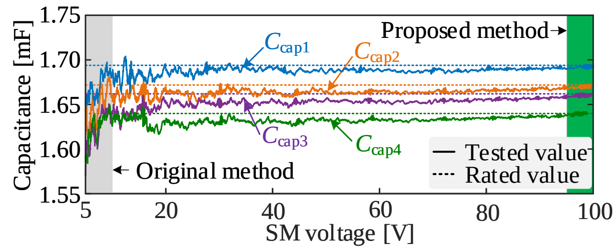

Fig. 11. Estimated SM capacitances under different SM voltages.

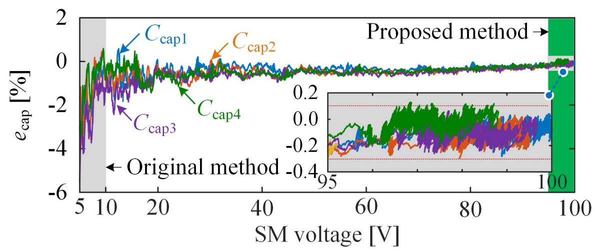

Fig. 12. SM capacitances estimation error under different SM voltage.

method is independent of the loading condition of the MMC.

Additionally, the voltage difference between v_{ref} and v_{m} can be observed in Fig. 10 (b) and (c). By applying (3), the monitored capacitance can be estimated and the experimental results with different capacitances listed in Table II are shown in Fig. 11 in terms of different SM voltages. It can be seen that when the SM voltage is low (e.g., below 15 V), the estimated capacitance fluctuates significantly around its rated value. As the voltage grows, the estimation results tend to become stable and accurate as shown in Fig. 12. In order to better illustrate the impact of the applied SM voltage range on the measurement error, Fig. 13 takes the four testings (i.e., $C_{\mathrm{cap1}}...C_{\mathrm{cap4}}$) into account. 100 V SM voltage range is divided into 20 intervals (5 V per interval) with the maximum error in each interval being shown. When the SM voltage is lower than 10 V (equivalent to 10% SM voltage utilization rate), the capacitance detection error is higher than 2.43%, which agrees well with the result in Fig. 5(c). The lower the voltage is, the larger the error will be. Therefore, for the original method utilizing SM voltage ripple below 10%, the error larger than 2.43% will make it pretty difficult or even fail to detect the 5% capacitance drop of film capacitors at the end-of-life. By contrast, by utilizing the full SM voltage sensor range (100 V in this case study), the capacitance estimation error is as low as 0.3% for the proposed method. It agrees well with the analytical result of 0.26% (10 bits) in Fig. 5(b). When the loading of the MMC is lighter with reduced voltage ripple, ten or more times accuracy over the original method will be achieved by the proposed method.

VII. CONCLUSION

This paper proposed a new reference SM based capacitor condition monitoring method with enhanced monitoring accuracy. Its advantages are summarized as below: 1) full voltage sensor range utilization ensures the error reduction

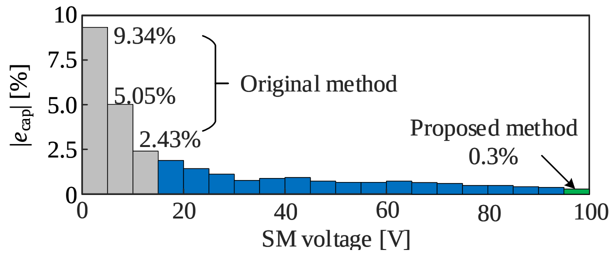

Fig. 13. SM capacitances estimation error under different SM voltages.

from 2.4% to 0.3% with respect to 0.1% voltage sensor accuracy; 2) load-independent of the MMC; 3) capacitances can be estimated directly from the measured instantaneous voltages without the detection of peak-to-peak voltages; 4) insignificant computational burden is introduced.

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