Reconsideration of Grid-Friendly Low-Order Filter Enabled by Parallel Converters

Quan, Zhongyi; Li, Yun Wei; Pan, Yiwei; Jiang, Changpeng; Yang, Yongheng; Blaabjerg, Frede

Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3009056

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Reconsideration of Grid-Friendly Low-Order Filter Enabled by Parallel Converters

Zhongyi Quan, *Member, IEEE*, Yun Wei Li, *Fellow, IEEE*, Yiwei Pan, *Student Member, IEEE*, Changpeng Jiang, *Student Member, IEEE*, Yongheng Yang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—High-order filters like LCL filter have been popular in grid-tied power converters. Although featuring small size, LCL filters are not grid-friendly due to inherent resonance, especially when a large number of converters are in parallel operation in today's electric grid to attain modularity, reliability and redundancy advantages. Thus, this paper reconsiders the low-order L filter in parallel converters to eliminate the resonance and in turn to simplify the control. It is found that by interleaving a certain number of converters, the L filter will be the sufficient to meet the harmonic limit requirements of the standards while the filter size can be even smaller than the LCL filter. This further contributes to cost reduction as a promising solution for grid-friendly converters.**

***Index Terms*—Parallel converter, grid-tied converter, interleaving, L filter.**

I. Introduction

Grid-tied power converters employ passive filters to attenuate the high frequency harmonics within the limits set by the standards, e.g. the IEEE std 1547-2018 [1] or the IEEE std 519-2014 [2]. To reduce the size and cost, high-order filters, e.g., the LCL filter, are popular in many ground-based non-critical applications [3], [4]. To further reduce filter size, more complicated high-order filters like $LLCL$ filter have been proposed in the literature [3]. While featuring excellent harmonics filtering performance, high-order filters are not grid-friendly due to their inherent filter resonance [5]. With the increasing penetration of power electronics, the utility grid will face severe resonance issues caused by the high-order filters [6], [7].

On the other hand, paralleling power converters has become a popular practice in many grid-tied applications. Depending on the types of applications, parallel converters can be built with a common dc link or separate dc links [8]. Both architectures have been popular in applications such as interfacing converters in a hybrid ac/dc microgrid [9]-[11], active front-ends of motor drives [12]-[14], wind turbines [15]-[17], and solar farms [7], [18]. With either type of parallel converters, modularity can be realized, improving the overall system reliability and efficiency [10], [17]-[19]. However, despite these advantages, high-order filters, e.g., the LCL, have been used for almost all parallel converters in the literature. As a result, issues like multi-resonance [6] and sideband harmonics resonance [20] will appear, in addition to the traditional resonance issue in an LCL-filtered single converter. Such issues may become even aggravated if more complicated high-order filters are applied. Taking the common dc-link type system as an example, the typical structure of a parallel converter system is shown in Fig. 1 (a). In practice, a common mode choke, which is not shown in Fig. 1 for simplicity, may also be included in each converter module in addition to the LCL filter.

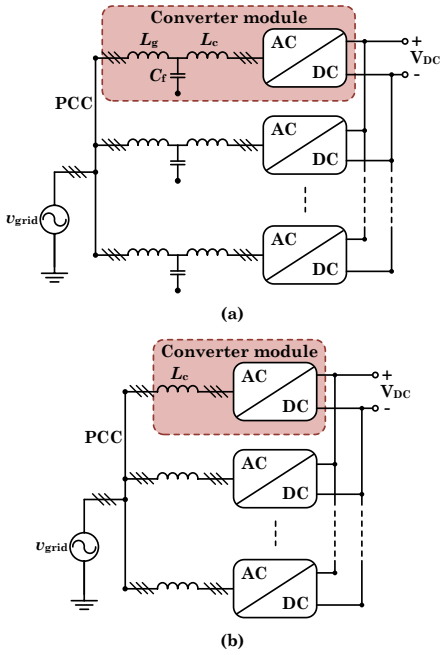


Fig. 1. Common dc-link type modular parallel converter architecture with (a) an LCL filter in each converter module, and (b) an L filter in each converter module.

Although many attempts have been made to address various resonance issues [5]-[7], [20]-[28], these methods either assume that the parallel converters have the same switching frequency and filter parameters [6], [21], [22] or that the overall system specifications are known such that the controller design of each converter can be accurately tuned [23]. However, these conditions cannot always be met. As a result, in practice, there is always a limit on the line impedance to

This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC).

Part of this work was presented in APEC 2019, Anaheim, CA, USA.

Z. Quan, Y. W. Li, and C. Jiang are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. Y. Pan, Y. Yang, and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark

Y. Pan, Y. Yang, and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark

Email: zquan@ualberta.ca, yunwei.li@ualberta.ca, changpen@ualberta.ca, ypa@et.aau.dk, yoy@et.aau.dk, fbl@et.aau.dk

ensure stable operation [29]. In addition, studies have shown that stable single converter operation with proper damping cannot guarantee the overall system stability [21], [22]. Further considering that in many applications, the number of active converters can vary and the resultant resonant frequency seen by the active converters can change in a wide range, the stable operation of parallel converters can be a challenge. Moveover, the large-scale adoption of wide band-gap devices in the future could further complicate the problem as the grid side filter inductance of an LCL filter will become smaller. More importantly, in the future power electronics-dominated grid, it is more likely that the converters will have different control and hardware parameters, e.g., new and legacy products in parallel, and the overall system specifications, including line impedance, the number of parallel converters, etc. are unknown, e.g., in a residential microgrid or an industry drive system where a group of parallel converters has a different set of parameters than the other group. As an example, Fig. 2 demonstrates the multi-resonance effect of two converters when the switching frequency and filter parameters are different. It is clear that in vast contrast to the multi-resonance phenomenon in [6], [21], [22] where a fixed resonant frequency can be seen by the converters, the resonant frequencies seen by each converter in Fig. 2 are both different from its original resonant frequency. This will make some damping control methods that are effective in single converter operation become ineffective in a system with parallel converters. In particular, for converter 2, the higher resonant frequency is outside its control bandwidth and may even overlap with switching frequency harmonics or sidebands, which would be difficult to be damped. As a consequence, the methods that have been reported in the literature may not be effective in these scenarios. This example is a simple but representative case of what could be seen in real applications, especially in a residential microgrid, as different families will choose products from different manufacturers. In parallel with the continuous investigation on new control methods to address these issues, eliminating high-order filters is highly desirable for today's and future power grids with high penetration of power converters and intermittent renewable energy sources. The most effective way is to reconsider the use of low-order L filters. As such, stable operation of the system can be easily achieved and many filter resonance-induced issues, e.g., multi-resonance, can be naturally eliminated [30]. Moreover, removing the filter capacitors can also improve the overall system reliability [31], reduce the number of sensors, and eliminate the reactive power issue [32]. However, the L filter is typically bulky and costly as compared to the LCL filter, and thus is rarely adopted.

To enable the use of low-order L filter without sacrificing the point of common coupling (PCC) current quality and system power density, one promising way is to use multilevel converters. With a sufficiently high number of levels in the output voltage, the L filter may be applied. As of now, such a resonance-free design can be found with cascaded H-bridges (CHB) converters [33], [34] or modular multilevel converters (MMC) [35]. With CHB converters, phase-shifting of H-bridge modules offers harmonic cancellation and increases the

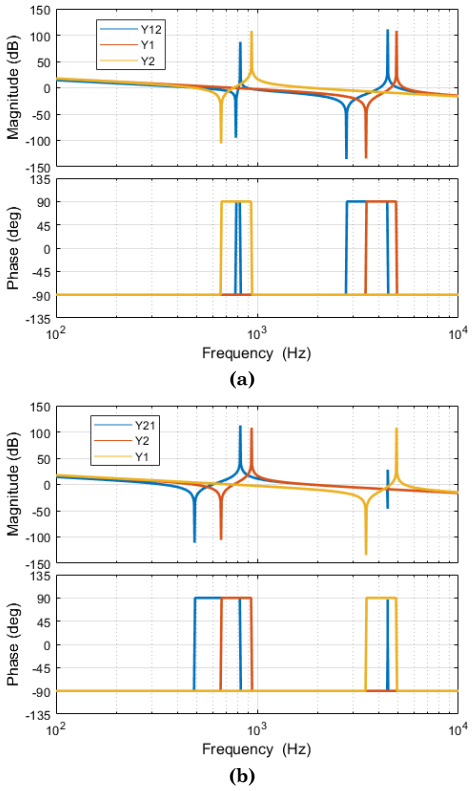


Fig. 2. Multi-resonance issue when two converters have different filter parameters, (a) the resonances seen by converter 1 (Y12) when paralleled with converter 2, (b) the resonances seen by converter 2 (Y21) when paralleled with converter 1. In both (a) and (b), Y1 shows the original filter resonance in converter 1 when it operates as a single converter. Likewise, Y2 shows the original resonance in converter 2 when it operates individually. The two converters have the same inductances, i.e., 105 uH at both converter side and grid side, but the capacitance is 20 uF in converter 1 and 550 uF in converter 2.

number of levels in the output voltage. Therefore, the single L filter becomes possible when sufficient H-bridge modules are applied. Similar to the CHB converters, MMC also can produce an output voltage with many levels. Moreover, the arm inductor in an MMC also provides filtering, and additional high order filters will not be necessary [35]. Beside CHB converters and MMCs, other high-level multilevel converters may also achieve the resonance-free design provided that a practical converter topology can be found. In general, high-level multilevel converters are more suitable for medium- and high-voltage applications, whereas simple two-level (2L) and three-level (3L) converters attract much popularity in low-voltage applications. Therefore, a resonance-free design methodology for low-voltage applications is still demanded.

As aforementioned, paralleling converters is popular, especially in low-voltage high power applications. Instead of simply paralleling LCL-filtered converters, it is necessary to rethink the system design of parallel converters and reconsider the use of L filter. In this regard, the modular parallel converter system with interleaving technique offers a great opportunity. By interleaving the converters, the frequency of the dominant harmonic can be pushed to the higher order region while its

amplitude can be reduced [36]-[38]. As such, twofold filtering requirement reduction is achievable, as can be observed in Fig. 3. It implies that with a certain number of parallel converters, there is a chance that the equivalent filter impedance provided by the parallel L filter would be sufficient to suppress the harmonics within the standard limits. Although interleaving has been a popular approach in the literature, many efforts have been focused only on the circulating current control of parallel converters [36]-[40]. Thus far, only a number of studies looked into the LCL filter designs for two interleaved converters [41], [42]. However, a system level design considering only L filters has never been discussed even with interleaving as an option. Therefore, in this paper, the feasibility of a system level design of parallel converters that adopts the interleaving technique and only an L filter in each converter is explored. It is envisaged that this paper can offer an alternative and practical implementation solution to the grid-tied parallel converters.

With only L filters, the conceptualized system architecture can be illustrated in Fig. 1 (b). As aforementioned, a common mode inductor may be included in each converter module. It should be noted that when an LCL filter is used in each converter module, interleaving or using asynchronous carriers is undesirable due to the potential instability issue [20]. Also, as the grid-side current harmonics are already below the limit, interleaving of LCL-filtered converters will not further reduce the filter size. On the contrary, interleaving will require the LCL filter to be larger due to the presence of circulating currents at the converter-side. It should also be noted that the conceptualized L filter-based system can utilize the same carrier synchronization approaches, e.g., optic fiber [43] or RS485 [18], which are currently used in parallel LCL-filtered converters, since the parallel converters are located close to each other in a PV inverter system, an AFE system of drives, or an interlinking converter station. Advanced methods such as decentralized carrier synchronization [44]-[46] and phase-locked loop-based synchronization [47] may also be applied to further enhance system reliability. Furthermore, by eliminating the filter resonance, the current control for each converter can be simplified. It will be unnecessary to have the knowledge of the overall system specifications when tuning controllers. Control methods such as deadbeat control [48] and model predictive control [49] may also be easily implemented. Based on the above discussion, a comparison between the proposed design and the LCL-filter-based design is summarized in Table I. In general, the proposed design does not introduce an additional challenge to system design. Many existing LCL-filter-based systems may even be retrofitted to the proposed L-filter-based system by simply removing the filter capacitor and modifying the carrier synchronization angle.

In light of the above concerns, the feasibility of the conceptualized L-filter-based grid-interfacing parallel converter system is investigated considering the power quality requirements on both the PCC current and voltage. It is anticipated that with a certain number of converters in parallel, only employing small-size L filters will be sufficient to meet the relevant demands in terms of harmonics. The key to the design is therefore the determination of the required number of converters that can produce a grid code-compatible PCC current.

TABLE I
COMPARISON BETWEEN THE PROPOSED PARALLEL CONVERTER SYSTEM AND LCL-FILTER-BASED SYSTEM.

	LCL-based	Proposed
Control complexity	complicated	simplified
Filter size	small	small
Filter resonance	multiple	none
System stability	less robust	robust
Carrier sync.	required	required
Reliability	high	very high

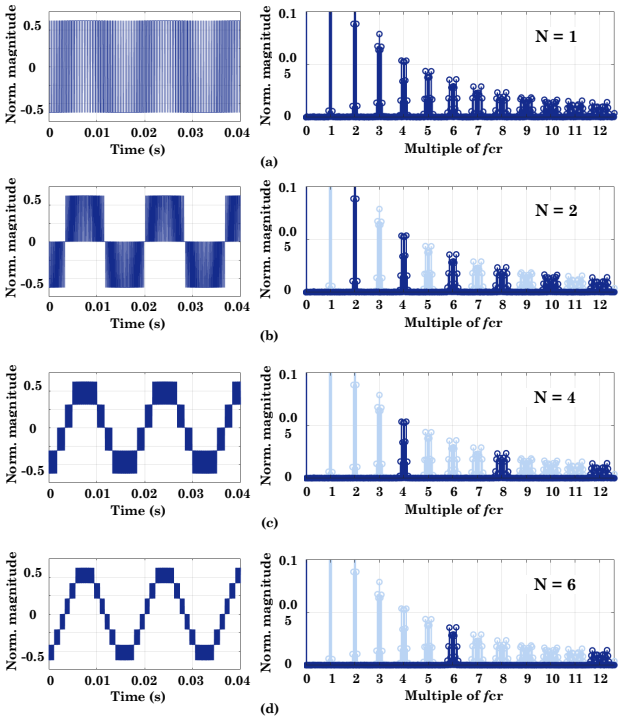


Fig. 3. Harmonics of parallel converters with the interleaving technique: (a) N = 1, (b) N = 2, (c) N = 4, and (d) N = 6. The waveforms and spectra are obtained by interleaving single phase-legs, and thus contain both differential-mode and common-mode harmonics in a three-phase system. The voltage waveforms are obtained by combining the voltages before the inductors to clearly show the number of voltage levels. In the spectra, the light color harmonics are canceled, and the remaining harmonics are highlighted in dark blue.

The analysis in this paper reveals that this number is irrelevant to the converter type or system parameters, e.g., the dc link voltage, carrier frequency, and power rating. As such, the study results can be adopted in a very wide range of applications. Moreover, it is found that compared to the LCL filter, the total inductance can be reduced with the proposed design. This indicates that with the proposed design, the dc link voltage can be even lower, which will further reduce the harmonics injected to the grid. It is also beneficial to the overall system efficiency as the switching loss could be reduced. Based on the general filter design principles [50], a filter size analysis indicates that for the same number of converters and same design criteria, the L-filter-based design can achieve over 32% filter size reduction in comparison to that with the minimized LCL, i.e., same inductance at the converter side and grid side [51], [52]. In practical applications, the converter side inductance of an LCL filter may be larger than the grid

side inductance, which will result in larger filter size and make the L-filter-based design even more favorable. Indeed, with more sophisticated LCL filter design techniques, e.g., magnetic integration [53], [54], the size of LCL filter can be reduced by about 20%, and may even be similar to that of the L filter with the conceptualized design. However, it should be pointed out that even with similar filter sizes, the L-filter based design is still desirable owing to the elimination of filter resonances. Also, in high power applications where standard cores are normally used, magnetic integration could be difficult and costly. In addition to current harmonics, a discussion on the impact of L-filter-based system design on the PCC voltage harmonics is also presented in this paper.

The rest of the paper is organized as follows: The analysis on the required number of interleaved converters is presented in Section II. The analysis starts from parallel two-level (2L) converters and is extended to multilevel converters. Section III discusses the practical considerations including filter size and the impact of interleaving on grid voltage harmonics. The proposed design is exemplified on a practical system in simulations, which is presented in Section IV. Simulation results with interleaved 2L converters and interleaved 3L converters (both with 6 converters in parallel) are presented to demonstrate the proposed design scheme. In Section V, the experimental results based on three interleaved 2L converters are presented to further verify the analysis. Finally, concluding remarks are provided in Section VI. Notably, the design approach in this study can be easily generalized to parallel converters with separate dc links. The findings of this study will serve as additional design criteria for the overall system. Particularly considering that many future projects, e.g., solar farms and energy storage systems, will be directly built in a modular structure with parallel inverters, the L-filter-based design methodology will be a very promising solution to achieve a resonance-free system.

II. Determination of the Required Number of Converters for the L-Filter-Based System

The key of the proposed design is to find the minimum number of N that can meet the standards. A generalized analysis without pre-defining specific system parameters is conducted. For simplicity, the following variables are defined: I_{tt} is the total root-mean-square (RMS) current at the PCC; ΔI_{pp} is the maximum peak-to-peak current ripple of each converter unit; K_{rp} is the ratio of ΔI_{pp} over the peak value of the fundamental current of each converter unit; $I_{h,N}$ is the amplitude of the dominant high frequency harmonic current seen at the PCC with N converters; $V_{h,N}$ is the amplitude of the dominant high frequency harmonic voltage seen at the PCC with N converters; $Z_{rq,N}$ is the required filtering impedance to limit $I_{h,N}$ according to the grid code; L_c is the filter inductance of each converter; $Z_{c,eq}$ is the equivalent filtering impedance at the PCC provided by N parallel converters; f_{cr} is the carrier frequency; f_s is the average device switching frequency; λ_N is the ratio of the maximum $V_{h,N}$ over the dc link voltage V_{DC} with different N and within a certain range of modulation index M.

The design of the conceptualized system has similar criteria as the design of an LCL-filter. The design procedure is illustrated in Fig. 4. Similar to the design of an LCL filter, the maximum converter side current ripple is considered to determine the filter inductance in each converter module. Then, the minimum filter inductance in each converter module, as well as the equivalent filtering impedance at the PCC, can be determined. Based on the harmonic limit requirement of the standards, the required impedance at the PCC can be derived. By ensuring that the equivalent filtering impedance is larger than the required impedance, the grid code can be satisfied and the required number of converters, N, can also be determined. It should be noted that the design presented in this section uses the common dc link type system as an example. However, the design procedure can also be performed for parallel converters with separate dc links.

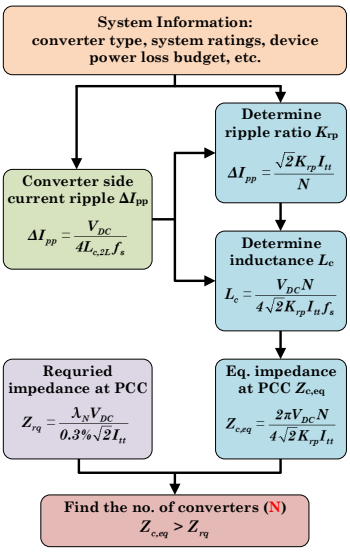


Fig. 4. Procedure of the determination of the required number of converters for the proposed architecture using the common dc link type parallel 2L converter system as an example.

The PCC current harmonic limits are defined by the standards IEEE std 519-2014 and IEEE std 1547-2018. The limits given in Table II are defined as "*be in percent of the maximum demand current*" in the IEEE std 519-2014 and "*in percent of rated current* " in the IEEE std 1547-2018. In the worst case, the harmonics beyond the 35th-order must be lower than 0.3% of the rated current [52], as given in Table II. Although the grid impedance will be large with smaller short circuit ratio (SCR), a conservative design is normally adopted in practice, especially for transformer-less applications. Therefore, 0.3% is selected as the design criterion for the dominant harmonics. Note that the IEEE std. 1547-2018 requires that all distributed energy resource systems should satisfy the limits with SCR less than 20.

A. Converter Side Current Ripple with Interleaving

When multiple 2L VSCs are interleaved, the output current of each converter is dominated by the high frequency circulating current (CC). The value of ΔI_{pp} can be determined

TABLE II
ODD ORDER CURRENT HARMONIC LIMITS DEFINED BY GRID CODES.

SCR	<11	[11,17)	[17,23)	[23,35)	≥35	THD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20...50	7.0	3.5	2.5	1.0	0.5	8.0
50...100	10.0	4.5	4.0	1.5	0.7	12.0
100...1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

according to Fig. 5, where the ripple current waveform i_{ripple} within one switching cycle is illustrated. As the CC is irrelevant to the load, a no-load condition is assumed in Fig. 5. Note that only two converters are assumed with $Cr1$ and $Cr2$ being the carrier of each converter. Furthermore, for 2L VSCs, the switching cycle period $T_s = 1/f_s = 1/f_{cr}$.

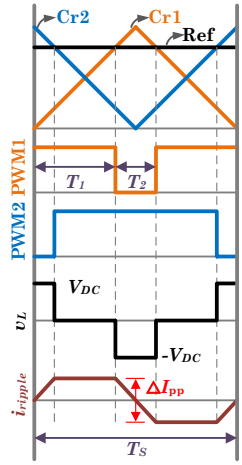


Fig. 5. Illustration of the converter side current ripple in each converter when interleaving is applied. $N = 2$ is assumed.

With a sinusoidal reference, T_1 and T_2 can be given as (1) and (2), respectively, where ω_1 is the fundamental angular frequency. Based on Fig. 5, the peak-to-peak current ripple can be expressed as (3). It indicates that ΔI_{pp} is a fixed value, which can be given as (4). Note that this result is also valid for all pulse-width modulation (PWM) strategies and for systems with more than two interleaved converters.

$$T_1 = \frac{1}{2}T_s\left(M\sin\left(\omega_1 t\right)+1\right) \tag{1}$$

$$T_2 = \frac{1}{2}T_s\left(1-M\sin\left(\omega_1 t\right)\right) \tag{2}$$

$$i_{ripple} = \frac{V_{DC}T_2}{2L_{c,2L}} = \frac{V_{DC}T_s}{4L_{c,2L}}\left(1-M\sin\left(\omega_1 t\right)\right) \tag{3}$$

$$\Delta I_{pp} = \frac{V_{DC}T_s}{4L_{c,2L}} = \frac{V_{DC}}{4L_{c,2L}f_s} \tag{4}$$

B. Required Number of Converters to Meet the Standards

As mentioned previously, the converter-side current ripple ratio K_{rp} is usually adopted in filter designs, which can be written as (5) for a system with N 2L VSCs. As such, the filtering inductance of each converter can be given in (6). The equivalent filtering impedance at the PCC can then be determined by (7).

$$\Delta I_{pp} = \frac{\sqrt{2}K_{rp}I_{tt}}{N} \tag{5}$$

$$L_{c,2L} = \frac{V_{DC}N}{4\sqrt{2}K_{rp}I_{tt}f_s} \tag{6}$$

$$Z_{c,eq,2L} = 2\pi f_s\frac{L_{c,2L}}{N}N = \frac{2\pi V_{DC}N}{4\sqrt{2}K_{rp}I_{tt}} \tag{7}$$

To meet the grid-connection requirements, $Z_{c,eq,2L}$ must be larger than the required impedance, $Z_{rq,N}$, as written in (8), where $Z_{rq,N}$ can be given by (9). Substituting (7) and (9) into (8) gives the minimum N in (10).

$$Z_{c,eq,2L} \geq Z_{rq,N} \tag{8}$$

$$Z_{rq,N} = \frac{V_{h,N}}{I_{h,N}} = \frac{\lambda_N V_{DC}}{0.3\%\sqrt{2}I_{tt}} \tag{9}$$

$$N \geq \frac{4K_{rp}\lambda_N}{2\pi\times 0.3\%} \approx 212.21K_{rp}\lambda_N \tag{10}$$

It is interesting to see from (10) that N is irrelevant to the specific system parameters, e.g., V_{DC}, f_s, or I_{tt}. As such, the relationship derived in (10) is not limited to any specific applications. The only variable needs to be considered is the converter-side current ripple ratio K_{rp}. The value of K_{rp} is normally determined based on the requirement of conduction losses and the allowed filter inductor size. In most designs, the range of K_{rp} is usually within 50% to 20%. For λ_N, the double Fourier integral analysis [55] or simulations can be carried out to find the maximum value for a given range of M. Depending on the structure of the converter module, different modulation schemes may be implemented, resulting in various harmonics. Different PWM schemes can be applied, which may lead to diverse harmonic amplitudes. Here, the most commonly used space vector modulation (SVM) is assumed. If a common mode inductor (CMI) is employed in each converter module, the PWM scheme proposed in [38] may also be applied to reduce the size of the CMI. Other modulation strategies such as various types of discontinuous PWM (DPWM) methods may also be applied. Using the SVM as an example, the values of λ_N are calculated and listed in Table III. Depending on the applications, the nominal operating point of M can be various. However, the rule-of-thumb is to operate the converter at a higher M value to increase the dc voltage utilization. Therefore, the selected range of M is from 0.9 to 1.1. In the event of fault ride-through, M may be reduced and the harmonic amplitude may increase. However, the latest versions of the grid codes also allow the harmonics to exceed the limits in a short period [2], and the requirements are generally defined under rated and normal conditions.

According to the results in Table III, the value of N can be determined based on (10). Assuming K_{rp} is 50%, which stands for the minimum filtering inductance, N should be equal or higher than 5 in order to meet the harmonic limit

TABLE III
λ_N WITH RESPECT TO N FOR 2L CONVERTERS.

N	2	3	4	5	6
λ_N	0.149	0.0586	0.085	0.0364	0.0541

requirement. In practical applications like a hybrid ac/dc grid and low voltage drives, the number of converters can be much higher than 5, which suggests that interleaving the converters can be a viable solution.

C. System Design with Multilevel VSCs

The analysis for 2L VSCs is generalized to multilevel converters based on the CC scaling law given in (11), where R is the equivalent switching frequency ratio, f_s is the average switching frequency of each device, N_L is the number of converter levels, and L_f is the filter inductance.

$$MAX_{CC} \propto \frac{V_{DC}}{R * f_s \left(N_L - 1\right) L_f} \tag{11}$$

Based on (11), given the same filter and device switching frequency, the amplitudes of the CC are determined by R and N_L, which are further defined by the topology of the converter. For example, the 5-level active neutral point-clamped (5L ANPC) converter results in $R = 2$ and $N_L = 5$. This scaling law also reflects the scaling of the converter-side current ripple, upon which (4) can be adapted for different types of converters. Following the same design procedure, the determinations of N of 3L VSCs and 5L VSCs are given in (12) and (13), respectively.

$$N_{3L} \geq 424.43 K_{rp} \lambda_{N,3L} \tag{12}$$

$$N_{5L} \geq 848.83 K_{rp} \lambda_{N,5L} \tag{13}$$

The values of λ_N for 3L and 5L VSCs are listed in Table IV. For 3L VSCs, the PWM scheme proposed in [36] is selected to reduce the common mode CC. Whereas for the 5L VSCs, the phase shift PWM is considered. Assuming K_{rp} is 50% for all types of converters, the required N for 3L VSCs is 6 and for 5L VSCs is 5. It is interesting to see that the numbers of required converters are similar for converters with a different number of levels. The reason is that with high-level VSCs and the same K_{rp}, the filter inductance and λ_N are reduced at the same rate.

TABLE IV
VALUES OF λ_N WITH RESPECT TO N FOR 3L AND 5L VSCS.

N	2	3	4	5	6
$\lambda_{N,3L}$	0.0862	0.0236	0.0315	0.0343	0.0233
$\lambda_{N,5L}$	0.0335	0.0234	0.0124	0.0103	0.00727

III. PRACTICAL CONSIDERATIONS

In this section, some practical design considerations, including a filter size comparison and the PCC voltage quality with L filter are discussed.

A. Potential Filter Size Reduction Opportunity

To demonstrate that the proposed design can eliminate the filter resonance while maintaining a reasonable filter size, a general volume comparison analysis is presented without assuming any system parameters. Provided that the filter design for the LCL filter-based system has met the harmonic limit standard, its converter side inductance $L_{c,LCL,2L}$ can be used as a base value L_b, upon which the filter inductance for the proposed L filter-based design can be obtained, being proportional to L_b. Notably, to ensure a fair comparison, K_{rp} remains unchanged.

Taking a 2L converter as an example, the converter side inductance $L_{c,LCL,2L}$ is usually selected according to the requirement of K_{rp}. When the parallel converters are synchronized, the maximum converter-side current ripple $\Delta I_{pp,LCL}$ is given by (14) due to the absence of the CC [35]. As a result, $L_{c,LCL,2L}$ can be designed following (15).

$$\Delta I_{pp,LCL} = \frac{V_{DC}}{6 L_{c,LCL,2L} f_s} \tag{14}$$

$$L_{c,LCL,2L} = \frac{V_{DC} N}{6\sqrt{2} K_{rp} I_{tt} f_s} \tag{15}$$

To minimize the total size of the LCL filter, the grid side inductance $L_{g,LCL,2L}$ should be the same as the converter side inductance [50], [51]. The volume of an inductor can be evaluated based on the area product, A_p, as given by (16), where K_j is the winding current density, k_f is the filling factor of the winding area, and B_m is the maximum flux density [49].

$$Vol \propto {A_p}^{3/4} = (\frac{L I^2}{K_j k_f B_m})^{3/4} \tag{16}$$

Given the same design condition, the total volumes resultant from the two designs can be obtained as (17). The inductance values are normalized to the base value L_b. The filter inductance in each converter module with the L-filter-based design is $1.5 L_b$. With the LCL filter, both inductors in one converter module will be L_b. Consequently, the ratio of Vol_L over Vol_{LCL} can be calculated as 0.678, suggesting that the L-filter-based design can potentially reduce filter size by 32%.

$$Vol_L \propto (1.5 L_b)^{3/4} \quad Vol_{LCL} \propto 2 {L_b}^{3/4} \tag{17}$$

For multilevel converters, the comparison result will still be the same, as the inductances in synchronous and interleaved cases scale with the same order. The above result confirms that the proposed method can eliminate the filter resonance issues without increasing the filter size. Moreover, a potential filter size as well as cost reduction opportunity may be available with the proposed design. However, it is noteworthy that the analysis in this section only considers the standard design of an LCL filter without magnetic integrations. If magnetic integration designs are applied to the LCL filter, the total filter wolume with the proposed system could be similar to that with LCL filter. Nevertheless, in this case, the proposed L-filter-based design is still favorable due to the elimination of the filter resonance.

B. Impact on Voltage Quality

In addition to the current harmonics, the impact of the filter configuration on the voltage quality should also be discussed. In the latest version of the IEEE std 1547-2018 [1], the voltage harmonic limits are excluded from the power quality requirement on the grid-tied converters. Therefore, only using L filter in grid-tied distributed energy resource (DER) systems, e.g., a PV farm, will not raise any concerns on the voltage quality.

On the other hand, the IEEE std 519-2014 [2] limits the individual voltage harmonic below 5% of the rated voltage and the total harmonic distortion (THD) less than 8% for applications with the bus voltage at the PCC lower than 1 kV. With the LCL filter, a sinusoidal voltage can be achieved. However, without any filter capacitor, the grid voltage may be affected by the PWM harmonics depending on the grid impedance. If the grid is stiff, all harmonics will be imposed at the converter side and the grid voltage will be clean. In contrast, in weak grid condition, a large portion of PWM harmonics will be applied at the grid side. However, this should not become a concern. Based on the IEEE Std 519-2014, the PCC grid voltage harmonics should be measured at the high voltage side of the dedicated service transformer for industry users. Therefore, the transformer leakage inductance can be included as part of the filter inductance and the ratio between the grid impendence and the filter impedance will usually not be large. As such, a smaller portion of harmonics will be propagated to the grid voltage. Moreover, as given in Fig. 3, with more converters, the amplitude of harmonics can generally be reduced. Therefore, with a sufficient number of converters, the individual harmonic amplitudes will not exceed the limits even under very weak grid conditions. Simulations to be presented in the next section will confirm that with 6 or more converters, the voltage harmonic limits can be satisfied under very weak grid conditions. Finally, the IEEE std 519-2014 defines that the THD should be calculated "*considering harmonic components up to the 50th order*". Moreover, the utility companies are more concerned of the low-order harmonics, as high-order harmonics may not appear significantly in a large system with multiple units. Therefore, as long as the control system does not generate large low-order harmonics, the voltage harmonic limits can be easily satisfied for the proposed design, especially considering that the dominant harmonics will be much higher than the 50th-order frequency with interleaving operation.

IV. Simulation Results

For a fair comparison, an LCL-based benchmark with properly designed filter parameters must be selected. A benchmark design for the LCL filter reported in [52] is selected to demonstrate the proposed design in simulations. The objective of the benchmark was to minimize the weight of the LCL filter for a 1.2-MW 690 Vac single 2L inverter with a 50 Hz grid frequency. With the analysis and design in [52], it is found that the optimal filter parameters for the benchmark system are: 104 uH inductor at the converter side, 552 uF filter capacitor, and 105 uH inductor at the grid side, when the SVM scheme is applied with a 2.6 kHz switching frequency. To compare with the proposed interleaving-based design, this benchmark is scaled to 6 parallel 200-kW 2L VSCs and 3L VSCs, and the filter parameters are scaled accordingly, which is given in Table V. As analyzed in previous sections, 5 converters are sufficient to meet the harmonic requirement with only L filters. However, in the simulation with 3L VSCs, the modulation scheme in [36] is applied and 6 converters are required to meet the harmonic limit requirement. Therefore, 6 converters are adopted for both 2L and 3L VSCs in most of the simulation results. However, simulation results with $N = 5$ and $N = 4$ are also presented for 2L converters, as shown in Fig. 6. The filter parameters are obtained by scaling the system in [52] to 5 parallel converters or 4 converters. With the proposed L-filter based design, the filter parameters are 746 uH for $N = 5$ and 597 uH for $N = 4$ when K_{rp} of 50% is considered. With 5 converters in parallel, the high frequency harmonics in the output current is below the limit set by the standards. However, when only using 4 converters, the harmonics will exceed the limit. But according to (10), when K_{rp} is less than 22.18%, 4 converters will be sufficient to satisfy the harmonic standard. This can be confirmed by the simulated grid current spectrum with K_{rp} being 22% as given in Fig. 6 (c).

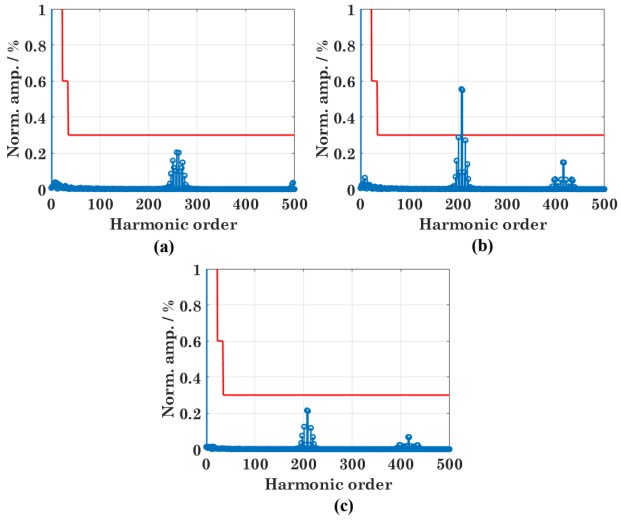


Fig. 6. Simulated grid current spectrum with (a) 5 converters and 50% K_{rp}, (b) 4 converters and 50% K_{rp}, and (c) 4 converters and 22% K_{rp}.

For the rest of the simulation, the system parameters are shown in Table V, where L-2L means the L-filter-based design with 2L converters and L-3L means parallel 3L converters with L-filters. Based on the proposed design approach, the filter parameters for interleaved 2L converters and interleaved 3L converters are also designed. As seen in Table V, for the 2L converter-based system, the proposed design uses less inductance than the benchmark design.

The performance of the benchmark design has been proved in [40], and thus, will not be repeated. The simulation results with 6 interleaved 2L converters are shown in Fig. 7 for the rated operation condition. As observed in Fig. 7, the output current of one converter has obvious switching frequency ripples. However, the current flowing into the PCC is clean.

TABLE V
SYSTEM PARAMETERS FOR SIMULATION.

Parameter	Benchmark	L-2L	L-3L
Line-to-line voltage		690 V	
DC link voltage		1100 V	
Rated total power		1.2 MW	
Power factor		1.0	
Grid frequency		50 Hz	
Carrier frequency		2600 Hz	
K_{rp}		50%	
N		6	
L_c	624 uH	895 uH	447 uH
Filter capacitance	92 uF	N/A	N/A
Grid side inductance	630 uH	N/A	N/A
Total inductance	209 uH	150 uH	75 uH

The harmonic spectrum of the PCC current in the normal operation condition is shown in Fig. 8 (a), where the red line denotes the limit set by the standard. It can be seen that the dominant switching frequency harmonics are pushed to the sixfold switching frequency. More importantly, the grid code is satisfied. As aforementioned, lower grid voltage and thus lower M may result in higher harmonics. For 6 interleaved 2L VSCs, the dominant harmonics reach their highest value when M is around 0.6, the PCC current with a 390 V grid voltage is also simulated. The spectrum in Fig. 8 (b) confirms an increase of the dominant harmonics in the PCC current.

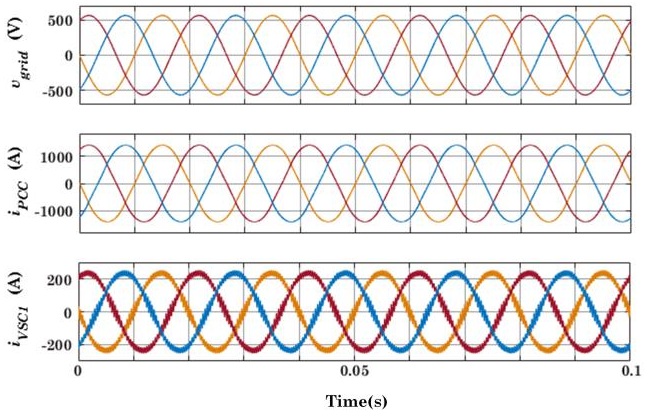


Fig. 7. Simulated waveforms with 6 interleaved 2L converters, where v_{grid} is the grid voltage, i_{PCC} is the total current injected into PCC, i_{VSC1} is the output current of converter 1.

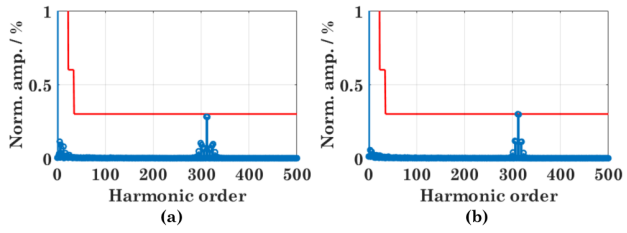


Fig. 8. Harmonic spectrum of the PCC current i_{PCC} of 6 interleaved 2L converters (a) in the normal operation and (b) when the grid voltage is 390 V.

In all, the above simulation results confirm that with the proposed resonance-free design methodology, L filter, same as LCL filter, can also meet the current harmonic limit requirement. Based on the area product approach, the filter volume with different designs can be compared using the parameters in Table V. As the converter side inductors are subjected to current ripples, the actual peak current, i.e., 255 A, should be considered for the converter side inductor L_c, while a pure sinusoidal current, i.e., 237 A, can be assumed when evaluating the grid side inductor in the LCL filter. Assuming the same core material and allowed peak flux, the volume of an inductor is proportional to $(LI^2)^{3/4}$ according to (16). Therefore, the inductor in each converter of the L-filter-based design is proportional to a coefficient of 21. The volume coefficient for L_c of the LCL filter is 16 and for the grid side inductor is 14.5, resulting in a total volume coefficient of 30.5. Compared to the LCL filter, the L filter can reduce the total filter size by around 31.1%, which is close to the theoretical result in Section III-A. Moreover, the total filter inductance in each converter with the proposed L-filter based design is smaller than that with the LCL-filter. As such, the dc link voltage with the proposed design can actually be lower. This will further reduce the switching loss of the converter and the current harmonics injected to the grid.

The spectrum of the PCC current in simulations with interleaved 3L converters are shown in Fig. 9 (a) for the normal operation, indicating that the performance of the design in fact excels to a large extent. The reason is that with 6 3L VSCs, K_{rp} can actually be higher than 50% in order to satisfy the grid code. Therefore, the filter inductance in Table V can still be smaller, or with a lower grid voltage, and hence lower M, the grid code can still be met with the same filters. This can be confirmed by the PCC current spectrum shown in Fig. 9 (b) when the grid voltage is set to 350 V. It can be observed in Fig. 9 (b) that the magnitude of the dominant harmonic almost hits the limit (i.e., still below the standard limit).

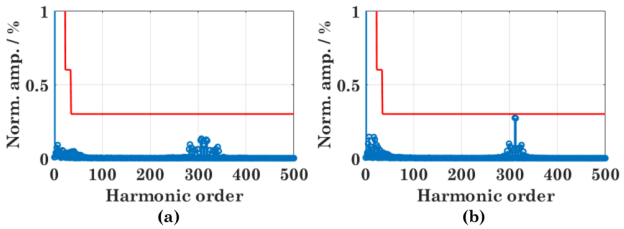


Fig. 9. Harmonic spectrum of the PCC current i_{PCC} resultant of 6 interleaved 3L converters (a) in the normal operation and (b) when the grid voltage is 350 V.

Furthermore, simulations with different N and K_{rp} are also performed. With 5 interleaved 3L VSCs, L_c in each converter is 373 uH for $K_{rp} = 50\%$. The spectrum of the PCC current in this case is shown in Fig. 10 (a), implying that the harmonic limit requirement is not satisfied, as indicated by (12). However, if the requirement on K_{rp} is 25% (i.e. $L_c = 596uH$), $N = 4$ will be sufficient to meet the grid code. The corresponding spectrum of the PCC current in this case is shown in Fig. 10 (b), demonstrating the effectiveness of the proposed design.

To show the impact on the PCC voltage, simulation results

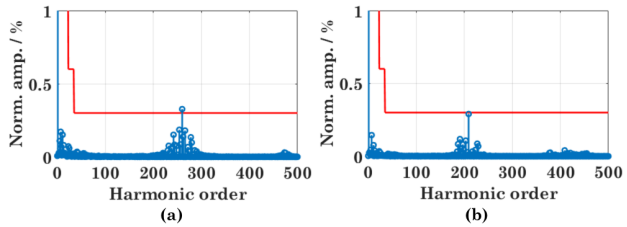


Fig. 10. Harmonic spectrum of the PCC current i_{PCC} of (a) 5 interleaved 3L converters and $K_{rp} = 50\%$, and (b) 4 interleaved 3L converters and $K_{rp} = 25\%$.

considering the grid impedance are also obtained. Fig. 11 (a) shows the spectrum of the PCC grid voltage using 6 interleaved 2L converters with parameters given in Table V and the SCR of 10. The amplitude of the largest dominant harmonic is 4.9% of the fundamental component suggesting that the voltage harmonic limit can be met under this very weak grid condition. However, if the grid is extremely weak, the harmonics will exceed the limit as can be seen from the spectrum in Fig. 11 (b), which is obtained with an SCR less than 1 and the grid inductance being 20 times of the total filter inductance seen by the grid. Nevertheless, since the dominant harmonics are around the 300th order, which is much higher than the 50th order, these harmonics will not be limited anyway. Moreover, if the number of converters is increased to 7 with the same total system power capacity, the individual harmonic amplitude can be limited within 5%, even when the SCR is less than 1 and the grid inductance is 20 times of the total filter inductance. This can be seen from the spectrum in Fig. 11 (c). Note that the transformer was not applied in the above simulations. In practical applications, the leakage inductance of the transformer will further mitigate the harmonics drop on the PCC voltage.

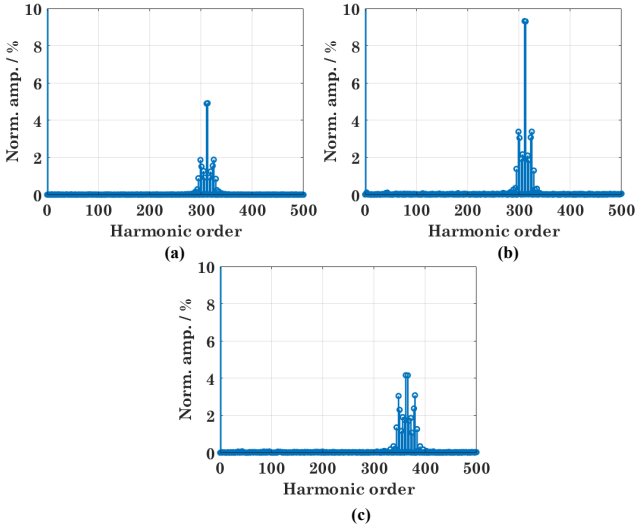


Fig. 11. Harmonic spectra of the PCC voltage with (a) 6 interleaved 2L converters and SCR = 10, (b) 6 interleaved 2L converters and SCR $\leq$ 1, and (c) 7 interleaved 2L converters and SCR $\leq$ 1.

V. Experimental Results

Experimental verifications have been carried out with three interleaved three-phase 2L converters. The nominal RMS line-to-line grid voltage is 120 V. The grid frequency is 50 Hz. The dc link voltage is 185 V. The switching frequency is 10 kHz. The total power at the nominal grid voltage is 2 kW. Based on Table III and (13), K_{rp} should be less than 24% for $N = 3$ in order to satisfy the grid code. The corresponding filter inductance in each converter module should be larger than 4.1 mH for the experimental setup. In the experimental tests, each converter adopts three 4.5 mH filter inductors. Experimental results with the nominal grid voltage are shown in Fig. 12. As expected, ripples can be observed in the output current from one converter module. While after interleaving, the total output current becomes clean.

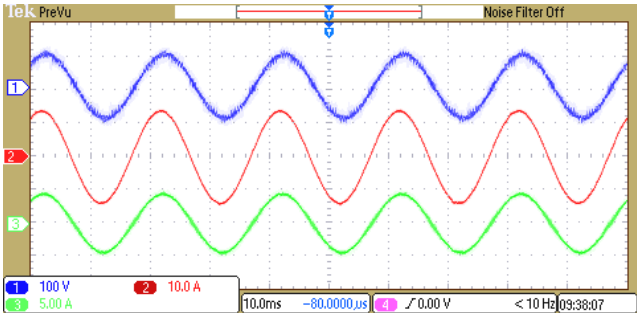


Fig. 12. Experimental waveforms at the nominal grid voltage. Ch1: line-to-neutral grid voltage. Ch2: total output current. Ch3: output current from one converter module.

The spectra of the total current and module current are shown in Fig. 13. The harmonic amplitudes are normalized with respect to the corresponding fundamental component. As shown in Fig. 13 (c), switching-frequency harmonics around the 200th-order and 400th-order present in the output current of an individual converter. After interleaving, these harmonics are canceled. The dominant harmonics of the total current are below the harmonic limit of the grid code. Moreover, since the filter inductance is higher than the required value, and the actual modulation index M is higher than the point where λ_N in Table III is obtained, the harmonic amplitude at the 600th order is much lower than 0.3%. Using the same system parameters, the spectrum of the total output current obtained from simulations is compared, as given in Fig. 13 (b), further confirming the theoretical analysis and the effectiveness of the proposed.

With a lower grid voltage, i.e., 55 V RMS line-to-neutral voltage, the experimental results are presented in Fig. 14. The ripples in the output current of one converter increase as the modulation index drops. The spectra of the measured total current, simulated total current, and measured output current of one converter are presented in Fig. 15. An obvious rise in the dominant harmonics in the total output current can be observed. As the filter in the experiment is larger than the minimum required value, the grid code can still be met in this case. As seen in Fig. 15 (b), the experimental results are in a close agreement with the simulations, which verifies the analysis. In all, the above simulations and experimental

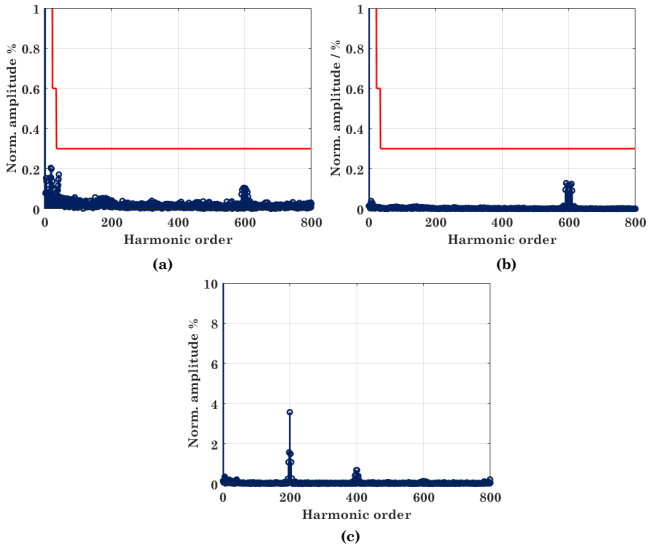


Fig. 13. Harmonic spectra of (a) total output current in the experimental, (b) simulation results using the same system parameters, and (c) output current of one module in the experiment. The red line indicates the harmonic limit set by the grid code.

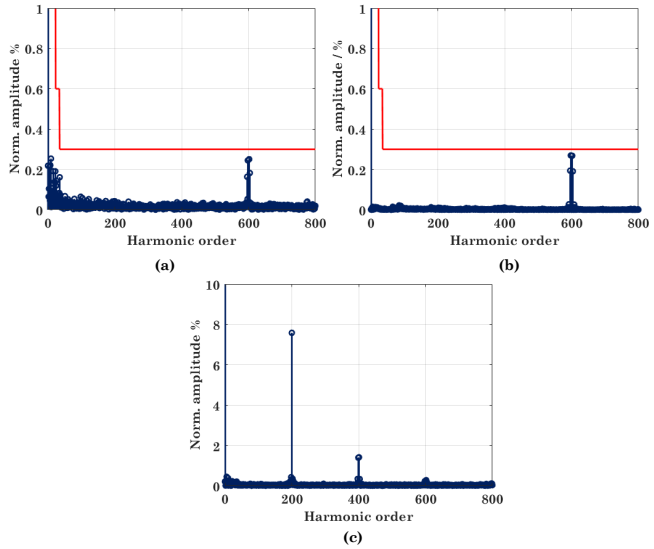


Fig. 15. Harmonic spectra of (a) total output current in the experiment, (b) simulation results using the same system parameters, and (c) output current of one module in the experiment. The red line indicates the harmonic limit set by the grid code.

tests have verified the effectiveness of the proposed design with L filters, which can be a promising solution to parallel converters.

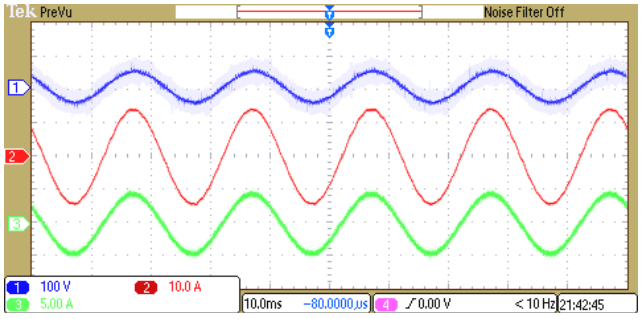


Fig. 14. Experimental waveforms at lower grid voltage. Ch1: line-to-neutral grid voltage. Ch2: total output current. Ch3: output current from one converter module.

VI. Conclusion

This paper reconsiders the utilization of low-order L filters in modular parallel converters to achieve resonance-free and satisfactory power quality. By leveraging the interleaving technique, only using small size L filters will be sufficient to meet the harmonic requirements set by the standards. As such, the LCL filter and the associated filter resonance issues can be eliminated in parallel converters. Moreover, the L filter in the proposed design can be even smaller than the LCL filter. The analysis reveals that the minimum number of converters that can meet the grid code is not related to the specific system parameters, e.g., the switching frequency or power rating. Rather, it is only determined by the converter side current ripple ratio and the harmonic amplitude resultant from a certain PWM strategy. In addition, the impact of the proposed design on the PCC voltage harmonics is also discussed based on the latest grid codes, indicating that the PCC voltage can still comply with the grid codes with only L filters. Simulation results based on a LCL benchmark design have been obtained, considering both interleaved 2L and 3L converters. Experimental results obtained with three interleaved 2L converters also confirm the effectiveness of the design approach. In conclusion, the proposed solution can be very promising for parallel power converter applications with reduced total costs and simplified control, while maintaining the high-performance in power quality at the PCC.

References

[1] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003) pp.1-138, 6 April 2018.

[2] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," IEEE Std 519-2014 (Revision of IEEE Std 519-1992) pp.1-29, 11 June 2014.

[3] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg and C. L. Bak, "A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54-69, March 2016.

[4] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-Filter Design for a Multimegawatt Medium-Voltage Voltage-Source Inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205-1217, April 2011.

[5] J. He, Y. W. Li, R. Wang, and C. Zhang, "Analysis and Mitigation of Resonance Propagation in Grid-Connected and Islanding Microgrids," *IEEE Trans. Energy Convers.*, vol. 30, no. 1, pp. 70-81, March 2015.

[6] J. He, Y. W. Li, D. Bosnjak and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 234-246, Jan. 2013.

[7] R. Pena-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez and Y. Yang, "LCL-Filter Design for Robust Active Damping in Grid-Connected Converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 4, pp. 2192-2203, Nov. 2014.

[8] J. S. Siva Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76-91, Jan. 2014.

[9] C. Wang, B. Liang and J. He, "An Enhanced Power Regulation and Seamless Operation Mode Transfer Control Through Cooperative Dual-Interfacing Converters," *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 5576-5587, Nov. 2018.

[10] X. Yu, A. M. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system", *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3881-3889, Oct. 2012.

[11] P. Yang, Y. Xia, M. Yu, W. Wei and Y. Peng, "A Decentralized Coordination Control Method for Parallel Bidirectional Power Converters in a Hybrid ACCDC Microgrid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6217-6228, Aug. 2018.

[12] Ki-Bum Park, Frederick Kieferndorf, Uwe Drofenik, Sami Pettersson, Francisco Canales, "Optimization of LCL filter with intercell transformer for interleaved voltage source converter", Industrial Electronics Society IECON 2017 - 43rd Annual Conference of the IEEE, pp. 1375-1380, 2017.

[13] E. C. dos Santos, C. B. Jacobina, N. Rocha and E. R. C. da Silva, "Six-Phase Machine Drive System With Reversible Parallel ACCDCCAC Converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 2049-2053, May 2011.

[14] G. Konstantinou, J. Pou, G. J. Capella, K. Song, S. Ceballos and V. G. Agelidis, "Interleaved Operation of Three-Level Neutral Point Clamped Converter Legs and Reduction of Circulating Currents Under SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3323-3332, June 2016.

[15] C. Ditmanson, P. Hein, S. Kolb, J. Molck and S. Bernet, "A New Modular Flux-Switching Permanent-Magnet Drive for Large Wind Turbines, *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3787-3794, Nov.-Dec. 2014.

[16] R. Li and D. Xu, "Parallel Operation of Full Power Converters in Permanent-Magnet Direct-Drive Wind Power Generation System," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1619-1629, April 2013.

[17] G. Chen and X. Cai, "Adaptive Control Strategy for Improving the Efficiency and Reliability of Parallel Wind Power Converters by Optimizing Power Allocation," *IEEE Access*, vol. 6, pp. 6138-6148, 2018.

[18] T. Xu and F. Gao, "Global Synchronous Pulse Width Modulation of Distributed Inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6237-6253, Sept. 2016.

[19] Z. Quan and Y. W. Li, "Impact of PWM Schemes on the Common-Mode Voltage of Interleaved Three-Phase Two-Level Voltage Source Converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 852-864, Feb. 2019.

[20] D. Yang, X. Wang and F. Blaabjerg, "Sideband Harmonic Instability of Paralleled Inverters With Asynchronous Carriers," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4571-4577, June 2018.

[21] J. L. Agorreta, M. Borrega, J. Lopez and L. Marroyo, "Modeling and Control of N -Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 770-785, March 2011.

[22] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 894-899, Feb. 2017.

[23] X. Wang, F. Blaabjerg and P. C. Loh, "Passivity-Based Stability Analysis and Damping Injection for Multiparalleled VSCs with LCL Filters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8922-8935, Nov. 2017.

[24] Adapa Anil K. and Vinod John. "Virtual resistor based active damping of LC filter in standalone voltage source inverter." Applied Power Electronics Conference and Exposition (APEC), 2018, pp. 1834-1840.

[25] Chilipi, Raja Sekhara Reddy, Naji Al Sayari, Khalifa Hassan Al Hosani, and Abdul R. Beig. "Adaptive Notch Filter-Based Multipurpose Control Scheme for Grid-Interfaced Three-Phase Four-Wire DG Inverter." *IEEE Trans. Ind. Appl.*, vol.53, no. 4, 2017, pp.4015-4027.

[26] Yongsheng Fu, Yang Huang, Xi Lu, Ke Zou, Chingchi Chen and Hua Bai, "Imbalanced Load Regulation Based on Virtual Resistance of A Three-phase Four-wire Inverter for EV Vehicle-to-Home Applications, *IEEE Trans. Transp. Electr.*, vol.5, no.1, 2019, pp.162-173.

[27] X. Wang, Y. W. Li, F. Blaabjerg and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019-7037, Dec. 2015.

[28] J. He and Y. W. Li, "Analysis, Design, and Implementation of Virtual Impedance for Power Electronics Interfaced Distributed Generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2525-2538, Nov.-Dec. 2011.

[29] SMA technical document, "Important Requirements for Medium-Voltage Transformers SUNNY TRIPOWER".

[30] T. Xu and F. Gao, "Stability performance of multi-connected inverters with global synchronous pulse width modulation," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 3871-3876.

[31] D. Zhou, H. Wang, H. Wang and F. Blaabjerg, "Reliability analysis of grid-interfaced filter capacitors," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 21-28, September 2018.

[32] Y. Jiao and F. C. Lee, "LCL Filter Design and Inductor Current Ripple Analysis for a Three-Level NPC Grid Interface Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4659-4668, Sept. 2015.

[33] J. E. Huber and J. W. Kolar, "Optimum Number of Cascaded Cells for High-Power Medium-Voltage ACCDC Converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 213-232, March 2017.

[34] M. Kasper, D. Bortis, G. Deboy and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm ^{3}) Isolated ACCDC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750-7769, Oct. 2017.

[35] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662-669, June 2005.

[36] Z. Quan and Y. W. Li, "Phase-Disposition PWM Based 2DoF-Interleaving Scheme for Minimizing High Frequency ZSCC in Modular Parallel Three-Level Converters," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10590-10599, Nov. 2019.

[37] S.K.T. Miller, T. Beechner, J. Sun, "A Comprehensive Study of Harmonic Cancellation Effects in Interleaved Three-Phase VSCs," in Power Electronics Specialists Conference, 2007. PESC 2007. IEEE , vol., no., pp.29-35, 17-21 June 2007

[38] Z. Quan and Y.W. Li, "Suppressing Zero-Sequence Circulating Current of Modular Interleaved Three-Phase Converters Using Carrier Phase Shift PWM," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3782-3792, July-Aug. 2017.

[39] J. S. S. Prasad, R. Ghosh and G. Narayanan, "Common-Mode Injection PWM for Parallel Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 789-794, Feb. 2015.

[40] T. Wu, L. Yu, Y. Huang, Y. Jhang and B. Zeng, "SPWM-Based Direct Digital Control With Average-Voltage Model and DC Process for Paralleled 33W Grid-Connected Converters to Reduce Circulating Currents," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4436-4446, June 2019.

[41] Ki-Bum Park, Frederick Kieferndorf, Uwe Drofenik, Sami Pettersson, Francisco Canales, "Optimization of LCL filter with intercell transformer for interleaved voltage source converter", Industrial Electronics Society IECON 2017 - 43rd Annual Conference of the IEEE, pp. 1375-1380, 2017.

[42] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes and F. Blaabjerg, "Line Filter Design of Parallel Interleaved VSCs for High-Power Wind Energy Conversion Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775-6790, Dec. 2015.

[43] M. Borrega, L. Marroyo, R. Gonzlez, J. Balda and J. L. Agorreta, "Modeling and Control of a MasterCSlave PV Inverter With N-Paralleled Inverters and Three-Phase Three-Limb Inductors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2842-2855, June 2013.

[44] J. He, Z. Dong, Y. Li and C. Wang, "Parallel-Converter System Grid Current Switching Ripples Reduction Using a Simple Decentralized Interleaving PWM Approach," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8581-8592, Aug. 2020.

[45] J. He, Z. Dong, Y. Wang and C. Wang, "Cost-Effective Islanded Electrical System with Decentralized Interleaving PWM for Converter Harmonic Reduction," *IEEE Trans. Ind. Electron.*, early access, 2020.

[46] G. Gateau, M. Cousineau, M. Mannes-Hillesheim, T. Robert and P. Q. Dung, "High Dynamic Current Control Using Decentralized PWM Generation for Parallel Multiphase Converter," 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 480-486.

[47] T. Xu, F. Gao, X. Wang and F. Blaabjerg, "A Carrier Synchronization Method for Global Synchronous Pulsewidth Modulation Application Using Phase-Locked Loop," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10720-10732, Nov. 2019.

[48] Z. Xueguang, Z. Wenjie, C. Jiaming and X. Dianguo, "Deadbeat Control Strategy of Circulating Currents in Parallel Connection System of Three-Phase PWM Converter," *IEEE Trans. Energy Conver.*, vol. 29, no. 2, pp. 406-417, June 2014.

[49] C. Jiang, Z. Quan, D. Zhou and Y. Li, "A Centralized CB-MPC to Suppress Low-Frequency ZSCC in Modular Parallel Converters," *IEEE Trans. Ind. Electron.*, early access, 2020.

[50] Colonel Wm. T. McLyman, Transformer and Inductor Design Handbook, 4th edition, CRC Press, 2011.

[51] M. L. Heldwein and J. W. Kolar,"Design of minimum volume EMC input filters for an ultra compact three-phase PWM rectifier," in Proc. 9th Brazilian Power Electron. Conf., 2007, pp. 454C461.

[52] K. B. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson and F. Canales, "Weight Minimization of LCL Filters for High-Power Converters: Impact

of PWM Method on Power Loss and Power Density," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2282-2296, May-June 2017.
[53] Y. Liu, K. Y. See, K. J. Tseng, R. Simanjorang and J. Lai, "Magnetic Integration of Three-Phase LCL Filter With Delta-Yoke Composite Core," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3835-3843, May 2017.
[54] D. Pan, X. Ruan, C. Bao, W. Li and X. Wang, "Magnetic Integration of the LCL Filter in Grid-Connected Inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1573-1578, April 2014.
[55] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Piscataway, NJ: IEEE Press, 2003

Zhongyi Quan (S12-M'19) received the B.Eng. degree from Tianjin University, Tianjin, China in 2010, M.Sc. degree from Beihang University, Beijing, China, in 2013, and Ph.D. degree in electrical engineering in 2019 from University of Alberta, Canada, where he is currently a Postdoctoral Fellow. From Oct. 2019 to Nov. 2019, He was a visiting research fellow at the Institute for Power Generation and Storage Systems (PGS), E.ON Energy Research Center, RWTH Aachen University, Germany.

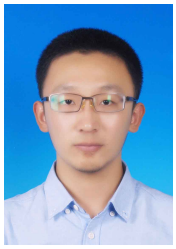
He is the recipient of IEEE PELS ECCE Best Student Project Demonstration on Emerging Technology 3rd Prize Award in 2018 and the Albeta GreenSTEM Fellowship.

His current research interests include design of high density and high efficiency power converters for applications such as renewable energy, electric vehicles, and other energy efficient equipment.

Yun Wei Li (S'04-M'05-SM'11-F'20) received the B.Sc. in Engineering degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2006.

In 2005, Dr. Li was a Visiting Scholar with Aalborg University, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow at Ryerson University, Canada. In 2007, he also worked at Rockwell Automation Canada before he joined University of Alberta, Canada in the same year. Since then, Dr. Li has been with University of Alberta, where he is a Professor now. His research interests include distributed generation, microgrid, renewable energy, high power converters and electric motor drives.

Dr. Li serves as Editor-in-Chief for IEEE Transactions on Power Electronics Letters. Prior to that, he was Associate Editor for IEEE Transactions on Power Electronics, IEEE Transactions on Industrial Electronics, IEEE Transactions on Smart Grid, and IEEE Journal of Emerging and Selected Topics in Power Electronics. Dr. Li received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from IEEE Power Electronics Society in 2013 and the second prize paper award of IEEE Transactions on Power Electronics in 2014. He is listed as a Highly Cited Researcher by the Web of Science Group.



Yiwei Pan (S'19) received the B.S. degree in automation and M.S. degree in power electronics from Shandong University, Jinan, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree at Aalborg University, Aalborg, Denmark.

He was an exchange student with Tianjin University, China, from 2016 to 2018. His current research interests include multilevel converters and distributed power generation.

Changpeng Jiang (S'18) received the BSc degree in electrical and computer engineering from the University of Alberta, Edmonton, Canada, in 2017. He is currently working towards M.Sc. degree in electrical engineering from the University of Alberta, Edmonton, Canada. He completed an eight-month internship in 2019 by working as a wind electrical engineer at TransAlta Corp. Canada.

His current research interests include design and control of the power converters for renewable energy applications. He was the recipient of the Alberta Innovates Graduate Student Scholarship in 2018.

Yongheng Yang (SM'17) received the B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, Shaanxi, China, in 2009 and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2014.

He was a postgraduate student with Southeast University, China, from 2009 to 2011. In 2013, he spent three months as a Visiting Scholar at Texas A&M University, USA. Currently, he is an Associate Professor with the Department of Energy Technology, Aalborg University, where he also serves as the Vice Program Leader for the research program on photovoltaic systems. His current research is on the integration of grid-friendly photovoltaic systems with an emphasis on the power electronics converter design, control, and reliability.

Dr. Yang is the Chair of the IEEE Denmark Section. He serves as an Associate Editor for several prestigious journals, including the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the IEEE Industry Applications Society (IAS) Publications. He is a Subject Editor of the IET Renewable Power Generation for Solar Photovoltaic Systems, including the Maximum Power Point Tracking. He was the recipient of the 2018 IET Renewable Power Generation Premium Award and was an Outstanding Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2018.

Frede Blaabjerg (S'86-M'88-SM'97-F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

He is nominated in 2014-2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.