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New Design of PI Regulator Circuit Based on Three-Terminal Memristors

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ABSTRACT Three-terminal memristors (MRs), extended from two-terminal ones, have been reported to have strong controllability and thus a wide application potential. In this paper, two three-terminal MR emulators are designed based on the junction gate field-effect transistor (JFET) and the operational amplifier (op amp), respectively, aiming to control the memductance quantitatively by adjusting the voltage applied on the third terminal. To obtain adjustable control parameters, a proportional-integral (PI) controller was designed based on the op amp-based three-terminal MR emulator. Then, the proposed emulators and controller were simulated repeatedly. The simulated results agree well with the theoretical analysis, revealing the good performance and feasibility of our design. The research findings shed new light on improving the controllability of controllers.

INDEX TERMS Memristors (MRs), proportional-integral (PI) controllers, junction gate field-effect transistor (JFET), current feedback operational amplifier (CFOA), pinched hysteresis loop (PHL).

I. INTRODUCTION

In 1976, the memristive system was proposed by Leon Chua and Sung Mo Kang. It is defined as a passive nonlinear dynamic system with two terminals, which can record historical information in a variable resistance called the memductance [1]. Compared with other nonlinear dynamic systems, the memristive system has a unique pinched hysteresis loop (PHL) [2], which reflects the variation of memductance with the quantity of the electric charges. In essence, the memristive system is a resistive random-access memory (RRAM), an emerging research device (ERD) in the International Technology Roadmap for Semiconductors (ITRS) [3], that can switch between two resistance states under proper terminal voltages.

The memristive system was generalized from memristors (MRs), which boast high potentials to structure new functional devices for industrial applications. Technically, the MRs have been widely utilized for memory devices [4]–[12] and many other applications, such as signal oscillators [13]–[16], logic and arithmetic circuits [17], [18], programmable analog circuits [19], [20], as well as emulation of dynamic neuron behaviors [21], [22].

In the past five decades, many three-terminal non-passive dynamic devices have emerged, showing similar memory effects to the memristive system [22]. For example, the gated three-terminal MRs were developed based on Bi_2O_2Se [23] and metal oxides [24]. These gated MRs can be programmed or erased by imposing a suitable gate voltage on the third terminal.

Recently, the dynamic behaviors and control performance of three-terminal MRs have attracted growing attention in the design of neural networks (NNs). For instance, reference [25] creates a synapse chip of the NN integrating the complementary metal–oxide–semiconductor (CMOS) circuits and the three-terminal ferroelectric MRs. Reference [26] selects the three-terminal ferroelectric MRs as the electric synapse device to store the analog synaptic weight, and develops a supervised learning model that enables error backpropagation for spiking neural network (SNN) to suit the hardware implementation. Reference [27] modulates the conductance of a bioinspired learning device by the gate voltage, without considering the signal flow through the channel, and thus achieves pattern recognition and learning at the same time.

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However, the existing studies on the circuits based on three-terminal MRs are mainly theoretical analysis and simulation, due to the limited application of three-terminal MRs [22].

The MRs have often been adopted to construct proportional-integral (PI) controllers. These controllers are very popular in industrial applications, thanks to the good performance of the PI compensation. Focusing on permanent magnet synchronous motor (PMSM) drives, reference [28] determines the parameters of the PI controller considering the phase margin, gain margin and bandwidth. Reference [29] discusses how the parameters of dual-loop PI controller affect the operation of three-phase voltage source pulse-width modulation (PWM) rectifier. Reference [30] designs a PI controller based on a slide-mode observer that can estimate the rotor speed and load torque, and uses it to stabilize the direct current (DC) motor system with complete or partial sensor failure.

To achieve flexible and optimal control, the PI controllers with adjustable parameters are mainly implemented using digital processors. But this implementation mode requires a huge controller size and a high hardware cost. By contrast, analog PI controllers can be structured based on operational amplifier (op amp) and basic circuit elements (e.g. resistor and capacitor). The problem is that both resistance and capacitance are maintained constantly, making it impossible to tune the controller parameters online.

In reference [31], an adaptive PI controller is designed based on the MR, and applied to boost DC/DC converter; Using the variable memristance, the MR circuit automatically refreshes the controller parameters by gradient descent method, and thereby minimizing the output error of the closed-loop system. In reference [32], the resistor in the proportional-integral-derivative (PID) controller circuit is replaced with an MR, followed by the discussion on the dynamic performance of the MR-based PID controller. In reference [33], an adaptive optimization method is presented for the PID NN controller: a nanoscale MR is employed to analog electronic synapse, laying the basis for hardware realization and weight update.

To sum up, the above PI/PID controllers were all constructed with two-terminal MRs. The memristance of the two-terminal MRs can only be altered by the input flux or charge, adding to the difficulty in adjusting controller parameters. To enhance the controllability of PI/PID controllers, it is necessary to introduce the write and read circuit to tune the memristance of the two-terminal MRs.

Considering the advantages of three-terminal MR over two-terminal MR in controllability, this paper proposes two three-terminal MR emulators using off-the-shelf components, and demonstrates the performance of one of the emulators. Then, a PI controller circuit with adjustable parameters was constructed based on the proposed emulator.

II. EMULATOR DESIGN

The main differences between the two-terminal MR and other nonlinear dynamic systems include the frequency-dependent PHL and the zero-crossing property (i.e. the system output is always zero if the input is zero). The mathematical expression for a flux-controlled two-terminal MR is as follows:

$$\begin{aligned} \frac{dw}{dt} &= f(w, \varphi, v, t) \\ y &= g(w, \varphi, t)v \end{aligned} \tag{1}$$

where t is time; v and y are the input and output of the MR, respectively; φ is the flux, a.k.a. the time integral of voltage v; w is a multi-dimensional vector representing the system state; f is a continuous n-dimensional vector function; g is a continuous scalar function. Meanwhile, a flux-controlled three-terminal MR can be described as:

$$\begin{aligned} \frac{dw}{dt} &= f(w, \varphi_d, \varphi_q, v_d, v_q, t) \\ i_g &= g(w, \varphi_d, \varphi_q, t)v_g \\ i_d &= g(w, \varphi_d, \varphi_q, t)v_d \end{aligned} \tag{2}$$

where v_{d} and v_{g} are the inputs; $\varphi_{\mathrm{d}}$and φ_{g} are the fluxes, a.k.a. the time integral of v_{d} and v_{g}, respectively.

In this section, two three-terminal MR emulators are designed based on the junction gate field-effect transistor (JFET) and the op amp. The equivalent memductance of the three-terminal MR was theorized by the input-output function of current feedback op amps (CFOA) AD844 and AD633. In the input stage, the CFOAs replace the differential circuit of the voltage feedback op amps (VFOAs) with complementary follower circuit. In this way, the conversion rate is improved in the input stage. Moreover, the closed-loop bandwidth of the CFOAs is independent of gain, eliminating the constraint on gain-bandwidth product. Thus, the CFOAs enjoy advantages over VFOAs in operation bandwidth.

A. JFET-BASED THREE-TERMINAL MR EMULATOR

As shown in Figure 1, the JFET-based three-terminal MR emulator consists of three op amps, one multiplier, four CFOAs and one JFET. In the upper dotted frame, the circuit can operate as a two-terminal MR if the control terminal of the JFET is connected to a constant voltage [34]. In the blue frame, the circuit runs to achieve the integral operation. In the third dotted frame, the circuit runs to add the third terminal to the two-terminal MR emulator.

According to the operational function of CFOA (AD844), the voltage of terminal x equals the voltage of terminal y [35]. Thus, the following equations hold:

$$v_{\mathrm{u1}} = \frac{R_2}{R_1} v_{\mathrm{AB}} \tag{3}$$

$$v_{\mathrm{u3}} = -\frac{\varphi_{\mathrm{AB}}}{C_1 R_1} \tag{4}$$

where φ_{AB} is the time integral of v_{AB}; v_{u1} and v_{u3} are the output voltages of CFOAs U1 and U3, respectively. Then, the op amp U5 was introduced to realize the inverting adder circuit (IAC).

In the light of AD844's configuration, the voltage of terminal z equals the output voltage of terminal p. Hence, the

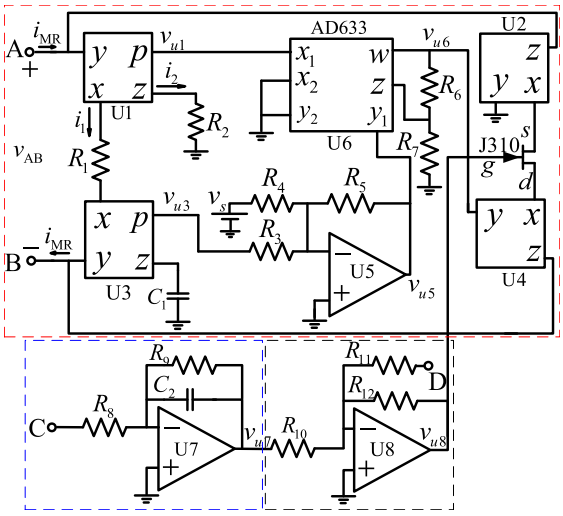

FIGURE 1. Circuit schematic of the JFET based 3T-MR emulator.

output voltage of U5 can be described as:

$$v_{u5} = \frac{R_5}{R_1 R_3 C_1}\varphi_{AB} - \frac{R_5}{R_4}v_s \tag{5}$$

To ensure the performance of the MR emulator, the v_s must have a proper negative value. Referring to the datasheet of AD633JN, v_{u6} can be derived by:

$$v_{u6} = \frac{R_6 + R_7}{10R_6}v_{u1}v_{u5} \tag{6}$$

Based on the actions of U2 and U4, the current i_{MR} passing through terminals A and B can be decided by v_{u6}:

$$i_{MR} = v_{u6}G_J \tag{7}$$

where G_J is the voltage-controlled conductance of the JFET. To obtain the value of G_J, the control voltage v_{gs} of the JFET can be obtained from the output voltage of op amp U7,

$$\frac{v_C}{R_8} = -\frac{v_{u7}}{R_9} - C_2\frac{dv_{u7}}{dt} \tag{8}$$

where v_c is the voltage applied to terminal C. Since the initial value of v_{u7} is zero, v_{u7} can be deduced by:

$$v_{u7} = -\frac{R_9 v_C(1 - ex(t))}{R_8} \tag{9}$$

where

$$ex(t) = e^{-\frac{t}{C_2 R_9}}$$

The output voltage of the op amp U8 can be calculated by:

$$\frac{v_{u7}}{R_{10}} = -\frac{v_D}{R_{11}} - \frac{v_{u8}}{R_{12}} \tag{10}$$

where v_D is the voltage applied to terminal D. Hence, v_{u8} can be obtained by:

$$v_{u8} = \frac{R_{12}R_9 v_C(1 - ex(t))}{R_8 R_{10}} - \frac{R_{12}v_D}{R_{11}} \tag{11}$$

Because terminal y of U2 is grounded, the source voltage of JFET equals zero. Therefore, v_{gs} can be determined by:

$$v_{gs} = v_g = v_{u8} = \frac{R_{12}R_9 v_C(1 - ex(t))}{R_8 R_{10}} - \frac{R_{12}v_D}{R_{11}} \tag{12}$$

According to the conductance features of JFET, the conductance G_J is zero when v_{gs} reaches the cutoff gate-source voltage of -2.7V. The conductance can be increased by amplifying v_{gs} at a constant rate of 10mS/V. Hence, G_J can be described as:

$$G_J = 10v_{gs} = 10R_{12}\left[\frac{R_9 v_C(1 - ex(t))}{R_8 R_{10}} - \frac{v_D}{R_{11}}\right] \tag{13}$$

Combining (7) and (13), we have

$$i_{MR} = \zeta v_{AB}(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)\left[\frac{R_9 v_C(1 - ex(t))}{R_8 R_{10}} - \frac{v_D}{R_{11}}\right] \tag{14}$$

where

$$\zeta = \frac{R_{12}R_2(R_6 + R_7)}{R_1 R_6}, \quad \sigma = \frac{R_5}{R_1 R_3 C_1}.$$

The memductance W can be derived as:

$$W(\varphi_{AB}, v_C) = \zeta(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)\left[\frac{R_9 v_C(1 - ex(t))}{R_8 R_{10}} - \frac{v_D}{R_{11}}\right] \tag{15}$$

Obviously, the equivalent memductance $W(\varphi_{AB}, v_C)$ is controlled by flux and voltage.

In order to analyze the memductance between the terminals A and B in terms of the voltage imposed on terminal C, four voltages are selected here for demonstration. When sinusoidal voltage of $v_C = \sin t$ is imposed on terminal C, the memductance W can be expressed as:

$$W(\varphi_{AB}, \sin t) = \zeta(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)\left[\frac{R_9 \sin t(1 - ex(t))}{R_8 R_{10}} - \frac{v_D}{R_{11}}\right] \tag{16}$$

Formula (16) shows that, with the elapse of t, the value of $ex(t)$ will decrease to zero, that is, 1-$ex(t)$ will increase to one. This means the memducance $W(\varphi_{AB}, v_C)$ can be easily adjusted by changing the control voltage v_C.

At the v_C of zero, the memductance W can be computed by:

$$W(\varphi_{AB}, 0) = -\frac{\zeta v_D}{R_{11}}(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s) \tag{17}$$

Thus, when v_C is zero, the memductance is only controlled by φ_{AB} and the emulator can operate as a two-terminal MR. Under the special condition of

$$v_C = (\frac{v_D}{R_{11}} + Q)\frac{R_8 R_{10}}{R_9(1 - e^{-\frac{t}{C_2 R_9}})} \tag{18}$$

where Q is a random constant, The memductance can be computed by :

$$W(\varphi_{AB}) = \zeta(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)Q \tag{19}$$

In this case, the three-terminal MR emulator also runs as a two-terminal MR emulator, and the memductance W is only controlled by the input voltage φ_{AB}.

Assuming that v_C is excited by a square voltage with cycle T, the memductance $W(\varphi_{AB}, v_C)$ increases with φ_{AB} during $k\mathrm{T} \le t < k\mathrm{T}+t_h$, when $v_C = \mathrm{V_{OH}}$. Here, t_h is the duration of high voltage level during one cycle of v_C. Then, the following can be derived from formula (13):

$$W(\varphi_{AB}, v_C) = \zeta(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)\left[\frac{R_9\mathrm{V_{OH}}(1-ex(t))}{R_8R_{10}} - \frac{v_D}{R_{11}}\right] \tag{20}$$

Formula (20) reveals the positive correlation between $W(\varphi_{AB}, v_C)$ and φ_{AB}.

When $v_C = -\mathrm{V_{OH}}$, the memductance $W(\varphi_{AB}, v_C)$ varies with φ_{AB} during $t_h \le t \le (k+1)\mathrm{T}$. Thus, we have:

$$W(\varphi_{AB}, v_C) = \zeta(\sigma\varphi_{AB} - \frac{R_5}{R_4}v_s)\left[\frac{-R_9\mathrm{V_{OH}}(1-ex(t))}{R_8R_{10}} - \frac{v_D}{R_{11}}\right] \tag{21}$$

With the elapse of time, 1-$ex(t)$ will eventually reach one. Hence, when v_D equals -15V and $\mathrm{V_{OH}} > 0$, the value of $-R_9\mathrm{V_{OH}}/(R_8R_{10}) - v_D/R_{11}$ must be negative.

Furthermore, if an input voltage v_{AB} is added to terminals A and B within the finite period $[0, t_s]$, we have:

$$\varphi_{AB} = \int_{-\infty}^{\infty} v_{AB}dt = \int_0^{t_s} v_{AB}dt = \Phi_{AB} \tag{22}$$

Since v_{AB} is a known voltage signal and t_s is constant, φ_{AB} must be a constant equal to Φ_{AB}. In this case, the three-terminal MR is only controlled by terminal C exceeds the time t_s. Note that, when $v_C = 0$ and $v_D = 0$, the gated-source voltage $v_{gs} = 0$ and $G_J = 26$mS can be obtained from the characteristic curve of JFET.

B. DESIGN OF THE OP AMP-BASED THREE-TERMINAL MR EMULATOR

The design of the op amp-based three-terminal MR emulator is shown in Figure 2. Different from the JFET-based three-terminal MR emulator [36], the JFET was replaced with a common resistor R_{13}, and the control action of terminal C was realized with an adder circuit structured by U8. The output voltage of U6 (AD633) was connected to the negative pin of the op amp U8, whose output terminal was in turn connected to pin y of CFOA U4 (AD844). The mathematical expression of the op amp-based three-terminal MR emulator is similar to that of the JFET-based one. The main difference lies in the derivation of v_{u8}:

$$v_{u8} = \frac{R_{12}R_9v_C(1-ex(t))}{R_8R_{10}} - \frac{R_{12}v_{u6}}{R_{11}} \tag{23}$$

Based on the actions of U2 and U4, the current i_{MR} passing through terminals A and B can be decided by v_{u8}:

$$i_{MR} = \frac{v_{u8}}{R_{13}} = \kappa v_C(1-ex(t)) - \lambda v_{AB}(\frac{R_5}{R_1R_3C_1}\varphi_{AB} - \frac{R_5}{R_4}v_s) \tag{24}$$

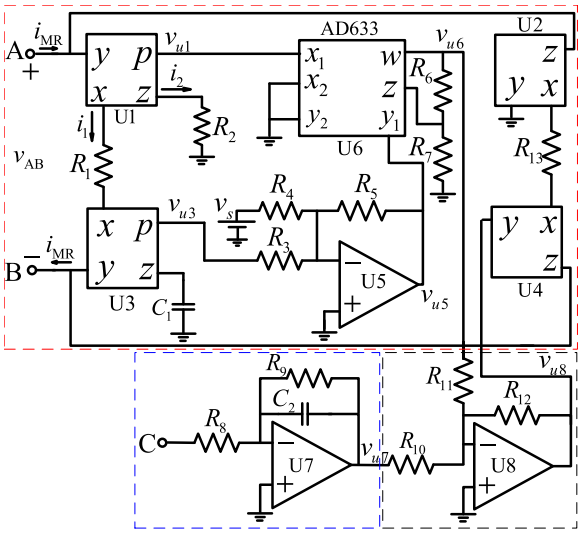

FIGURE 2. Design of the op amp-based three-terminal MR emulator.

where

$$\kappa = \frac{R_9R_{12}}{R_8R_{10}R_{13}}, \quad \lambda = \frac{(R_6+R_7)R_2R_{12}}{10R_1R_6R_{11}R_{13}}.$$

Then, the voltage-controlled memductance W can be derived by:

$$W(\varphi_{AB}, v_C) = \frac{\kappa v_C(1-ex(t))}{v_{AB}} - \lambda(\frac{R_5}{R_1R_3C_1}\varphi_{AB} - \frac{R_5}{R_4}v_s) \tag{25}$$

It is evident that the three-terminal MR emulator in Figure 1 requires an extra voltage signal source to regulate the control voltage for the JFET via terminal D. The JFET conductance hinges on two factors, namely, the voltage across the terminals of Source (S) and Drain (D), and the voltage on terminal Gate (G), and thus becomes highly nonlinear. The strong nonlinearity drags down the control accuracy of the JFET-based three-terminal MR emulator, as compared with that of the op amp-based one. As shown in Figure 2, thirteen resistors were deployed instead of the extra voltage signal source.

In the JFET-based three-terminal MR emulator, the memductance is regulated by the control voltage v_C via multiplication operation in formula (15). In the op amp-based three-terminal MR emulator, the memductance regulation is achieved by the control voltage v_C via summation operation. Therefore, the op amp-based three-terminal MR emulator is dwarfed by the JFET-based three-terminal MR emulator in terms of control sensitivity.

III. PI CONTROLLER DESIGN

Based on the controllability of three-terminal MRs, many functional circuits can be designed by controllable memductance. For simplicity, a new PI controller circuit (Figure 3) was built on the op amp-based three-terminal MR emulator.

The equality of $i_R = i_C$ can be achieved according to the circuit performance of op amp U9. Hence, i_R and i_C can be

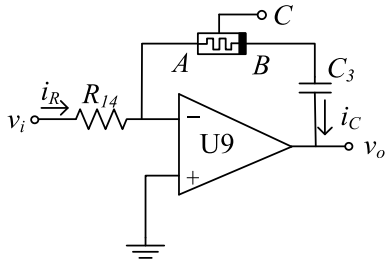

FIGURE 3. The sketch map of the designed PI controller circuit.

respectively derived by:

$$i_R = \frac{v_\mathrm{i}}{R_{14}}, i_C = \frac{0 - v_\mathrm{o}}{\frac{1}{W} + \frac{1}{sC_3}} \tag{26}$$

On this basis, the output voltage v_o, the proportional coefficient K_P and the integral coefficient K_I can be calculated by:

$$v_\mathrm{o} = K_\mathrm{P} v_\mathrm{i} + K_\mathrm{I} \int v_\mathrm{i} dt \tag{27}$$

where

$$K_\mathrm{P} = -\frac{1}{R_{14}W}, \quad K_\mathrm{I} = -\frac{1}{R_{14}C_3}$$

For the designed PI controller circuit, the input signal v_i is usually sampled from the feedback error signals of the system to be controlled and collected by sensors in time. Thus, we have:

$$v_\mathrm{AB} = \frac{v_i}{R_{14}W} \tag{28}$$

Substituting formula (25) into formula (27), the output control signal v_o can be further expressed as:

$$v_\mathrm{o} = \frac{-v_i}{R_{14}} \left[\frac{\kappa v_\mathrm{C}(1 - ex(t))}{v_\mathrm{AB}} - \lambda \left(\frac{R_5}{R_1 R_3 C_1} \varphi_\mathrm{AB} - \frac{R_5}{R_4} v_\mathrm{s} \right) \right]^{-1} - \frac{1}{R_{14}C_3} \int v_i dt \tag{29}$$

Since v_i is dependent on the system state, formula (29) reveals that the output signal v_o can be adjusted by the voltage on terminal C.

IV. SIMULATION VERIFICATION

In this section, an op amp-based three-terminal MR emulator is built to test the feasibility and performance of the designed PI controller circuit.

A. TESTING OF OP AMP-BASED THREE-TERMINAL MR EMULATOR

The op amp-based three-terminal MR emulator was tested to see if it carries the typical fingerprints of the MR. The simulation parameters were configured as follows: $R_1 = 51\mathrm{k}\Omega$, $R_2 = R_3 = R_4 = 100\mathrm{k}\Omega$, $R_5 = 10\mathrm{k}\Omega$, $R_6 = 100\mathrm{k}\Omega$, $R_7 = 91\mathrm{k}\Omega$, $R_8 = 100\mathrm{k}\Omega$, $R_9 = 1\mathrm{M}\Omega$, $R_{10} = 15\mathrm{k}\Omega$, $R_{11} = 1\mathrm{k}\Omega$, $R_{12} = 1\mathrm{k}\Omega$, $R_{13} = 1\mathrm{k}\Omega$, $C_1 = 100\mathrm{nF}$ and

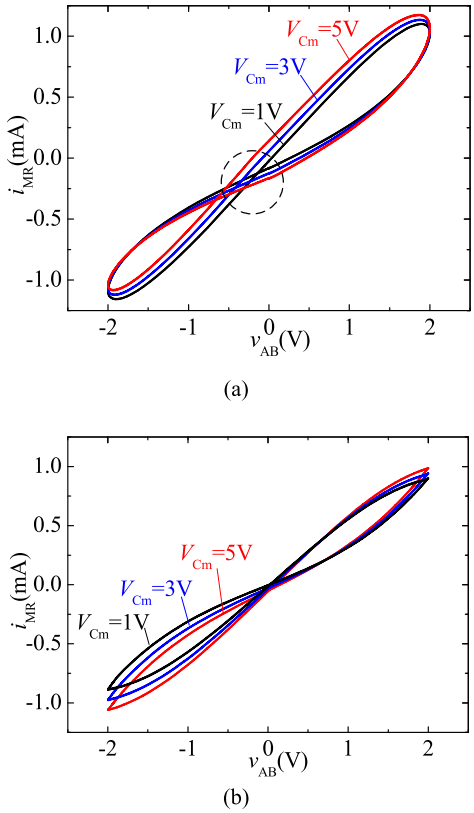

FIGURE 4. The simulated PHLs (a) sinusoidal voltage on A and B (b) isosceles triangular voltage on A and B.

$C_2 = 470\mathrm{nF}$. Terminals A and B were excited by a sinusoidal voltage of $2\sin(20\pi t)$, a isosceles triangular voltage (frequency: 10Hz; amplitude 2V), and a square voltage (frequency: 10Hz; amplitude: $-2 \sim 2\mathrm{V}$; duty cycle: 25%), respectively, while the third terminal C was excited by square voltages (frequency: 10Hz; duty cycle: 50%) at different amplitudes (1V, 3V and 5V). The isosceles triangular voltage was applied on A and B to verify the memductance features of the emulator, and the square voltage was applied on the two terminals to test the ability to control the memductance via terminal C.

Three Lissajous curves of i_MR vs. v_AB are displayed in Figure 4(a), which shows that the PHLs, shaping as inclined eights, all passed through the origin, and shrunk with the decrease of control amplitude. The maximum values of i_MR were 1.1, 1.13 and 1.17mA, respectively, under amplitudes of 5V, 3V and 1V, and could be further increased with the growth of the control amplitude. In the dotted circle, the phase deviation between voltage and current of the three-terminal MR emulator could be observed. The deviation is the result of the common practice to connect a resistor (R_9) in parallel with a capacitor (C_2), which aims to minimize the DC offsets, especially when the capacitor is used as an integral circuit. Of course, the deviation is rather small and reduced with the increment of frequency.

Similarly, when v_AB was an isosceles triangular voltage, the three PHLs of i_MR vs. v_AB (Figure 4(b)) all existed in the

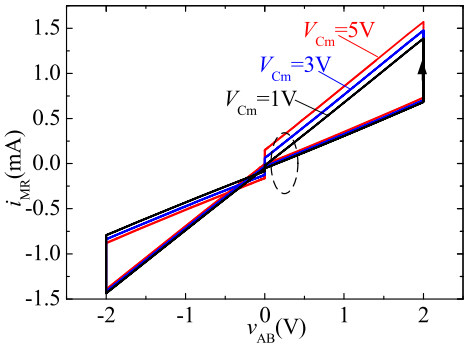

FIGURE 5. PHLs of the adder circuit based 3T-MR emulator excited by a square wave.

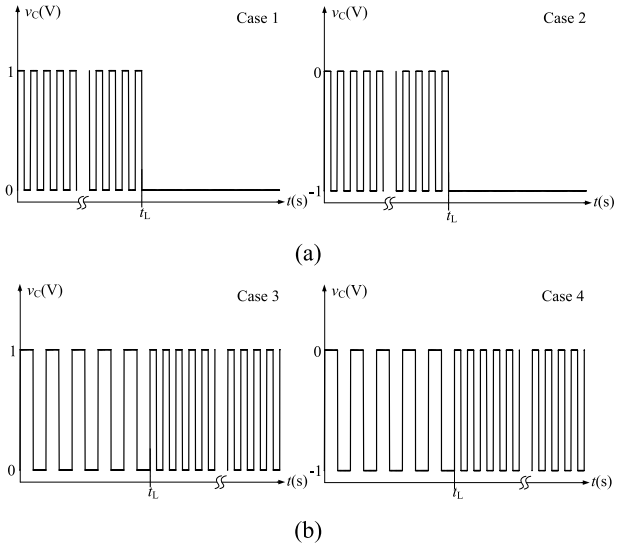

FIGURE 6. The control voltages applied to terminal C.

form of irregular eights. The maximum values of i_{MR} were 0.986, 0.940 and 0.899mA, respectively, under amplitudes of 5V, 3V and 1V, and could be further reduced by decreasing the control amplitude v_C.

As shown in Figure 5, when the v_{AB} was 2V, the memductance W increased according to the constitutive relation in formula (25); when $v_{AB} = -2$V, the memductance continued to decrease; when $v_{AB} \neq \pm 2$V and $v_{AB} = 0$, the current-voltage relationship of the three-terminal MR emulator was basically linear, like that of the two-terminal MR emulator, and the memductance remained constant. The final memductance recorded by the three-terminal MR emulator determined the amplitude of the abrupt changes of the current i_{MR}. The maximum values of i_{MR} were 1.57, 1.47 and 1.39A, respectively, under amplitudes of 5V, 3V and 1V, and could be further reduced with the decrease of the control amplitude v_C. According to formula (24), the broken line of PHLs in the dotted ellipse is resulted from the phase deviation between the output voltage v_{u8} of amplifier U8 and input voltage v_{AB}.

It can be easily derived that the operation bandwidth of the op amp-based three-terminal MR is below 20kHz, in terms of v_{AB} at the amplitude of 2V. The maximum frequency of v_{AB} could reach 20kHz by properly tuning the emulator parameters, especially the integral capacitance. Under such a high frequency, the emulator may act as a normal resistor with a fully shrunk hysteresis loop, which is a typical feature of the MR. Thus, the op amps and the CFOAs with high bandwidth must be employed to satisfy the operation requirements of the excitation frequency.

B. TESTING OF THE 3T-MR EMULATOR BASED PI REGULATOR

The proportional and integral coefficients directly bear on the performance of the PI controller. Generally, the greater the proportional coefficient K_p, the faster the response and the shorter the transient process. However, the increment of K_p may also increase the overshot and narrow the stability margin of the controlled system. This calls for proper tuning of the coefficient value depending on the specific conditions. If the output deviates greatly from the reference, the coefficient should be increased to speed up the response and shorten the transient process; if the output is close to the reference, the coefficient should be decreased to minimize the overshot and maintain system stability.

Due to the high nonlinearity of the JFET, the JFET-based three-terminal MR emulator is more complex than the op amp-based one. For simplicity, the latter was selected to design the PI controller for performance verification. Four different voltages were applied on the terminal C in turn to fully disclose the dynamic behavior of the designed PI controller.

As shown in Figure 6, the terminal C was sequentially applied with a square voltage (frequency: 20Hz; duty cycle: 50%) whose voltage suddenly decreased to zero when $t > t_L$ (case 1), a square voltage (frequency: 20Hz; duty cycle: 50%) whose voltage suddenly decreased to -1V when $t > t_L$ (case 2), a square voltage (frequency: 20Hz; amplitude: 1V) whose duty cycle decreased from 50% to 20% when $t > t_L$ (case 3), and a square voltage (frequency: 20Hz; amplitude: -1V) whose duty cycle decreased from 50% to 20% when $t > t_L$ (case 4). In all four cases, the input voltage v_i of the PI controller was set as a sinusoidal voltage $10\sin(40\pi t)$V. The parameters of the PI controller were configured as: $R_4 = 74.9$kΩ, $R_{14} = 100$kΩ and $C_3 = 1$uF.

The simulation results of case 1 (Figure 7) reflect that the peak-to-peak value of the output voltage with no control voltage ($v_C = 0$) was 1.85V greater than that with the control voltage. When the v_C suddenly decreased at $t = 1$s, the amplitude of v_o increased abruptly and quickly reached the steady state.

The memductance characteristics represented by the PHLs are shown in Figure 8, of which we can see that when the control voltage v_C is applied, the amplitude of v_{AB} can be increased. The PHLs corresponding to the change of v_{AB} is shown in Figure 8(a), of which the black PHL is corresponding to the testing condition of $v_C = 0$. The arrow shows the decreasing direction of the amplitude of v_{AB}. This simulation

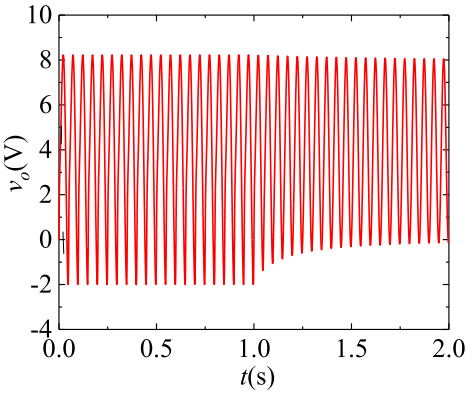

FIGURE 7. The output voltage of PI regulator controlled by v_C of case 1.

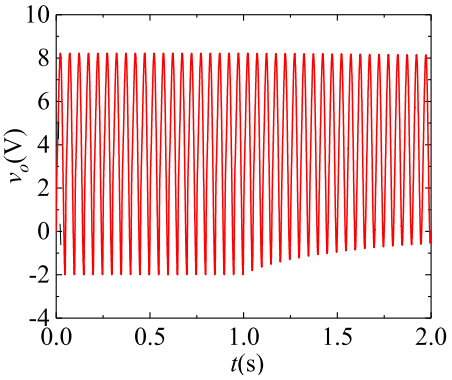

FIGURE 9. The output voltage of PI regulator controlled by v_C in case 3.

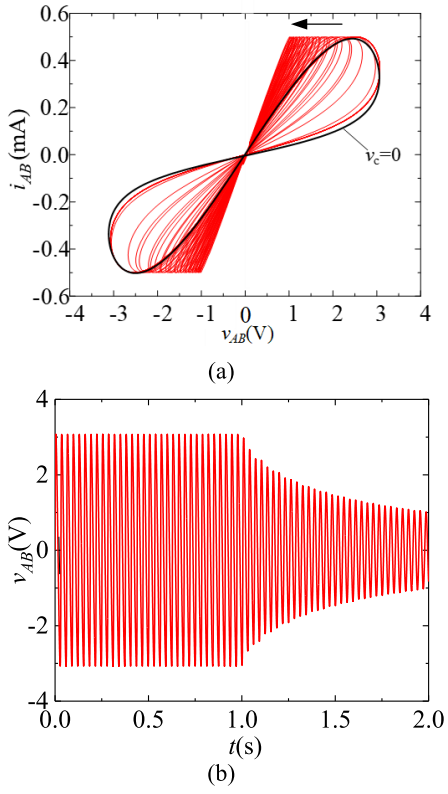

FIGURE 8. Simulation results. (a) The PHLs of controlling case 1. (b) The terminal voltage v_{AB} of the 3T-MR.

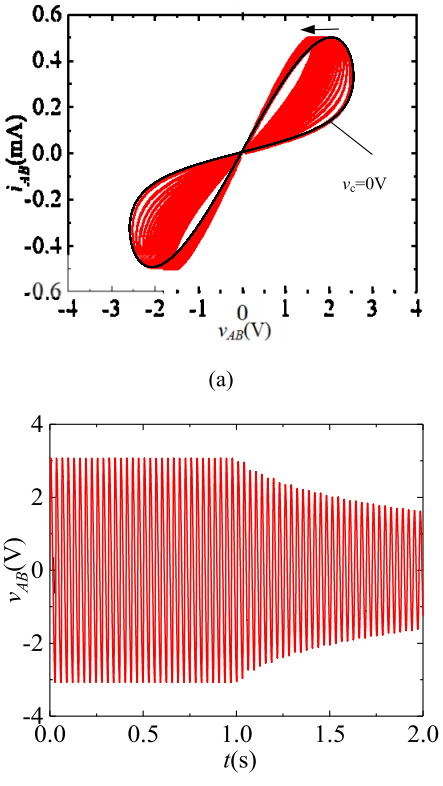

FIGURE 10. Simulation results. (a) The i_{MR} versus v_{AB} PHLs in case 3. (b) The terminal voltage v_{AB} of the 3T-MR.

result shows that the output voltage of PI regulator can be efficiently controlled by the voltage added to the control electrode C.

The simulation results of case 3 (Figure 9) indicate that the peak-to-peak value of the output voltage at the duty cycle of 50% was 1.16V greater than that at the duty cycle of 20%. When the v_C suddenly decreased at $t = 1$s, the peak-to-peak value of the output voltage immediately increased before reaching the steady state after about 0.75s. This means the output voltage can be regulated by adjusting the duty cycle of the voltage on terminal C. The PHLs in Figure 10 represent the memductance features of the controller, among which the black PHL was recorded at $v_C = 0$. The arrow shows the decreasing direction of the amplitude of v_{AB}. It can be seen that the amplitude of v_{AB}decreased all the way to 3.2V with the duty cycle of the control voltage v_C. The result verifies that the proportional coefficient of the PI controller can be regulated by adjusting the duty cycle of the control voltage v_C.

In case 2, the amplitude of output voltage v_o decreased after $t > 1$s, which is different from the results in case 1 and 3, but

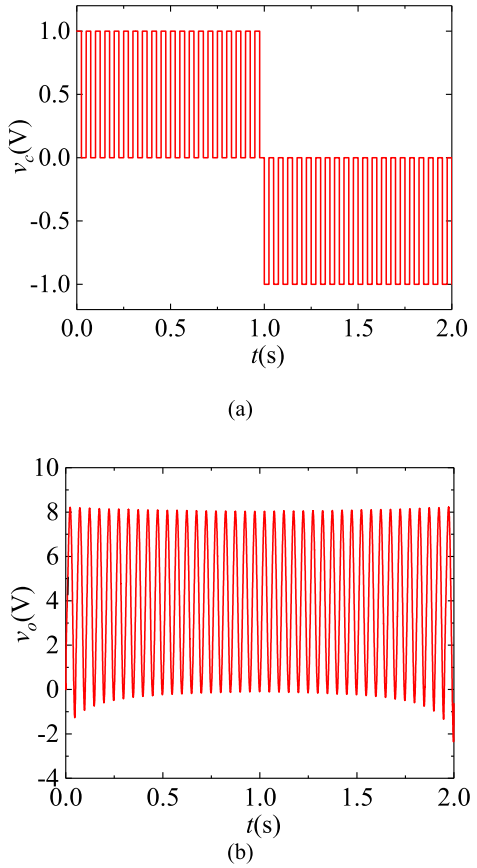

FIGURE 11. The wave of v_C and v_o. (a) The square voltage of v_C. (b)The output voltage v_o of the PI regulator.

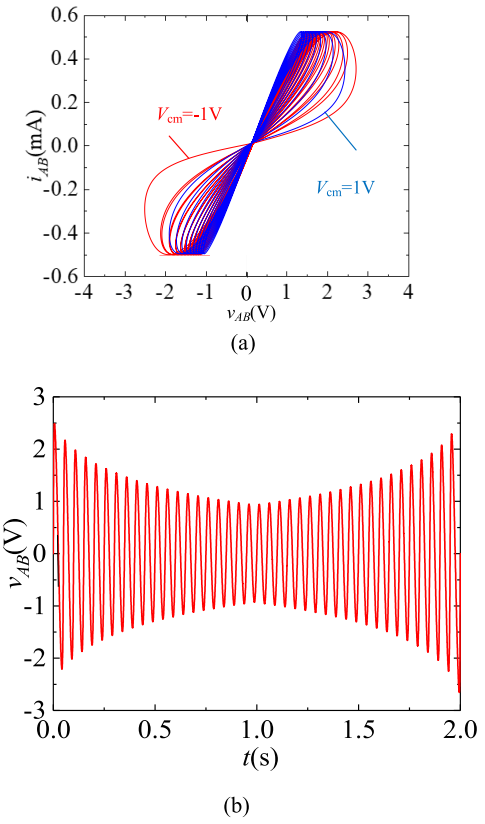

FIGURE 12. Simulation results. (a) The memductance characteristics of PHLs. (b) The input voltage v_{AB} of the 3T-MR emulator.

the memductance features were similar to those of case 1. In case 4, the amplitude of the output voltage v_o firstly decreased and then increased, which is different from the results of case 3.

To further verify the controllability of the PI regulator, terminal C was applied with a square voltage (frequency: 20Hz; duty cycle: 50%), whose amplitude suddenly dropped from 1V to -1V at t $=$ 1s. As shown in Figure 11(a). In Figure 11(b), it can be observed that the amplitude of the output voltage is first decreased and then increased. It can be concluded that the amplitude of output voltage of v_o can be efficiently controlled by adjusting the square voltage on terminal C.

As shown in Figure 12(a), the PHLs continuously expanded with the growing amplitude of voltage v_{AB} before t $=$ 1s, and shrunk significantly after the amplitude of the control voltage plugged to -1V at t $=$ 1s. These trends prove that it is possible to adjust the memductance and achieve the proportional coefficient of the PI controller by changing the amplitude of the control voltage on terminal C. Compared with a normal PI controller, the PI controller based on the three-terminal MR emulator can be controlled easily online, thanks to its adjustable parameters. The proportional coefficient K_P can be adjusted quantitatively by tuning the parameters of the control voltage on terminal C, such as amplitude and duty cycle.

Considering the constraints of R_{14} and C_3 on the integral coefficient K_I (formula (26)), the proportional coefficient K_P was quantitatively analyzed on MATLAB/Simulink, with the aim to disclose the control role of our three-terminal MR emulator in a PI controller circuit. Firstly, the input voltage v_i was set to $3\sin(10\pi t + \pi/3)$V, the control voltage was configured as 10Hz, 1V and 50%, and the proportional coefficient K_P was adjusted from 1 to 2. The simulated results are recorded in Figure 13(a), where the inner PHL corresponds to $K_P = 1$ and the outer PHL corresponds to $K_P = 2$. The results show that the proportional coefficient K_P can be controlled quantitatively by adjusting the control voltage on the PI controller designed on the three-terminal MR emulator.

Next, the input voltage v_i was changed to $v_i = 10\sin(10\pi t + \pi/3)$V, and the i_{MR} was changed at crossing point near zero by adding a high-amplitude sinusoidal voltage on the input terminals. The simulated results are displayed in Figure 13(b), where the two blue dotted ellipses in the second and fourth quadrants are caused by the zero crossing of i_{MR}. It can be learned that an excessively large input voltage on the PI controller circuit may lead to a

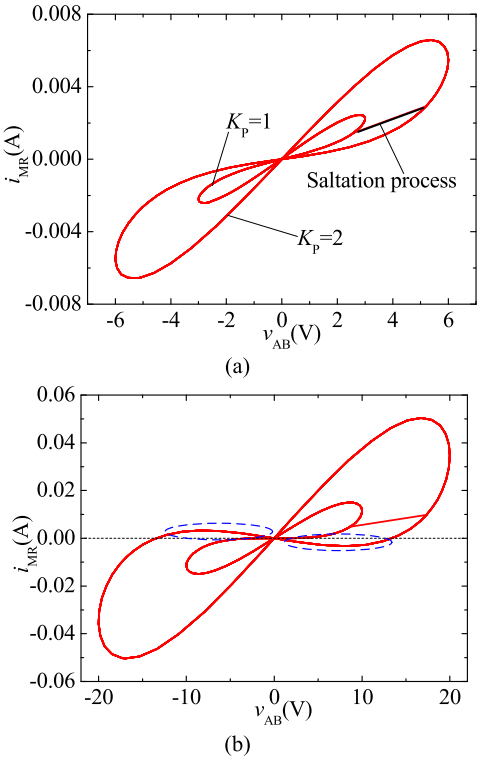

FIGURE 13. PHLs under the condition of forced K_P. (a) $v_i = 3\sin(10\pi t + \pi/3)$ V. (b) $v_i = 10\sin(10\pi t + \pi/3)$V.

negative resistance in the op amp-based three-terminal MR emulator.

V. CONCLUSION

This paper proposes two three-terminal MR emulators based on a JFET and an op amp, respectively, and theoretically analyzes them to disclose the memductance features by controlling the third terminal voltage. The two emulators were designed to simulate whether the three-terminal MR can adjust the memductance in a nonvolatile and continuous manner. Next, the op amp-based three-terminal MR emulator was selected to construct a novel PI controller circuit. The proportional coefficient and output voltage of the designed PI controller circuit were both simulated under different control voltages on terminal C. The simulated results agree well with the theoretical results, revealing that the designed PI controller boasts a strong controllability with its adjustable proportional coefficient and the output voltage. The future research will explore the potential applications of the proposed three-terminal MR emulators.

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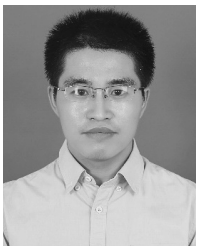

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