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# Unipolar Double-Star Submodule for Modular Multilevel Converter With DC Fault Blocking Capability

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**ABSTRACT** Adopting overhead lines is an effective way to reduce the cost of flexible high voltage direct current (HVDC) systems. However, the dc short-circuit fault is easily occurred and the development of the overhead lines based HVDC system is hampered. This paper proposes a unipolar double-star submodule (UDSSM) with the dc fault blocking capability. Under the dc fault condition, the UDSSM based modular multilevel converter (MMC) could block the fault current by switching all power switching devices off to protect the MMC system. In each proposed submodule, two capacitors work under almost the same condition and could be in series or parallel connection to output different voltage levels. Then two voltage sensors of the two capacitors are redundant each other, which improves the reliability of the MMC system. Additionally, voltage balancing methods for the capacitors under both normal operation and sensor fault conditions of the MMC submodule are developed in this paper. The effectiveness of the proposed submodule and the capacitor voltage balancing strategy are validated by the simulation and experiment results.

**INDEX TERMS** Capacitor voltage balancing, dc fault blocking, HVDC, MMC, submodule topology.

## I. INTRODUCTION

Modular multilevel converter (MMC) has been widely adopted in high voltage direct current (HVDC) transmission system due to its excellent features, such as high modularity, superior ac output performance, and low voltage stress on power switching devices [1], [2]. In high voltage applications, there might be hundreds of identical submodules connected in series in each arm of the MMC. Normally, the submodule with half-bridge circuit is applied, which has the characteristics of minimum components count and the lowest power losses [3]–[6]. However, the arm current of the half-bridge submodule (HBSM) based MMC is uncontrollable under the dc short-circuit fault condition. Then the arm current would have a great increment going through the dc short-circuit point and the anti-parallel diodes even though all the power switching devices are switched off, and the components of the MMC might be destroyed [7]. In particular, the technology of high-voltage dc circuit breaker is still immature and could not be available economically now. Therefore, the cable instead of overhead line is used in the present flexible HVDC system to reduce the possibility of dc short-circuit fault, which increases the cost of HVDC system greatly [8].

Aiming to develop the flexible HVDC system with overhead line, the MMC with dc fault handling capability has been studied by scholars from the industry and academia. The dc fault handling capability could be divided into two categories, namely fault blocking capability and fault ride-through capability. If all the power switching devices are switched off under dc fault condition, the capacitors in submodules could be connected into the circuit through the remained diodes to block the fault current, which means that the MMC is with dc fault blocking capability. Supposing the blocking time of the dc short-circuit fault is short, the discharging of the capacitor in submodules could be neglected and the capacitor voltage is almost stable. Then, the MMC

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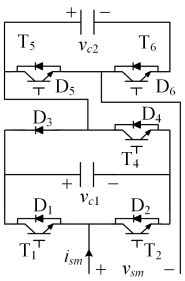
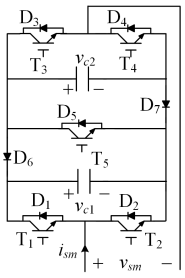
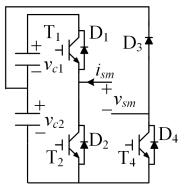
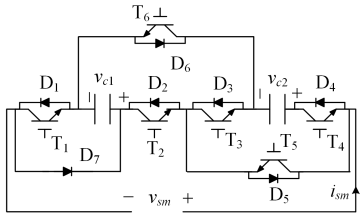
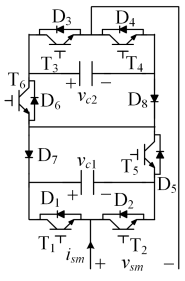
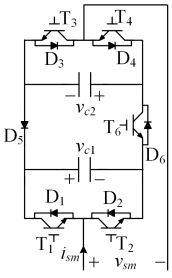
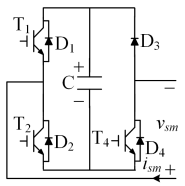
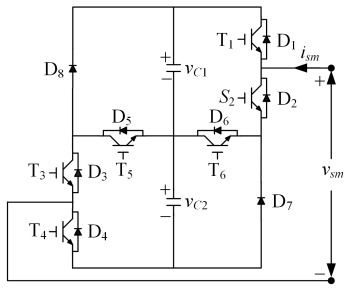
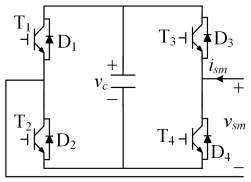
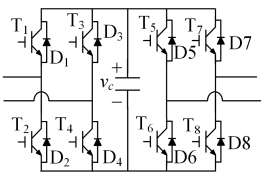
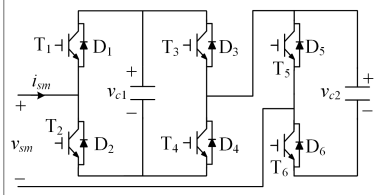
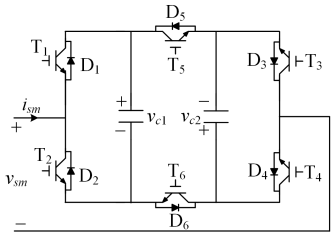
**TABLE 1.** Topology of existing submodule circuits.

| Circuits with DC Fault Blocking Capability | | | |
|---|---|---|---|
| HDSM | CDSM | DCSM | SCSM |
|  |  |  |  |
| CCSM | SCDSM | UFBSM | ACTSM |
|  |  |  |  |
| **Circuits with DC Fault Ride-Through Capability** | | | |
| FBSM | TFBSM | HSSM | CCDSM |
|  |  |  |  |

could restart without charging process for the submodule capacitors after the clearance of the dc fault, which increases the availability of the MMC. The submodule circuits in the MMC with dc fault blocking capability include hybrid-double submodule (HDSM) [9], clamp-double submodule (CDSM) [10], [11], diode-clamp submodule (DCSM) [12], [13], switched capacitor submodule (SCSM) [14], clamp-circuit-double submodule (CCSM) [15], series-connected-double submodule (SCDSM) [16], unipolar-voltage full-bridge submodule (UFBSM) [16], and active clamp T-type submodule (ACTSM) [17].

If the MMC is with the dc fault ride-through capability, it could be operated as a static synchronous compensator (STATCOM) under the dc fault condition to support the ac grid by providing reactive power. During the fault ride-through period, the capacitor voltage in each submodule is under control. Then the restart process of the MMC after the fault clearance could avoid the charging process and the availability of the MMC is increased. The full-bridge submodule (FBSM) [18], two-port FBSM (TFBSM) [19], hybrid-series-connected submodule (HSSM) [20]–[22], and cross-connected-double submodule (CCDSM) [23] are the available submodule circuits for the MMC with dc fault ride-through capability.

Table 1 shows all above-mentioned submodule circuits. The MMC with dc fault ride-through capability also owns fault blocking capability. However, the MMC with fault ride-through capability has a higher cost as more power switching devices are required in each submodule to output negative voltage. In the applications of flexible HVDC system, isolating the fault point and suppressing the fault current are the most important task during the period of dc

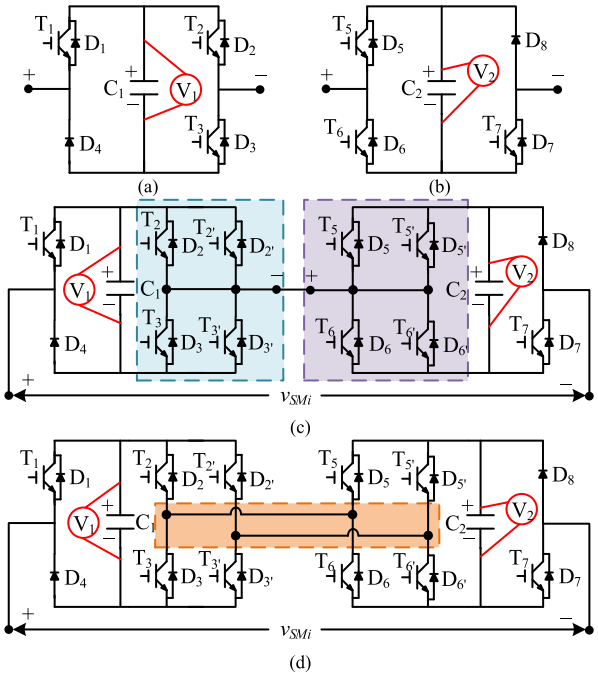



**FIGURE 1.** Derivation process of UDSSM. (a) UFBSM circuit 1. (b) UFBSM circuit 2. (c) Modified submodule circuit 1. (d) Proposed UDSSM circuit.

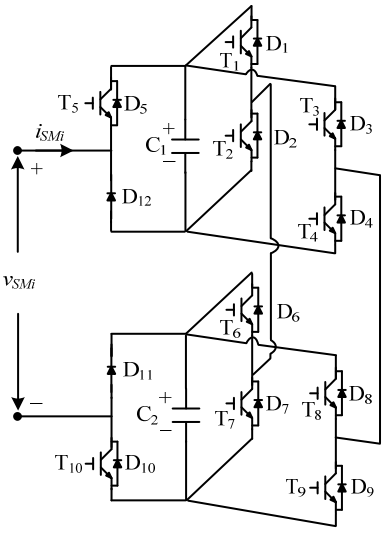



**FIGURE 2.** Topology of the UDSSM.

fault. Additionally, in an overhead line based HVDC system, the occurrence possibility of short-time dc short-circuit fault is higher than a permanent dc fault. Therefore, this paper focuses on the MMC topology with dc fault blocking capability, which is more economical than the one with dc ride-through capability.

This paper proposes a novel unipolar double-star submodule (UDSSM) for high reliability MMC system with dc fault blocking capability. There are two capacitors in the UDSSM, and normally a voltage sensor is required for each capacitor to implement capacitor voltage balancing control. The voltage sensor of the capacitors plays a significant role to the reliability of the MMC system since not only the voltage balancing control but also the protection of the submodules is related [24]. Based on the redundancy of two voltage sensors in the UDSSM, the capacitor voltage balancing control under malfunction of the voltage sensor would be researched in this paper.

The remainder of this paper is organized as follows. Section II gives the topology of the UDSSM submodule. Its control strategies are discussed in Section III. Section IV presents the simulation results of the UDSSM based MMC. The experimental results are given in Section V. Section VI gives the conclusions of this paper.

## II. TOPOLOGY

### A. SUBMODULE CIRCUIT

The UFBSM is a widely accepted submodule with dc fault blocking capability, which has two specific circuits, as shown in Fig. 1(a) and 1(b). In a UFBSM based MMC system, each capacitor requires a voltage sensor for capacitor voltage balancing. In order to improve the reliability of the MMC system, the following steps are adopted, as shown in Fig. 1(c) and 1(d). Firstly, the power switching devices $T_{2'}(D_{2'})$, $T_{3'}(D_{3'})$, $T_{5'}(D_{5'})$, and $T_{6'}(D_{6'})$ are connected in parallel to another group $T_2(D_2)$, $T_3(D_3)$, $T_5(D_5)$, and $T_6(D_6)$, respectively. Then the two U-FBSMs are connected in series, as shown in Fig. 1(c). Finally, the connection between two submodules is modified as Fig. 1(d), which is the proposed UDSSM circuit.

The proposed UDSSM is redrawn in Fig. 2, which consists of two capacitors, two clamp diodes, and ten power switching devices with anti-parallel diodes. Supposing the two capacitor voltages in UDSSM are well balanced, under the normal operation, the UDSSM could output three voltage levels. They are 0, $v_c$, and $2v_c$, where $v_c$ is the capacitor voltage. Fig. 3 shows the current paths under different output voltage levels. In Fig. 3, only $T_5$ and $T_{10}$ are always switched on, and other power switching devices are switched on or off depending on the required output voltage level.

If a UDSSM needs to output zero voltage level, $T_1$ ($D_1$), $T_3$ ($D_3$), $T_7$ ($D_7$) and $T_9$ ($D_9$) are switched on, and the two capacitors in this submodule are both bypassed, as shown in Fig. 3(a). As the direction of the current is positive, the specific current path is $D_5$, $T_1$, $T_3$, $T_7$, $T_9$, and $D_{10}$. As the direction of the current is negative, the specific current path is $T_5$, $D_1$, $D_3$, $D_7$, $D_9$, and $T_{10}$. There are two current paths in U-DSSM to output the first voltage level ($v_c$), as shown in Fig. 3(b) and 3(c). On path 1, the UDSSM outputs the first voltage level through $T_2$ ($D_2$), $T_3$ ($D_3$), $T_7$ ($D_7$), and $T_8$ ($D_8$), while through $T_1$ ($D_1$), $T_4$ ($D_4$), $T_6$ ($D_6$), and $T_9$ ($D_9$), the same output could be obtained on path 2. Both on path 1 and 2, two capacitors in a submodule are connected in parallel, which means two capacitor voltages could be balanced naturally. Here, the current would go through $D_5$, $C_1$, $D_2$, $T_7$, $T_3$, $D_8$, $C_2$, and $D_{10}$ as the direction of the current is positive. The current would go through $T_{10}$, $C_2$,

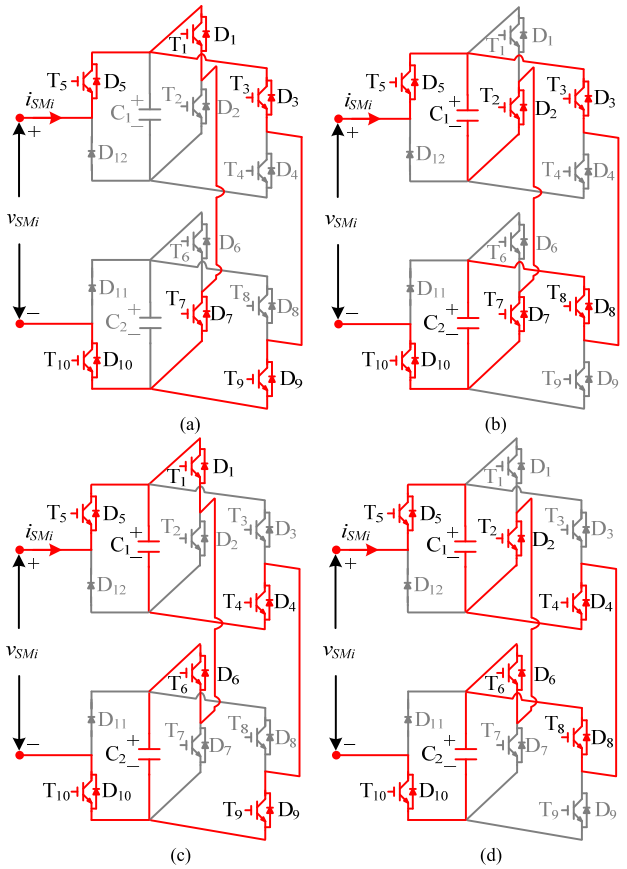



**FIGURE 3.** Current paths in the UDSSM under different outputting voltage levels. (a) The path for zero voltage level. (b) Path 1 (P1) for the first voltage level. (c) Path 2 (P2) for the first voltage level. (d) The path for the second voltage level.

$T_8$, $D_3$, $D_7$, $T_2$, $C_1$, and $T_5$ as the direction of the current is negative, as shown in Fig. 3(b). Fig. 3(c) shows, the current would go through $D_5$, $C_1$, $D_4$, $T_9$, $T_1$, $D_6$, $C_2$, and $D_{10}$ as the direction of the current is positive. As the direction of the current is negative, the current would go through $T_{10}$, $C_2$, $T_6$, $D_1$, $D_9$, $T_4$, $C_1$, and $T_5$. In Fig. 3(d), UDSSM outputs the second voltage level ($2v_c$) by switching $T_2$ ($D_2$), $T_4$ ($D_4$), $T_6$ ($D_6$) and $T_8$ ($D_8$) on. Under this situation, the two capacitors in this submodule are connected in series, which means the same current passes through two capacitors. Here, the current would go through $D_5$, $C_1$, $D_2$, $D_6$, $D_4$, $D_8$, $C_2$, and $D_{10}$ as the direction of the current is positive. The current would go through $T_{10}$, $C_2$, $T_8$, $T_4$, $T_6$, $T_2$, $C_1$, and $T_5$ as the direction of the current is negative. Table 2 gives the operating states of power switching devices under different output voltage levels, where $S_{ij}$ ($i = 1, \ldots, N; j = 1, \ldots, 10$) is the operation state for a $j$th power switching device in $i$th submodules, one arm of the MMC.

### B. NUMBER OF POWER SWITCHING DEVICES

The proposed submodule contains two clamp diodes and ten power switching devices with anti-parallel diodes, which seems that there is a higher number of components than

**TABLE 2.** Operation states of power switching device.

| L | $S_{i1}$ | $S_{i2}$ | $S_{i3}$ | $S_{i4}$ | $S_{i5}$ | $S_{i6}$ | $S_{i7}$ | $S_{i8}$ | $S_{i9}$ | $S_{i10}$ | O |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1(P1) | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | $v_c$ |
| 1(P2) | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | $v_c$ |
| 2 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | $2v_c$ |

● L represents the voltage level; O represents the output voltage of the submodule.

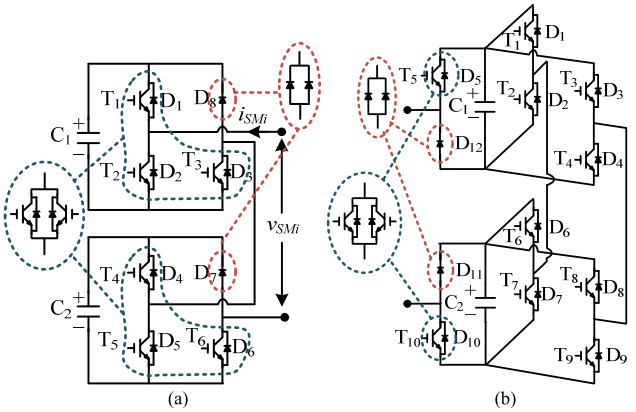



**FIGURE 4.** Circuit Comparison. (a) Two UFBSMs. (b) UDSSM.

the existing submodules with the same dc fault blocking capability. However, in the proposed UDSSM, it can be seen from Fig. 3 that the current on $T_1$ ($D_1$), $T_2$ ($D_2$), $T_3$ ($D_3$), $T_4$ ($D_4$), $T_6$ ($D_6$), $T_7$ ($D_7$), $T_8$ ($D_8$), and $T_9$ ($D_9$) are only the half of submodule current ($i_{SMi}$), which means that the proposed UDSSM does not enlarge the number of components in a practical application.

To explain it better, the widely accepted submodule UFBSM with the same dc blocking capability is taken as an example to compare with the proposed UDSSM. Because a FBSM could only output two voltage levels, two UFBSMs in series connection has the same output voltage levels under normal operation and same dc fault blocking capability as one UDSSM. Fig. 4 shows the comparison of the submodule circuit. In a practical application, the power switching devices might need parallel connections to tolerate the current stress on them, especially in a high power application. Assuming that two power switching devices in parallel connection could meet the requirement of current stress, in UFBSM, all the power switching devices and diodes should be in parallel connection as shown in Fig. 4(a). Then, 4 clamp diodes and 12 power switching devices for two U-FBSMs are required to meet the requirement of current stress. However, in the proposed UDSSM, only two clamp diodes and two power switching devices with anti-parallel diodes should be in parallel connection to meet the requirement of the same current stress as two UFBSMs. Then, there requires 4 clamp diodes and 12 power switching devices with anti-parallel diodes in UDSSM, which is the same as two UFBSMs. Therefore, the proposed UDSSM does not increase the number of power switching devices in a practical application.

**TABLE 3.** Comparison of switching actions.

| Level transition | UFBSM | UDSSM |
|---|---|---|
| 0→1 | 2 devices(OFF)<br>2 devices(ON) | 2 devices(OFF)<br>2 devices(ON) |
| 0→2 | 4 devices(OFF)<br>4 devices(ON) | 4 devices(OFF)<br>4 devices(ON) |
| 1→2 | 2 devices(OFF)<br>2 devices(ON) | 2 devices(OFF)<br>2 devices(ON) |

### C. POWER LOSSES

The power loss is a critical concern on the converter, which is directly related to the power transmission efficiency. The MMC is constructed by a lot of identical submodules, and then the power losses in each submodule determine the efficiency of the MMC system. The power losses include conducting losses and switching losses. The conducting losses are the main losses in a MMC system, which are related to the value of the current and the number of power switching devices on the current path.

For evaluating the conducting losses of the proposed UDSSM, its conducting losses are compared with the ones of the UFBSM. In order to make a reasonable comparison, the number of power switching devices is calculated under the same current stress. Therefore, the circuits of UFBSM and UDSSM shown Fig. 4 are adopted during the comparison. Fig. 4(a) and 4(b) show that there are always eight power switching devices on the current path under the normal operation condition for both circuits. Therefore, it could be concluded that the UDSSM based MMC system has the same conducting losses with the UFBSM based MMC system.

The switching losses are mainly related to the switching frequency, voltage and current on the power switching devices. In an MMC system, the comparison of the switching losses could be conducted by counting the number of switching actions on the power switching devices during the transition of different output voltage levels. Based on the topologies shown in Fig. 4, the comparison of switching actions is given in Table 3. It is obvious that the UDSSM has the same number of switching actions as the UFBSM during the transition of different output voltage levels. Therefore, the UDSSM has the same switching losses as the UFBSM.

### D. DC FAULT BLOCKING

During the dc short-circuit fault period, all the power switching devices in UDSSM should be switched off. And the capacitors in UDSSM would be connected in series through the remained diodes in the circuits to block fault current. The equivalent circuits of the UDSSM during the blocking period, under the positive and negative fault current, are shown in Fig. 5(a) and 5(b), respectively. As the current is positive, two capacitors in a UDSSM are connected in series into the circuits through $D_5$, $D_2$, $D_4$, $D_6$, $D_8$, and $D_{10}$. As the current is negative, two capacitors in a UDSSM are connected in series into the circuits through $D_{11}$, $D_7$, $D_8$, $D_1$, $D_3$, and $D_{12}$. It can be seen from Fig. 5 that the sum voltage of two capacitors could always block the fault current no matter what the current direction is.

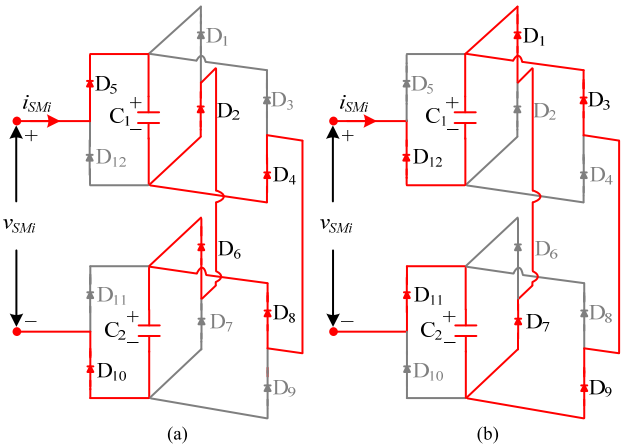



**FIGURE 5.** Equivalent circuits of the UDSSM. (a) $i_{SMi} > 0$. (b) $i_{SMi} < 0$.

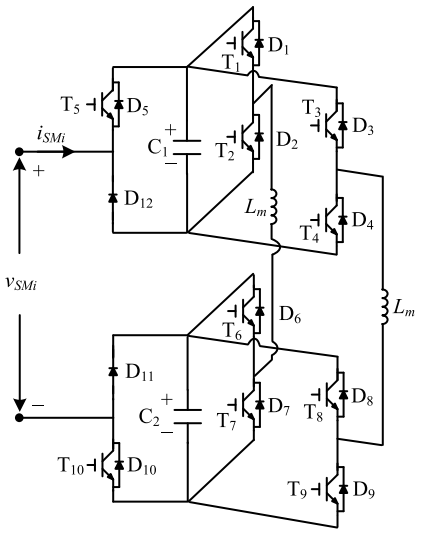



**FIGURE 6.** An alternative implementation of UDSSM.

### E. ALTERNATIVE IMPLEMENTATION

The mismatch of the two capacitors in one submodule might challenge the operations of the proposed UDSSM in applications. If the mismatch of capacitance exists, under the condition of series-connection of two capacitors, the divergence of capacitor voltages in one submodule would appear under the condition of series connection of two capacitors. Then, when two capacitors are in parallel connection, a surge current would emerge. In order to solve this problem, two small inductors could be used in each submodule to suppress the surge current [6]. Then, the alternative circuit of proposed UDSSM could be shown in Fig. 6. When the two capacitors in a submodule are connected in parallel to output the first voltage level, two inductors in this submodule are connected in series to suppress the surge current caused by the capacitance mismatch. In addition, two inductors are always connected

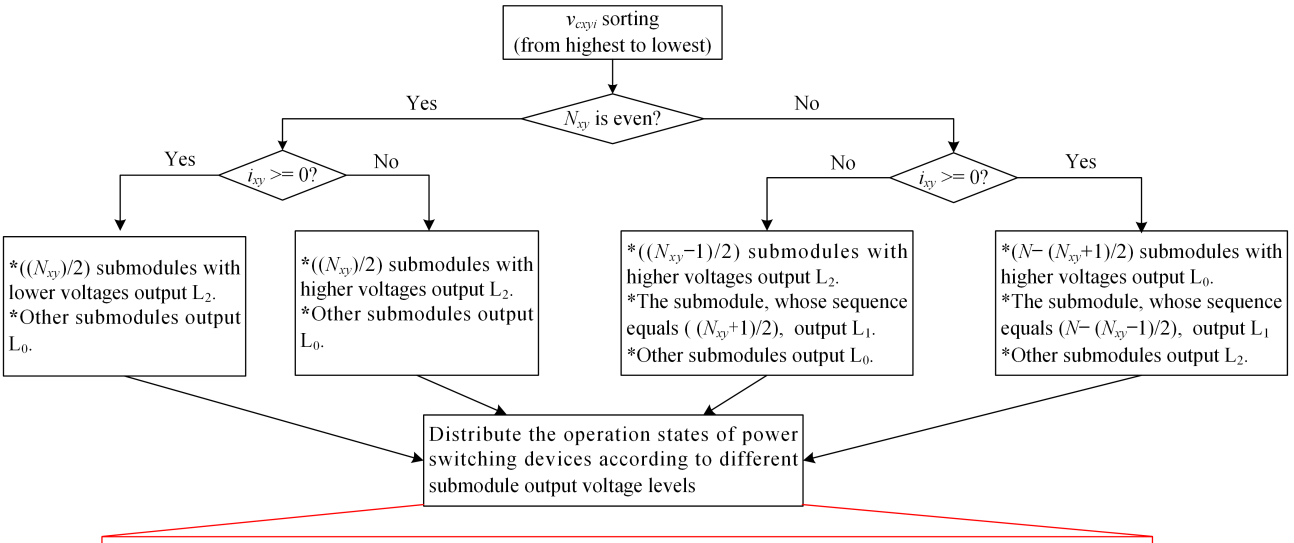



TABLE
Operation States of Power Switching Device (U-DSSM)

| L | $S_{xyi1}$ | $S_{xyi2}$ | $S_{xyi3}$ | $S_{xyi4}$ | $S_{xyi5}$ | $S_{xyi6}$ | $S_{xyi7}$ | $S_{xyi8}$ | $S_{xyi9}$ | $S_{xyi10}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $L_0$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| $L_1$(P1) | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| $L_1$(P2) | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| $L_2$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

*$Sxyij$ ($x$=$a$, $b$, $c$; $y$=$p$, $n$; $i$=1,⋯, $N$; $j$=1,⋯, 10) represents the operation states of power switching device in phase $x$, arm $y$, $i$th submodule.

**FIGURE 7.** Sorting process for proposed submodules based MMC under normal operation.

into the circuits, so they could be considered as a part of the arm inductor to suppress the circulating current and the fault current. The inductance value in each submodule, which could be equivalent as a part of the arm inductance, is $L_m/2$.

## III. CONTROL STRATEGIES

Because the UDSSM always outputs non-negative voltage levels under normal operation, which is same with traditional MMC system based on HBSM, some controllers for HBSM based MMC system could be directly applied for UDSSM based MMC system, including the grid current control and circulating current suppression control. Only the capacitor voltage balancing is different for the UDSSM based MMC system.

In the traditional HBSM based MMC, the voltage of all capacitors should be measured for the capacitor voltage balancing control. Then a sorting process is implemented to regulate the operation states of power switching devices according to the capacitor voltage, the direction of the arm current, and the number of inserted submodules. The sorting process of the UDSSM based MMC is different with the traditional MMC, where each UDSSM has two capacitors and the total number of the capacitor voltage sensor is $2N$ for the UDSSM based MMC with $N$ submodules in each arm. To indicate the voltage level of the capacitors in different submodules, the average voltage of two capacitors is adopted as the submodule voltage for the UDSSM. Then the capacitors in submodule with higher submodule voltage should be preferentially selected to be discharged or would have a low priority to be charged. Because there only needs to compare the $N$ submodule voltage for $2N$ capacitors, the sorting burden is reduced from $(2N * (2N - 1)/2)$ to $(N * (N - 1)/2)$ compared with the UFBSM based MMC.

The sorting process of the UDSSM based MMC is shown in Fig. 7, where $v_{cxyi}$ ($x = a, b, c$; $y = p, n$; $i = 1, .., N$), is considered as the submodule voltage for one submodule, and $i_{xy}$ ($x = a, b, c$; $y = p, n$) is the arm current. The UDSSM has two capacitors and could output three voltage levels, $N_{xy}$ ($x = a, b, c$; $y = p, n$) shown in Fig. 7 is the desired number of voltage level for each arm with UDSSMs, which is equivalent to the number of the inserted submodules in HBSM based MMC system. If the desired number of voltage levels for an arm is three, the arm voltage would be $3v_c$, under the capacitor voltage balancing condition.

The capacitor voltage balancing strategy for UDSSM based MMC under normal operation could be given as follows. Firstly, the submodule voltages for each submodule are sorted from highest to lowest. The desired voltage levels $N_{xy}$ for an arm could be even or odd, which is discussed as follows.

Under the condition of $N_{xy}$ being even, supposing the arm current $i_{xy}$ is positive, $(N_{xy})/2$ submodules with lower submodule voltages output second voltage level, other submodules output zero voltage level. If the arm current is negative, $(N_{xy})/2$ submodules with higher submodule voltages output second voltage level, other submodules output zero voltage.

**TABLE 4. Comparison of existing topologies in large power applications.**

| Submodule | HDSM | CDSM | DCSM | CCSM | SCDSM | UFBSM | ACTSM | SCSM | UDSSM |
|---|---|---|---|---|---|---|---|---|---|
| Number of IGBTs | 10 | 10 | 6 | 12 | 10 | 6 | 12 | 12 | 12 |
| Number of extra diodes | 2 | 4 | 2 | 4 | 2 | 2 | 4 | 2 | 4 |
| Number of output voltage levels | 3 | 3 | 2 | 3 | 3 | 2 | 3 | 3 | 3 |
| Dc fault blocking capability | $+2v_c$ $-v_c$ | $+2v_c$ $-v_c$ | $+v_c$ $-0.5v_c$ | $+2v_c$ $-v_c$ | $+2v_c$ $-2v_c$ | $+v_c$ $-v_c$ | $+2v_c$ $-2v_c$ | $+2v_c$ $-v_c$ | $+2v_c$ $-2v_c$ |
| Conducting losses | $1.5P_{c\text{-}HB}$ | $1.5P_{c\text{-}HB}$ | $1.5P_{c\text{-}HB}$ | $2P_{c\text{-}HB}$ | $2P_{c\text{-}HB}$ | $2P_{c\text{-}HB}$ | $2P_{c\text{-}HB}$ | $1.5P_{c\text{-}HB}<P_c<2P_{c\text{-}HB}$ | $2P_{c\text{-}HB}$ |
| Sensor fault tolerance | NO | NO | NO | NO | NO | NO | NO | YES | YES |
| Control complexity | Simple | Simple | Simple | Simple | Simple | Simple | Simple | Complex | Complex |

* $P_{c\text{-}HB}$ is the conducting losses of the two HBSMs in series.

Under the condition of $N_{xy}$ being odd, if the arm current is positive, $N-(N_{xy}+1)/2$ submodules with higher submodule voltage would output zero voltage level. The submodule, whose sequence is $N-(N_{xy}-1)/2$, would output the first voltage level. And other submodules output the second voltage level. If the arm current is negative, $(N_{xy}-1)/2$ submodules with higher submodule voltage output the second voltage level. The submodule, whose sequence is $(N_{xy}+1)/2$, outputs the first voltage level. And other submodules output the zero voltage level. At last, according to Table 2, the operation states of each power switching devices under different desired voltage levels could be determined to achieve capacitor voltage balancing.

In order to further illustrate Fig. 7, the MMC system with $N = 10, N_{xy} = 10$ and $N = 10, N_{xy} = 11$ are taken as examples. In the case of MMC system with $N = 10, N_{xy} = 10$, if the arm current is positive in the MMC system with $N = 10$, $N_{xy} = 10$, five $(10/2 = 5)$ submodules in this arm with lower submodule voltage are preferentially selected to output the second voltage level, and other submodules output zero voltage level. If the arm current is negative, five $(10/2 = 5)$ submodules in this arm with higher submodule voltage are preferentially selected to output the second voltage level, and other submodules output zero voltage level.

In the case of MMC system with $N = 10, N_{xy} = 11$, if the arm current is negative, five $((11-1)/2 = 5)$ submodules with higher submodule voltage are preferentially selected to output the second voltage level. The submodule, whose sequence of the submodule voltage is six $((11+1)/2 = 6)$, is selected to output the first voltage level. And other submodules output zero voltage level. If the arm current is positive, four $(10-(11+1)/2 = 4)$ submodules with higher submodule voltage are selected to output zero voltage level. The submodule, whose sequence of the submodule voltage is five $(10-(11-1)/2 = 5)$, outputs the first voltage level. And other submodules output the second voltage level.

For two capacitors in each UDSSM always have almost the same operating condition, (both bypassed for zero voltage level, parallel-connected for first voltage level, serial-connected for second voltage level), two voltage sensors in the UDSSM are redundant each other. Therefore, the malfunction of one voltage sensor will not influence normal operation of the submodule and the MMC system by adopting the voltage of the normal sensor, instead of the average voltage of two sensors, as the submodule voltage.

Table 4 shows the comparisons of the existing topologies considering the same current stress in large power applications (analysis in Part B, Section II). It should be noted that in Table 4 the conducting losses are calculated under the same conditions of output voltage levels.

Both the SCSM and the proposed UDSSM could tolerate the sensor fault, which improves the reliability of the MMC system. It can be seen from Table 4 that the proposed UDSSM have a slightly higher number of diodes, compared with SCSM in large power applications. The SCSM only has an asymmetrical dc fault blocking capability, where two capacitors in the SCSM could be connected in series to block the fault current under the positive fault current while under the negative fault current, only one capacitors in the SCSM could be connected into the circuit to block the fault current. However, the proposed UDSSM has a symmetrical dc fault blocking capability, which means two capacitors would always be connected in series into the circuit to block the fault current no matter what the direction of the fault current is. Therefore, the proposed UDSSM has a better dc fault blocking capability than the SCSM.

## IV. SIMULATIONS

In order to validate the dc fault blocking capability of the MMC with proposed UDSSM, an MMC system is modeled in the Matlab/Simulink surrounding. The phase disposition (PD) pulse width modulation and the circulating current

**TABLE 5. Parameters for simulations.**

| Symbol | Parameter | Value |
|---|---|---|
| $U_{a,\,b,\,c}$ | Grid voltage | 100 kV |
| $E$ | DC-side voltage | 240 kV |
| $C$ | Submodule capacitance | 666 μF |
| $L_s$ | Arm inductance | 38 mH |
| $R$ | Load resistance | 240 Ω |
| $f_c$ | Carrier frequency | 2 kHz |
| $v_c$ | Reference capacitor voltage | 24 kV |
| $N$ | Number of submodules per arm | 5 |
| $P$ | Active power | 240 MW |
| $Q$ | Reactive power | 0 MVar |
| $f$ | Fundamental frequency | 50 Hz |
| $t_0/t_1$ | B/R time for UDSSM | 0.5/0.52 s |

● B represents blocking; R represents recovering.

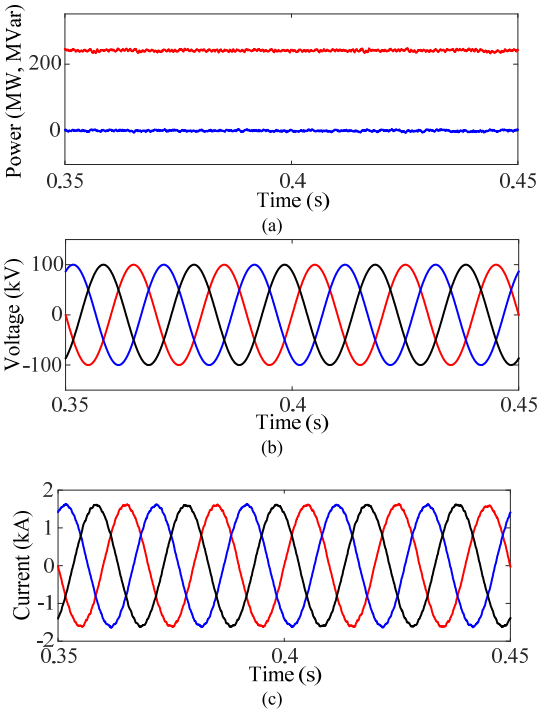



**FIGURE 8. Simulation results 1 under normal operation. (a) Active and reactive power. (b) Grid voltages. (c) Grid currents.**

suppression strategy proposed in [25] are applied in this simulation. The system parameters are given in Table 5.

### *A. NORMAL AND SENSOR FAULT OPERATION*

The simulation results of UDSSM based MMC under normal operation are shown in Fig. 8. Fig. 8(a) shows the waveforms of active and reactive power, which are stable at 240 MW and 0 MVar, respectively. The waveforms of grid voltage are presented in Fig. 8(b), where their amplitude is 100 kV and frequency is 50 Hz. Fig. 8(c) gives the waveforms of the grid current, which are in good sinusoidal characteristic, and their amplitude is 1.6 kA.

Fig. 9(a) shows the waveforms of arm currents in phase *A*, where they contain both dc and alternating component. It shows that the dc and fundamental component are the main components of upper arm current, with their amplitudes being

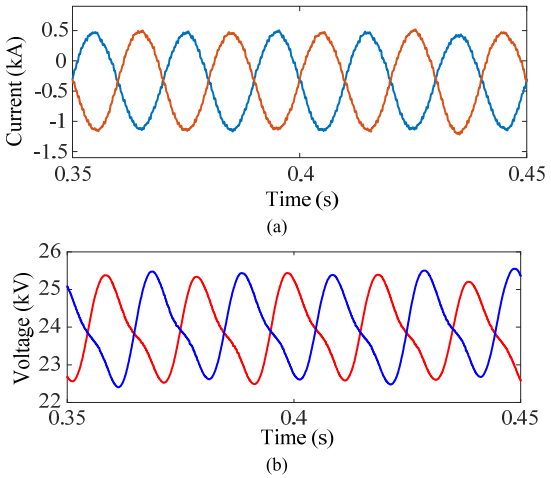



**FIGURE 9. Simulation results 2 under normal operation. (a) Arm currents in phase *A*. (b) Capacitor voltages in phase *A*.**

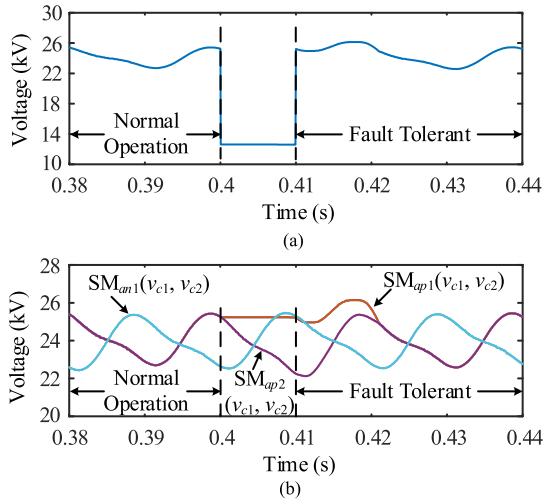



**FIGURE 10. Simulation results under voltage sensor fault. (a) Submodule voltage for $SM_{ap1}$. (b) Capacitor voltages in different submodules.**

about 330.2 A and 797.6 A, respectively. The waveforms of the capacitor voltages are shown in Fig. 9(b), where the capacitor voltages are well balanced at 24 kV.

The control strategies under voltage sensor fault are also verified. The voltage sensor of $C_2$ in the first submodule of the positive arm in phase *A* is in failure and its output becomes zero at time 0.4 s. The fault tolerant control enables at 0.41 s, which means the submodule voltage for $SM_{ap1}$ substituted by the output of the normal voltage sensor after 0.41 s. Then the submodule voltage of the first submodule is shown in Fig. 10(a).

Fig. 10(b) shows the waveforms of the capacitor voltage in different submodules. Before 0.4 s, the capacitor voltages are well balanced not only in the same submodule, but also among different submodules. From 0.4 s and 0.41 s, though two capacitor voltages in $SM_{ap1}$ are well balanced, the capacitor voltages in $SM_{ap1}$ are different obviously from other submodules in the same arm due to the faulty voltage sensor.

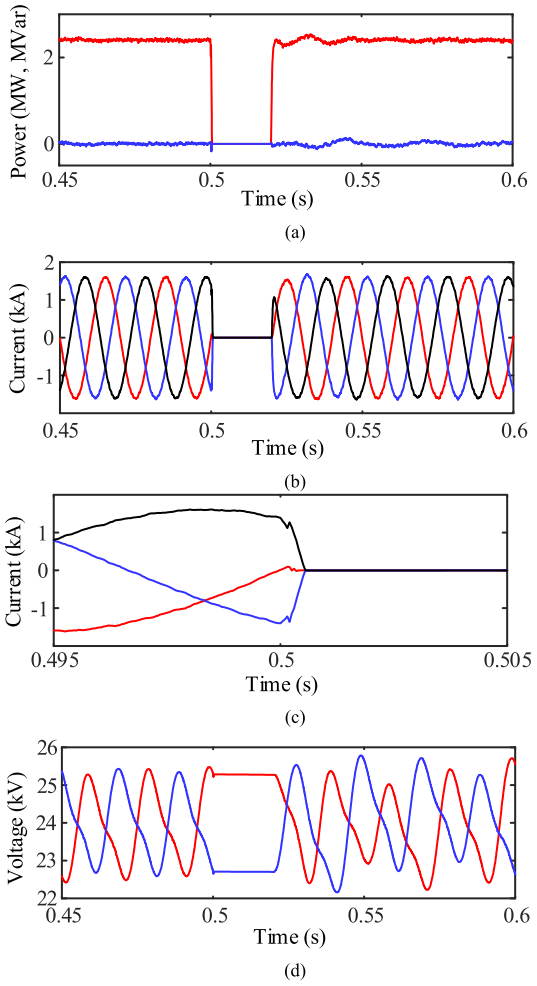



**FIGURE 11.** Simulation results of UDSSM based MMC under dc fault. (a) Active and reactive power. (b) Gird currents. (c) Enlarged plots of grid currents. (d) Capacitor voltages.

As the fault tolerant control enables at 0.41 s, all the capacitor voltages are well balanced again. The simulation results verify the effectiveness of the proposed control strategies.

### B. BLOCKING CAPABILITY OF UDSSM

Fig. 11 shows the simulation results of UDSSM based MMC during the dc fault period. The dc fault occurs at 0.5 s, and is cleared at 0.52 s. At 0.5001 s, all the power switching devices in UDSSM based MMC are switched off to block the fault current. Fig. 11(a) shows the active and reactive power are 240 MW and 0 MVar respectively, before the occurrence of dc fault. During the blocking period, both the value of active and reactive power becomes zero. The value of active and reactive power recovers to be the ones before the occurrence of the dc fault, as the dc fault is cleared.

In Fig. 11(b), the grid currents decrease quickly to be zero as all the power switching devices are switched off at 0.5001 s. And the grid currents recover fast as the dc fault is cleared. Fig. 11(c) shows the enlarged plots of grid currents, where the time-consuming of current decreasing is

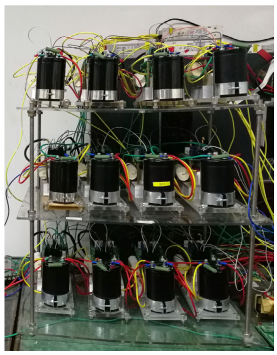


**FIGURE 12.** Experimental porotype.

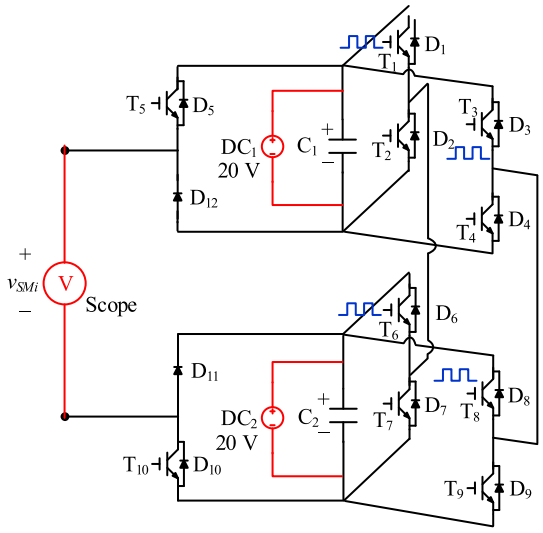



**FIGURE 13.** Diagram of experiment 1.

less than 500 $\mu$s. In Fig. 11(d), all the capacitor voltages are balanced during the normal operation, and they keep constant during the blocking period. After the clearance of dc fault, the capacitor voltages are also well balanced during the operation period.

## V. EXPERIMENTS

For validating the effectiveness of the proposed UDSSM, two submodule-level experiments are conducted. The first experiment is about the validation of submodule output voltage level. The second experiment is about the dc fault blocking capability of the U-DSSM. the experimental porotype is shown in Fig. 12.

### A. OUTPUT VOLTAGE LEVEL

Fig. 13 shows the diagram of experiment 1, where each capacitor connects to a dc voltage and their outputs are both 20 V. An oscilloscope is set at the ac output terminal of UDSSM to measure its output voltage. In this experiment, the drive signals for each power switching devices are given according to Table 2.

The drive signals and the output voltage of UDSSM are shown in Fig. 14. It can be seen that the relationships between

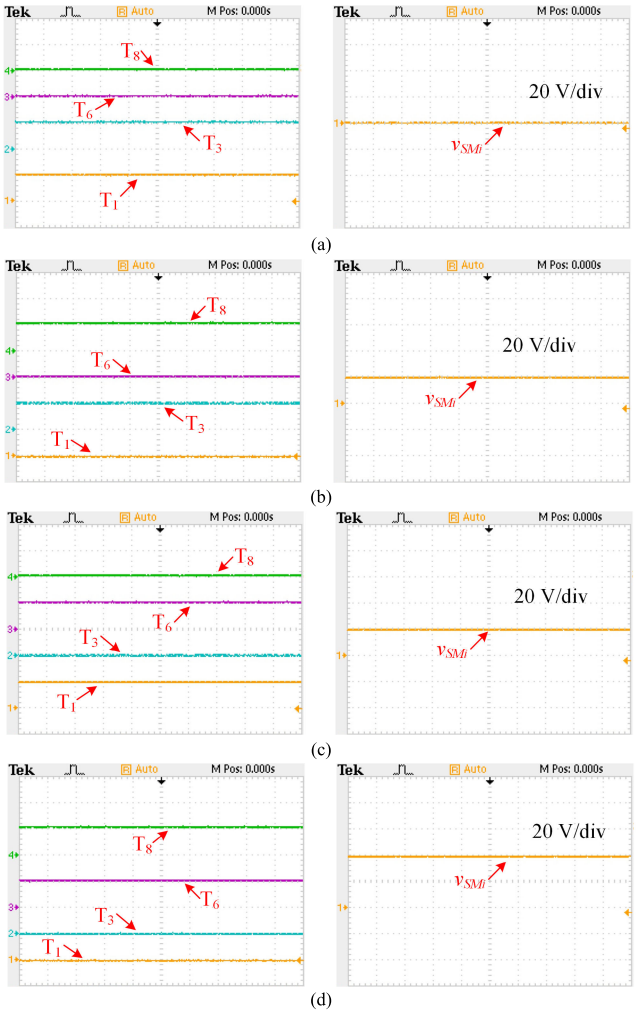



**FIGURE 14.** Results of experiment 1. (a) Zero voltage level. (b) First voltage level-P1. (c) First voltage level-P2. (d) Second voltage level.

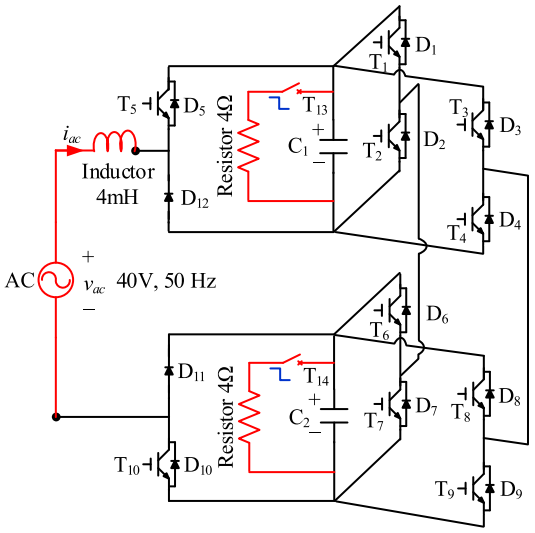



**FIGURE 15.** Diagram of experiment 2.

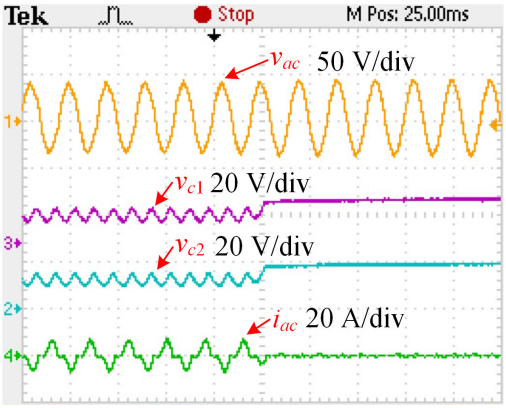



**FIGURE 16.** Results of experiment 2.

the driven signals and output voltage in UDSSM agree with the ones in Table 2.

### B. DC FAULT BLOCKING CAPABILITY

The diagram of the experiment 2 is shown in Fig. 15, where an ac source connects to the ac output terminals of UDSSM through an inductor. The output of the ac source is 40 V, 50 Hz, and the inductance is 4 mH. Each capacitor is connected with a 4 Ω resistor through a breaker. At first, all the power switching devices in UDSSM are switched off, however, two breakers, $T_{13}$ and $T_{14}$ are switched on. Under this situation, the circuit shown in Fig. 15 is equivalent to an uncontrolled rectifier. Two capacitors in UDSSM would be charged and the power is transferred from the ac voltage source to the dc side. When two breakers are switched off, the circuit in Fig. 15 will be equivalent to a real MMC circuit under the dc fault blocking period. The line-to-line voltage and the arm inductor in a real MMC are the ac voltage source and the inductor in Fig. 15, respectively.

The experimental results of dc fault blocking performance of UDSSM are shown in Fig. 16. Before the time point of 25 ms, the voltage of two capacitors varies because of the current supplied by the ac voltage source. After triggering two breakers at 25 ms, the current is suppressed to zero, and the voltage in two capacitors is stable at 20 V. The experiment results verify the dc fault blocking capability of the UDSSM.

## VI. CONCLUSION

This paper proposes a UDSSM circuit for the MMC to handle the dc short-circuit fault. The proposed UDSSM has a symmetrical dc fault blocking capability, where twice capacitor voltage could be output to block the fault current under both positive and negative current directions. In each UDSSM, two capacitors are under the almost same operating condition and the voltage sensors of the submodule capacitor are redundant, which improves the reliability of the MMC. Based on the redundancy of two voltage sensors in each submodule, this paper proposes capacitor voltage balancing control method for the UDSSM based MMC under both normal operation and

sensor fault condition. The simulation and experiment results validate the effectiveness of the proposed submodule.

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