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Control of Grid-Following Inverters under Unbalanced Grid Conditions

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Abstract— This paper proposes a new control scheme to eliminate the 3rd harmonic in the output currents of grid-following inverters under unbalanced grid conditions. Unbalanced grids adversely affect the performance of grid-following inverters due to the oscillations appearing on the DC-link voltage with a frequency twice the line frequency. The paper is based on instantaneous active reactive control (IARC) technique due to its advantages over other existing methods. However, the presence of severe asymmetrical 3rd harmonic distortions in the inverter output currents is the main challenge with IARC method, which impairs the power quality requirements. This paper enhances the IARC scheme by proposing a 3rd harmonic elimination approach by adopting a current reference generation method using the symmetric sequence components concept. Furthermore, the proposed scheme complies with the grid code requirements by injecting the requested reactive current. Finally, the proposed approach is evaluated by theoretical and simulation analysis and validated experimentally using a hardware setup.

Index Terms— Asymmetrical short circuit faults, DC-link voltage control, grid-following inverters, instantaneous active reactive control, output currents 3rd harmonics, unbalanced grid conditions.

I. INTRODUCTION

Grid-following inverter-based distributed generators (DGs) are future energy sources in electric power systems. They provide a cleaner environment, decrease the electricity production cost and power loss, and offer ancillary services for the grid such as reactive power support and active filtering [1-3]. By the end of 2017, the cumulative installed capacity of wind and photovoltaic energies have been increased to about 539 GW and 402 GW, respectively, and the total capacity has passed 1000 GW in 2018 [4, 5]. This amount of power is just a small portion of the available reachable power, and the interests for more of such clean energies are on the rise. However, non-ideal grid conditions such as imbalances and asymmetrical temporary short circuit faults are the inherent part of these systems, which degrade the performance of the inverters [6-8]. In such circumstances, the net power drawn from the DC-link capacitor carries a component with a frequency of twice the line frequency ($2\omega_0$) [9-11]. Also, in this situation, the output filter pulsating powers do not cancel out each other, which again causes more pulsating power taken from the DC side [12, 13]. Furthermore, in case of unbalanced input filters, even with a balanced grid, a pulsating power will be drawn from the DC side [14]. Accordingly, these pulsating components lead to oscillations on the DC-link voltage, and thereby, more stress on the DC-link capacitor [12].

The $2\omega_0$ ripple is also an important issue for single-phase inverters and DC-link capacitor selection [15]. As the power increases or the DC-link capacitance decreases, the ripples on DC link increases. Then, the capacitance should be selected high enough to mitigate the ripples [16]. To reduce the capacitor

size while keeping the level of ripples low, changing the inverter topology is one alternative [17]. Also, using a power decoupling circuit and power interfaces for the capacitor such as synchronous buck converter and H-bridge are suggested in [18-20]. However, removing the ripples in three-phase inverters is totally different. This is the main challenge that is solved in this paper.

Grid-forming inverter-based energy resources are the other kind of sources in the system, and the operation under grid unbalanced condition and asymmetrical short circuit fault is also a concern for this type of inverters. Accordingly, different methods are introduced in the literature to improve their performance under such conditions [21]. However, due to different operational principle and control structure, these remedies cannot be applied for grid-following inverters. In fact, the DC link of grid-forming inverters is connected to a stiff DC source; and then, the DC link voltage control is not an issue for this kind of inverters.

This paper is organized as follows. Section II reviews the variety of approaches available in the literature for the control of grid-following inverters under unbalanced conditions. Among different control schemes, Instantaneous Active Reactive Control (IARC) strategy is used for the inverter control in this paper. Section III describes the control structure of a grid-following inverter with IARC scheme. In section IV, the related issue associated with the IARC, i.e. high 3rd harmonic distorted output current, is addressed and resolved. Sections V and VI are dedicated to the simulation results and experimental verifications. Finally, the conclusions are summarized in Section VII.

II. GRID-FOLLOWING INVERTER CONTROL STRATEGIES UNDER UNBALANCED GRID CONDITIONS

Generally, there are five active power control approaches for grid following inverters to handle unbalanced conditions [22, 23]. Table I summarizes the control schemes under unbalanced conditions. As it can be seen from Table I, three methods of IARC, Instantaneously Controlled Positive-Sequence (ICPS), and Positive-Negative-Sequence Compensation (PNSC) for the inverter control remove the $2\omega_0$ ripples from the active power and correspondingly from the DC-link voltage. For this reason, these methods are preferred for the sake of ripple-free DC-link voltage control. The two first methods (i.e., IARC, and ICPS) violate the related power quality standards by injecting harmonic polluted currents into the grid. However, the third method (PNSC) provides sinusoidal output currents [24, 25]. Using the PNSC, both positive and negative sequence currents will be injected to the grid in order to provide instantaneous constant active power. The negative sequence current value depends on the value of the injected active power and the amount of grid voltage imbalance. In this method, the injected

TABLE I. INVERTER CONTROL STRATEGIES UNDER UNBALANCED CONDITIONS [22-23].

Control Strategies	Description	Advantages	Disadvantages
Instantaneous Active Reactive Control (IARC)	The inverter is controlled to deliver instantaneous constant active power to the grid.	<ul style="list-style-type: none"> • Elimination of $2\omega_0$ components from DC link voltage. • Grid voltage support by injecting current with higher amplitude to the phase with lower amplitude. • High BW for control system comparing to PNSC. • Closed loop active power control system. • Independency to filter inductance or operating point. 	<ul style="list-style-type: none"> • Injecting highly distorted current components to the grid.
Instantaneously Controlled Positive-Sequence (ICPS)	Instantaneously controlling the positive-sequence current to deliver constant active power and imposing negative sequence current to zero.	<ul style="list-style-type: none"> • Similar to IARC 	<ul style="list-style-type: none"> • Injecting non-sinusoidal distorted current components to the grid.
Positive-Negative-Sequence Compensation (PNSC)	Delivering active power to the grid by injecting sinusoidal positive- and negative-sequence currents.	<ul style="list-style-type: none"> • Elimination of $2\omega_0$ components from DC link voltage. • Sinusoidal output currents. • Grid voltage support by injecting current with higher amplitude to the phase with lower amplitude. 	<ul style="list-style-type: none"> • Low BW for control system comparing to IARC. • Open loop active power control system. • Dependency to filter inductance or operating point.
Average Active-Reactive Control (AARC)	Controlling the average of instantaneous active power.	<ul style="list-style-type: none"> • Sinusoidal output currents. 	<ul style="list-style-type: none"> • Large second order harmonics on active power and correspondingly on the DC link voltage.
Balanced Positive-Sequence Control (BPSC)	Injecting positive sequence current to the grid	<ul style="list-style-type: none"> • Sinusoidal output currents. • Using full current capacity of the inverter. 	<ul style="list-style-type: none"> • Second order harmonics on active power and correspondingly on the DC link voltage.

current into the faulty phase has a higher amplitude, which may help the grid to support the phase voltage. The Average Active-Reactive Control (AARC) scheme controls the average active power but creates large oscillations on the output power under unbalanced conditions [22]. The control strategy of the Balanced Positive-Sequence Control (BPSC) requires injecting a positive sequence current into the grid. This method provides the use of the full current capacity of the inverter [26]. However, it results in $2\omega_0$ oscillations on the DC-link voltage.

Control of positive and negative sequence currents based on the PNSC scheme has been widely used in the literature for the control of the inverter under unbalanced conditions. To realize this approach, the control of the currents in a dual “ dq ” frame has been presented in [27]. In this method, in addition to the conventional clockwise synchronous “ dq ” frame, another counter-clockwise synchronous “ dq ” frame is used to control both the positive and negative sequence current components. References [28] and [29] have developed mathematical expressions for the instantaneous power and have presented current set-points calculation methods to achieve constant instantaneous active power. In these studies, the output filter inductance was not modeled. With the same strategy, [30] has developed a unified dynamic model and control of the inverters and has calculated the current references by taking into account the output filter impact on the instantaneous power. Furthermore, [14] and [31] have employed a control scheme in a hybrid synchronous stationary frame. Above all, the PNSC control method has been performed in the stationary $\alpha\beta$ frame and a combined “ dq ” and $\alpha\beta$ frames in [10, 32-34]. The dual “ dq ” frame concept is also employed for current control strategies under voltage sags [35]. It is further used for studying fault ride through of grid-following inverters [36, 37], and current limiting strategy under unbalanced grid condition [38]. However, the sequence component extraction from the measured currents and its control is a challenge in the PNSC method using dual “ dq ” frame [39, 40]. Negative sequences in the conventional “ dq ” frame and positive sequences in a counter-clockwise “ dq ” frame appear as pulsating components

with the frequency of $2\omega_0$ [12]. Those components result in a non-zero steady-state error for the current control loops [27]. To remove these pulsating terms, notch filters are used [30]. Using notch filters limits the current control loop bandwidth (BW) to $2\omega_0$, which requires a low BW for the outer DC-link voltage control loop. Using a decoupled double synchronous reference frame removes the need for the notch filters. This method simultaneously uses the current references and the measured currents to remove the pulsating components from the currents in the dual “ dq ” frame [27, 41]. However, this method requires a low BW DC-link voltage control loop to provide constant non-oscillatory current references.

In summary, despite the advantages of the PNSC scheme (see Table I), the PNSC-based methods have a complex control structure. They work based on an open-loop active power control system since the oscillatory part of the active power is indirectly controlled by computing the negative sequence currents. Also, extracting positive and negative sequence components imposes a delay to the DC-link voltage control loop as the outer control loop in the system, which requires a low DC-link loop BW to avoid any interference between the current and the DC-link voltage control loops. The need to know system parameters and operating points are other issues associated with some of the PNSC-based methods.

IARC-based method can solve the above concerns. To realize an IARC scheme, a resonant compensator with the characteristic frequency of $2\omega_0$ is added to the conventional proportional-integral (PI) controller of the DC-link voltage. In this method, the DC and $2\omega_0$ components of the DC-link voltage, and consequently, the active power are directly controlled in a closed-loop control system without any need to calculate the positive/negative sequence components. Therefore, those limitations in the methods based on the PNSC method no longer exist. The effectiveness of this method on the control of the DC-link voltage and removing the $2\omega_0$ ripples has been validated by experiments in [42]. Also, the proportional-

integral-resonant (PIR) compensator design methodology has been provided in [43]. Despite the advantages of the IARC scheme, a large 3rd harmonic distortion on the output currents still remains an issue. The harmonics are unbalanced and cannot be filtered by using an output transformer with a delta connection. Therefore, the grid-following inverter injects distorted currents into the grid. The harmonic distortion is the most severe, and of course, unacceptable issues arise under asymmetrical voltage sags and fault conditions.

In this paper, an improved IARC control scheme using a PIR compensator as a controller has been adopted for the DC-link voltage control system. First, the fundamental concept of the main cause of the 3rd harmonic current distortion has been introduced and proved mathematically. Then, a 3rd harmonic current elimination method based on positive and negative sequence components concept (without any need to calculate these components in the control system) has been proposed and evaluated by a mathematical analysis. The proposed IARC method not only takes the benefits of the IARC scheme without its shortcoming but also keeps the advantages of the PNSC scheme by producing sinusoidal positive and negative sequence current components under unbalanced conditions.

III. IARC CONTROL SCHEME FOR GRID-FOLLOWING INVERTERS

The DC-link voltage, reactive power, and output current control loops are the cascaded control loops in grid-following inverters. The first two controllers, i.e. the DC-link voltage and the reactive power, are the outer control loops, and the last one is the inner control loop with a faster dynamic. Equation (1) represents the power balance in the DC-link capacitor, in which P_{in} is the input power from the DC primary source, and $1.5V_d i_d$ is the injected power to the ac grid. This relation is the fundamental dynamic equation for the DC-link voltage control. As it can be seen from (1), using the DC-link capacitor energy (W_{dc}) instead of the DC-link voltage (V_{dc}) results in a linear control system [12]. Also, the output reactive power is obtained from (2). In this scheme, the DC-link capacitor energy and reactive power controllers generate current references in the “dq” frame.

$$\frac{d}{dt} \left(\frac{1}{2} \frac{C_{dc} V_{dc}^2}{W_{dc}} \right) = P_{in} - \frac{3}{2} V_d I_d \quad (1)$$

$$Q = \frac{3}{2} V_d I_q \quad (2)$$

Using the grid voltages, the current controller generates the inverter terminal voltages to set the output currents at the reference values [44]. Fig. 1 shows the power circuit schematic and dynamic control model of a grid-following inverter in the “dq” frame including DC link energy and reactive power controls. In this structure, a phase locked loop (PLL) extracts the grid voltage angular frequency, and using abc/dq transformation, the system variables are obtained in the “dq” frame. The structure of the PLL under unbalanced conditions has been discussed in [12]. Fig. 2 represents the detailed DC-link capacitor energy (the outer) and the terminal current (the inner) control loops block diagrams. In this figure, the inverter current I_d is multiplied by $1.5V_d$ which results in the output power, and then, an integrator produces the DC-link capacitor

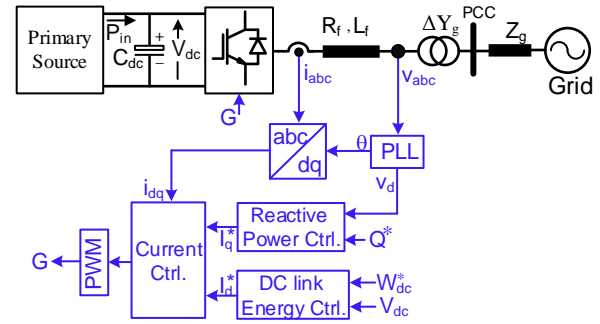


Fig. 1. Single line power circuit schematic and dynamic control block diagram of a three-phase grid-following inverter.

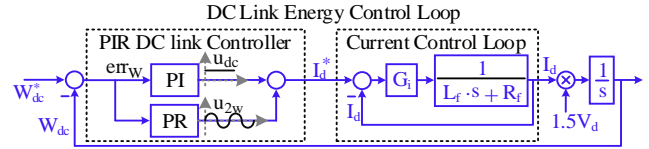


Fig. 2. DC link capacitor energy and terminal current control loop block diagram.

energy [12]. It is a well-known procedure to use (3) as a PI compensator for the current controller (G_i), which results in a first-order closed-loop transfer function from the reference value to the actual value of currents, where τ^{-1} is the current control loop bandwidth (BW), and L_f, R_f are output filter inductance and resistance [45].

$$G_i = \tau^{-1} \cdot \frac{L_f s + R_f}{s} \quad (3)$$

It is worth noting that the BW is limited by the inverter switching frequency. In this regard, $\tau^{-1} \ll 2\pi f_{sw}$ can be used as a rule of thumb, where f_{sw} is the switching frequency [12]. Also, the DC-link energy controller is a PIR (PI+PR) compensator in the IARC control scheme. As shown in Fig. 2, the PI and PR control signals are u_{dc} and u_{2w} , respectively. The PI compensator is responsible for regulating the DC component of the DC link energy, while the PR compensator controls the $2\omega_0$ component and force it to zero. Then, u_{dc} and u_{2w} are the DC and $2\omega_0$ components at steady state of control system. Accordingly, DC-link energy error of err_w is ensured to be zero for DC and $2\omega_0$ components. As shown in this figure, the control of the DC-link voltage (active power) for both DC and $2\omega_0$ components is done in a closed-loop system. Therefore, the concerns regarding the open-loop control of active power with positive/negative sequence currents in the PNSC scheme no longer exist. However, the 3rd harmonic current is a concern, which is addressed in the next section.

IV. PROPOSED STRATEGY FOR ELIMINATION OF OUTPUT CURRENT 3RD HARMONICS

In this section, the proposed IARC control strategy is introduced to enhance the performance of grid-following inverters under unbalanced and asymmetrical fault conditions. In this method, a feed-forward based strategy is proposed to eliminate the output current 3rd harmonic components.

As shown in Fig. 2, the PR compensator control signal, u_{2w} , has a pulsating component with the frequency of $2\omega_0$, which is needed to remove the same frequency components from DC-

link capacitor energy. This control signal is a part of the current reference, which logically provides the necessary negative sequence currents for the elimination of the $2\omega_0$ components of the DC-link capacitor energy. Despite this advantage, this control signal is the main cause for the 3rd harmonic component. To clarify the subject, consider the general form of (4) for the current references in the “dq” frame.

$$\begin{aligned} I_d^* &= I_d + I_{2d} \cdot \cos(2\omega_0 t + \theta_d) \\ I_q^* &= I_q + I_{2q} \cdot \cos(2\omega_0 t + \theta_q) \end{aligned} \quad (4)$$

where, I_d and I_q are the DC components for the “d” and “q” axes, respectively. Also, I_{2d} and I_{2q} represent the amplitudes of the oscillating components in the “d” and “q” axes, respectively, and θ_d and θ_q are the corresponding phase angles.

Using the “dq” to “abc” transformation matrix of (5), the current references of (4) are transferred to the “abc” frame as shown in (6). In this equation, $[I_{abc}]^*$ and $\overline{\text{COS}}^\pm(\cdot)$ are matrices as given in (7)-(8), respectively. There is the same definition for $\overline{\text{SIN}}^\pm(\cdot)$ by replacing cosine with sine in (8). Eq. (6) consists of three parts. The first and second parts are the positive and negative sequence components of the output currents references, while the third one indicates the 3rd harmonic component.

$$\begin{bmatrix} I_a^* \\ I_b^* \\ I_c^* \end{bmatrix} = \begin{bmatrix} \cos(\omega_0 t) & -\sin(\omega_0 t) & 0.5 \\ \cos(\omega_0 t - \frac{2\pi}{3}) & -\sin(\omega_0 t - \frac{2\pi}{3}) & 0.5 \\ \cos(\omega_0 t + \frac{2\pi}{3}) & -\sin(\omega_0 t + \frac{2\pi}{3}) & 0.5 \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \\ I_0^* \end{bmatrix} \quad (5)$$

$$\begin{aligned} [I_{abc}]^* &= \{I_d \cdot \overline{\text{COS}}^+(\omega_0 t) - I_q \cdot \overline{\text{SIN}}^+(\omega_0 t)\} \\ &+ \left\{ \frac{1}{2} I_{2d} \overline{\text{COS}}^-(\omega_0 t + \theta_d) + \frac{1}{2} I_{2q} \overline{\text{SIN}}^-(\omega_0 t + \theta_q) \right\} \\ &+ \left\{ \frac{1}{2} I_{2d} \overline{\text{COS}}^+(3\omega_0 t + \theta_d) - \frac{1}{2} I_{2q} \overline{\text{SIN}}^+(3\omega_0 t + \theta_q) \right\} \end{aligned} \quad (6)$$

$$[I_{abc}]^* = [I_a^* \quad I_b^* \quad I_c^*]^T \quad (7)$$

$$\overline{\text{COS}}^\pm(h\omega_0 t \pm \theta) = \begin{bmatrix} \cos(h\omega_0 t + \theta) \\ \cos(h\omega_0 t + \theta \mp \frac{2\pi}{3}) \\ \cos(h\omega_0 t + \theta \pm \frac{2\pi}{3}) \end{bmatrix} \quad (8)$$

A simple and effective approach is now proposed to update the current references to remove the 3rd harmonic components in the output currents. The updated current references in the “abc” frame representation form without the 3rd harmonic components are given:

$$\begin{aligned} [I_{abc}]_u^* &= \{I_d \overline{\text{COS}}^+(\omega_0 t) - I_q \overline{\text{SIN}}^+(\omega_0 t)\} \\ &+ \left\{ \frac{1}{2} I_{2d} \overline{\text{COS}}^-(\omega_0 t + \theta_d) + \frac{1}{2} I_{2q} \overline{\text{SIN}}^-(\omega_0 t + \theta_q) \right\}. \end{aligned} \quad (9)$$

Using the “abc” to “dq” transformation, the “dq” components corresponding to the updated current references are:

$$\begin{bmatrix} I_{du}^* \\ I_{qu}^* \end{bmatrix} = \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{2} \begin{bmatrix} I_{2d} \cdot \cos(2\omega_0 t + \theta_d) + I_{2q} \cdot \sin(2\omega_0 t + \theta_q) \\ I_{2q} \cdot \cos(2\omega_0 t + \theta_q) - I_{2d} \cdot \sin(2\omega_0 t + \theta_d) \end{bmatrix}. \quad (10)$$

Then, using (10) instead of (4) as the current reference not only removes the $2\omega_0$ components of the DC-link capacitor energy but also eliminates the undesired 3rd harmonic components from the output currents. Accordingly, to achieve the updated current references in (10), the terms

$I_{2q} \cdot \sin(2\omega_0 t + \theta_q)$ and $I_{2d} \cdot \sin(2\omega_0 t + \theta_d)$ should be added to the conventional current references of (4) in “d” and “q” axes, respectively. To obtain the terms $I_{2q} \cdot \sin(2\omega_0 t + \theta_q)$ and $I_{2d} \cdot \sin(2\omega_0 t + \theta_d)$, the pulsating components of (4), respectively, in “q” and “d” axes are delayed by a quarter of the period ($\frac{1}{4} \cdot \frac{2\pi}{2\omega_0}$), i.e. 2.5 msec in a 50 Hz system. Now, by adding the obtained needed terms to the conventional current references in (4), the updated current references in (10) are achieved. Fig. 3 graphically shows the explained procedure of finding the updated current references in (10).

In (10), the reactive current reference of I_q is taken from the related grid codes under short circuit conditions, and I_q is zero at normal operations. Also, I_{2q} is the amplitude of the oscillatory part of the “q” axis current. I_{2q} is assumed zero since there is no clear requirement regarding this component in the available grid codes [46]. For the case of non-zero I_{2q} , the general form presented in this paper can be used. However, the oscillatory part of $I_{2d} \cdot \sin(2\omega_0 t + \theta_d)$ on the “q” axis current in (10) is needed to remove the 3rd order harmonic component from the output currents. Accordingly, (11) demonstrates the updated current references, and (12) represents the corresponding current references in the “abc” frame.

$$\begin{bmatrix} I_{du}^* \\ I_{qu}^* \end{bmatrix} = \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{2} \begin{bmatrix} +I_{2d} \cdot \cos(2\omega_0 t + \theta_d) \\ -I_{2d} \cdot \sin(2\omega_0 t + \theta_d) \end{bmatrix} \quad (11)$$

$$\begin{aligned} [I_{abc}]_u^* &= I_d \overline{\text{COS}}^+(\omega_0 t) - I_q \overline{\text{SIN}}^+(\omega_0 t) \\ &+ \frac{I_{2d}}{2} \overline{\text{COS}}^-(\omega_0 t + \theta_d) \end{aligned} \quad (12)$$

As it can be seen from (12), the output currents have three terms. The two first terms are positive sequence currents, which are used to inject the desired active and reactive powers into the grid. However, the third term demonstrates a negative sequence current which is used to remove the pulsating components of the active power and correspondingly the DC-link voltage.

Notably, the pulsating component of the current in the “d” axis, i.e. ($I_{2d} \cdot \cos(2\omega_0 t + \theta_d)$), can simply be found using (13) considering the fact that $u_{2\omega}$ is the PR compensator control signal (Fig. 2).

$$I_{2d} \cdot \cos(2\omega_0 t + \theta_d) = u_{2\omega}. \quad (13)$$

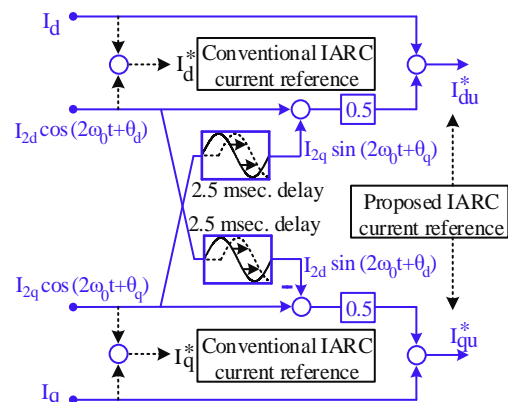


Fig. 3. Proposed current reference calculation for the 3rd harmonic elimination.

This means that the required pulsating component for the 3rd harmonic elimination directly comes from the outer control loop in a closed loop system. Therefore, the calculation of the references is instantaneous, and there is no need to adapt the controller for different operation conditions and compute the sequence components for the current reference calculation in an open loop structure. Also, no requirements for detecting voltage sags and grid faults are needed for the proposed 3rd harmonic elimination scheme since the scheme continuously works in the closed loop control structure. In other words, under unbalanced conditions, the proposed IARC method automatically generates $u_{2\omega}$ to remove $2\omega_0$ ripples from the DC-link voltage. In that sense, according to (13), the proposed scheme automatically avoids the flowing of 3rd harmonics in the output current.

Fig. 4 demonstrates the complete control system including the proposed current references of (11).

It is worth noting that using (10) instead of (4) as the updated references eliminates the 3rd harmonic without changing the positive and negative sequence components.

V. SIMULATION RESULTS

In order to evaluate the performance of the proposed approach, active and reactive currents injection under short circuit fault condition have been analyzed. The test system of Fig. 1 is simulated in Matlab/Simulink environment with the parameters given in Table II. The DC-link capacitor energy controller $G_w(s)$ is as:

$$G_w(s) = -0.16 \times \frac{s + 40}{s} - 0.58 \times \frac{s^2 + 130s + 63000}{s^2 + 394784}. \quad (14)$$

The DC-link capacitor energy control loop BW is 125 rad/sec, and the DC side source is modeled by a current source having the same characteristic like in PV systems.

In this case, a single-line-to-ground (SLG) fault is applied to the grid side of the transformer, reducing the faulty phase voltage to 0.15 p.u. Due to the transformer winding connection, the inverter sees the fault as a line-to-line fault with $V1=0.7$ p.u. and an imbalance ratio of $V2/V1=40\%$. Considering the grid code requirements, the inverter must inject a reactive current to support the grid voltage. As an example, the Danish grid code requires the injection of 100% reactive current to the grid for voltage drops more than 0.5 p.u [47]. The reactive current injection is zero for voltage drops less than 0.1 p.u. [46]. Then, for $V1=0.7$ p.u. voltage sag, a 50% reactive current injection is required. For this reason, the reactive current reference is set to $I_q=50$ A during the simulation. Also, $I_d=50$ A is used for the current reference in the “d” axis. Fig. 5 compares the simulation results for the control systems of conventional IARC and the proposed IARC. Fig. 5 (a)-(b) demonstrate the grid voltages at the inverter side of the transformer. Fig. 5 (c)-(d) show the current references in the “dq” frame for the conventional IARC and the proposed IARC, respectively. As shown in these figures, the DC-link capacitor energy controller produces the $2\omega_0$ references (“d” axis) to remove the same frequency components from the output instantaneous active power. The corresponding inverter output currents in the “abc” frame are depicted in Fig. 5 (e)-(f). As shown in Fig. 5 (e), employing the conventional IARC results in distorted current waveforms. The individual 3rd harmonic distortion for three phases are 15%-

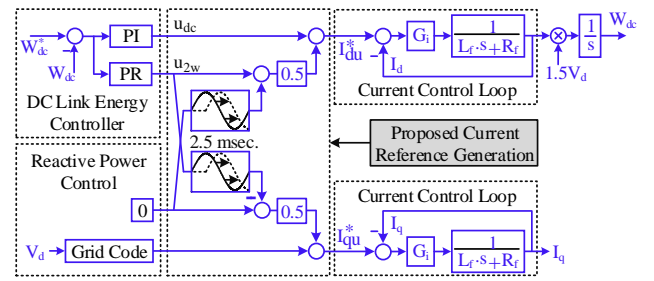


Fig. 4. Complete control system including the proposed current references.

TABLE II. PARAMETERS OF THE SIMULATION TEST SYSTEM.

Description	Symbol	Value
Apparent power	S_n	50 kVA
Nominal voltage	V_n	400 V
Switching frequency	f_{sw}	5 kHz
Sampling frequency	$f_{sampling}$	10 kHz
Current control loop BW	τ^{-1}	800 Hz
Output filter resistance	R_f	0.05 Ω
Output filter inductance	L_f	3 mH
DC link capacitor	C_{dc}	2500 μ F
DC link voltage	V_{dc}	1 kV
Discretization method	-	Tustin
Transformer Ratio	-	400(D)/400(YG)

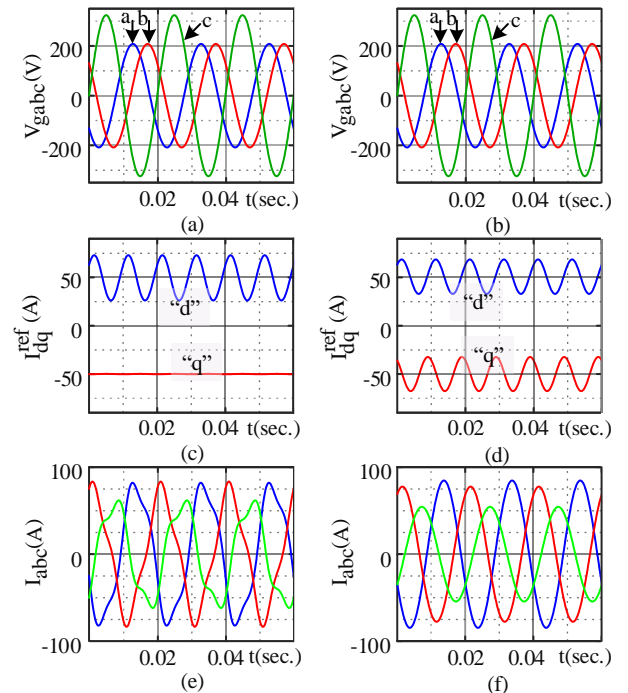


Fig. 5. Simulation results for the test system of Fig. 1 under an SLG fault with 85% voltage sag in the affected phase at the grid side of the transformer, (a)-(b) grid voltages at the inverter side of the transformer, (c)-(d) current references in the “dq” frame for the “conventional IARC” and the “proposed IARC”, respectively, (e)-(f) output three-phase currents for the “conventional IARC” and the “proposed IARC”, respectively.

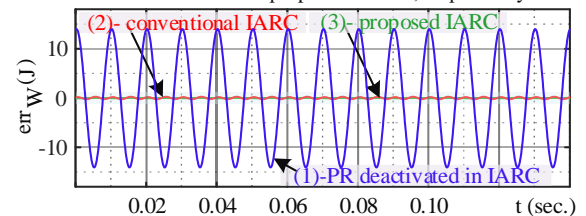


Fig. 6. $2\omega_0$ component of the DC link capacitor energy error (1) IARC is deactivated, (2), (3) the conventional IARC and proposed IARC, respectively.

TABLE III. PARAMETERS OF THE TEST SYSTEM FOR EXPERIMENTS.

Description	Symbol	Value
Apparent power	S_n	5 kVA
Nominal Voltage	V_n	400 V
ac side voltage	V_g	250 V
Switching and sampling frequency	$f_{sw}, f_{sampling}$	10 kHz
Current control loop BW	τ^{-1}	800 Hz
Output filter inductance	L_f	3 mH
DC link capacitor capacitance	C_{dc}	500 μ F
DC link voltage	V_{dc}	680 V
Controllers discretization method	-	Tustin

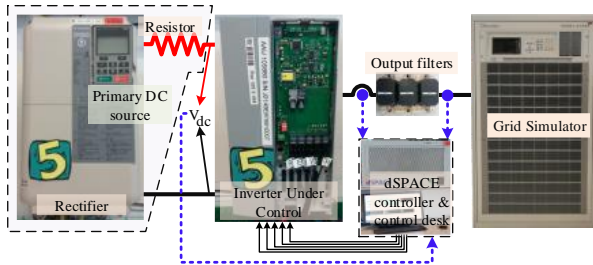


Fig. 7. Photography of test setup consisting of a 10 kVA rectifier as a dc source, a 5 kVA inverter as a grid-following inverter, a 45 kVA three-phase grid simulator.

16%-20% in this case. Fig. 5 (f) shows the performance of the proposed IARC method in removing the 3rd harmonic current components. Above all, the $2\omega_0$ components of the energy error err_W are extracted and depicted in Fig. 6 for three cases including (1) PR compensator is deactivated in IARC, (2) conventional IARC, and (3) the proposed IARC. As shown in this figure, using the conventional IARC and the proposed IARC effectively remove the $2\omega_0$ components.

VI. EXPERIMENTAL VERIFICATION

To verify the effectiveness of the proposed approach, the proposed control scheme is implemented on a test system shown in Fig. 7. In this system, a PWM rectifier in series with a resistance is used as a primary DC source in the setup available in the laboratory. The primary DC source can be regarded as a Thevenin model of the photovoltaic systems with the same V-I characteristic. The inverter under study is intended to control its DC-link voltage in this paper. By selecting a rectifier voltage higher than that of the inverter DC-link voltage set-point, active power flows from the primary DC source to the inverter (P_{in}), and correspondingly to the grid. The test system parameters are given in Table III. The DC-link capacitor energy controller is given in (14).

For the experimental test, grid simulator sets the grid positive sequence voltage V_1 to 146 V ($V_1 \approx 0.7$ p.u.), and the negative sequence voltage V_2 to 58 V which makes a severe unbalance ratio of 40% (similar to the unbalanced condition used in section V). The generated unbalanced voltages are shown in Fig. 8 (a)-(b). Considering the reactive current injection requirement of the Danish grid code [47], the reactive current set point is set to 5 A (50% of the nominal current). Also, the DC-link voltage reference is set to 645 V, and the current taken from the primary source is 1.75 A ($P_{in}=645 \times 1.75$) which makes $I_d = 5$ A for an active power injection into the grid. Since the grid is unbalanced, the DC-link capacitor energy

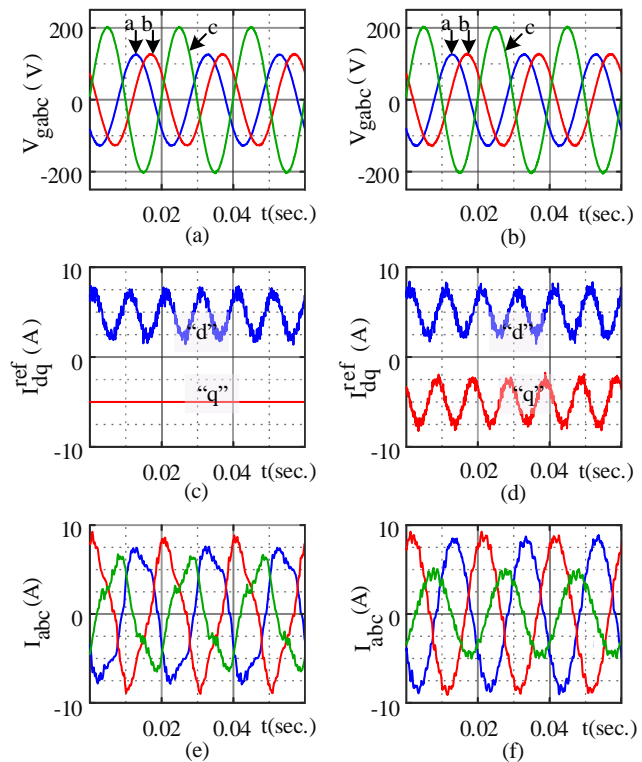


Fig. 8. Obtained experimental results for the inverter under a severe asymmetrical short circuit fault condition, (a)-(b) grid voltages produced by the grid simulator, $V_1=0.72$ p.u., the voltage unbalance ratio of 40%. (c)-(d) current references in the “dq” frame generated by the “IARC”, the “Proposed IARC”, respectively, (e)-(f) inverter output currents in the “abc” frame corresponding to the “IARC”, the “Proposed IARC”, respectively.

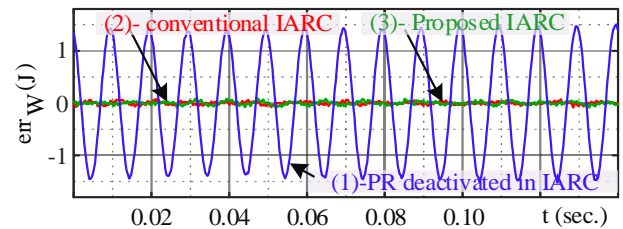


Fig. 9. Obtained experimental results, $2\omega_0$ component of the DC link capacitor energy error (1) PR compensator is deactivated in IARC, (2), conventional IARC and (3) proposed IARC.

controller regulates the DC-link voltage by producing the current references with the frequency of $2\omega_0$. The effect is reflected in the current references as shown in Fig. 8 (c)-(d), which are related to the conventional IARC and the proposed IARC, respectively. The corresponding output three-phase currents of the inverter are given in Fig. 8 (e)-(f). From these figures, the 3rd harmonic components are the main harmonic content of the output currents when the conventional IARC is utilized (see Fig. 8 (e)). The individual 3rd harmonic distortions are 16%-16%-22% for the three phases using the conventional IARC. Using the proposed IARC, the 3rd harmonic components of the currents are removed as shown in Fig. 8 (f). Above all, the $2\omega_0$ component of the DC-link capacitor energy error err_W is extracted and depicted in Fig. 9 for the conventional IARC, proposed IARC, and when the PR compensator in the IARC (see Fig. 2.) is deactivated. As it was expected, both the conventional and the proposed IARC schemes effectively remove the double frequency components. The DC-link voltage

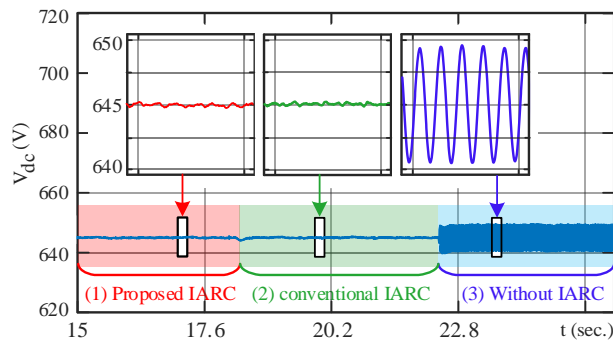


Fig. 10. Experimental results of the DC link voltage waveform showing the impact of the conventional IARC and the proposed IARC on the DC-link voltage by considering three scenarios including (1) the proposed IARC, (2) the conventional IARC, and (3) IARC is deactivated.

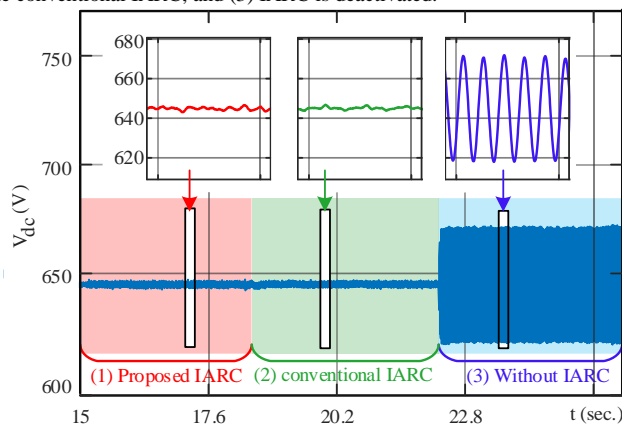


Fig. 11. Calculated DC link voltage waveform based on the experimental results of Fig. 10 in which the DC link capacitor is 100 μ F showing the impact of the conventional IARC and the proposed IARC on the voltage by considering three scenarios including (1) the proposed IARC, (2) the conventional IARC, and (3) IARC is deactivated.

waveform is depicted in Fig. 10 with a DC value of 645 V. It should be noted that this figure focuses on the $2\omega_0$ components of the DC-link voltage, and the high frequency components coming from the primary DC source is not shown in this figure. Fig. 10 shows comparative results for the three schemes of (1) the proposed IARC, (2) conventional IARC, and (3) IARC with the disabled PR compensator. The figure shows that whenever the proposed IARC and conventional IARC are activated (areas 1 & 2), the $2\omega_0$ components will be removed. Furthermore, by disabling the PR compensator in the IARC (as shown in area 3), the $2\omega_0$ component appears in the DC-link voltage as expected. Zoom-in plots are also given to compare the waveforms during the three different time intervals shown by three boxes. These three plots have the same operating conditions in which $V_{dc}=645$ V, $I_d = 5$ A, and $I_q = 5$ A.

To show the impact of the DC link capacitor value, the DC-link voltage variation is calculated for a DC-link capacitor of 100 μ F as shown in Fig. 11 using the experimental data obtained for a 500 μ F DC-link capacitor. In this respect, the DC-link capacitor energy and voltage variations are used. As it is anticipated and seen in Fig. 11, disabling the PR compensator in the IARC (area 3) leads to large $2\omega_0$ components variations in the DC-link voltage. Also, using the conventional IARC or

the proposed IARC schemes effectively removes the double frequency components from the DC-link voltage (areas 1 & 2).

VII. CONCLUSION

This paper has analyzed the control of grid-following inverters under unbalanced conditions and asymmetrical short circuit faults in the grid. A comprehensive overview on the existing methods under unbalanced conditions has been presented. The instantaneous active reactive control (IARC) method is adopted as the base for the control of the inverter under unbalanced conditions, which results in a ripple-free DC link voltage. Accordingly, the challenge associated with this scheme, which is the 3rd harmonic distortions in the output currents, has been elaborated. Then, a feed-forward based 3rd harmonic current elimination method, which is followed by a mathematical proof is proposed. In this method, the current references are corrected based on the $2\omega_0$ components of the outer loops control signals. It is shown that the output current 3rd harmonic distortion increases to about 22% for an asymmetrical fault ($V1 \approx 0.70$ p.u., and $V2/V1 \approx 40\%$ as a case) if the proposed method is not used. According to the results, the proposed IARC method enjoys the benefits of the conventional IARC scheme and also has the advantages of other schemes by producing sinusoidal positive and negative sequence current components under unbalanced conditions. The performance of the proposed method has been shown by discrete time domain simulations in the MATLAB/SIMULINK environment. Finally, experimental test results have been presented to successfully verify the functionality of the proposed method.

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