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Grid Integration of a Dual Two-Level Voltage-Source Inverter considering Grid Impedance and Phase-Locked Loop

Amir Aghazadeh, Masoud Davari*, *Senior Member, IEEE*, Hamed Nafisi, and Frede Blaabjerg, *Fellow, IEEE.*

***Abstract*—This paper proposes a dual two-level voltage-source inverter (DTL VSI) and its control to effectively integrate two dc sources into the multi-infeed ac/dc (MIACDC) power architecture of fully integrated power and energy systems (FIPESs). The current-controlled method is also synthesized and proposed to control the grid-connected DTL VSI. To this end, this article provides mathematical analyses comparing the DTL VSI with the conventional current-controlled grid-connected two-level VSIs (TL VSIs). The linearized state-space models of both systems are mathematically derived for analyzing the dynamics of both structures. These models reveal the salient feature of the proposed DTL VSIs used in grid integration. To this end, space-phasor analysis is employed, and the dynamics of the phase-locked loop (PLL) and the grid impedance are also considered. The proposed grid-connected DTL VSI (with the current-controlled algorithm) not only in weak grids (for normal grid conditions) but even after fault removal (for faulty grid conditions) stabilizes the active and reactive power dynamics with improved transient performance compared to that of its conventional counterpart. Therefore, it enhances the operation range of the VSIs integrating various entities in FIPES' MIACDC power architecture. This paper provides supportive simulation results and experiments generated by MATLAB and a scaled-down test rig, respectively.**

***Index Terms*—Dual two-level voltage-source inverter (DTL VSI), phase-locked loop (PLL) dynamics, space-phasor vector control, two-level voltage-source inverter (TL VSI), voltage-source inverter (VSI), weak grids.**

I. Introduction

Due to the significant amount of green gas emitted by human beings, and by considering its irrecoverable effects on the environment, many countries adopt renewables as an alternative to fossil fuels. Therefore, the energy sector has been significantly progressing and moving toward integrating power networks and energy storage systems, which forms the fully integrated power and energy systems (FIPESs). Energy storage systems will be mostly in the form of battery systems embedded in ac/dc grids. FIPESs use multi-infeed ac/dc (MIACDC) power systems. MIACDC simpler versions are found in super grids and meshed high-voltage direct current grids—in transmission systems—and hybrid multi-terminal ac/dc grids—in both distribution systems and modernized microgrids (MMGs) [1]. They have been employed in smart grids nowadays. In smart grids, the upgraded MIACDC concept brings many benefits to the operation, control, and demand supply within commercial power systems.

Thanks to the essential advances brought to the field of power electronics and semiconductor devices, different types of inverters are employed to connect renewables and sources to MIACDC power architecture of FIPESs [2]–[8]. Among different structures of voltage-source inverters (VSIs), dual two-level VSIs (DTL VSIs) are well-known due to its significant advantages brought in motor and drive controls (e.g., voltage THD, voltage weighted THD and switching losses, etc.) [9], [10].

The DTL VSI can be one of the up-and-coming power electronic topologies—which is employed in the FIPESs of MMGs. DTL VSIs empower an FIPES to be able to benefit from the MIACDC power systems' architecture. DTL VSI can be implemented by either a single dc source or two separate dc sources. Nonetheless, DTL VSI with two dc sources benefits from lower voltage and current THD, lack of circulating currents, and two isolated paths for transferring power to the power grid [9], [10]. The lower voltage and current THDs lead to a decrease in the cost of installation and maintenance decreases. Additionally, by utilizing two separate paths, the reliability of the system is augmented since, in case of missing one of the paths, another path is still able to transfer a portion of power. In comparison with systems containing single VSIs, DTL VSI provides some substantial benefits. For instance, with the given nominal power, this structure reduces the total manufacturing and installation cost [11]. Furthermore, DTL VSIs benefit from a higher magnitude of the output voltage with the same amount of dc-link voltage compared to VSI. This advantage reduces the turn ratio and output impedance of the transformer needed to step up the output voltage of the DTL VSI. Besides, the reliability of the system employing DTL VSI is improved because of using two paths of power supply. Therefore, inverters based on dual configurations attract more attention, and they are commonly utilized in grid-connected photovoltaic systems [11]–[14].

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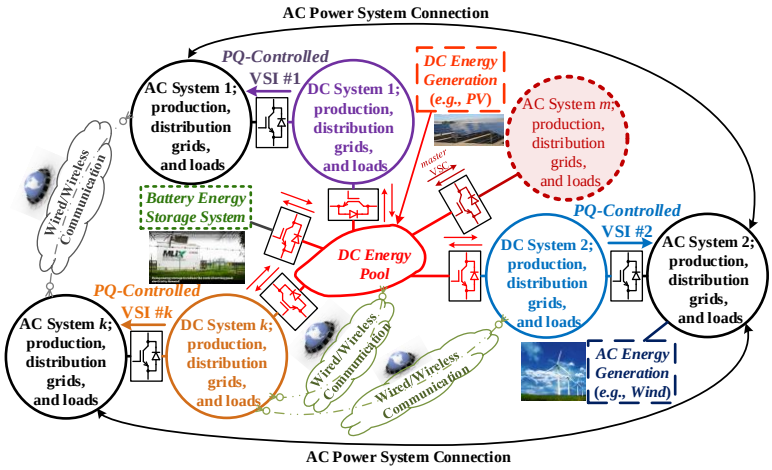

Fig. 1. Notional structure of an MIACDC power architecture.

DTL VSIs have been mainly employed in motor and drive controls so far. If DTL VSI is used in grid integration applications, its current benefits (elaborated in [2]–[14]) will be add-ons to the grids into which integrated. One fundamental example of those grids is the power network based on MIACDC architectures. Also, a significant amount of effort has been put to assess the stability of grid-connected, PQ-controlled VSIs under different grid conditions [15]–[29]. However, to the best of the authors' knowledge, the stability assessment of the grid-connected DTL VSI at a wide range of short-circuit capacity ratios (SCCRs) has not indeed and technically investigated yet. Based on these pieces of information, the contributions of this research have been listed as follows.

1) The grid-connected DTL VSI is proposed in order to be utilized as a single PQ-controlled VSI integrating two separated dc sources, which enhances the MIACDC's grid integration, effectively.

2) A simple, yet powerful current control algorithm is proposed for the PQ-controlled VSI.

3) The impacts of the grid weakness causing the instability, controller parameters, and the dynamics of the phase-locked loop (PLL) regardless of its type (see [19], [20]) on the stability of grid-connected VSIs is addressed in [23], [27]–[29]. The proposed grid-connected DTL VSI and its performance at different SCCRs and in normal and faulty grid conditions are comprehensively evaluated and demonstrate significant improvement in MIACDC's grid integration.

4) Based on the small-signal stability and eigenvalue analyses, the stability of the grid integration using grid-connected DTL VSIs is improved compared to that of conventional VSIs.

5) This research also reveals the key factors (including stability boundaries) affecting the stability of the closed-loop dynamic system formed by the proposed grid-connected DT VSI. The provided stability analysis aims to assess the stability of the grid-connected DTL VSI and TL VSI at different SCCRs when X_S/R_S equals to one (to have the worst case [26]), and the parameters of the PLL are constant.

6) It will be demonstrated that a grid-connected DTL VSI is able to enhance the integration of new upcoming dc power sources into MIACDC power systems effectively. As regards this, at different SCCRs and in normal and fault conditions, both converters have been analyzed, simulated, and experimentally tested. The results reveal that the proposed grid-connected DTL VSI is able to achieve a more extensive stable range of performance, compared to grid-connected VSIs, while having better and acceptable total harmonic distortion (THD), power quality, and losses.

The remainder of this article has been structured as follows. The system description of the grid-connected of DTL VSIs is shown in Section II. In Section III, the small-signal model and eigenvalue studies of the DTL VSIs are provided and compared with those of TL VSIs. Sections IV and V demonstrate simulation results and experiments. Section VI finally concludes this paper's outcomes.

II. System Description of Grid-Connected DTL VSIs

A notional architecture of an MIACDC's power grid (both power and communication one) has been shown in Fig. 1. As shown in Fig. 1, many power electronic links should work as PQ-controlled inverters transferring power from the dc side to the ac side, e.g., VSI #1, VSI #2, and VSI #*k* in Fig. 1.

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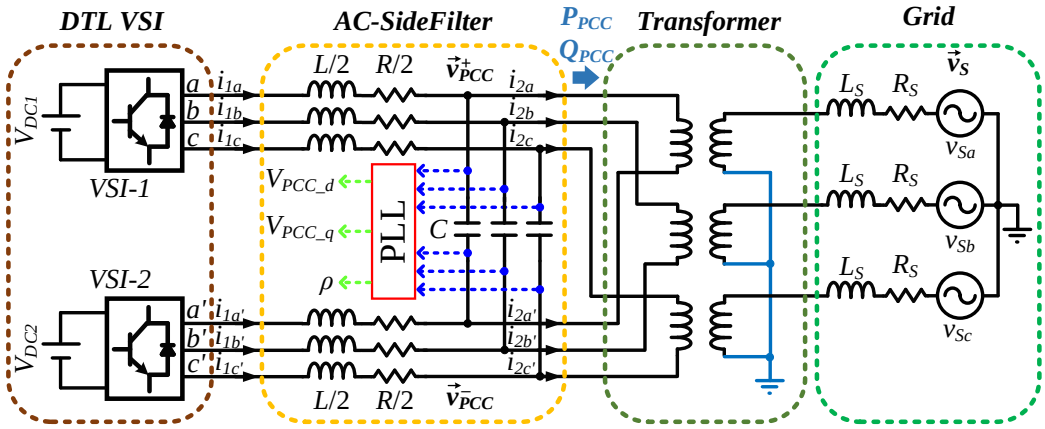

Fig. 2. A PQ-controlled, grid connected DTL VSI used in the MIACDC power grids.

A. Configuration

The DTL VSI connected to an MIACDC grid is depicted in Fig. 2, where each inverter is separately supplied by one dc source. In order to eliminate the generated harmonic contents at the output voltage of the DTL VSI, one *LC*-filter is installed. The inductance of this filter has been shown in Fig. 2 for each VSI constituting the DTL VSI; the capacitance of the aforementioned filter is *C*—shown in Fig. 2. In order to consider the resistance of the filter and that of the switch on-state, thereby increasing the accuracy of the model, a resistor is added to the system and termed by an *R*, which represents the sum of the resistance of each coil of the filter and that of the switch on-state (described by r_{on} in [19], [30]). A PLL is connected through *C* (referred to Fig. 2, the voltage between $\vec{v}^{+}_{PCC}$ and $\vec{v}^{-}_{PCC}$ is named as $\vec{v}_{PCC}$) to obtain the angle of $\vec{v}_{PCC}$, termed as ρ, to synchronize the DTL VSI with the grid.

B. Principle of Operation

As shown in Fig. 2, DTL VSI contains two conventional VSIs adjusting active and reactive powers at the point of common coupling (PCC). Therefore, based on the space-phasor control method (i.e., vector control algorithm), the output voltage of DTL VSI (i.e., the voltage between *a* and *a'*; *b* and *b'*; and *c* and *c'*), has to be controlled; their corresponding space-phasors are $+\vec{v}_{PCC}$ and $-\vec{v}_{PCC}$. An ac-side filter is employed to eliminate the switching voltage harmonics. However, since both VSIs generate voltage harmonics, two similar inductive filters have been used for each VSI. The capacitor of the filters, as can be seen, are connected between two pairs of three phases. It is noteworthy that for connecting DTL VSI to the grid, an open-ended transformer has to be employed because the number of output phases of DTL VSI is six. Nevertheless, the power network consists of three phases. While each winding of the primary side is connected between two analogous phases of each two-level VSI (e.g., between *a* and *a'*), the windings of the secondary side are connected in star, i.e., in "Y" configuration. In order to achieve the highest output voltage, as well as reduced harmonic contents in the output voltage of DTL VSI, the two VSIs of the DTL VSI should work with a 180º phase difference between their reference voltages [9], [10]. Consequently, the three reference voltages of VSI-1 are kept stationary, and the reference voltages of VSI-2 are shifted by 180º. Therefore, as soon as the reference voltages are generated and applied to VSI-1, these signals are shifted by 180º and used in VSI-2; a phase shifter, named "180-degree phase shifter" in Fig. 4, is employed to provide appropriate reference voltages for both VSIs. Furthermore, the switching pulses of each VSI are generated by conventional sinusoidal pulse width modulation (SPWM) technique.

Fig. 3 shows the principle of operation of a PQ-controlled DTL VSI. In Fig. 3, using the controller proposed in the Subsection II-B (i.e., Fig. 4, DTL VSI has undergone active power and reactive power changes, whose illustrative waveforms shown. In Fig. 3, 100% increase in active power and reactive power reference signals has been applied at t=1.5 s and t=2.5 s, respectively, while the DTL VSI's operating point is 10 kW/10 kvar for t<1.5 s. Fig. 3 has demonstrated P_{PCC}, Q_{PCC}; the magnitude and phase of space-phasors $\vec{v}_{PCC}$ and $\vec{v}_{S}$; different phase currents; and all of the modulation indices shown in Fig. 2—the data used for generating results of Fig. 3 have been reported through Table I in Appendix using SCCR=10. As stated, the modulations indices of phases *a'*, *b'*, and *c'* are the 180-degree shifted modulations indices of phases *a*, *b*, and *c*.

C. Proposed Control Structure

In this article, the current-controlled method is proposed for controlling the active power and reactive power of the PQ-controlled DTL VSI, which benefits from feedforward controls. It has been shown in Fig. 4, where V_{PCC_dn} is *d*-axis of the nominal voltage value at PCC. By employing this method, the inner control loops are responsible for adjusting the DTL VSI output currents by controlling the DTL VSI voltage in the *d*- and *q*- axes. For any control loops, based on the internal model principle in the classical control theory, proportional-integral controllers (PIs) are employed. Here, to control active power and reactive power, *d*-axis current and *q*-axis current are controlled according to the representation of the current space phasor in the *dq*-frame [30]. Also, in order to enhance the performance of the current controller, two feed-forward signals of *d*- and *q*-axis of $\vec{v}_{PCC}$ are included; the time constant of the utilized filters is *T*.

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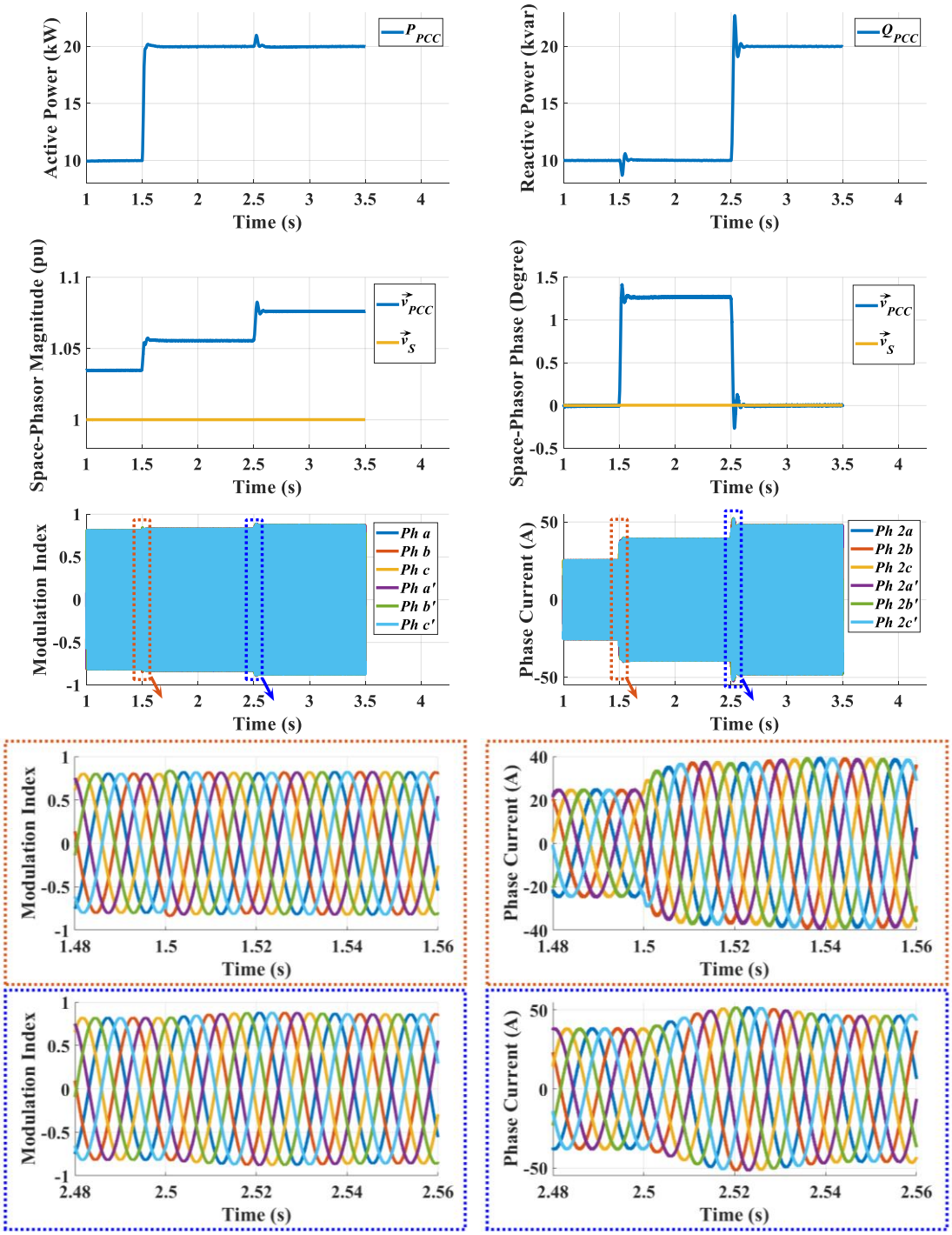

Fig. 3. A PQ-controlled DTL VSI (using the controller proposed in Fig. 4 in Subsection II-B), which has undergone active power and reactive power changes with illustrative waveforms showing the principle of operation.

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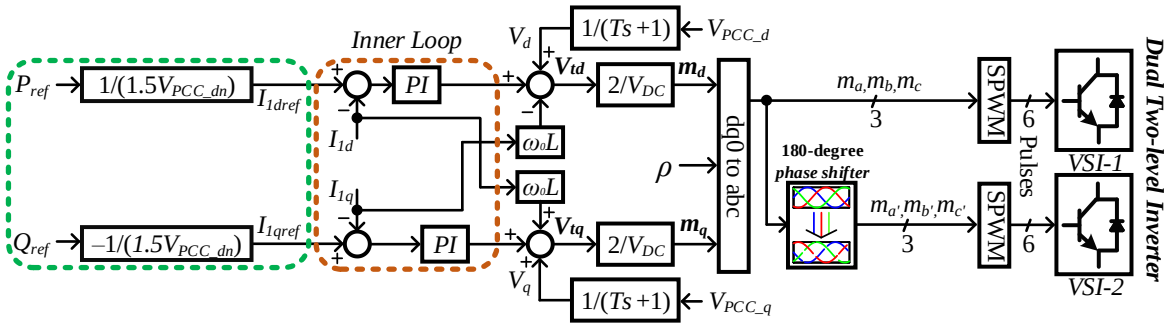

Fig. 4. The proposed control block diagram of the DTL VSI.

D. Power Network

As depicted in Fig. 2, the grid is modeled using its Thevenin's Equivalent circuit consisting of an ideal voltage, L_S, and R_S. Note that the amplitude of the voltage source is the same as the grid nominal voltage. To determine the values of passive components, the short circuit capacity (SCC) at PCC is derived using $SCC_{PCC} = SCCR \times S_{VSI}$, where S_{VSI} is the nominal power of the inverter connected to the grid, and in this article, $S_{VSI} = S_{DTL\text{-}VSI} = S_{TL\text{-}VSI}$. After calculating SCC_{PCC}, the Thevenin model impedance is derived based on $Z = \frac{V^2_{PCC-rms}}{SCC_{PCC}}$, where $V^2_{PCC\text{-}rms}$ is the rms value of the line-to-line nominal voltage at PCC. Finally, based on the assumptions mentioned in the introduction, R_S and L_S are determined as $R_S = \frac{Z}{\sqrt{2}}$ and $L_S = \frac{Z}{2\pi f\sqrt{2}}$, where f the frequency of the grid in Hz.

III. Eigenvalue Analysis of the Grid-Connected DTL VSIs

In order to evaluate grid-connected DTL VSIs and compare their performance with other commonly used VSIs' performance, the state-space model of the whole closed-loop system is required. For doing so, different parts of the system are considered, and their corresponding equations are derived. These parts include ac-side dynamics, control system, and the PLL.

A. AC-Side Dynamics in the dq-Frame

By employing the *dq*-frame representation of related space-phasors [30], the dynamics of interest in the three-phase *abc* frame are transformed into *dq*-frame. It should be pointed out that the voltage in the *d*-axis is in the in-phase with V_{PCC}. The dynamics of the grid-connected DTL VSI explained in Fig. 2 are formulated by (1)–(6) based on the equivalent circuit of the system. The equivalent circuit is depicted in Fig. 5. In (1)–(6), subscripts *d* and *q* represent the quantities in the *d*- and *q*-axes, and "1" and "2" show the currents of the inverter and grid sides, respectively. Besides, *L*, *R*, and *C*; and L_S and R_S are the inductance, its resistance, and the capacitance of the related *LC*-filter; and the equivalent inductance and the equivalent resistance of the grid, respectively. It is noteworthy that since both converters of the DTL VSI work with the same modulation index (MI)—but with the 180° phase difference—the output

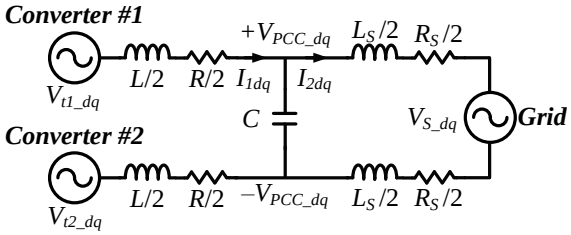

Fig. 5. Equivalent average model of the grid-connected DTL VSI.

voltages of each VSI in the *dq*-frame are $V_{t1d} = -V_{t2d} = V_{td}$ and $V_{t1q} = -V_{t2q} = V_{tq}$.

$$L\frac{dI_{1d}}{dt} = 2V_{td} - V_{PCC\_d} + L\omega(t)I_{1q} - RI_{1d}, \tag{1}$$

$$L\frac{dI_{1q}}{dt} = 2V_{tq} - V_{PCC\_q} - L\omega(t)I_{1d} - RI_{1q}, \tag{2}$$

$$L_S\frac{dI_{2d}}{dt} = V_{PCC\_d} - V_{S\_d} + L_S\omega(t)i_{2q} - R_S I_{2d}, \tag{3}$$

$$L_S\frac{dI_{2q}}{dt} = V_{PCC\_q} - V_{S\_q} - L_S\omega(t)i_{2d} - R_S I_{2q}, \tag{4}$$

$$C\frac{dV_{PCC\_d}}{dt} = I_{1d} - I_{2d} + C\omega(t)V_{PCC\_q}, \tag{5}$$

$$C\frac{dV_{PCC\_q}}{dt} = I_{1q} - I_{2q} - C\omega(t)V_{PCC\_d}, \tag{6}$$

where V_{S_d} is the *d*-component of the grid's Thévenin-equivalent voltage; V_{S_q} is the *q*-component of the grid's Thévenin-equivalent voltage; V_{td} is the *d*-component of the terminal voltage; V_{tq} is the *q*-component of the terminal voltage; V_{PCC_d} is the *d*-component of the PCC voltage (and V_d is its filtered signal using a filter with the time constant of *T*); V_{PCC_q} is the *q*-component of the PCC voltage (and V_q is its filtered signal using a filter with the time constant of *T*); I_{1d} is the *d*-component of the ac-side current of VSI-1, which is passing through the inductance *L*; I_{1q} is the *q*-component of the ac-side current of VSI-1, which is passing through the inductance *L*; I_{2d} is the *d*-component of the ac-side current of the grid; I_{2q} is the *q*-component of the ac-side current of the grid; *L* is the inductance of the filter; *R* is the sum of the resistance of the

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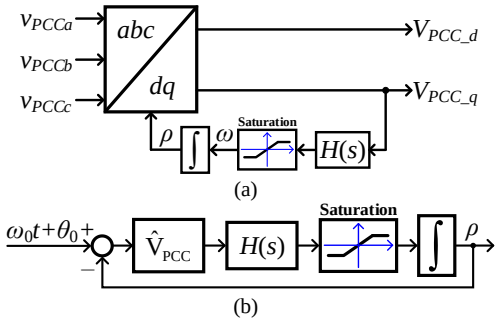

Fig. 6. (a) Implementation of PLL; and (b) linearized model of PLL.

filter and that of the switch on-state (r_{on} in [30]); C is the capacitance of the filter; L_S is grid inductance; R_S is grid resistance; and $\omega(t)$ is the angular frequency of the grid—all have been demonstrated in Fig. 2 and Fig. 5.

It is noteworthy that (1)–(6) describes the dynamics of a "PQ-controlled" dual two-level voltage-source "inverters" transferring power from dc sources to an ac grid—not dc-voltage power ports built by DTL VSIs (e.g., [18]). Therefor dc voltage is externally controlled by other entities' control loops for the dc-voltage; that is why the word "converter" has not been used like what is in [18], [19], and the word "inverter" has been adopted similar to [20]. Moreover, two first-order low pass filters are utilized in the control block diagram in order to remove the high-frequency switching noise. The inputs of those filters are V_{PCC_d} and V_{PCC_q}, and the outputs are V_d and V_q, respectively; the time constant of the filter employed is T as well.

Since the control structure uses two PI controllers in its most inner loops, two sets of dynamics are considered, which are written by (7) and (8). In this paper, the DTL VSI works in active and reactive power control mode (i.e., PQ Control). Consequently, the reference signals for active and reactive powers (P_{ref} and Q_{ref} in Fig. 4) generates the reference currents in the dq-frame (i.e., i_{1dref} and i_{1qref}).

$$\frac{dx_1}{dt} = I_{1dref} - I_{1d}, \tag{7}$$

$$\frac{dx_2}{dt} = I_{1qref} - I_{1q}, \tag{8}$$

where x_1 and x_2 are the states associated with two inner loop's PI controllers assigned to the d- and q- channels, respectively. As regards this, x_1 is the integrator outputs of the PI controllers assigned to the d-channel, and x_2 is that of the PI controllers assigned to the q-channel.

Since the average ac output voltage of the DTL VSI is proportional to the production of MI and dc voltage, V_{td} and V_{tq} are found as follows by considering Fig. 4.

$$V_{td} = K_{II}x_1 + K_{PI}I_{1dref} - K_{PI}I_{1d} + V_d - L\omega(t)I_{1q} + RI_{1d}, \tag{9}$$

$$V_{tq} = K_{II}x_2 + K_{PI}I_{1qref} - K_{PI}I_{1q} + V_q + L\omega(t)I_{1d} + RI_{1q}, \tag{10}$$

where K_{PI} and K_{II} are the proportional and integral coefficients of the current controllers, respectively.

B. PLL Dynamics

The linearized model of PLL is depicted in Fig. 6. In practice, $H(s)$ can be any transfer function—which is able to stabilize the closed-loop dynamics shown in Fig. 6. However, in this study, $H(s)$ is selected to be an industrially accepted controller, which is the proportional-integral-derivative (PID) controller described by (11); see [19], [30] and the references therein.

$$H(s) = \frac{K_D s^2 + K_P s + K_I}{s}, \tag{11}$$

where K_D, K_P, and K_I are derivative, proportional and integral coefficients, respectively.

It is noteworthy that this analysis can easily be generalized to other types of PLL controllers. However, it needs related mathematical manipulations to find its state-space model—which is similar to the way performed for the PID controller here. For the state-space model of the PID controller, the "diagonal" canonical form is employed. As a result, the PLL state-space model is represented by (12) and (13).

$$\frac{dx_{1PID}}{dt} = -\alpha x_{1PID} + V_{PCC\_q}, \tag{12}$$

$$\frac{dx_{2PID}}{dt} = -\beta x_{2PID} + V_{PCC\_q}, \tag{13}$$

where x_{1PID} and x_{2PID} are the states associated with two PLL PID controllers; and α and β are constants making the degree of the numerator of (11) equal to that of the denominator of (11)—thus making a "proper" transfer function. Thereby, it is possible to benefit from the diagonal canonical form of (11).

By using a diagonal canonical form, the angular frequency (ω) and phase angle (ρ) generated by the PLL are as follows.

$$\frac{d\rho}{dt} = \omega(t) = C_1 x_{1PID} + C_2 x_{2PID} + \frac{K_D}{\beta} V_{PCC\_q}, \tag{14}$$

where C_1 and C_2 are achieved from (15) and (16), respectively.

$$C_1 = \left.\frac{K_D s^2 + K_P s + K_I}{\beta s + 1}\right|_{s=-\alpha}. \tag{15}$$

$$C_2 = \left.\frac{\frac{K_D}{\beta}s^2 + \frac{K_P}{\beta}s + \frac{K_I}{\beta}}{s+\alpha}\right|_{s=-\frac{1}{\beta}}. \tag{16}$$

C. State-Space Model of Grid-Connected DTL VSIs

For evaluating the stability of the grid-connected DTL VSI, the linearized state-space model of the system is obtained. In this regard, all nonlinear equations are linearized around the given operating point and arranged in the form of $\Delta\dot{X} = A\Delta X + B\Delta U$. Therefore, the linear state-space model of the grid-connected DTL VSI is given in (17). It is in the form of $\Delta\dot{X} = A\Delta X + B\Delta U$—in which the state and input matrices, i.e., A and B, are equal to $M^{-1}A_d$, and $M^{-1}B_d$.

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$$\begin{bmatrix} \Delta\dot{x}_1 \\ \Delta\dot{x}_2 \\ \Delta\dot{i}_{1d} \\ \Delta\dot{i}_{1q} \\ \Delta\dot{i}_{2d} \\ \Delta\dot{i}_{2q} \\ \Delta\dot{v}_{PCC\_d} \\ \Delta\dot{v}_{PCC\_q} \\ \Delta\dot{v}_d \\ \Delta\dot{v}_q \\ \Delta\dot{\rho} \\ \Delta\dot{x}_{1PID} \\ \Delta\dot{x}_{2PID} \end{bmatrix} = M^{-1}A_d \begin{bmatrix} \Delta x_1 \\ \Delta x_2 \\ \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \\ \Delta v_{PCC\_d} \\ \Delta v_{PCC\_q} \\ \Delta v_d \\ \Delta v_q \\ \Delta\rho \\ \Delta x_{1PID} \\ \Delta x_{2PID} \end{bmatrix} + M^{-1}B_d \begin{bmatrix} i_{1dref} \\ i_{1qref} \end{bmatrix} = M^{-1} \begin{bmatrix} A_{d11} & A_{d12} \\ A_{d21} & A_{d22} \end{bmatrix} \begin{bmatrix} \Delta x_1 \\ \Delta x_2 \\ \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \\ \Delta v_{PCC\_d} \\ \Delta v_{PCC\_q} \\ \Delta v_d \\ \Delta v_q \\ \Delta\rho \\ \Delta x_{1PID} \\ \Delta x_{2PID} \end{bmatrix} + M^{-1} \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 2K_{PI} & 0 \\ 0 & 2K_{PI} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{1dref} \\ i_{1qref} \end{bmatrix}, \tag{17}$$

where M, A_{d11}, A_{d12}, A_{d21}, and A_{d22} are formulated by (A1)–(A5) in Appendix. In (A1)–(A5), Δ with "small letters" show the small-signal variation of the related variables; the subscript "0" denotes the equilibrium point of the corresponding state variable; $V_{LL\text{-}rms}$ is the line-to-line rms voltage of the grid, and α_0 is the phase difference between steady-state sinusoidal space-phasors $\vec{\boldsymbol{v}}_{\boldsymbol{PCC}}$ and $\vec{\boldsymbol{v}}_{\boldsymbol{s}}$.

The linearized model has been validated by comparing its time-domain simulation with that of nonlinear switching experiments. For doing the model verification, a 10% increase in active power and reactive power reference signals has been applied separately, while the DTL VSI's operating point is 0.33 per unit (pu)/0.33 pu. Fig. 7 and Fig. 8 show the aforementioned validation results—the scaled-down test rig used for model validation in Fig. 7 and Fig. 8 has been thoroughly described in Subsection V-A. The whole signals of V_{PCC_d} and V_{PCC_q} have been shown in Fig. 8(a), and in order to be able to demonstrate the dynamic performance of Fig. 8(a) accurately, its dc signal has been removed in Fig. 8(b).

D. State-Space Model of Grid-Connected TL VSIs

For comparing the grid-connected DTL VSI with a conventional system containing two-level VSIs, the linearized model of the grid-connected two-level VSI (grid-connected TL VSI) is derived. Although a similar control block diagram can be used for both inverter structures, for grid-connected two-level VSI (TL VSI), the control block diagram should generate pulses only for one VSI. As a result, the 180º shifter is omitted (see Fig. 4). Furthermore, the equivalent circuit is completely different for the grid-connected TL VSI. This circuit is depicted in Fig. 9. Based on the equations obtained from this figure, the linearized state-space model of the grid-connected TL VSI is described by (18). Similar to the DTL VSI, the state matrix of (18) consists of four matrices. It is noteworthy that two matrices—i.e., A_{t11} and A_{t12}—are not equal to A_{d11} and A_{d12}; however, two other matrices named as A_{t21} and A_{t22} are exactly analogous to their counterparts in A_d, which are termed as A_{d21} and A_{d22}. A_{t11} and A_{t12} are expressed by (A6) and (A7) in Appendix, respectively. Moreover, the matrix N is exactly the same as its counterpart in (17), which is termed as M. Note that, in (18) and (A1)–(A8) in Appendix, Δ, the subscript "0," V_m, and α_0 are the same as those defined in (A1)–(A5).

$$\begin{bmatrix} \Delta\dot{x}_1 \\ \Delta\dot{x}_2 \\ \Delta\dot{i}_{1d} \\ \Delta\dot{i}_{1q} \\ \Delta\dot{i}_{2d} \\ \Delta\dot{i}_{2q} \\ \Delta\dot{v}_{PCC\_d} \\ \Delta\dot{v}_{PCC\_q} \\ \Delta\dot{v}_d \\ \Delta\dot{v}_q \\ \Delta\dot{\rho} \\ \Delta\dot{x}_{1PID} \\ \Delta\dot{x}_{2PID} \end{bmatrix} = N^{-1}A_t \begin{bmatrix} \Delta x_1 \\ \Delta x_2 \\ \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \\ \Delta v_{PCC\_d} \\ \Delta v_{PCC\_q} \\ \Delta v_d \\ \Delta v_q \\ \Delta\rho \\ \Delta x_{1PID} \\ \Delta x_{2PID} \end{bmatrix} + N^{-1}B_t \begin{bmatrix} i_{1dref} \\ i_{1qref} \end{bmatrix} = N^{-1} \begin{bmatrix} A_{t11} & A_{t12} \\ A_{t21} & A_{t22} \end{bmatrix} \begin{bmatrix} \Delta x_1 \\ \Delta x_2 \\ \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \\ \Delta v_{PCC\_d} \\ \Delta v_{PCC\_q} \\ \Delta v_d \\ \Delta v_q \\ \Delta\rho \\ \Delta x_{1PID} \\ \Delta x_{2PID} \end{bmatrix} + N^{-1} \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ K_{PI} & 0 \\ 0 & K_{PI} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{1dref} \\ i_{1qref} \end{bmatrix}, \tag{18}$$

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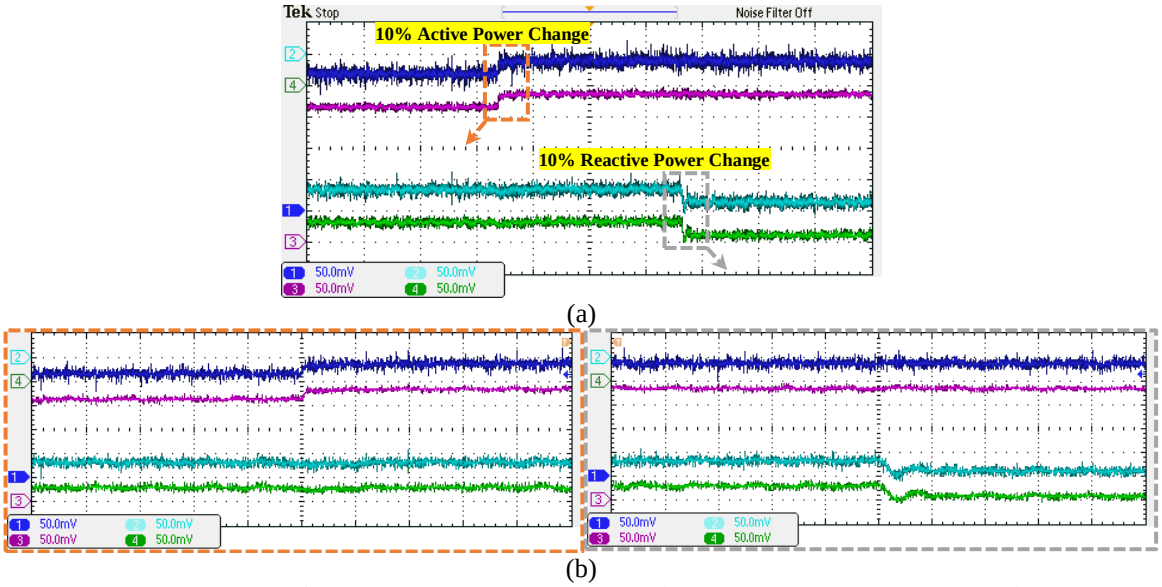

Fig. 7. Linearized state-space model validation of the DTL VSI by comparing the results of the linearized model and the response of experimental setup detailed in Subsection V-A (a) the whole picture (200 ms/div), and (b) the enlarged view of part (40 ms/div) (a), showing I_{1d} (Channel 1 in dark blue for the experiments and Channel 3 in dark magenta for the linearized model with 2.12 A/div) and I_{1q} (Channel 2 in cyan for the experiments and Channel 4 in lawn green for the linearized model with 2.12 A/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu.

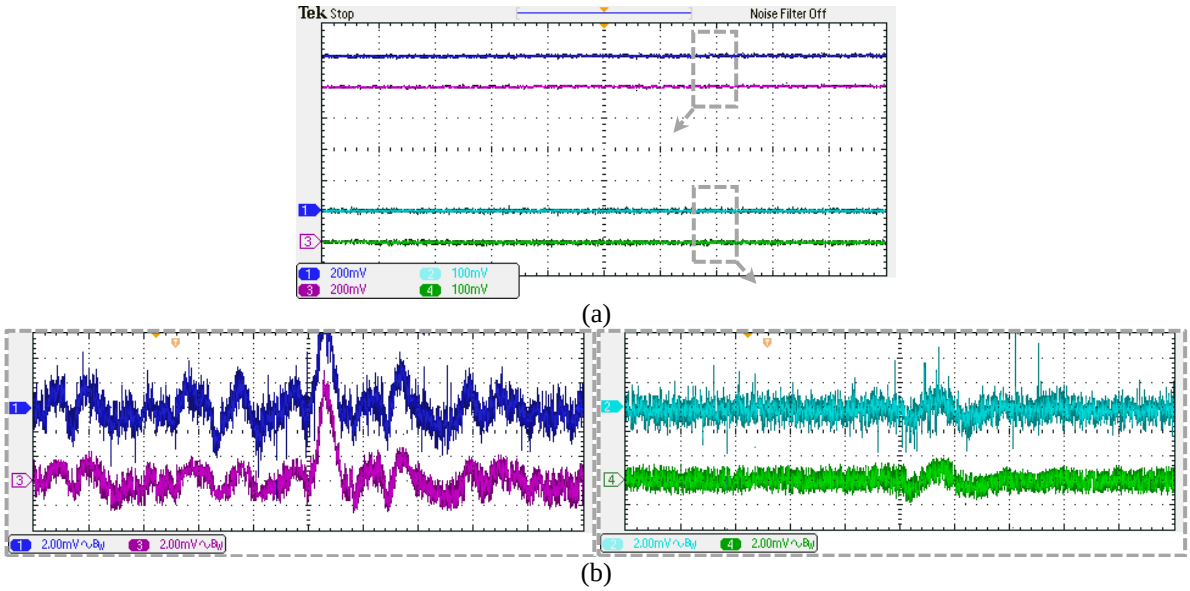

Fig. 8. Linearized state-space model validation of the DTL VSI by comparing the results of the linearized model and the response of experimental setup detailed in Subsection V-A (a) the whole picture (200 ms/div), showing V_{PCC_d} (Channel 1 in dark blue for the experiments and Channel 3 in dark magenta for the linearized model with 33.96 V/div) and V_{PCC_q} (Channel 2 in cyan for the experiments and Channel 4 in lawn green for the linearized model with 33.96 V/div); and (b) the enlarged view of the "*ac signal*" of part (a) (0.34 V/div with 20 ms/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu.

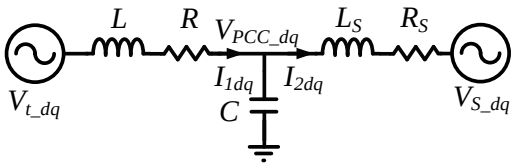

Fig. 9. Equivalent average model of the grid-connected TL VSI.

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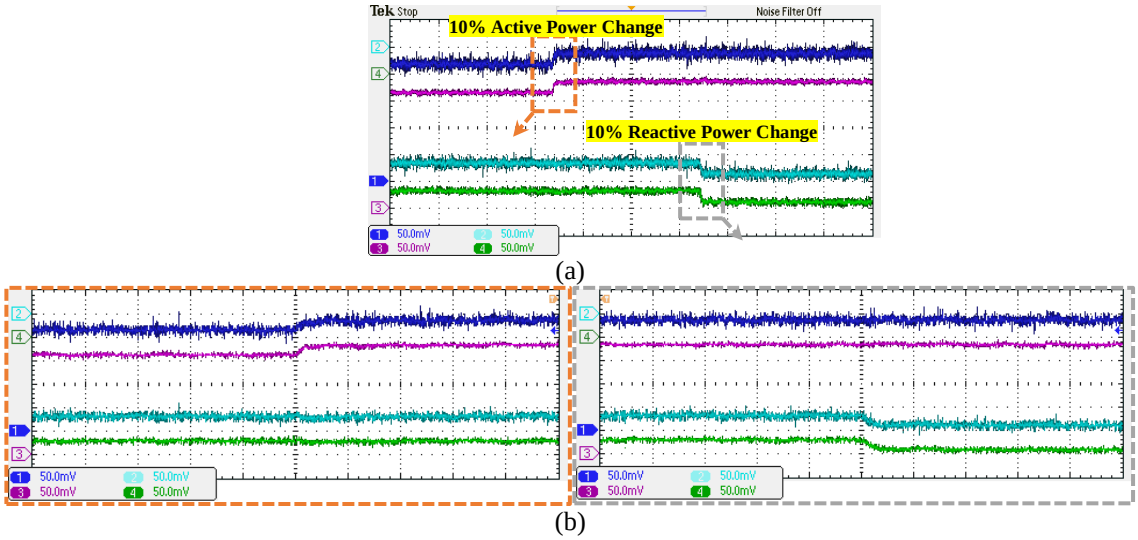

Fig. 10. Linearized state-space model validation of the DTL VSI by comparing the results of the linearized model and the response of experimental setup detailed in Subsection V-A (a) the whole picture (200 ms/div) and (b) the enlarged view of part (40 ms/div) (a), showing I_{1d} (Channel 1 in dark blue for the experiments and Channel 3 in dark magenta for the linearized model with 2.12 A/div) and I_{1q} (Channel 2 in cyan for the experiments and Channel 4 for the linearized model in lawn green with 2.12 A/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu.

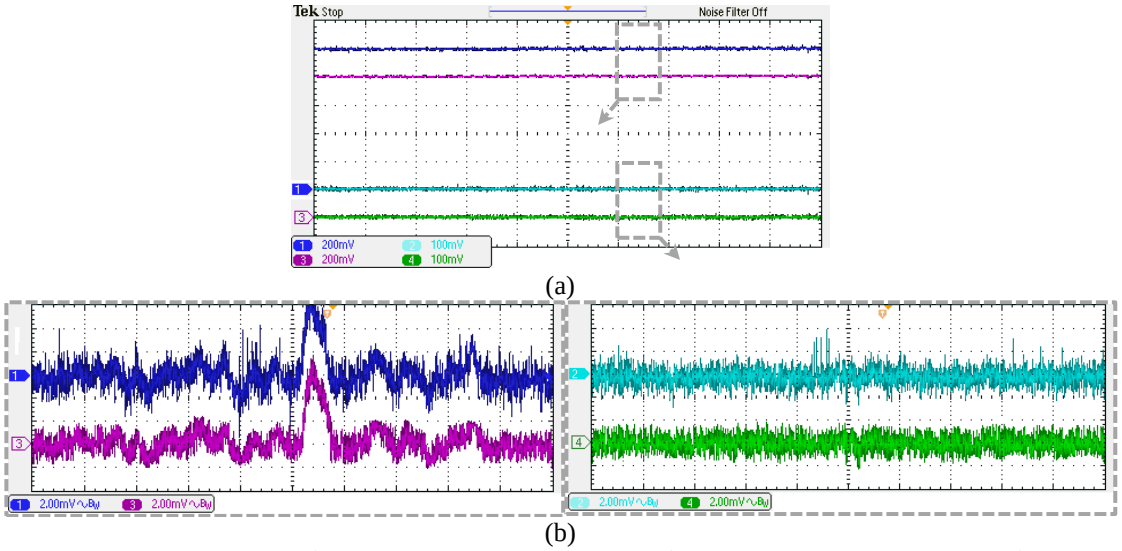

Fig. 11. Linearized state-space model validation of the DTL VSI by comparing the results of the linearized model and the response of experimental setup detailed in Subsection V-A (a) the whole picture (200 ms/div), showing V_{PCC_d} (Channel 1 in dark blue for the experiments and Channel 3 in dark magenta for the linearized model with 33.96 V/div) and V_{PCC_q} (Channel 2 in cyan for the experiments and Channel 4 for the linearized model in lawn green with 33.96 V/div); and (b) the enlarged view of only "*ac signal*" of part (a) (0.34 V/div with 40 ms/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu.

The linearized model of (18) has been validated by comparing its time-domain simulation with that of nonlinear switching experiments. For doing the model verification, a 10% increase in active power and reactive power reference signals has been applied, while the DTL VSI's operating point is 0.33 pu/0.33 pu. Fig. 10 and Fig. 11 show the aforementioned validation results—the scaled-down test rig used for model validation in Fig. 10 and Fig. 11 has been thoroughly described in Subsection V-A. The whole signals of V_{PCC_d} and V_{PCC_q} have been shown in Fig. 11(a), and in order to be able to demonstrate the dynamic performance of Fig. 11(a) accurately, its dc signal has been removed in Fig. 11(b).

E. Eigenvalue Analysis and Sensitivity Analysis

The closed-loop system's eigenvalues representing all states are found by (17)—for the system formed by a DTL VSI—and by (18)—for the system formed by a TL VSI. A sensitivity analysis is performed when the SCCR is changed from 10 (whose resulting eigenvalues are shown by green "*downward-pointing triangles*") to 1 (whose resulting eigenvalues are shown by red *downward-pointing triangles*) for both cases of DTL VSI and TL VSI—as it is demonstrated in Fig. 12 and Fig. 13. For producing those simulations, the data in Table I in Appendix have been used. In those figures, the resulting eigenvalues for 1<SCCR<10 are shown by blue "*crosses*."

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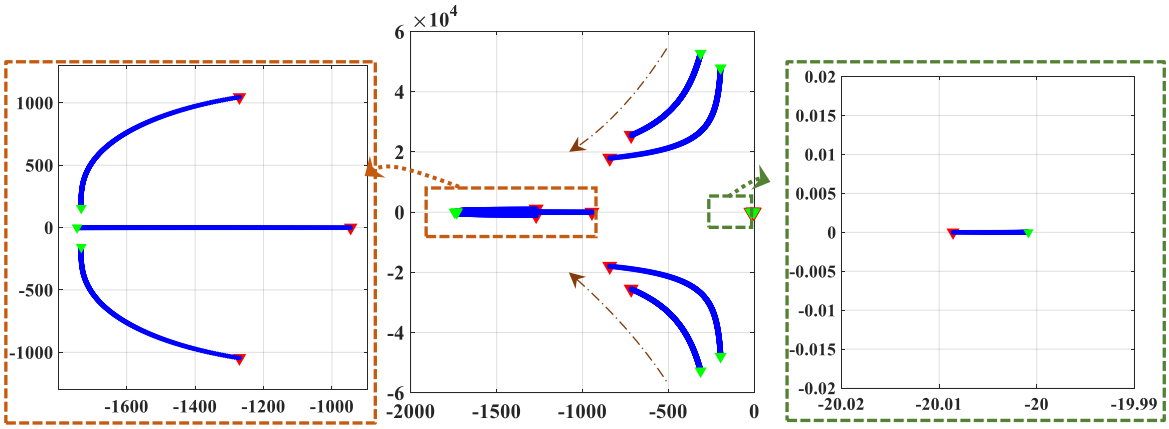

Fig. 12. Eigenvalue analysis associated with the DTL VSI—all eigenvalues including enlarged views.

Therefore, the traces start with green *downward-pointing triangles* going to red *downward-pointing triangles*—associated with the SCCR, which varies from 10 to 1.

It is noteworthy that the controllers of both current loops and PLL have been synthesized with an adequate margin of stability criteria and acceptable performances. In this regard, by considering Fig. 6(b) and Table I in Appendix and following the methods detailed in [18]–[20], [30], it will be revealed that the PLL controller has induced 90° phase margin. Using the same data reveals that the time constants τ_c of both structures have been set to 1 ms, thus resulting in the current closed-loop bandwidth of $\omega_c=1/\tau_c=1000$ rad/s. ω_c should be considerably smaller (i.e., 10 times, which is almost 51 times in this paper) than the switching frequency of the VSI (in rad/s)—which is an important requirement for PWM-based VSIs.

Comparing Fig. 12 and Fig. 13 reveals that the eigenvalues associated with the closed-loop system formed by the DTL VSI are further located in the left half-plane (LHP) with respect to the $j\omega$-axis. Therefore, Fig. 12 and Fig. 13 have demonstrated that the closed-loop dynamic system formed by the DTL VSI is more stable than the closed-loop dynamic system formed by the TL VSI—since DTL VSI pushes the LHP closed-loop eigenvalues further left with respect to the $j\omega$-axis. On top of the purely mathematical eigenvalue analysis, another rationale (which is based on the physics of the problem) is as follows. Indeed, the 180-degree phase shifter employed in generating voltages a', b', and c' of the VSI-2 in the DTL VSI (shown in Fig. 3 and Fig. 4) effectively and internally cancels some of the DTL VSI's ac-side's dynamics. This phenomenon does not happen in TL VSIs.

It should be pointed out that based the above-mentioned discussions, bad performances, instability, and eigenvalue variations will not be triggered by bad tuning of either the current control loops or the PLL; in this article, they are only coming from the ac grid impedance (regarded as grid weakness), which will be linked through PLL dynamics because all loops have been appropriately tuned in order to avoid "bad tuning problems."

F. Boundaries of Stability Limit

For both DTL VSI and TL VSI, V_{t_dq} is connected to MI with the PWM nonlinear characteristic; for example, see [31]. According to that nonlinear characteristic, in the linear region of 0 < MI <1, $\frac{\hat{V}}{V_{dc}}$ is linearly varying concerning modulation index (MI), however, for MI > 1, i.e., in over-modulation, $\frac{\hat{V}}{V_{dc}}$ can only increase up to $4/\pi$ non-linearly. For transferring a specific amount of active power P and reactive power Q in equivalent circuits depicted in Fig. 5 and Fig. 9, $\frac{\hat{V}}{V_{dc}}$ is accordingly changed. Consequently, $\frac{\hat{V}}{V_{dc}}$ is derived based on other parameters such as P, Q, $V_{LL\text{-}rms}$ (secondary line-to-line rms voltage), V_{dc}, and the impedance of the system, i.e., z. By applying Kirchhoff's voltage law (i.e., KVL), (19a) and (19b) are derived for calculating $\frac{\hat{V}}{V_{dc}}$ based on other parameters of the related equivalent circuits.

where z and θ are the magnitude and angle of the related impedance utilized between two sources containing the impedance of the filter and the grid for DTL VSI and TL VSI, respectively.

For different SCCRs—ranging from 10 (for the strongest grid) to 1 (for the weakest grid) by changing R_S and L_S (all parameters are tabulated in Table I in Appendix)—and for P=20 kW and Q=20 kvar, $\frac{\hat{V}}{V_{dc}}$ of both structures has been demonstrated in Fig. 14 by means of switching model (noted by "-S") and equivalent circuit models (indicated by "-E").

Based on Fig. 14, it can be seen that TL VSIs suffer from an inability to synthesize the voltage to transfer active and reactive powers at low SCCRs because $\frac{\hat{V}}{V_{dc}}>4/\pi$. In other words, for those SCCRs, TL VSIs are not capable of synthesizing the required voltage. While the limit for TL VSI's operation is SCCR=3.6 based on the analysis of the equivalent circuit, this number for switching model is 2.6. The main reason for this difference at lower SCCRs is 1) the PLL's impact, which we cannot simply model and consider in the equivalent circuit, thereby playing a significant role at low

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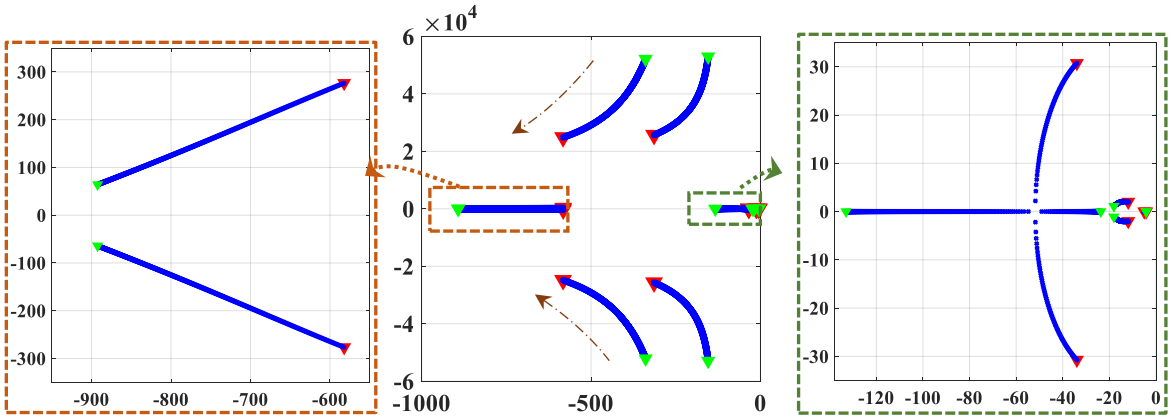

Fig. 13. Eigenvalue analysis associated with the TL VSI—all eigenvalues including enlarged views.

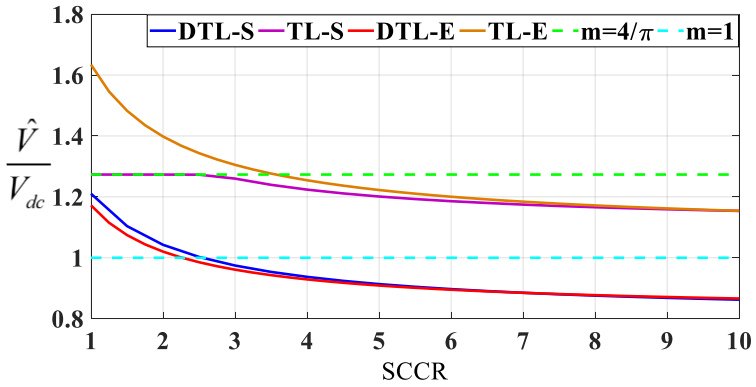

Fig. 14. $\frac{\hat{V}}{V_{dc}}$ for different SCCRs associated with switching and equivalent models (for both DTL VSI and TL VSI).

$$\frac{1}{z^2}(V_{dc})^4\left(\frac{\hat{V}}{V_{dc}}\right)^4-\left[\frac{2P\cos\ \theta}{z}+\frac{2Q\sin\ \theta}{z}+\frac{\left(\sqrt{2}V_{LL-rms}\right)^2}{z^2}\right](V_{dc})^2\left(\frac{\hat{V}}{V_{dc}}\right)^2+\left(P^2+Q^2\right)=0,\quad \text{for DTL VSI} \tag{19a}$$

$$\frac{1}{z^2}\left(\frac{V_{dc}}{2}\right)^4\left(\frac{\hat{V}}{V_{dc}}\right)^4-\left[\frac{2P\cos\ \theta}{z}+\frac{2Q\sin\ \theta}{z}+\frac{\left(\sqrt{\frac{2}{3}}V_{LL-rms}\right)^2}{z^2}\right]\left(\frac{V_{dc}}{2}\right)^2\left(\frac{\hat{V}}{V_{dc}}\right)^2+\left(P^2+Q^2\right)=0,\quad \text{for TLVSI} \tag{19b}$$

SCCRs; 2) the PWM nonlinear characteristic, which is not implementable in the equivalent circuit; and 3) the small amount of reactive power injected by the ac-side switching filter.

Last not least, as shown above, the stability boundaries of the TL VSI has been met during the aforementioned range of operation, under which DTL VSI is controllable. In other words, the TL VSI is not even controllable under some of the range of operation. Next section will show that Fig. 14 is valid and demonstrate that at SCCR=2.6, TL VSI is not able to control active power and reactive power.

IV. Simulation Results

The grid-connected DTL VSI shown in Fig. 2 is simulated in MATLAB Simulink in order to investigate the performance of this system. All required data have been tabulated in Table I in Appendix and also explained here. The DTL VSI is connected to a 60 Hz, 260 V ac grid where the voltage is stepped up to 25 kV via an open-ended transformer with a turn ratio of 1:96.15. The short circuit ratio of the power network at SCCR=1 equals to 30 kVA. The VSIs of DTL VSI are controlled separately with 8,100 Hz switching frequency. Each VSI is connected to

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an isolated 500 V dc source. The current-controlled DTL VSI is depicted in Fig. 4. For the ac-side filter, 2.4 mH inductance with 0.01 Ω resistance, as well as 1μF capacitance, is utilized. It is noteworthy that in order to compare this system with the conventional ones, the grid-connected TL VSI is assumed and implemented in the same environment with similar parameters tabulated in Table I in Appendix. Thus, the aforementioned VSI is connected to the same grid (but with a regular Yd1 three-phase transformer in this case) with the turn ratio of 1:96.15—similar to that of the open-ended transformer in the DTL VSI case.

A. PQ-Controlled DTL VSI

The grid-connected DTL VSI's performances associated with tracking active/reactive power reference signals at different SCCRs are demonstrated in Fig. 15 and Fig. 16. In these figures, the reference signals have been shown by blue traces, and the output signals are depicted by red traces (for the proposed controller with the feedforward signals) and orange traces (for the controller without the feedforward signals). Orange traces indeed reveal that the feedforward in the proposed control is able to improve its performance—especially for the low SCCRs—by removing coupling signals.

From 0.0 s to 0.5 s, the VSI has been set to inject 0 kW and 0 kvar so that all initial conditions' impacts on the simulation results diminish. Afterward, at 0.5 s, the active power reference changes from 0 kW to 10 kW; at 0.8 s, the reactive power reference varies from 0 kvar to 10 kvar; at t=1.3 s, the active power reference changes from 10 kW to 20 kW; and finally, at t=1.6 s, the reactive power reference varies from 10 kvar to 20 kvar—all by step functions. From Fig. 15, it is evident that not only at high SCCRs but also at very low SCCRs like SCCR=1.50, the grid-connected DTL VSI is able to track the active power reference. For SCCR=1, it is also able to do so, but with more oscillations—for removing them, we can design separate controllers [19]. However, by a decrease in SCCR, the system needs more time to damp the generated oscillation after stepping up the reference values at t=1.3 s and t=1.6 s; this is because of having the eigenvalues, which are more closed to the $j\omega$-axis—for improving them, separate optimal controllers can be synthesized by separate research if required [19]. A similar response is also seen in Fig. 16. The grid-connected DTL VSI is capable of responding to the reactive power demanded. Nevertheless, similar to Fig. 15, after any changes in reference values, the magnitude of the oscillation increases by decreasing the SCCR. At SCCR=1, the highest oscillations in the active and reactive powers are observed. It can also be seen that at this SCCR with the highest reference values—i.e., at 20 kW and 20 kvar—the magnitude of the oscillations is intensified. As a result, the system requires 0.7 s to damp the oscillation and track the reference values perfectly.

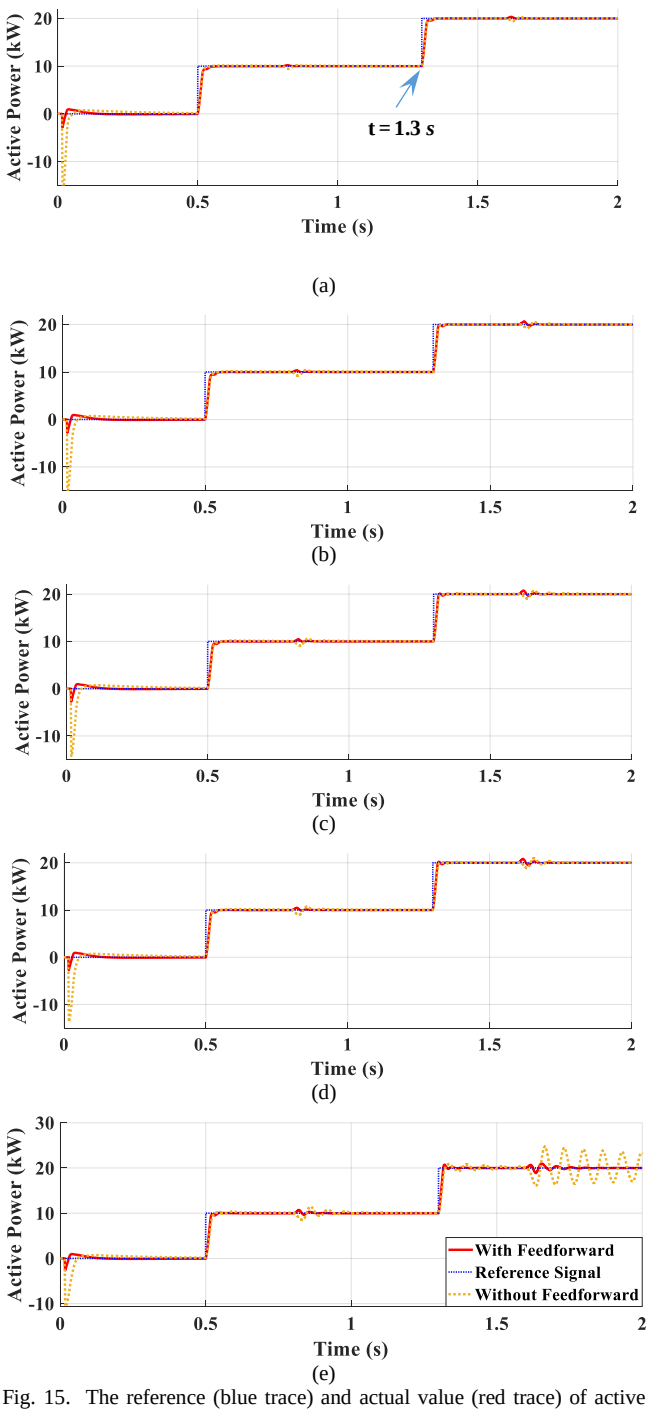

Fig. 15. The reference (blue trace) and actual value (red trace) of active powers delivered by grid-connected DTL VSI using the proposed controller with/without feedforward signals at (a) SCCR=10, (b) SCCR=4, (c) SCCR=3, (d) SCCR=2.6, and (e) SCCR=1.50.

1) Operation without a Grid Fault: Another factor which is essential to assess the performance of the system is to determine when over-modulation happens during power control while SCCR changes. In other words, in which range of the SCCR the controller generates a modulation index, which is higher than one so that it is able to provide the

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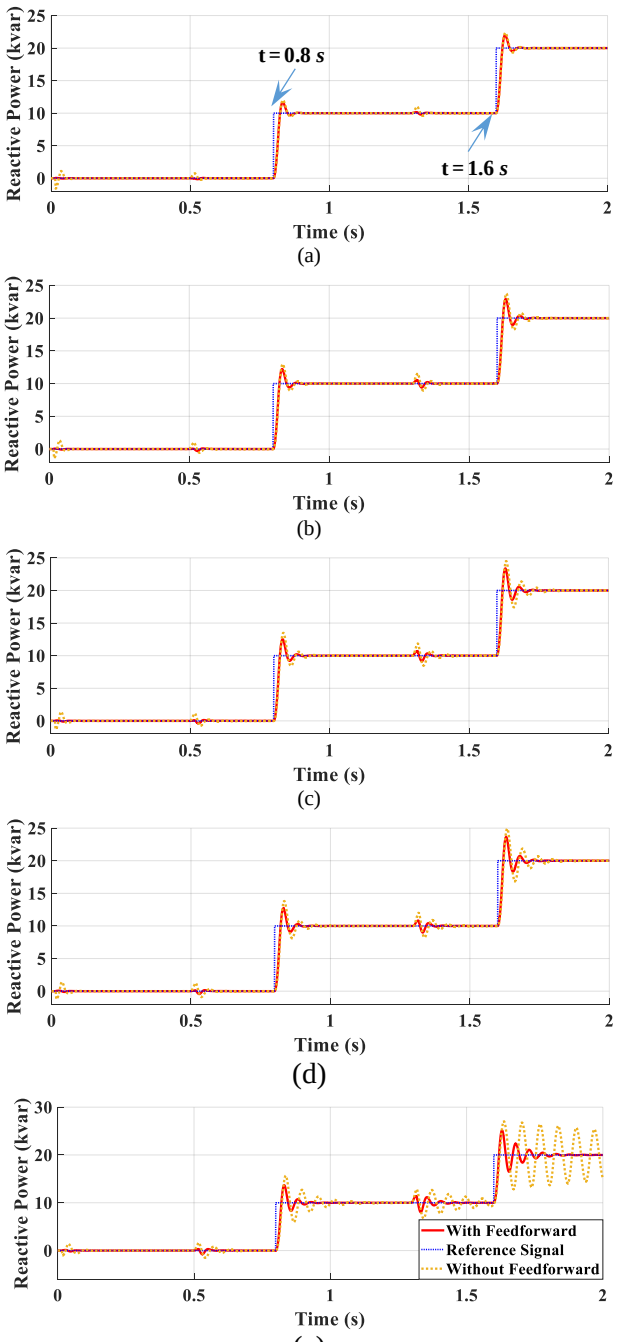

Fig. 16. The reference (blue trace) and actual value (red trace) of reactive powers delivered by the grid-connected DTL VSI using the proposed controller with/without feedforward signals at (a) SCCR=10, (b) SCCR=4, (c) SCCR=3, (d) SCCR=2.6, and (e) SCCR=1.50.

active/reactive power. For the system employing DTL VSI, it experiences over-modulation for SCCRs between one to 2.6, notably when the apparent power is 28.3 kVA (20 kW and 20 kvar). The MI curves of grid-connected DTL VSI at SCCR=1 and SCCR=2.6 are demonstrated in Fig. 17. Based on this figure, at SCCR=2.6, the controller generates an MI, which is higher than one, when it needs to inject 28.4 kVA. Though, by a decrease in SCCR, for example at SCCR=1, over-modulation occurs even for providing 22.36 kVA. For a lower amount of

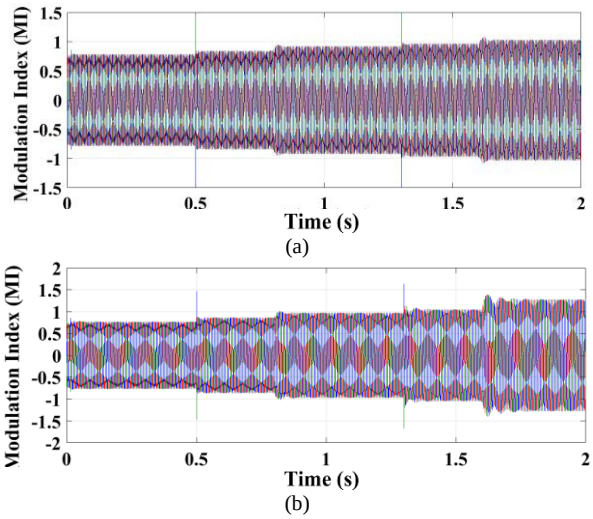

Fig. 17. Modulation index (MI) for three phases (the rest of the phases use the 180-degree phase shifter shown in Fig. 4) at (a) SCCR=2.6 and (b) SCCR=1.5.

active/reactive power, at SCCR=1, the controller produces an MI, which is approximately equal to1 (referred to Fig. 17(a)).

2) Operation with a Grid Fault: To investigate the performance of the grid-connected DTL VSI in all aspects, the performance of this system in faulty grid conditions should be studied as well. Thereafter, a solid three-phase fault (i.e., short-circuit without any impedance) occurs at 1.1 s, and is cleared after one cycle (i.e., 16.67 ms) while the DTL VSI's active power and reactive power have been set to 20 kW and 20 kvar for t < 1.1 s, respectively. For short-circuit evaluation, the reference currents are limited to nominal currents in the *dq*-frame. The performances of the system at SCCR=3, SCCR=2, and SCCR=1.78 are shown in Fig. 18. It can be seen that while the grid-connected DTL VSI shows stable performance at different SCCRs in normal condition, the stable performance after fault removal completely depends on the value of SCCR. For SCCRs above 1.78, the system retrieves its stable performance; however, at SCCRs lower than 1.78, the system does not track the reference values after fault removal.

Fig. 19 shows one of the phases' current (e.g., Phase "A" here) in the high-voltage side of the transformer for SCCR=5, 4, 3, and 1.78. According to Fig. 19, in the worst-case scenario, i.e., SCCR=1.78, the system needs about 0.25 s to recover its performance after a fault removal. Indeed, SCCR≥1.78 is the exact range of SCCR in which stable performance after fault removal is achieved. It is noteworthy that the settings used here for the current controllers follow those of industrial converters because the amount of fault current (in pu) has been matched with that of practical cases during the same type of faults, e.g., see "*Fig. 13*" in [32]—subfigure of the section captioned "*Bus 4; Top: Injected Current (kA)*."

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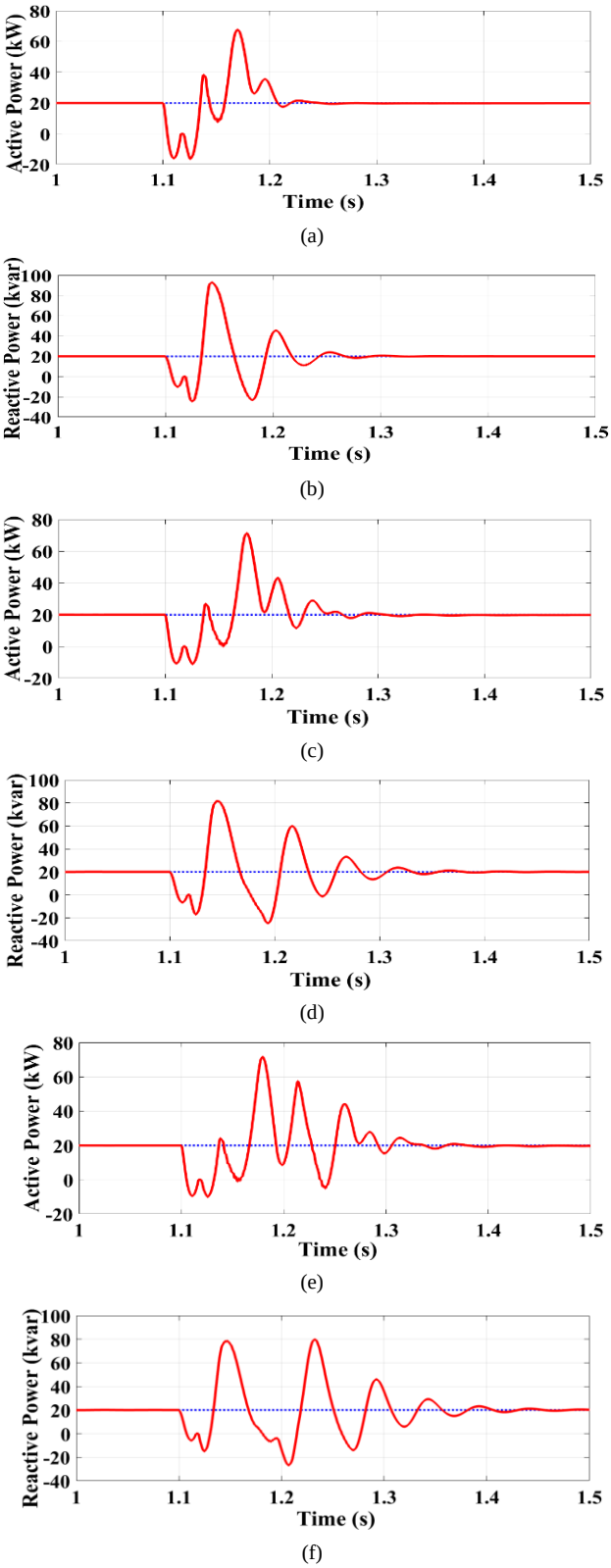

Fig. 18. The reference (blue trace) and actual value (red trace) of (a) active power at SCCR=3, (b) reactive power at SCCR=3, (c) active power at SCCR=2, (d) reactive power at SCCR=2, (e) active power at SCCR=1.78, (f) reactive power at SCCR=1.78 for grid-connected DTL VSI.

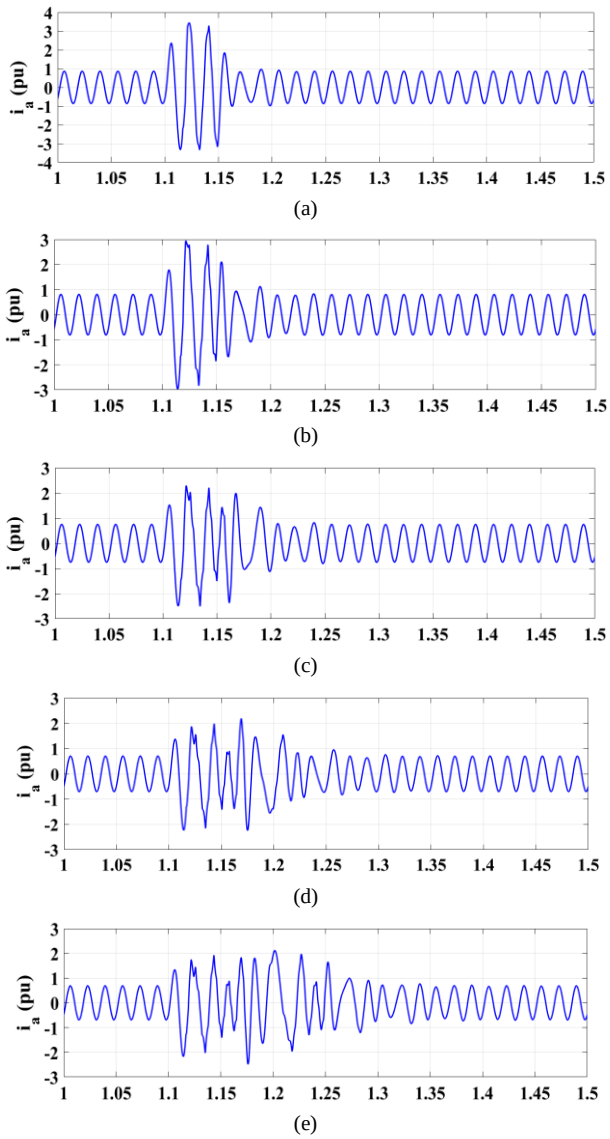

Fig. 19. The current of Phase A at high-voltage side of the open-ended transformer shown in Fig. 2 (a) SCCR = 5, (b) SCCR = 4, (c) SCCR = 3, (d) SCCR = 2, and (e) SCCR = 1.78.

Also, just in case, the same simulations have been repeated for a five-cycle fault to check the performance of the system—although the five-cycle fault is not tolerable in practical power electronic systems. The simulations associated with the five-cycle fault have concluded that the aforementioned threshold has been calculated as SCCR≥2.87.

B. PQ-Controlled TL VSI

1) Operation without a Grid Fault: In Fig. 20 and Fig. 21, the grid-connected TL VSI's performance associated with tracking active/reactive power reference signals at SCCR=10, 4, 3, 2.6, and 1.50 is depicted. Similar to the case of grid-connected DTL VSI, the system should track the reference values. For SCCR higher than 2.6, the system is able to provide the demand even if at a lower value of SCCR, the system needs more time to damp the generated oscillations after experiencing a change in the references. However, at

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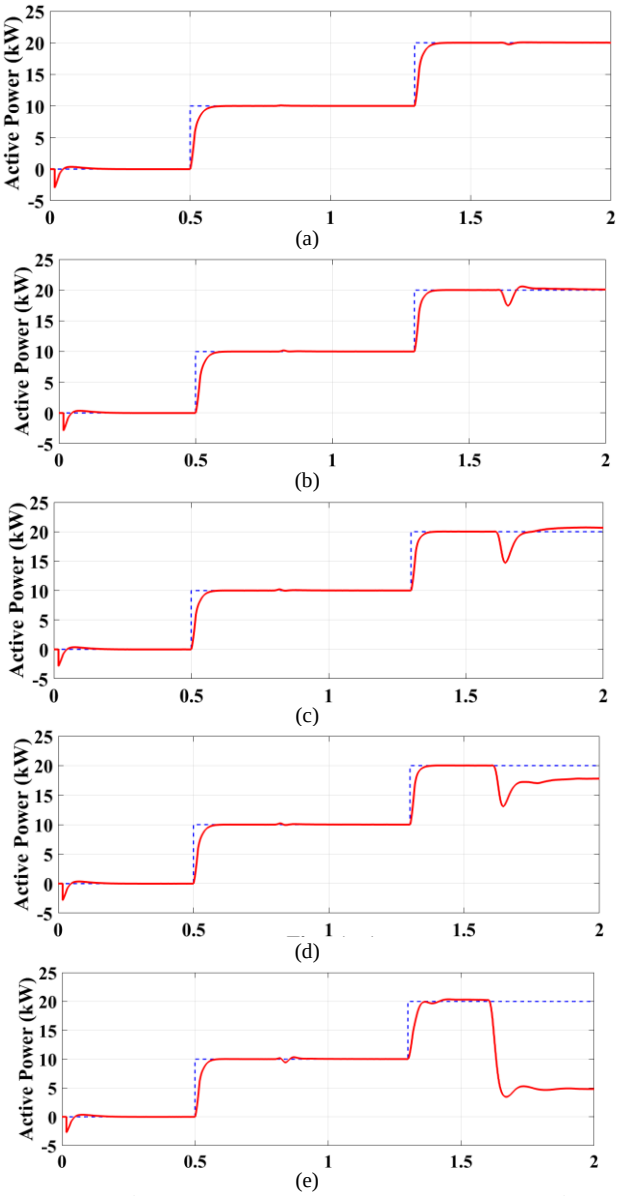

Fig. 20. The reference (blue trace) and actual value (red trace) of active powers by grid-connected TL VSI at (a) SCCR=10, (b) SCCR=4, (c) SCCR=3, (d) SCCR=2.6, and (e) SCCR=1.50.

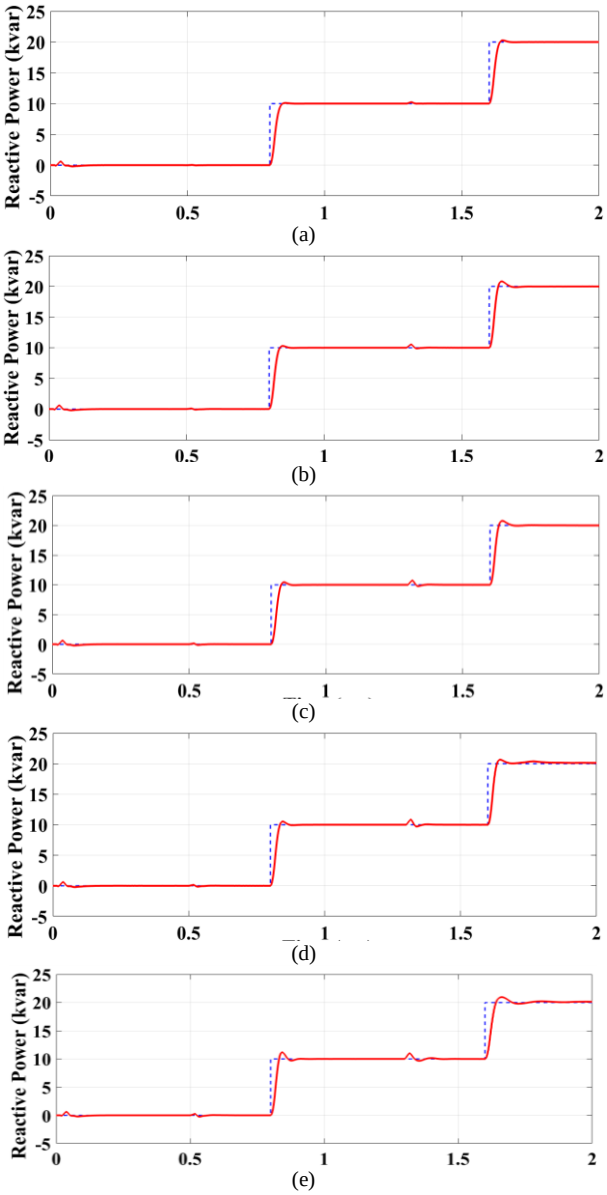

Fig. 21. The reference (blue trace) and actual value (red trace) of reactive powers by grid-connected TL VSI at (a) SCCR=10, (b) SCCR=4, (c) SCCR=3, (d) SCCR=2.6, and (e) SCCR=1.50.

SCCR≤2.6, for reference power equals to 28.42 kVA, the system is not able to generate 20 kW (referred to Fig. 20(c)). The amount of generated active power at SCCR=2.6 is equal to 17.9 kW. The lower the SCCR compared to 2.6, the lower the system ability to provide the active power. For example, at SCCR=1 (referred to Fig. 20(d)), the system ability to provide the reference power is also reduced in comparison with when SCCR=2.6. In case of SCCR=1, the system is not capable of providing 20 kW, when the reactive power reference is 10 kvar (the apparent power reference is 22.36 kVA). It is noteworthy here that for any SCCR, the system is able to provide the reactive power reference. However—for the low SCCRs—the power capacity of the system is remarkably reduced because of the fact that the grid-connected TL VSI should be able to provide a significant amount of reactive power (which is the case in all VSCs' integration into weak grids).

For comparing both grid-connected inverters, the range of SCCR in which the grid-connected TL VSI controller generates MI higher than one is accordingly evaluated. Consequently, the MI curves of grid-connected TL VSI at SCCR=10 and SCCR=2.6 are depicted in Fig. 22. Concerning Fig. 22, it can be seen that at SCCR=10 and for lower values of the apparent power reference (lower than 28.42 kVA) the system benefits from operation in normal MI range (i.e., without any over-modulations required). However, for the apparent power reference of 28.42 kVA, the system needs to employ over-modulation, thus suffering from its consequences. A similar response is obtained for SCCR=2.6. The only difference is that the magnitude of MI should be increased when SCCR decreases from 10 to 2.6—the highest value of MI changes from 1.5 to around 3.

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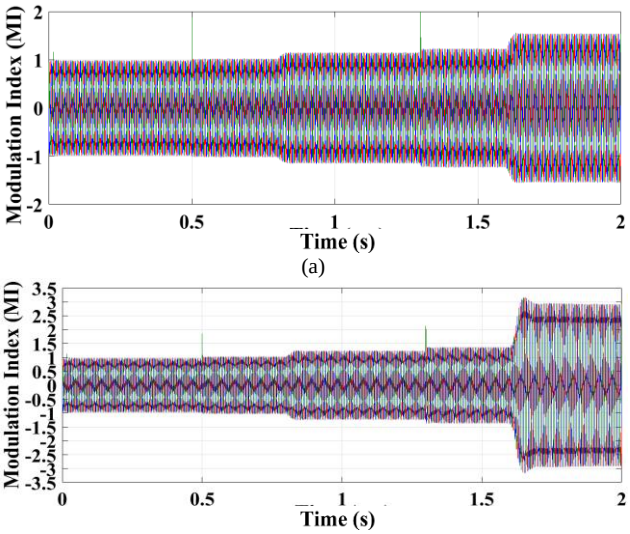

Fig. 22. Modulation index (MI) at (a) SCCR=10, and (b) SCCR=2.6.

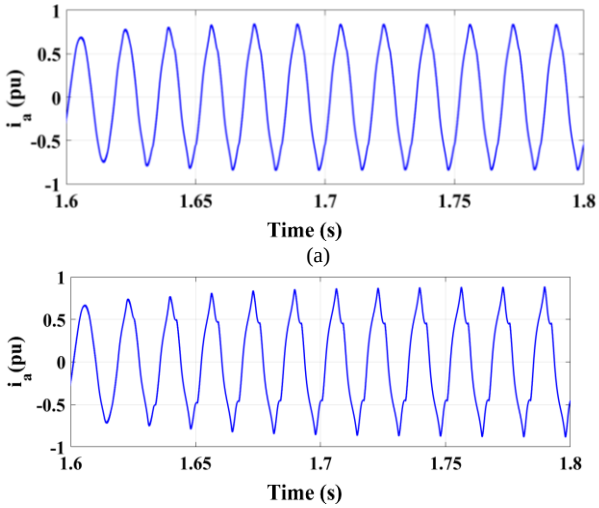

Fig. 23. The current of Phase A at (a) SCCR=4, and (b) SCCR=2.6.

The Phase A current of the high-voltage side of the Yd1 three-phase transformer at SCCR=4 and SCCR=2.6 is presented in Fig. 23. According to Fig. 23, the associated current contains harmonics when the grid-connected TL VSI generates 28.42 kVA. The current THDs associated with SCCR=4 and SCCR=3 are equal to 4.22% and 11.42%, respectively. The corresponding values for grid-connected DTL VSI are less than 0.5%; for example, the current THD is 1.62% at SCCR=1.5, hence getting much current THD in the much worse scenario. As a result, it has been demonstrated that not only does the grid-connected TL VSI suffer from higher current THD compared to another one, but also this problem worsens by a decrease in SCCR (lower than 4). Furthermore, this increase in the current THD is another effect showing that over-modulation dramatically happens and makes the performance weaker.

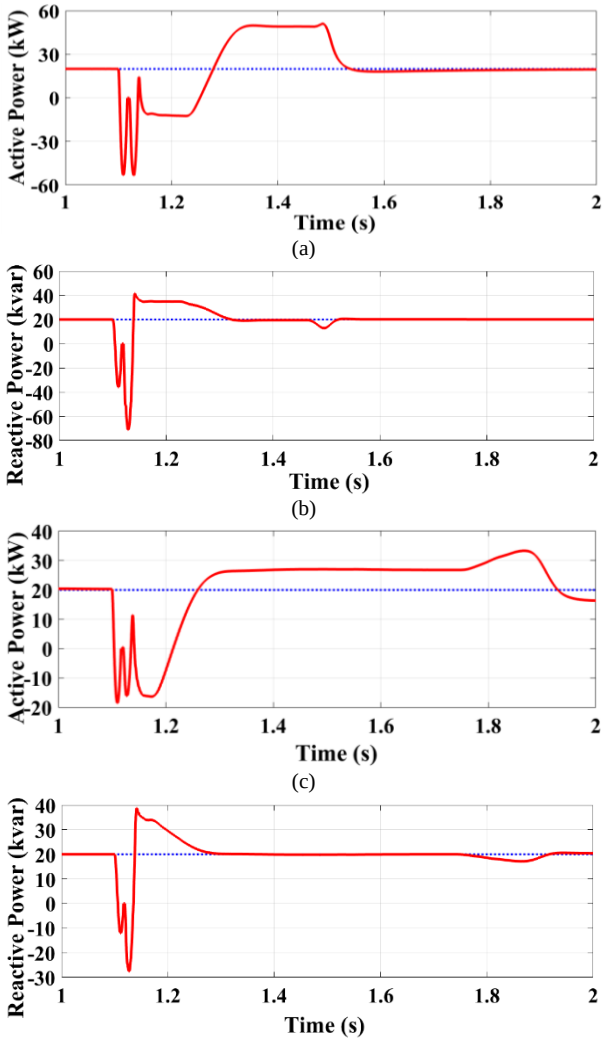

Fig. 24. The reference (blue trace) and actual value (red trace) of (a) active power at SCCR=10, (b) reactive power at SCCR=10, (c) active power at SCCR=3.5, and (d) reactive power at SCCR=3.5 for grid-connected TL VSI.

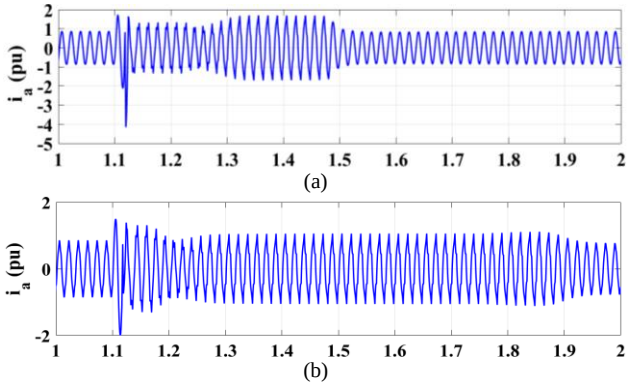

Fig. 25. The current of phase A at the high-voltage side of Yd1 transformer (a) SCCR=10, and (b) SCCR=3.5.

2) Operation with a Grid Fault: For comparing the two inverter structures, the performance of the grid-connected TL VSI in faulty grid conditions is also assessed. The same conditions as for the ones simulating the grid-connected DTL VSI's results are again taken into account here. The performance of the grid-

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connected TL VSI to track the reference values at different SCCRs is shown in Fig. 24. According to Fig. 24(a) and Fig. 24(b), after fault removal, the controller of grid-connected TL VSI is able to obtain a stable performance after about 0.45 s. Albeit the system is able to track these reference signals after removing the fault, it should be considered that for SCCR=10, the system needs about 0.45 s to track the references which compared to 0.15 s of the grid-connected DTL VSI, the time required to reach stable performance is significantly extended. For the SCCR=3.5, the system fails to provide the demand because although the reactive power reference is realized, the system is not able to generate the active one. The range of SCCR, in which the grid-connected TL VSI is able to stabilize active/reactive power demanded after the fault removal, is gained at SCCR≥3.5—which is SCCR≥ 1.78 for DTL VSIs for comparison purposes. It concludes that DTL VSIs are able to operate desirably in a broader range.

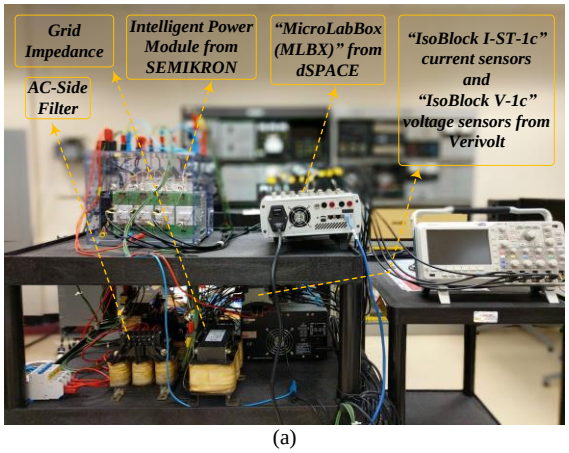
The fault currents of grid-connected TL VSI for SCCR=3.5 and SCCR=10 are demonstrated in Fig. 25. Based on Fig. 25(a), at about t = 1.5 s, the system preserves a stable performance, which is similar to the case before fault happened, i.e., t = 1.1 s. However, for SCCR=3.5—after fault removal—the current contains harmonics showing that the controller is not able to recover its stable performance (even by synthesizing MI higher than 1).

V. Experimental Results

For experimental evaluations, a scaled-down test rig, which is able to excite the dynamics of interest [18], [19], is being employed to emulate the dynamics of the grid-connected DTL VSI. It has been utilized for testing converter's performance when being used in the modernized microgrid's FIPES architecture. The experimental system consists of the voltage-source converter based on intelligent power modules from SEMIKRON, which includes insulated gate bipolar transistors (IGBTs) built by "SKM 50 GB 123 D" modules, "SKHI 21A (R)" gate drives, and protection circuits. The switching frequency has been set to 8,100 kHz. The ac-side filter inductance and resistance are 2.4 mH and 0.06 Ω, respectively, with an SCCR around 3. The dc-link capacitance and inductance are 2.04 mF and 1.50 mH, respectively. The three-phase converter is operated at 30 A and 208 V (line-to-line rms) and 400 V (dc)—which have the ratio similar to that of the simulations. The converter's inductor currents and the voltages are measured by "IsoBlock I-ST-1c" current sensors and IsoBlock V-1c" voltage sensors from Verivolt, respectively. The converter is interfaced with a "MicroLabBox (MLBX)" from dSPACE. The proposed control algorithm is executed and run by a dual-core, 2 GHz "NXP (Freescale) QorlQ P5020" real-time processor. The PWM signals are generated by "Xilinx Kintex-7 XC7K325T" field-programmable gate arrays (also known as FPGAs) connected to digital inputs/outputs (I/Os). The MLBX interface board is equipped with eight 14-bit, 10 megasamples per second (Msps), differential analog-to-digital channels to interface the measured signals to the controller (with the functionality of free-running mode). The software code is generated by the Real-Time-WorkShop in the Simulink environment.

A. PQ-Controlled DTL VSI

The experiments have been conducted to replicate simulations as accurate as possible. In this regard, based on the available facilities and devices, the DTL VSI's simulation results shown in Fig. 15 and Fig. 16 have been tested and duplicated. Here, Fig. 26 and Fig. 27 show the aforementioned experimental outcomes associated with the "DTL VSI." All results have been reported and generated in pu; $S_{base\text{-}3phase}$ for active/reactive power per unitization is 10.81 kVA, $I_{base\text{-}peak}$ for "peak" current per unitization is 42.43 A, and $I_{base\text{-}rms}$ for rms current per unitization is 30.00 A. In Fig. 26, Channels 1 and 2—with traces in dark blue and cyan colors—have been assigned to the measurements of active power and reactive power; Channels 3 and 4—with traces in dark magenta and lawn green colors—have been assigned to the reference signals of active power and reactive power, respectively. In Fig. 27, Channels 1 and 2 have been assigned to the measurements of active power and reactive power; Channels 3 and 4 have been assigned to Phase A of the ac-side current and the related modulation index (as the main control input/lever), respectively. Similar to Fig. 15 and Fig. 16, after 0.00/0.00 pu set points for active/reactive power, the first operating point is 0.33/0.00 pu active/reactive power and then the test rig is set to 0.33/0.33 pu active/reactive power; next, the third reference signal is 0.66 pu active power while the reactive power is 0.33 pu; finally, the forth one is 0.66 pu reactive power while the active power is 0.66 pu. Fig. 26 (including value per division of each channel) shows all test cases in one snapshot, and Fig. 27(a)–(e) depicts the enlarged view of the aforementioned operating point changes demonstrated in Fig. 26, respectively. In all figures, the volts per division (V/div) of each channel has been shown at the left-bottom corner. As they show, experiments are able to validate the simulations results of DTL VSI very well. For Fig. 26, Table II details the breakdown of power losses regarding different active/reactive power changes applied to the practical test rig.



(a)

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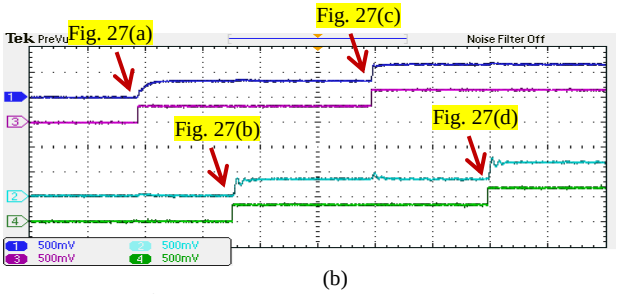
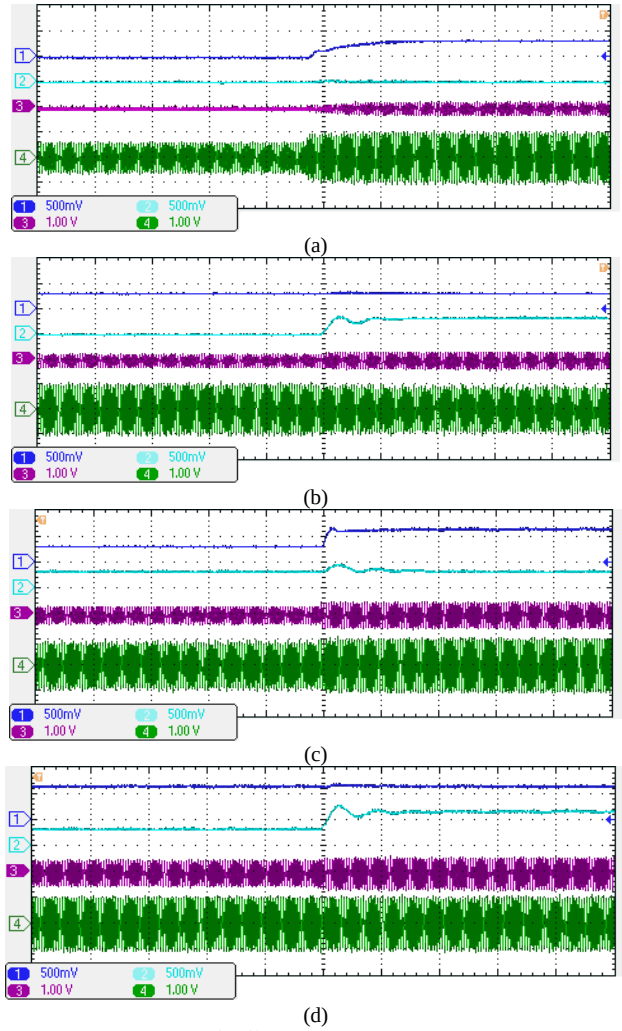


(b)

Fig. 26. (a) Some of the components used in the test rig and (b) snapshot of the experimental results associated with the "DTL VSI," for the test cases similar to those in Fig. 15 and Fig. 16, showing active power and its reference signal (Channel 1 in dark blue for the measurement and Channel 3 in dark magenta for the reference signal of active power with 5.40 kW/div) and reactive power and its reference signal (Channel 2 in cyan for the measurement and Channel 4 in lawn green for the reference signal of reactive power with 5.40 kvar/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu with time horizontal axis 200 ms/div.



(a)

(b)

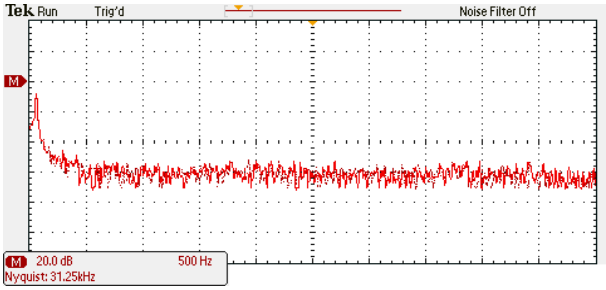
(c)

(d)

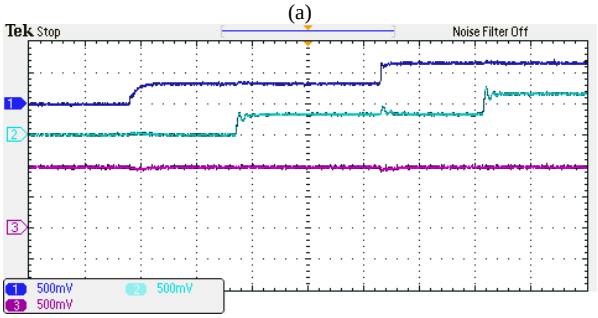
Fig. 27. Enlarged view of different parts and changes shown in Fig. 26: (a) active power change, (b) reactive power change, (c) active power change, and (d) reactive power change with Phase A of the ac-side current (Channel 3 in dark magenta with 42.43 A/div) and the modulation index (Channel 4 in green with 1.00 V/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu with time horizontal axis 40 ms/div.

TABLE II
BREAKDOWN OF POWER LOSSES IN FIG. 26 AND FIG. 27

Component Loss \ Period	1st Change	2nd Change	3rd Change	4th Change
Total DC-Side Filter Loss in %	0.016	0.017	0.063	0.065
Total Converter Loss in %	0.48	0.65	1.05	1.31
Total AC-Side Filter Loss in %	0.099	0.17	0.37	0.53
Total Loss in %	0.60	0.83	1.48	1.91



(a)



(b)

Fig. 28. (a) Frequency content of the ac-side current of Fig. 27 (20 dB per vertical division and 500 Hz per horizontal division) and (b) dynamic response of dc voltage of Fig. 26—showing active power (Channel 1 in dark blue with 5.40 kW/div), reactive power (Channel 2 in cyan with 5.40 kvar/div), and dc voltage (Channel 3 in dark magenta with 200 V/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu with time horizontal axis 200 ms/div.

Fig. 28(a) demonstrates the power quality of the PQ-controlled DTL VSI under test using the fast Fourier transform (FFT). Because over-modulation does not happen here (shown in Fig. 27), the current has acceptable harmonic contents with the THD of 1.05%. In this test case, since DTL VSI needs to track different active/reactive power references as per ac grid's need, it should be able to work at various power factors (PFs). In Fig. 28(b), PF ranges from 0.71 to 1.00 based on the applied active/reaction power set-points—similar to simulations results of Fig. 15 and Fig. 16. Fig. 28(b) also shows the dynamic response of dc voltage when the active/reaction power changes in Fig. 26.

B. PQ-Controlled TL VSI

For comparison, the test rig has also been reconfigured to the TL VSI architecture in this part—considering all requirements elaborated in Section IV. In this regard, the "TL VSI's" simulation results shown in Fig. 20 and Fig. 21 have been tested and duplicated. Here, Fig. 29 (including value per division of each channel) and Fig. 30 show the aforementioned

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experimental outcomes associated with the "TL VSI"—undergoing the same conditions and test cases used in Fig. 29 and Fig. 30. In all figures, the V/div of each channel has been shown at the left-bottom corner. They show that TL VSI is experiencing the over-modulation as predicated by simulations as well. Again, they are able to validate the simulations results of TL VSI. For Fig. 29, Table III details the breakdown of power losses regarding different active/reactive power changes applied to the experimental testbed.

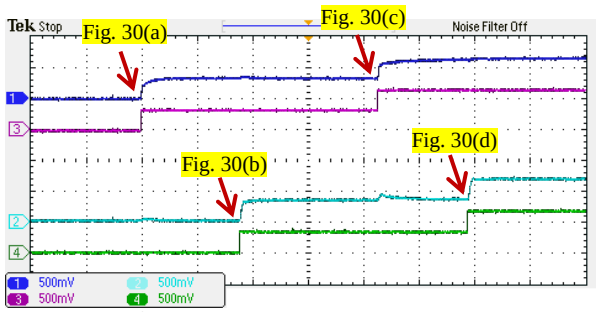
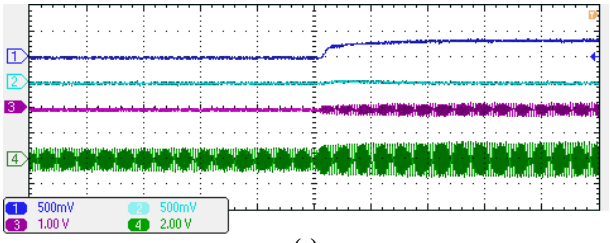
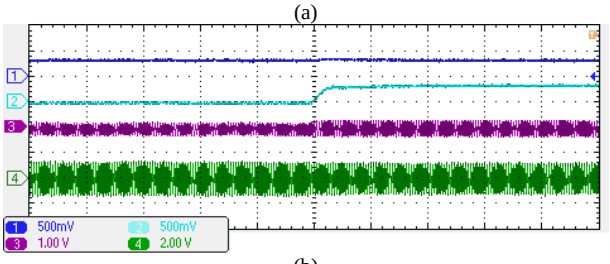


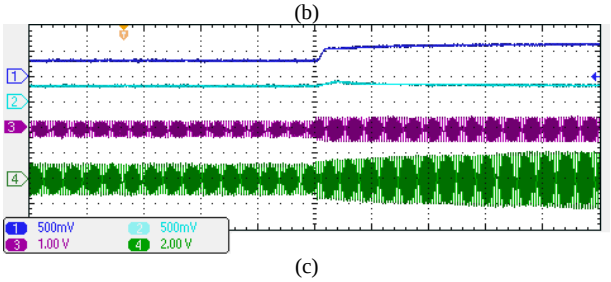
Fig. 29. Snapshot of the experimental results associated with the "TL VSI," for the test cases similar to those in Fig. 20 and Fig. 21, showing active power and its reference signal (Channel 1 in dark blue for the measurement and Channel 3 in dark magenta for the reference signal of active power with 5.40 kW/div) and reactive power and its reference signal (Channel 2 in cyan for the measurement and Channel 4 in lawn green for the reference signal of reactive power with 5.40 kvar/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu with time horizontal axis 200 ms/div.



(a)



(b)



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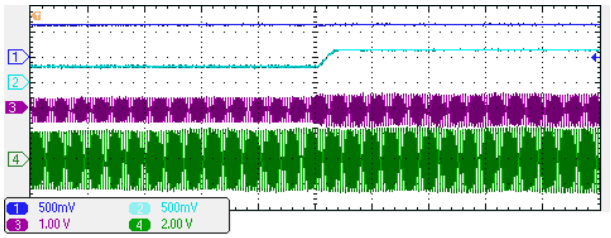
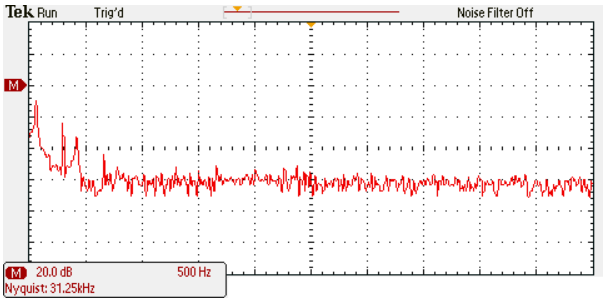
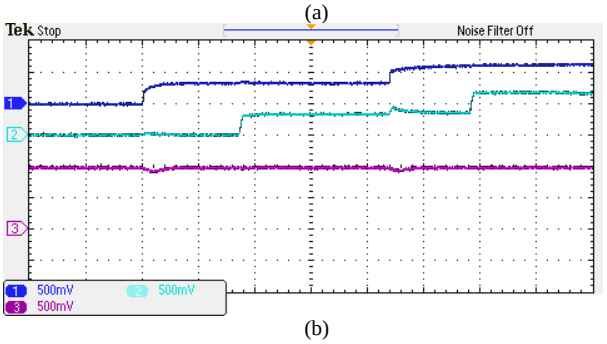


(d)

Fig. 30. Enlarged view of different parts and changes shown in Fig. 29: (a) active power change, (b) reactive power change, (c) active power change, and (d) reactive power change with Phase A of the ac-side current (Channel 3 in dark magenta with 42.43 A/div) and the modulation index (Channel 4 in green with 2.00 V/div) with time horizontal axis 40 ms/div.



(a)



(b)

Fig. 31. (a) Frequency content of the ac-side current of Fig. 30 (20 dB per vertical division and 500 Hz per horizontal division) and (b) dynamic response of dc voltage of Fig. 29—showing active power (Channel 1 in dark blue with 5.40 kW/div), reactive power (Channel 2 in cyan with 5.40 kvar/div), and dc voltage (Channel 3 in dark magenta with 200 V/div)—V/div of each channel has been shown at the left-bottom corner for all variables in pu.

TABLE III
BREAKDOWN OF POWER LOSSES IN FIG. 29 AND FIG. 30

Component Loss \ Period	1st Change	2nd Change	3rd Change	4th Change
Total DC-Side Filter Loss in %	0.029	0.030	0.12	0.13
Total Converter Loss in %	0.43	0.61	1.02	1.30
Total AC-Side Filter Loss in %	0.26	0.46	1.05	1.55
Total Loss in %	0.72	1.10	2.18	2.98

Comparing Table II and Table III shows that power losses are better in DTL VSIs. Also, Fig. 31(a) demonstrates the power quality of the PQ-controlled TL VSI under test using FFT. Because over-modulation does happen here (shown in Fig. 30), the current has unwanted harmonic contents—especially for low-frequency harmonics—with the THD of 11.14%. In Fig. 31(b) [like Fig. 28(b)], PF ranges from 0.71 to

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1.00 based on the applied active/reaction power set-points—similar to simulations results of Fig. 20 and Fig. 21. Fig. 31(b) also shows the dynamic response of dc voltage when the active/reaction power changes in Fig. 26. It is noteworthy that there are always some practical uncertainties (which are frequent) in any experiments compared to simulations, especially when dealing with creating weak-grid conditions. Considering those uncertainties and simulation results in Section IV, experiments shown in Fig. 26–Fig. 31 can genuinely demonstrate a good comparison between the performance of DTL VSI and that of the TL VSI very well.

VI. Conclusion

This paper has revealed that dual two-level voltage-source inverters (DTL VSIs) have been able to integrate dc sources into the future/present modernized FIPESs using MIACDC architecture more effectively—compared to the conventional two-level voltage-source inverters (TL VSIs). For doing so, this paper has investigated the stability of the grid-connected DTL VSIs. In order to assess the proposed structure's stability mathematically, a linearized state-space model of the system has been derived, validated, and compared with that of conventional grid-connected TL VSI. In the aforementioned linearized models, the effects of both PLL and grid parameters on the whole dynamic system have been investigated. The theoretical analyses, simulation results, and experiments are able to verify the significant advantages of the grid-connected DTL VSI over the grid-connected TL VSI regarding stability and ability to operate in a broader range of the grid weakness. The salient benefits of employing a grid-connected DTL VSI in the MIACDC architecture of the future/present FIPES—instead of using a conventional TL VSI—have concluded as follows.

1) While the proposed PQ-controlled DTL VSI could track the reference powers for any value of SCCR, even at SCCR=1, the grid-connected TL VSI failed to demonstrate a stable performance in a broad range of SCCRs and becomes unstable for SCCR lower than 2.6.
2) The power quality of the PQ-controlled DTL VSI is higher than that of TL VSI, for the same grid condition.
3) The proposed grid-connected DTL VSI showed better transient performance to preserve the stability after fault removal. Whereas SCCR=1.78 was the lowest value that the grid-connected DTL VSI was able to retrieve its stable performance after removal of the one-cycle fault, the grid-connected TL VSI was not able to preserve and obtain its appropriate performance even for SCCR=3.5 (for a one-cycle, solid, three-phase fault). Similarly, for faults with the other number of cycles, the DTL VSI showed better transients to preserve the stability after fault removal for lower SCCRs compared to those of the TL VSL.
4) Only for the SCCRs lower than 2.6, the controller of grid-connected DTL VSI dynamically generated a modulation index higher than 1 (i.e., having over-modulations during transients) in order to be able to generate the active/reactive power demanded. However—for the same system conditions and parameters—the stated over-modulation occurred even at SCCR=10 when grid-connected TL VSI was utilized (while injecting 28.28 kVA for both of them).
5) While the current injected to the grid by DTL VSI had much fewer harmonics considering (i.e., 1.62% for SCCR=1.5), the current of the grid-connected TL VSI contained significant harmonics even for higher values of the SCCRs (i.e., 4.22% for SCCR=4).

Appendix

TABLE I
Parameters Required for Fig. 2–Fig. 25

Nominal rated power of the inverter, i.e., S_n for DTL VSI or TL VSI	30 kVA
Range of SCCR changes (with $R_S=2\pi f_S L_S$)	10.00 to 1.00
Secondary/primary nominal line-to-line rms voltage	260/25,000 V
Fundamental frequency f_S	60 Hz
Angular fundamental frequency ω_S	$2\pi\times60$ rad/sec
Current controller gains K_{PI}/K_{II}	2.4/10.0
LC-Filter inductance and total resistance (including the switch on-state resistance of r_{on}) /capacitance	2.4 mH with 0.01 Ω /1.0 μF
dc-link voltage	500 V
Switching frequency	8,100 Hz (≈ 50,894 rad/s)
Transformer ratio	1:96.15
PLL $K_P/K_I/K_D$ and time constant for derivative action	180/3200/1 and 1×10^{-4}
α and β	0.001/0.001

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$$M=\begin{bmatrix}1&0&0&0&0&0&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0&0&0&0&0&0\\0&0&L&0&0&0&0&0&0&0&0&0&0\\0&0&0&L&0&0&0&0&0&0&0&0&0\\0&0&0&0&L_S&0&0&0&0&0&0&0&0\\0&0&0&0&0&L_S&0&0&0&0&0&0&0\\0&0&0&0&0&0&C&0&0&0&0&0&0\\0&0&0&0&0&0&0&C&0&0&0&0&0\\0&0&0&0&0&0&0&0&1&0&0&0&0\\0&0&0&0&0&0&0&0&0&1&0&0&0\\0&0&0&0&0&0&0&0&0&0&1&0&0\\0&0&0&0&0&0&0&0&0&0&0&1&0\\0&0&0&0&0&0&0&0&0&0&0&0&1\end{bmatrix}. \tag{A1}$$

$$A_{d11}=\begin{bmatrix}0&0&-1&0&0&0&0\\0&0&0&-1&0&0&0\\2K_{II}&0&(R-2K_{PI})&\begin{matrix}-L(C_1X_{1PID0}\\+C_2X_{2PID0}\\+\frac{K_D}{\beta}V_{PCC\_q0})\end{matrix}&0&0&-1\\0&2K_{II}&\begin{matrix}[L(C_1X_{1PID0}\\+C_2X_{2PID0}\\+\frac{K_D}{\beta}V_{PCC\_q0})]\end{matrix}&(R-2K_{PI})&0&0&0\\0&0&0&0&-R_S&\begin{matrix}[L_S(C_1X_{1PID0}\\+C_2X_{2PID0}\\+\frac{K_D}{\beta}V_{PCC\_q0})]\end{matrix}&1\\0&0&0&0&\begin{matrix}[-L_S(C_1X_{1PID0}\\+C_2X_{2PID0}\\+\frac{K_D}{\beta}V_{PCC\_q0})]\end{matrix}&-R_S&0\\0&0&1&0&-1&0&0\end{bmatrix}. \tag{A2}$$

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$$A_{d12}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -L\frac{K_D}{\beta}I_{1q0} & 2 & 0 & 0 & -LC_1I_{1q0} & -LC_2I_{1q0} \\ (L\frac{K_D}{\beta}I_{1d0}-1) & 0 & 2 & 0 & LC_1I_{1d0} & LC_2i_{1d0} \\ L_S\frac{K_D}{\beta}I_{2q0} & 0 & 0 & -\sqrt{\frac{2}{3}}V_{LL-rms}\sin(\alpha_0) & L_SC_1I_{2q0} & L_SC_2I_{2q0} \\ (1-L_S\frac{K_D}{\beta}I_{2d0}) & 0 & 0 & \sqrt{\frac{2}{3}}V_{LL-rms}\cos(\alpha_0) & -L_SC_1I_{2d0} & -L_SC_2I_{2d0} \\ C(C_1X_{1PID0}+C_2X_{2PID0}+2\frac{K_D}{\beta}V_{PCC\_q0}) & 0 & 0 & 0 & CC_1V_{PCC\_q0} & CC_2V_{PCC\_q0} \end{bmatrix}. \tag{A3}$$

$$A_{d21}=\begin{bmatrix} 0 & 0 & 0 & 1 & 0 & -1 & -C(C_1X_{1PID0}+C_2X_{2PID0}+\frac{K_D}{\beta}V_{PCC\_q0}) \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{T} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{A4}$$

$$A_{d22}=\begin{bmatrix} -C\frac{K_D}{\beta}V_{PCC\_d0} & 0 & 0 & 0 & -CC_1V_{PCC\_d0} & -CC_2V_{PCC\_d0} \\ 0 & -\frac{1}{T} & 0 & 0 & 0 & 0 \\ \frac{1}{T} & 0 & -\frac{1}{T} & 0 & 0 & 0 \\ \frac{K_D}{\beta} & 0 & 0 & 0 & C_1 & C_2 \\ 1 & 0 & 0 & 0 & -\alpha & 0 \\ 1 & 0 & 0 & 0 & 0 & -\beta \end{bmatrix}. \tag{A5}$$

$$A_{i11}=\begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ K_{II} & 0 & -K_{PI} & 0 & 0 & 0 & -1 \\ 0 & K_{II} & 0 & -K_{PI} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R_S & L_S(C_1X_{1PID0}+C_2X_{2PID0}+\frac{K_D}{\beta}V_{PCC\_q0}) & 1 \\ 0 & 0 & 0 & 0 & -L_S(C_1X_{1PID0}+C_2X_{2PID0}+\frac{K_D}{\beta}V_{PCC\_q0}) & -R_S & 0 \\ 0 & 0 & 1 & 0 & -1 & 0 & 0 \end{bmatrix}. \tag{A6}$$

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$$A_{t12}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 \\ L_S\dfrac{K_D}{\beta}I_{2q0} & 0 & 0 & -\sqrt{\dfrac{2}{3}}V_{LL-rms}\sin(\alpha_0) & L_SC_1I_{2q0} & L_SC_2I_{2q0} \\ (1-L_S\dfrac{K_D}{\beta}I_{2d0}) & 0 & 0 & \sqrt{\dfrac{2}{3}}V_{LL-rms}\cos(\alpha_0) & -L_SC_1I_{2d0} & -L_SC_2I_{2d0} \\ C(C_1X_{1PID0}+C_2X_{2PID0}+2\dfrac{K_D}{\beta}V_{PCC\_q0}) & 0 & 0 & 0 & CC_1V_{PCC\_q0} & CC_2V_{PCC\_q0} \end{bmatrix}. \tag{A7}$$

$$A_{t21}=A_{d21}, \text{ and } A_{t22}=A_{d22}. \tag{A8}$$

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