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Fault Detection and Protection Strategy for Islanded Inverter-Based Microgrids

Seyed Fariborz Zarei, Hossein Mokhtari, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*

Abstract—This paper proposes a fault detection and protection strategy for islanded inverter-based microgrids (IBMGs). Reliable and accurate protection is one of the main challenges in the proliferation of modern microgrids (MGs). Considering the limited fault current of the voltage-frequency controlled inverter-based distributed energy resources (VF-IBDERs), the protection is more challenging in islanded IBMGs. In this regard, the control scheme of VF-IBDER with a current limiting strategy plays an important role. Due to the limited fault currents close to the converter nominal current, the conventional fault detection methods do not work properly. In addition, bi-directional fault currents worsen protection coordination. In this paper, first, an analytical sequence network modeling for VF-IBDERs is derived to specify their behavior under fault conditions. Then, a voltage-restrained negative-sequence resistance-based fault detection approach is proposed, which is based on the derived sequence networks. This quantity inherently detects the fault and its direction and is independent from the fault current magnitude. The proposed feature can be employed in both conventional and communication-assisted coordination strategies. Also, a protection coordination strategy based on definite-time grading approach is employed. Finally, the performance of the proposed scheme is demonstrated by applying different faults in a test MG in PSCAD/EMTDC environment.

Index Terms—fault detection method, inverter-based microgrid, islanded mode, microgrid (MG), microgrid protection strategy.

I. INTRODUCTION

IN recent years, the environmental concerns associated with fossil fuels from one side, and strict rules of modern electric power systems to minimize the electricity outage from the other side have made power industry to invest more in the distributed generation of power at users sides. This remedy may decrease the generation cost, reduce the power loss, and increases the overall reliability of the system by allowing an islanded operation under the name of microgrid (MG) [1]. In this respect, some technical challenges have been highlighted including the MG protection. Emerging distributed energy resources (DERs) in distribution systems change a passive power system into an active one with bi-directional short-circuit currents [2]. In an MG operating in an islanded mode, the short circuit level decreases considerably [3, 4]. This issue is more challenging if the voltage-frequency controlled inverter-based DERs (VF-IBDERs) with limited fault current are the power sources [5]. This results in mal-operation of conventional overcurrent (OC) relays, fuses, and reclosers [6].

VF-IBDERs are responsible for regulating the voltage and frequency, which are essential for reliable operation in an islanded mode of operation. Short circuit current contributions by VF-IBDERs are limited and mostly depends on their control loops [7]. This paper focuses on the short circuit analysis of the VF-IBDERs and proposes a fault detection method and an MG protection strategy considering this type of energy resources. It is worth noting that the short circuit behavior of grid-following inverter-based distributed generations (so-called PQ-IBDGs) such as photovoltaic and the type

IV wind turbine DGs are not considered. However, to describe the impact of PQ-IBDGs on the proposed scheme, one subsection is provided in section IV according to the existing studies available in the literature.

For the protection of an islanded MG containing synchronous generators, OC relays, fuses and reclosers are the commonly used protective devices [8, 9]. In addition, directional OC relays are widely employed to identify fault directions [10, 11]. Also, there have been works on the coordination and optimal setting selection of OC relays [12]. These remedies are not effective in islanded inverter-based MGs (IBMGs) containing VF-IBDERs as energy sources. In this respect, several approaches have been proposed in the literature as follows.

Some methods try to detect a fault using the VF-IBDERs voltage signal. This can be done by using an under-voltage (UV) relay or determining the output voltage total harmonic distortion (THD) [13-15]. Under short circuit faults, faulty phase voltages drop considerably which give an opportunity to detect the fault by UV relay. However, when a fault occurs, the voltages in all busbars drop considerably which complicates finding the fault location. In this respect, although the fault occurrence is identified effectively by UV relays, the fault location and the relays coordination for the fault isolation still remain a challenge. Also, by using the improved current limiting strategy for VF-IBDERs (explained in section II), the THD level considerably decreases, and the applicability of the voltage THD-based approach cannot be guaranteed.

There are some methods, which use current signals for fault detection. As mentioned earlier, the OC relay cannot be used for islanded inverter-based MGs due to the reduced fault currents. Ref. [16] has used the wavelet transform to detect the fault, but the noise immunity of such approaches remains still a concern. Monitoring the transient response of the inverter current waveform is another method proposed in [17]. In both methods, the fault direction cannot be determined at the relay point which complicates the coordination among the relays. Ref. [18] uses differential current protection, and [19] utilizes a phase angle comparison of the current signals at both sides of a given distribution line to detect the fault. However, differential-based protection schemes are adversely affected by current transformers (CTs) mismatches [20]. Also, these schemes completely rely on the communication system not only for coordination but also for fault detection. Ref. [21] has proposed a method based on current sequence components for fault detection. Using this remedy, [6] proposes a method based on current sequences along with UV relays. However, the inherent unbalanced nature of distribution systems may cause mal-operation of such methods specially in an islanded IBMG [22, 23]. A method based on differential current sequences is proposed in [24]. This method also relies on a communication system for fault detection and coordination.

Using both voltage and current signals for fault detection is another method in the literature. This method is used in [25] with a data-mining-based protection scheme for fault detection. This study

TABLE I. COMPARING DIFFERENT FAULT DETECTION METHODS FOR ISLANDED INVERTER-BASED MGS.

Category	Methodology	Fault occurrence detection	Fault location and direction detection	Noise immunity	Dependency to system condition	Communication infrastructure	Fault detection speed	Accuracy
Using Voltage Signal	Output voltage THD	- Not guaranteed	- Not effective	- Not-proven	- Not-proven	+ Not needed	One cycle ⁴	- Not guaranteed
	Voltage drop (UV ¹)	+ Effective	- Not effective	+ Immune	+ Not-dependent	+ Not needed	One cycle ⁴	± Accurate ⁶
	Over-current relay	- Not effective	- Not effective	+ Immune	+ Not-dependent	+ Not needed	One cycle ⁴	- Not accurate
Using Current Signal	Current transients	- Not guaranteed	- Not effective	- Not-proven	- Not-proven	+ Not needed	Within a cycle ⁵	- Not guaranteed
	Neg. Seq. current ²	+ Effective	- Not effective	+ Immune	- May affected by imbalances	+ Not needed	One cycle ⁴	- May affected by imbalances
	Differential current	+ Effective	+ Effective	+ Immune	+ Not-dependent	- Necessary ³	Within a cycle ⁵	- May affected by CTs mismatch
	Differential Neg. Seq. current	+ Effective	+ Effective	+ Immune	+ Not-dependent	- Necessary ³	One cycle ⁴	- May affected by CTs mismatch
Using Voltage & Current Signals	Phase angle comparison of currents	+ Effective	+ Effective	+ Immune	+ Not-dependent	- Necessary ³	One cycle ⁴	- May affected by CTs mismatch
	Data-mining-based differential protection scheme	+ Effective	+ Effective	- Not-proven	- Not-proven	- Necessary ³	One cycle ⁴	- Not-proven
	Line impedance based distance protection	- Not effective	- Not effective	+ Immune	- Inaccurate for systems with short lines	+ Not needed	One cycle ⁴	- Not accurate

¹ Under-voltage.

² Negative sequence.

³ Communication infrastructure is necessary for both i) fault detection and ii) coordination among relays.

⁴ These fault detection methods use Fast Fourier Transform (FFT) concepts to calculate parameters such as voltage and current amplitudes and angles, positive and negative sequences of voltages and currents. Then, one cycle information is required for the analysis and calculation. This time delay is well-enough for medium and low voltage systems such as microgrids.

⁵ Such methods use few samples of data for fault detection purposes. Then, they can detect the fault within one cycle.

⁶ Under-voltage relay is accurate in fault occurrence detection since severe voltage drop effectively shows the faulty condition. However, the accuracy in terms of fault direction is under question since voltage-drop occurs in all substations in the system. Then, fault direction detection and correspondingly protection coordination cannot be done easily.

does not propose a coordination scheme and completely relies on a communication system. Also, VF-IBDERs are not included in this study. Furthermore, the method based on measuring the line impedance such as distance relay suffers from the accuracy specifically for the distribution system with short lines and correspondingly small line impedance values. Under such conditions, the seen impedance by the relay and also the operation threshold are low (unlike the transmission lines with hundreds of kilometers length), which cannot assure a reliable condition for correct fault detection. In other words, the impedance trajectory may throw out the operating protection zone leading to mal-operation of the relay in the MG [26, 27].

The functionality and performance of the above-mentioned methods are compared in Table I. Among them, communication-based differential protections are accurate for fault detection. Also, differential protections are regarded as unit protection which protects a specified protection zone [28]. Then, they accurately detect the fault direction and location. However, their functionality is completely dependent on the communication infrastructure which is limited due to the high investment cost and is not normally available for distribution systems. Furthermore, communication failure threatens the whole system protection since not only the coordination but also fault detection relies on the communication system. Any mismatch in the CTs of the two sides of the line also adversely affects this method. Also, dependency on the system conditions, noise immunity, relying on the communication system for fault detection, and lack of coordination scheme are the concerns of the other existing studies. This paper proposes a fault detection scheme that is based on short circuit behavior of a VF-IBDER to overcome the shortcomings of the existing methods. Using the proposed method,

a fault and its direction can be detected locally by the relays. Also, the proposed method uses the fundamental components of voltages and currents, and therefore, its performance cannot be affected by system harmonics and non-fundamental components. Its functionality is also independent of system operating conditions as will be shown in section IV.

In this paper, first, the modeling of VF-IBDERs under short circuit conditions is presented in section II. The equivalent sequence networks for the VF-IBDERs are introduced in section III, which specify the VF-IBDER behavior under short circuit fault condition. Using this model and knowing VF-IBDER fault behavior, a fault detection method and a protection strategy are proposed in sections IV and V, respectively. Finally, simulation results and the conclusions of the work are given in sections VI and VII, respectively.

II. CONTROL OF VF-IBDERs UNDER SHORT CIRCUITS

Fig. 1 (a) depicts a power circuit diagram of a VF-IBDER, in which VF-IBDER controls the voltages V_{oabc} . Fig. 1 (b) represents the dynamic control model of a VF-IBDER in the “ α ” axis. The same control system is used for the “ β ” axis, which is not shown for the sake of brevity. The control system consists of four blocks as follows:

- Output voltage control system
- Current limiter
- Anti-windup mechanism
- Terminal current control system.

Block (1) output voltage control system [29]: The input to this block is the sinusoidal nominal voltage reference ($V_{o\alpha}^*$). A

proportional-resonant (PR) compensator ($C_v=P+R$) is used as the controller to guarantee a zero steady state error for sinusoidal inputs. Under normal conditions, the output of g_2 ($i_{ta2} \cdot (g_1^{-1} - 1) \cdot g_2$) is zero since the current limiter of Block (2) is not activated ($g_1 = 1$). Also, the output current $i_{o\alpha}$ is used as a feed-forward signal. The output of this block is called unlimited current reference of i_{ta1}^* .

Block (2) current limiter [3, 30]: An instantaneous saturation limit strategy for a current limiter is a conventional method to limit the current. However, this limiter cuts the crest of the sinusoidal unlimited current reference i_{ta1}^* and creates distortions on the current reference. Instead, limiting the amplitude of i_{ta1}^* makes a distortion-free limitation, which is used in this paper. In this scheme, the current limiter is represented by the gain g_1 , which is "1" at normal condition. Under a short circuit condition, the voltage controller tries to regulate the output voltage by increasing i_{ta1}^* , which activates the current limiter. In this condition, g_1 takes values lower than 1 ($0 < g_1 < 1$), which limits the current peak to the predefined permissible value. The output of this block is i_{ta2}^* which is the limited current reference. Then, the gain g_1 is not a constant predefined value and is continuously calculated and updated according to the amplitude of i_{ta1}^* . However, at a fault steady state, it converges to a final value depending on the fault severity and g_2 value. It is worth noting that g_1 calculation does not require any knowledge on the type of fault since i_{ta1}^* is known from Block (1). Fig. 2 represents the methodology to find the limiter gain of g_1 . In this figure, first, the unlimited current references of i_{ta1}^* and i_{tb1}^* are transformed into i_{ta}^* , i_{tb}^* , and i_{tc}^* . As the quantities are sinusoidal in $\alpha\beta$ frame, the amplitude of the currents is obtained by summing the squares of the current and the delayed version of the current by 90° ($1/4$ cycle). Then, the maximum current among three phases is called I_p . When I_p is greater than I_{max} (permitted current), the gain g_1 is defined by I_p/I_{max} , otherwise it is "1".

Block (3) anti-windup mechanism [30]: Using only a current limiter cannot guarantee a stable loop since the voltage controller still tries to increase the output voltage by increasing i_{ta1}^* while the short circuit exists. In other words, the voltage controller saturates in this condition, and an anti-windup mechanism must be employed to release the controller. In this scheme, the anti-windup gain of g_2 has a constant and predefined value. Using this scheme guarantees that no saturation occurs in the control system even under short circuit faults, and therefore, the derived equations are valid. Regarding the selection of g_2 , it is recommended to use a value in the range of $(0.35 \sim 0.7) \times Z_{base}$, where Z_{base} is the base impedance of the VF-IBDER.

Block (4) terminal current controller [29]: This block controls the VF-IBDER current and generates the terminal voltage. C_i and $V_{o\alpha}$ are the PR controller and the voltage feed-forward signal, respectively. The input to this block is generally unbalanced current reference which is produced by voltage control block to supply the unbalanced currents demanded by unbalanced grid and loads. Since positive and negative sequence currents are sinusoidal in a " $\alpha\beta$ " stationary frame, the PR controller of C_i simultaneously controls both currents by zero steady-state error. Therefore, the extraction of positive and negative sequence currents and their separate control are not required in this scheme.

III. EQUIVALENT SEQUENCE NETWORKS FOR VF-IBDERS

In this section, positive/negative/zero sequence equivalent networks are derived for a VF-IBDER with the control structure described in the previous section. The models specify VF-IBDER behavior under different types of faults.

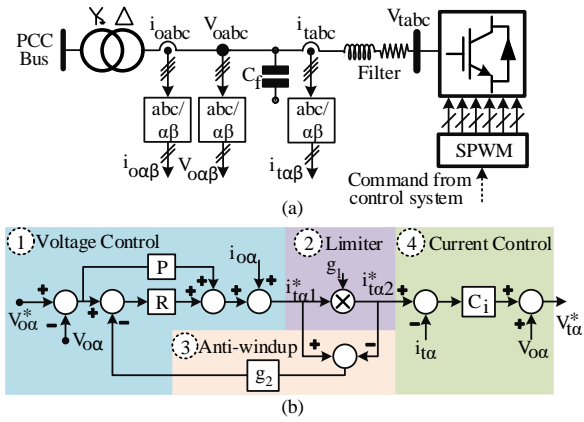


Fig. 1. (a) Schematic power circuit diagram of a VF-IBDER, (b) General dynamic model of a VF-IBDER for normal and fault condition.

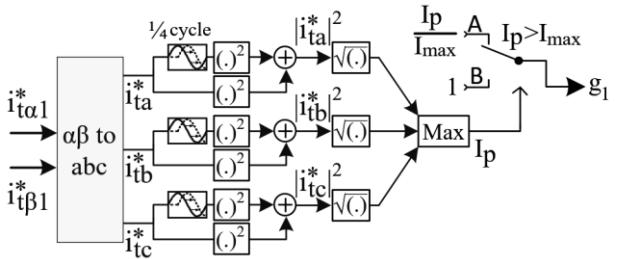


Fig. 2. The methodology to find the limiter gain of g_1 .

The control scheme of Fig. 1 (b) is taken as a base for modeling. The use of PR compensators for C_v and C_i result in zero steady-state errors of voltage and current reference tracking at nominal frequency. Since the quantities are sinusoidal and saturation does not happen using the anti-windup mechanism, not only in normal condition but also in faulty grid, the mentioned statement is valid. Hence, equations in (1) are met for the control loop at steady-state operating points under both faulty and normal conditions. It is worth noting that all quantities in Fig. 1 (b) are sinusoidal, therefore, phasor representation of quantities are used in the equations in the rest of the paper.

$$\begin{cases} V_{o\alpha}^* - i_{ta2}^* \cdot (g_1^{-1} - 1) \cdot g_2 - V_{o\alpha} = 0 \\ V_{o\beta}^* - i_{tb2}^* \cdot (g_1^{-1} - 1) \cdot g_2 - V_{o\beta} = 0 \end{cases} \quad (1)$$

Considering a zero steady-state error for the current control loop, current references i_{ta2}^* and i_{tb2}^* are equal to the terminal currents of i_{ta} and i_{tb} , respectively. Also, the output current $i_{o\alpha\beta}$ is the sum of the terminal current $i_{t\alpha\beta}$ and the injected current by the output capacitor C_f . Considering a low value for the output capacitor current, specifically under short circuit conditions with lower voltage amplitudes, the output current is equal to the terminal current ($i_{o\alpha\beta} \approx i_{t\alpha\beta}$). Therefore, (1) can be rewritten as:

$$\begin{cases} V_{o\alpha} = V_{o\alpha}^* - i_{o\alpha} \cdot (g_1^{-1} - 1) \cdot g_2 \\ V_{o\beta} = V_{o\beta}^* - i_{o\beta} \cdot (g_1^{-1} - 1) \cdot g_2 \end{cases} \quad (2)$$

Using $\alpha\beta 0$ to $pn0$ transformation matrix of (3), one can calculate the sequence components of (2) as given in (4), in which $z_{VF-IBDER} = (g_1^{-1} - 1) \cdot g_2$. In these equations, "p", "n" and "0" represent positive, negative and zero sequences, respectively.

$$T_{\alpha\beta 0 \rightarrow pn0} = \frac{1}{2} \cdot \begin{bmatrix} 0 & 0 & 2 \\ 1 & j & 0 \\ 1 & -j & 0 \end{bmatrix} \quad (3)$$

$$\begin{cases} V_{op} = V_{op}^* - z_{VF-IBDER} \cdot i_{op} \\ V_{on} = V_{on}^* - z_{VF-IBDER} \cdot i_{on} \end{cases} \quad (4)$$

Fig. 3 shows the VF-IBDER sequence component model based

on (4). In this model, the positive and negative sequence networks have the same impedance as:

$$Z_{VF-IBDER} = (g_1^{-1} - 1) \cdot g_2. \quad (5)$$

where, g_1 is the current limiter gain and g_2 is a predefined constant value, and also the voltage source amplitude $E\angle\delta$ is taken from droop control. Then, both g_1 and g_2 determine the VF-IBDER behavior under a short circuit condition.

From Fig. 3, the sequence networks for VF-IBDERs are the same as those for a conventional synchronous machine-based DG, but the equivalent impedance for the VF-IBDER is considerably higher. This impedance limits the output currents to the values close to the nominal values.

Regarding the validity margin of the impedance model, the model of Fig. 3 is correct for both normal and short circuit fault conditions. Under normal condition, $g_1=1$ and the impedances are zero; however, under short circuit condition, g_1 takes lower values which results in non-zero impedances according to (5).

IV. PROPOSED FAULT DETECTION METHOD BASED ON VF-IBDER EQUIVALENT SEQUENCE NETWORKS

In the following subsections, the basics of the proposed fault detection method are presented.

A. Fundamental Principles of the Proposed Fault Detection Scheme

Using the sequence networks of a VF-IBDER, a short circuit fault discriminative quantity is introduced to identify the faults. The details are in the following. In a short circuit condition, the currents of the faulty or affected phases are typically limited to the maximum value of $1.25 \times I_b$, where I_b is the VF-IBDER base current [3, 6]. Fig. 4 shows a VF-IBDER circuit subjected to a single-line-to-ground (SLG) fault. From this figure, the fault current in the “ $\alpha\beta$ ” frame is as given in (6)-(7) in a phasor representation form where $z_a = r_a + jx_a$ is the equivalent fault impedance seen by the VF-IBDER. Also, the faulty phase current in the “ abc ” frame is as given in (8) which is limited to $1.25 \times I_b$.

$$I_{o\alpha} = \left(\frac{\sqrt{3}}{2}\right) \cdot \frac{\sqrt{3} \cdot V_{o\alpha} - V_{o\beta}}{r_a + jx_a} \quad (6)$$

$$I_{o\beta} = \left(\frac{-1}{2}\right) \cdot \frac{\sqrt{3} \cdot V_{o\alpha} - V_{o\beta}}{r_a + jx_a} \quad (7)$$

$$I_{fault} = \left(\frac{\sqrt{3}}{2}\right) \cdot \left(\frac{\sqrt{3} \cdot V_{o\alpha} - V_{o\beta}}{r_a + jx_a}\right) \quad (8)$$

Substituting (6)-(7) into (2) yields $V_{o\alpha}$ and $V_{o\beta}$ versus $V_{o\alpha}^*$ and $V_{o\beta}^*$. Now, substituting $V_{o\alpha}$ and $V_{o\beta}$ into (8) and considering $1.25 \times I_b \times \sqrt{2}$ for I_{fault} , the relationship between g_1 and g_2 for an SLG fault can be found as in (9), where Z_{base} is the base impedance based on the VF-IBDER nominal ratings. Eq. (10) gives the relationship for a line-to-line (LL) fault using the same strategy. The details of the mathematical proof are not given due to space limitation. It is worth noting that $V_{o\alpha}^*$ and $V_{o\beta}^*$ are substituted by $|V_m^*| \angle 0$ and $|V_m^*| \angle -90$, respectively, in which $|V_m^*|$ is the peak value of nominal system voltage ($|V_m^*| = \sqrt{2} V_{ll} / \sqrt{3}$ and V_{ll} is nominal system line-to-line voltage).

$$g_1 = g_2 \cdot \left(g_2 + \sqrt{(0.7 \times Z_{base})^2 - \left(\frac{x_a}{2}\right)^2} - \frac{r_a}{2} \right)^{-1} \quad (9)$$

$$g_1 = g_2 \cdot \left(g_2 + \sqrt{(0.8 \times Z_{base})^2 - \left(\frac{x_a}{6}\right)^2} - \left(\frac{r_a}{12}\right) \right)^{-1} \quad (10)$$

Since $r_a + j \cdot x_a$ is negligible as compared to Z_{base} , (9) and (10) can be simplified to (11) and (12), respectively.

$$g_1 \approx \frac{g_2}{g_2 + 0.7 \times Z_{base}} \quad (11)$$

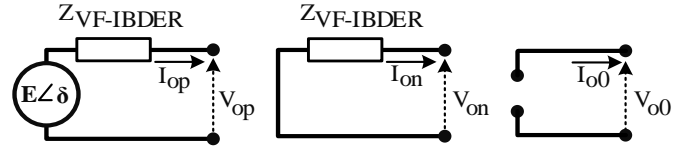


Fig. 3. VF-IBDER sequence network model: (a) Positive sequence; (b) negative sequence; (c) zero sequence.

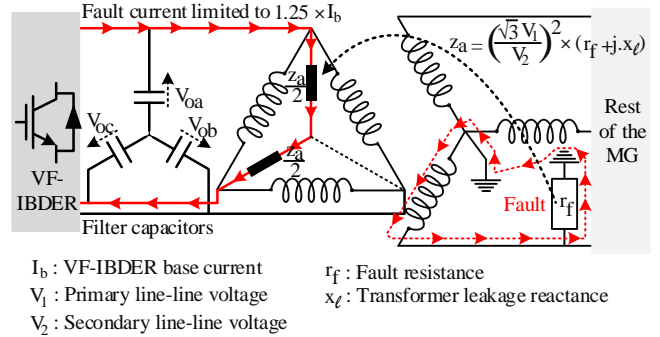


Fig. 4. A VF-IBDER subjected to an SLG fault.

$$g_1 \approx \frac{g_2}{g_2 + 0.8 \times Z_{base}} \quad (12)$$

Substituting (11) and (12) into (5) results in (13) and (14), which gives the VF-IBDER sequence impedances for SLG and LL faults, respectively.

$$Z_{VF-IBDER} \approx 0.7 \times Z_{base} \quad (13)$$

$$Z_{VF-IBDER} \approx 0.8 \times Z_{base} \quad (14)$$

Eqs. (13)-(14) provide important insight into the behavior of the VF-IBDER under short circuit conditions. They reveal that the VF-IBDER equivalent impedance increases to large values, while it is zero at normal conditions. This is a valuable finding since the significant impedance variation from a normal to a short circuit condition ensures reliable and precise discrimination between these two conditions. Also, it is shown that the impedance is resistive, and for this reason, $Z_{VF-IBDER}$ is replaced by $r_{VF-IBDER}$ in the rest of the paper. This concept is the basis for the proposed protection scheme. All discussions till now are about an equivalent impedance which is based on the introduced model. However, a physical quantity is required for practical applications. Looking at the negative sequence network of Fig. 3, it is concluded that the derived equivalent impedance is the only element in this sequence network. Then, measuring the output voltages and currents and calculating their sequence components, (15) gives the required negative sequence impedance (resistance), where V_{on} and I_{on} are the voltage and current negative sequences.

$$Z_{VF-IBDER} (= z_2) = \frac{V_{on}}{I_{on}} \quad (15)$$

It should be noted that the resistance of (15) is a negative value considering the negative sequence network of Fig. 3.

Since the VF-IBDER equivalent resistance can be found by calculating the negative sequence impedance, this quantity can be implemented through digital relays for fault detection purposes. In this regard, it is necessary to find a proper setting, which results in the reliable operation of the protective relay. The given impedances in (13) and (14) are $r_{VF-IBDER}$ for severe SLG and LL faults with zero fault resistance, respectively. Considering the fact that $r_{VF-IBDER}$ is a function of the fault type and its severity, it is then necessary to consider both to determine the relay setting. In (9) and (10), $r_a + j \cdot x_a$ represents the equivalent impedance seen by the VF-IBDER which includes the fault resistance. For VF-IBDERs with the parameters given in Table I, the gain g_1 and correspondingly $r_{VF-IBDER}$ variations are depicted versus the fault resistances in Fig.

5 (the faults occur at the Yg side as shown in Fig. 4). As shown in this figure, increasing R_f mostly affects $r_{VF-IBDER}$ for SLG faults and for a VF-IBDER with higher ratings. For secure and selective protection, considering a fault resistance of $R_f = 45\Omega$, the resistance of $r = 0.2$ p.u. is selected as the setting. In this respect, the impedance of the VF-IBDER with a higher rating will be the limiting impedance for setting selection (VF-IBDER1 in this case).

It is worth noting that the proposed fault detection method does not sense the overload condition. As the current limiter is activated at currents above $1.25 \times I_b$, for currents lower than this value, the equivalent impedance of the converter is zero ($g_1 = 1$). This means that under overload condition the seen negative sequence impedance (resistance) is zero and the proposed method correctly does not respond to this condition.

B. Extending the Applicability of the Proposed Fault Detection Method to the System Relays

As mentioned earlier, the negative sequence resistance of a VF-IBDER considerably increases during a short circuit condition. This feature can be used in the relays as a fault detection method. Fig. 6 shows a simple system containing a VF-IBDER and a distribution feeder equipped with a relay "R". This figure also shows the sequence networks for an SLG and a LL short circuits. Using the negative sequence circuit and (15), the negative sequence impedance seen by the relay (z_{2R}) for the SLG and LL faults are:

$$z_{2R} = -(r_{VF-IBDER} + j \cdot x_l) \quad (16)$$

$$z_{2R} = -(r_{VF-IBDER} + j \cdot x_l) \quad (17)$$

As previously mentioned, only the real (resistive) parts of (16)-(17) are required for a correct decision, which are equal to $r_{VF-IBDER}$. Then, using (13)-(14), the negative sequence resistances seen by the relay (r_{2R}) for SLG and LL faults are simplified as:

$$r_{2R} = -0.7 \times Z_{base} \quad (18)$$

$$r_{2R} = -0.8 \times Z_{base}. \quad (19)$$

Considering (18)-(19), it can be concluded that the negative sequence resistance seen by the relay is equal to the resistive impedance of the VF-IBDER sequence models, which can be used for the fault detection. In this respect, $r_{2R} = 0.2$ p.u. can also be used as a setting value for fault detection.

Since the source impedance during a fault is relatively high and the fault current is close to the nominal current, the effects of unbalanced loads, which are in the fault loop (between the source and fault location), are studied in the next subsection.

C. Evaluation of Unbalanced Loads Effects on the Proposed Fault Detection Quantity

The load currents are ignored in a short circuit analysis of the conventional power systems considering the high short circuit levels. However, in the presence of VF-IBDERs as IBMG sources, this assumption needs to be more investigated considering the high source equivalent impedance and the low short circuit current level (close to the nominal current). The first step is the sequence component modeling of the loads. Medium voltage (MV) distribution systems (e.g. 20 kV) are connected to low voltage (LV) systems via DYg transformers in which the Yg side provides a neutral wire for the single-phase loads. Therefore, the zero-sequence current cannot enter the MV side. Then, the MV side only sees the positive and negative sequence currents of the loads. To clarify more, consider the test system of Fig. 7 with an unbalanced feeder. In this system, a fault occurs at busbar B, and the effects of the loads in the fault loop (in this case the neighbor healthy feeder loads) on the negative sequence resistance seen by the relay R_{AB} is the concern. In this figure, all loads of the healthy feeder are shown by an equivalent impedance of $Z_{Load-eq}$ containing three impedances Z_{ab}, Z_{bc}, Z_{ca}

	Power rating	Output voltage	g_2
VF-IBDER 1	3 MVA	5 kV	4.5
VF-IBDER 2	2 MVA	5 kV	4.5

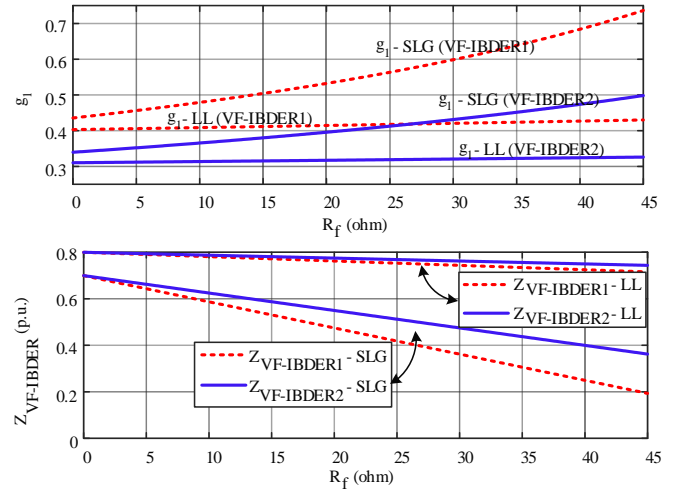


Fig. 5. The variations of g_1 and $Z_{VF-IBDER}$ for different fault resistances with the given VF-IBDERs parameters in Table I.

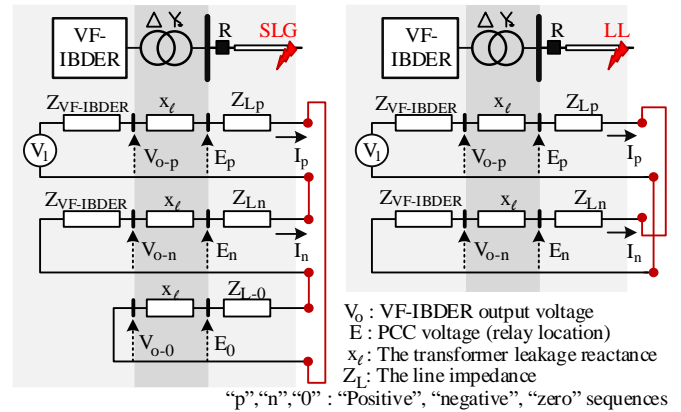


Fig. 6. Sequence networks of a test system for a SLG and a LL faults.

(see Fig. 7). Performing some mathematical calculations, (20) gives the positive and negative sequence component equivalents of this unbalanced three-phase load. As (20) shows, the impedance matrix is not a simple diagonal matrix. Therefore, the positive and negative sequence circuits are coupled together as graphically shown in Fig. 8.

$$\begin{cases}
 \begin{bmatrix} V'_p \\ V'_n \end{bmatrix} = \begin{bmatrix} Z_{L11} & Z_{L12} \\ Z_{L21} & Z_{L22} \end{bmatrix} \cdot \begin{bmatrix} I'_p \\ I'_n \end{bmatrix} \\
 Z_{L11} = Z_{L22} = \frac{\Delta}{3} \cdot \left(\frac{1}{Z_{ab}} + \frac{1}{Z_{bc}} + \frac{1}{Z_{ca}} \right) \\
 Z_{L12} = \frac{\Delta}{6} \cdot \left(\frac{2}{Z_{bc}} - \frac{1}{Z_{ab}} - \frac{1}{Z_{ca}} \right) + j \frac{\sqrt{3}\Delta}{6} \cdot \left(\frac{1}{Z_{ab}} - \frac{1}{Z_{ca}} \right) \\
 Z_{L21} = \frac{\Delta}{6} \cdot \left(\frac{2}{Z_{bc}} - \frac{1}{Z_{ab}} - \frac{1}{Z_{ca}} \right) - j \frac{\sqrt{3}\Delta}{6} \cdot \left(\frac{1}{Z_{ab}} - \frac{1}{Z_{ca}} \right) \\
 \Delta = \frac{Z_{ab} \cdot Z_{bc} \cdot Z_{ca}}{Z_{ab} + Z_{bc} + Z_{ca}}
 \end{cases} \quad (20)$$

In unbalanced cases, the dependent voltage sources impact on the negative sequence resistance must be investigated. Fig. 9 shows the sequence circuits for SLG and LL faults at busbar B. From Fig. 9, by dividing E_{An} by I_{AB-n} from negative sequence circuit, (21) gives the negative sequence impedance seen by the relay R_{AB} , in which Z_{2load} is the load imposed negative sequence impedance.

$$Z_{ABseen} = -(r_{VF-IBDER} + j \cdot x_l) \parallel \underbrace{\left(Z_{L22} + Z_{L21} \frac{I'_p}{I'_n} \right)}_{Z_{2load}} \quad (21)$$

Using Fig. 9, neglecting the transformer leakage reactance (x_l) and line AB impedances (Z_{ABp} , Z_{ABn} , Z_{AB0}), and with some calculations, (22) and (23) give the relationship between the positive and negative sequence currents of the unbalanced load during the SLG and LL faults conditions, respectively.

$$I'_p = -I'_n \frac{Z_{L22} + Z_{L12}}{Z_{L11} + Z_{L21}} \quad (22)$$

$$I'_p = I'_n \frac{Z_{L22} - Z_{L12}}{Z_{L11} - Z_{L21}} \quad (23)$$

Substituting (22)-(23) into Z_{2load} in (21), Z_{2load} is calculated as given in (24) and (25) during SLG and LL faults, respectively (see Δ in (20)).

$$Z_{2load} = \frac{1}{3} \cdot \frac{\Delta}{Z_{L11} + Z_{L21}} \quad (24)$$

$$Z_{2load} = \frac{1}{3} \cdot \frac{\Delta}{Z_{L11} - Z_{L21}} \quad (25)$$

Substituting the related quantities from (20) into (24) and (25) results in (26) and (27), respectively.

$$Z_{2load} = \frac{Z_{ab} \cdot Z_{bc} \cdot Z_{ca}}{z_{ca} (z_{ab} - z_{bc} \cdot e^{j\frac{2\pi}{3}}) + z_{ab} (z_{ca} - z_{bc} \cdot e^{j\frac{4\pi}{3}})} \quad (26)$$

$$Z_{2load} = \frac{Z_{ab} \cdot Z_{bc} \cdot Z_{ca}}{z_{bc} (z_{ca} - z_{ca} \cdot e^{j\frac{4\pi}{3}}) + z_{bc} (z_{ab} - z_{ab} \cdot e^{j\frac{2\pi}{3}})} \quad (27)$$

Since Z_{2load} is in parallel with $r_{VF-IBDER}$ (see Fig. 9), the lower Z_{2load} , the more reduction of (21), which may affect the relay functionality. To meet this condition, if $Z_{ab} = -Z_{bc} \cdot e^{j\frac{2\pi}{3}}$ and $Z_{ca} = -Z_{bc} \cdot e^{j\frac{4\pi}{3}}$, then the denominator of (26) is maximized. Substituting the impedances into (26) leads to (28). Applying the same procedure to (27) results in (29).

$$Z_{2load} = \left(\frac{Z_{ab}}{4} \right) \cdot e^{j\frac{\pi}{3}} \quad (28)$$

$$Z_{2load} = \left(\frac{Z_{ab}}{2\sqrt{3}} \right) \cdot e^{-j\frac{\pi}{6}} \quad (29)$$

On the other hand, the VF-IBDER rating is typically selected 1.5 times more than the system load depending on the operation strategy and required security. Then, aggregating all loads of the system in the healthy feeder and assuming a load peak condition as the worst possible case, the load impedance is $1.5 \times 3 \times Z_{base}$. Then, (28) and (29) can be rewritten as (30) and (31), respectively. The gain "3" in (30)-(31) is due to the use of delta connection in the load modeling of Fig. 7 ($Z_{Load-eq}$).

$$Z_{2load} = \left(1.5 \times 3 \times Z_{base} / 4 \right) \cdot e^{j\frac{\pi}{3}} \quad (30)$$

$$Z_{2load} = \left(1.5 \times 3 \times Z_{base} / 2\sqrt{3} \right) \cdot e^{-j\frac{\pi}{6}} \quad (31)$$

As a result, in the worst case, the impedances of (30) and (31) are about 1.6 times the impedances in (13)-(14). Then, considering (21), the load impedances do not considerably decrease the impedance seen by the relay AB. Hence, the negative sequence resistance with the selected setting ($0.2 \times Z_{base}$) is still valid for the protection purposes considering the load currents.

D. Performance Evaluation of the Proposed Quantity under Normal Condition- Unbalanced Loads

During a normal condition and when the current limiter is not activated, $r_{VF-IBDER}$ is zero, and the negative sequence network of the VF-IBDER is modeled by a short circuit. As a result, the transformer leakage reactance would be the only impedance in the negative sequence network of the VF-IBDER and its transformer. Considering a 5% leakage reactance for distribution transformers in parallel with the loads equivalent impedances, the impedances seen by the relays are almost equal to the transformer leakage reactance. Therefore, the negative sequence resistance seen by the relay is

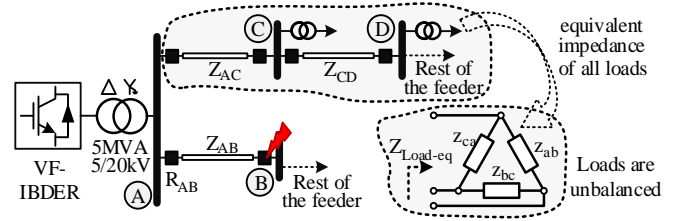


Fig. 7. Test system for evaluation of unbalanced loads effect on the proposed quantity.

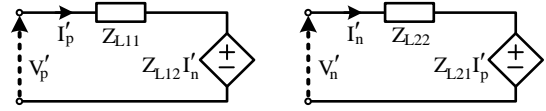


Fig. 8. Sequence component modeling of an unbalanced three phase load according to (20).

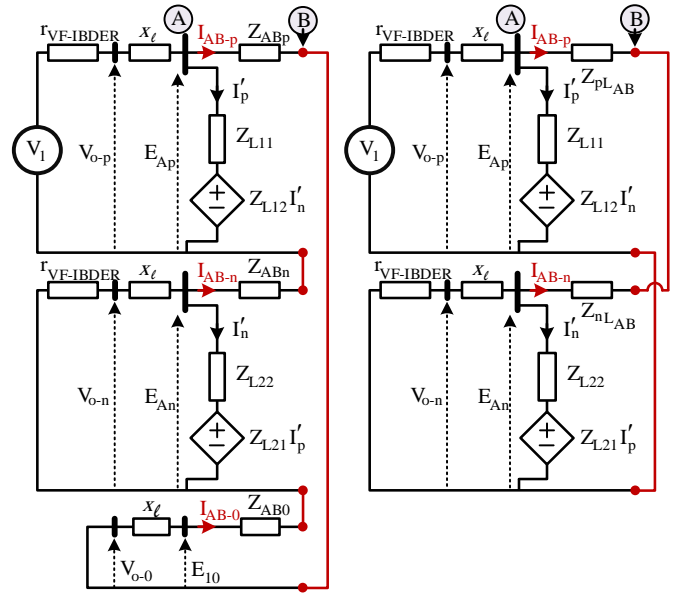


Fig. 9. Sequence circuit of Fig. 7 for SLG and LL faults at busbar B.

negligible, and the selected settings for the relays ($0.2 \times Z_{base}$) are valid in such circumstances.

It is worth noting that any change in the load and, consequently, the related transients do not affect the functionality of the proposed fault detection method since the current limiter is not activated under such transients. This means that the negative sequence impedance of VF-IBDER is zero according to (5) with $g_1=1$. Therefore, the negative sequence resistances seen by the protective relays are zero which does not cause malfunction of the relays.

E. Performance Evaluation of the Proposed Quantity under Normal Condition- Balanced Loads and No-Load Condition

When the system is balanced, both voltage and current negative sequences are small, and therefore, dividing the low negative sequence voltage by the low negative sequence current may result in an unreliable negative sequence impedance for fault detection. Consequently, it may cause wrong fault detection and relay mal-operation. This problem is also present at no-load or light load conditions. To restrain the relays operation in such conditions, the percentage of the negative sequence voltage divided by the positive sequence is employed as the criteria. This percentage rarely exceeds 5% at normal or light load conditions, but easily exceeds when a fault occurs [31].

F. A Discussion on the Impact of PQ Controlled Inverter-Based Distributed Generations on the Proposed Quantity

PQ controlled inverter-based distributed generations (PQ-IBDGs) are the second type of sources in an MG. They do not contribute to the voltage and frequency control task of an MG [32, 33]. Photovoltaic and Type IV wind turbine distributed generations are examples of PQ-IBDGs. Under short circuit conditions, two well-known requirements are requested by the grid codes which are (i) remaining connected to the system for a specified time and (ii) supporting the grid voltage by a reactive current injection [34]. Power system relaying and control (PSRC) committee has released a comprehensive report on fault current contributions from wind plants [35]. IEEE PES Industry Technical Support Task Force has investigated the protective relay issues related to the presence of PQ-IBDGs [36]. In these references, the short circuit fault current contribution of inverters has been specified for protective relaying purposes. Also, prior-art inverter control schemes have been included considering the present grid codes and different manufacturer specifications. The short circuit model of PQ-IBDGs is also provided. It is mentioned that the inverter controls employ current limiting functions and inject only a positive sequence current under all operating conditions including balanced and unbalanced short circuit faults. This is also highlighted by protection studies in which the negative sequence impedance-based directional element miss-operates under such conditions [37-39]. Therefore, the negative sequence impedance of PQ-IBDGs is represented by an open circuit or infinite impedance in the negative sequence circuit [35, 36]. As a conclusion, the negative sequence impedance of PQ-IBDGs is ignored in comparison with the remaining parallel impedances in the sequence network. Then, a PQ-IBDG does not affect the negative sequence resistances that are seen by the protective relays.

It should be noted that high impedance faults (HIFs) are not elaborated in this study. During HIFs, the voltage drop is not noticeable and even ground-fault relays may not detect HIFs [6]. For this reason, the conventional methods cannot be employed, and methods based on HIF current waveform characteristics such as the energy level and high-frequency components are utilized [40, 41]. An energy level based HIFs detection method has been elaborated in Ref. [6] for inverter-based MGs.

V. PROPOSED PROTECTION COORDINATION STRATEGY FOR AN MG CONTAINING VF-IBDERs

In the following, first, the relays response to a fault considering the proposed fault detection method is demonstrated by a case study. Then, the suggested protection coordination strategy is presented.

A. Case Study for Applying the Proposed Fault Detection Quantity to the Relays in a Sample System

A sample test system as shown in Fig. 10 is considered to analyze the relays operation. The voltage restraint negative sequence resistance-based fault detection method is used as described in the previous section. Fig. 11 shows the sequence circuit for an SLG fault in the middle of L_3 as an example. In this figure, “Li” corresponds to line “i”. Using the general form of (15) and considering the negative sequence circuit of Fig. 11, Eqs. (32)-(36) give the negative sequence impedances seen by the different relays in the test system for the fault.

$$Z_{R12} = -(r_{VF-IBDER1} + j \cdot x_{l-t1}) \quad (32)$$

$$Z_{R23} = -Z_{R21} = -(r_{VF-IBDER1} + j \cdot x_{l-t1} + Z_{L1n}) \quad (33)$$

$$Z_{R34} = -Z_{R32} = -(r_{VF-IBDER1} + j \cdot x_{l-t1} + Z_{L1n} + Z_{L2n}) \quad (34)$$

$$Z_{R43} = -Z_{R45} = -(r_{VF-IBDER2} + j \cdot x_{l-t2} + Z_{L4n}) \quad (35)$$

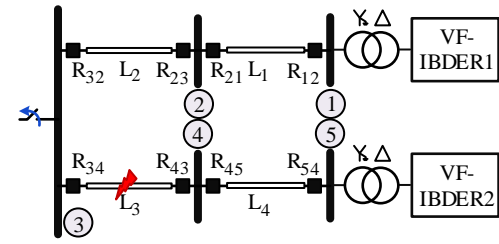


Fig. 10. A sample islanded microgrid for sequence circuit analysis of an SLG fault at the middle of line L_3 .

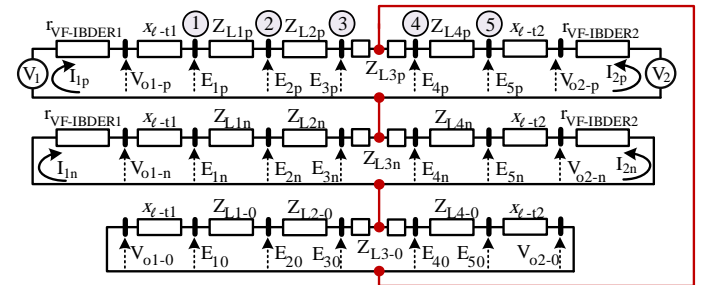


Fig. 11. The sequence circuit for an SLG fault at middle of line L_3 in Fig. 10.

$$Z_{R54} = -(r_{VF-IBDER2} + j \cdot x_{l-t2}) \quad (36)$$

Since line impedances are negligible compared to $r_{VF-IBDER1}$ and $r_{VF-IBDER2}$, and considering the inductive nature of the transformer leakage reactance, it can be concluded that the negative sequence resistance seen by each relay is equal to the impedance of the VF-IBDER located at behind of the relay as shown in (37)-(38), (e.g. for the fault shown in Fig. 10, VF-IBDER1 is located at behind of relays R_{12} , R_{21} , R_{23} , R_{32} , R_{34}). Therefore, the previously selected settings ($0.2 \times Z_{base}$) for the relays effectively detect the faults. It should be noted that the loads does not change the conclusion due to the earlier discussions.

$$r_{R12} = r_{R23} = -r_{R21} = r_{R34} = -r_{R32} = -r_{VF-IBDER1} \quad (37)$$

$$r_{R43} = -r_{R45} = r_{R54} = -r_{VF-IBDER2} \quad (38)$$

From (37)-(38), the relays in the same busbars see the same resistances but with opposite signs. Then, the sign of the resistance seen by each relay identifies the fault direction. Hence, the proposed quantity not only detects the fault but also determines the fault direction. In this respect, a negative sign represents a forward direction and vice versa. The forward direction for each relay is defined as towards the outside of its busbar (e.g., direction from busbar 1 to 2 is forward for R_{12}).

B. Proposed Coordination Strategy

As described in the previous subsection, when a fault occurs in the system, all relays detect the fault simultaneously since the negative sequence resistance seen by the relays increases considerably. To manage the relays operations, an appropriate grading method must be employed. Fig. 12 shows the proposed definite-time grading method with dashed lines employed in this paper. In this scheme, forward directions and the corresponding operating times are shown with dashed lines. The operating time for the fastest relays in the ring (R_{21} & R_{67}) is considered as t_{sm} which is the safety margin delay to avoid any unnecessary operation for temporary faults. A five cycle delay is considered for t_{sm} , i.e. 100 ms. For other relays, multiples of t_{cm} which is the coordination margin or the coordination time interval is added to ensure protection coordination among the relays. To clarify the operation, consider an arbitrary fault of F3, in which relays R_{34} and R_{43} are the operating relays. Using the proposed

grading method, other relays in the system have longer operating times comparing to R34 and R43, which ensures a proper protection coordination. Also, using this scheme, unnecessary isolation of the busbars can be avoided. As an example, R43 is responsible for a fault in F3 not R45, and busbar 4 is kept in service. The coordination margin delay of t_{cm} depends on the relays technology used in the system. For electromechanical relays, the coordination delay typically is considered 400 ~ 500 ms. However, using the nowadays breakers and digital relays, the delay can be further reduced typically to about 200 ms [42], which is used in this paper. As the multiples of t_{cm} are added into the relays operation time, last relays in the ring (R21 & R67) have long operating times. This long operating times are acceptable for most of the applications since the reduced fault currents close to the nominal value do not cause any damage to the equipment of IBMG [6]. If the system serves sensitive loads, the operating time becomes an important factor, and the definite time grading method will no longer be suitable. In this case, the communication assisted coordination must be employed in which the communication infrastructure and the microgrid central protection unit (MCPUC) is needed. In this method, all relays send their information (fault occurrence and direction) to the MCPUC. Now, the MCPUC processes the data and sends trip signals to the proper relays. In this case, the definite-time grading can be regarded as a redundant back-up scheme when the communication system fails. It is important to note that even in case of using a communication-assisted coordination scheme, the fault detection task is done by the proposed voltage-restraint negative sequence resistance. Then, the communication system failure does not result in the whole protection system failure since the fault detection is performed locally by the relays. This is the main difference between the proposed protection system and other existing methods based on communication infrastructure, in which both fault detection and coordination are done by MCPUC, and any communication system failure disrupts the whole protection system.

VI. SIMULATION RESULTS AND DISCUSSION

A. Simulation Results

To show the performance of the proposed fault detection method and protection strategy, the test system in Fig. 12 with the parameters given in Table II and Table III is simulated in the PSCAD/EMTDC environment. In this case, only the islanded operation of the system is considered, and VF-IBDERs are the sources in the MG. The voltage and frequency set-points of VF-IBDERs are obtained by conventional droop characteristics. To demonstrate the performance of the proposed method, different faults including SLG, LL and LLG faults at various locations (F1 to F6) are applied to the system. The operation times and the negative sequence resistances seen by all the relays for each fault are tabulated in Table IV and Table V, respectively. The negative sequence resistance setting for the relays is chosen as 26Ω (0.2 p.u. with $V_{base}=20$ kV and $S_{base}=3$ MVA). As shown in Table V, for all fault cases, the negative sequence resistances are considerably higher than the setting. To clarify more, the operation of all relays for an SLG fault (F3) is explained as an example. The output voltages and currents of VF-IBDERs are depicted in Fig. 13 during this fault. Also, the gains g_1 variation is shown in this figure. By fault occurrence, the gains g_1 decrease from 1 to 0.44 and 0.36 for VF-IBDER1 and VF-IBDER2, respectively. Accordingly, $Z_{VF-IBDER}$ increases from 0 to 0.68 p.u. and 0.64 p.u., for VF-IBDER1 and VF-IBDER2, respectively. The loads and line impedances are the reason for the difference between the obtained $Z_{VF-IBDER}$ values and the value given in (13). Also, as shown in Fig. 13, the output currents are limited to their maximum values as

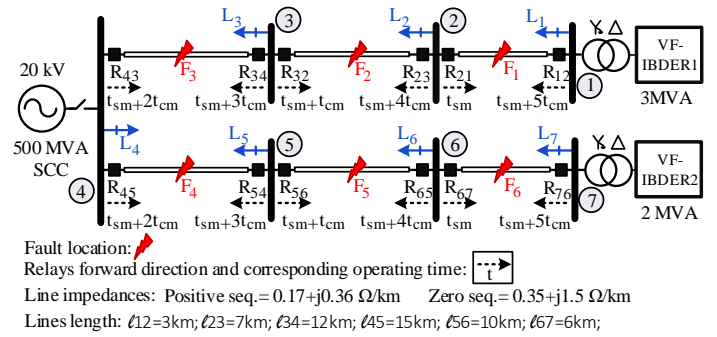


Fig. 12. A sample islanded microgrid with the given parameters in Table I and Table II.

expected. For this fault, the set of operating relays with forward direction are (R34, R23, R12) and (R43, R54, R65, R76). As shown in Table V, the negative sequence resistance seen by the relays in each set are close to each other, which corresponds to the resistance of the VF-IBDER in their behind (VF-IBDER1 for R34, R23, R12, and VF-IBDER2 for R43, R54, R65, and R76). Also, this resistance is about 0.7 times the VF-IBDER base impedance, which is in accordance with (18). The load impedance is the reason for the difference between the negative sequence resistances seen by the relays in each set. As mentioned earlier, the load impedances are in parallel with the VF-IBDER resistance. Therefore, they decrease the resistance seen by the relay.

Furthermore, the R-X diagram and negative sequence impedance trajectory of the relays R34 and R43 for the SLG short circuit at F3 are depicted in Fig. 14. In this figure, the real and imaginary axes represent the resistance and reactance of the negative sequence impedances seen by the relays, respectively. Under normal conditions, the negative sequence impedance is zero, then, the trajectory is at the origin of the R-X diagram. When a short circuit occurs, the impedance trajectory moves from the origin of R-X diagram to a final position corresponding to the steady-state operating point of the short circuit fault. Fig. 14 shows this final position with negative sequence resistances of -70Ω and -98.5Ω for R34 and R43, respectively. Both negative sequence resistances are considerably higher than the setting of 26Ω (0.2 p.u.) which results in correct operation of the relays. In fact, the relay timer starts to count whenever the impedance exceeds the relay setting (0.2 p.u.), and then, sends the trip command considering the definite-time protection coordination strategy as shown in Fig. 12 with dashed lines. Fig. 15 shows all the relays operation for this fault in which the horizontal axis represents the operating time of the relays, and the vertical axis shows the relays status with 0 (not tripped) or 1 (tripped). To clarify more, relay R43 first sends the trip command at 310 ms. after fault occurrence from the 2nd set of operating relays. In case of mal-operation of R43, R54 behaves as a backup relay which operates at 412 ms. From the 1st set, R34 is the main relay which responds at 412 ms, and R23 is the backup with 510 ms operating time for this fault. Looking at the operating times in Fig. 15 (and also Table IV), as it was expected, the relays are coordinated (with time intervals of 200 ms.) and they operate correctly when the fault occurs. The same explanation can be given for the faults at other locations.

It should be noted that, for the LLL faults, the negative sequence voltage and current do not exist, and the proposed fault detection scheme is not more effective. However, LLL faults rarely occur in power systems, and even LLL faults are normally begin with asymmetrical faults which may end up with LLL faults as the time goes by.

Table III. Parameters of the loads (with delta connection).

Loads	a-b		b-c		c-a	
	kW	p.f.	kW	p.f.	kW	p.f.
L ₁	124.5	0.96	125.1	0.97	131.9	0.97
L ₂	163.4	0.95	150.0	0.94	157.5	0.97
L ₃	158.1	0.95	145.8	0.94	151.6	0.96
L ₄	85.0	0.98	90.3	0.98	86.8	0.97
L ₅	92.7	0.94	89.8	0.95	95.2	0.95
L ₆	70.9	0.96	66.4	0.96	71.2	0.97
L ₇	67.7	0.96	59.0	0.96	67.6	0.98

TABLE IV

PERFORMANCE EVALUATION OF THE PROPOSED RELAYS IN AN ISLANDED MODE- OPERATING TIME (MS)

Loc.	type	R _{1,2}	R _{2,1}	R _{2,3}	R _{3,2}	R _{3,4}	R _{4,3}	R _{4,5}	R _{5,4}	R _{5,6}	R _{6,5}	R _{6,7}	R _{7,6}
F ₁	SLG	1010	113	×	313	×	510	×	710	×	910	×	1010
	LL	1016	115	×	314	×	513	×	712	×	915	×	1016
	LLG	1010	112	×	312	×	510	×	712	×	910	×	1010
F ₂	SLG	1010	×	910	312	×	510	×	712	×	910	×	1010
	LL	1016	×	915	314	×	512	×	712	×	910	×	1016
	LLG	1010	×	910	312	×	510	×	712	×	910	×	1010
F ₃	SLG	1010	×	910	×	712	510	×	712	×	910	×	1010
	LL	1016	×	910	×	712	513	×	712	×	910	×	1010
	LLG	1010	×	910	×	712	510	×	712	×	910	×	1010
F ₄	SLG	1010	×	910	×	712	×	510	712	×	910	×	1010
	LL	1016	×	910	×	712	×	512	712	×	910	×	1010
	LLG	1010	×	910	×	712	×	510	712	×	910	×	1010
F ₅	SLG	1016	×	915	×	712	×	510	×	312	910	×	1010
	LL	1016	×	915	×	712	×	512	×	314	910	×	1010
	LLG	1010	×	910	×	712	×	510	×	312	910	×	1010
F ₆	SLG	1016	×	915	×	712	×	510	×	312	×	112	1010
	LL	1016	×	915	×	715	×	512	×	313	×	114	1016
	LLG	1010	×	910	×	712	×	512	×	312	×	112	1010

TABLE V

PERFORMANCE EVALUATION OF THE PROPOSED RELAYS IN AN ISLANDED MODE- THE NEGATIVE SEQUENCE RESISTANCE SEEN BY THE RELAYS (Ω)

Loc.	type	R _{1,2}	R _{2,1}	R _{2,3}	R _{3,2}	R _{3,4}	R _{4,3}	R _{4,5}	R _{5,4}	R _{5,6}	R _{6,5}	R _{6,7}	R _{7,6}
F ₁	SLG	-88	-81	×	-89	×	-97.5	×	-102	×	-109	×	-115
	LL	-99.5	-88	×	-98	×	-110	×	-116	×	-126	×	-134
	LLG	-95	-86.5	×	-97	×	-108	×	-114	×	-123	×	-132
F ₂	SLG	-86	×	-78.5	-88.5	×	-97.5	×	-102	×	-108	×	-114
	LL	-98	×	-87.5	-99	×	-111	×	-118	×	-127	×	-136
	LLG	-94	×	-85	-96.5	×	-108	×	-114	×	-123	×	-132
F ₃	SLG	-82	×	-75	×	-70	-98.5	×	-103	×	-110	×	-116
	LL	-95	×	-85.5	×	-78	-113	×	-120	×	-130	×	-139
	LLG	-91	×	-82	×	-75	-109	×	-115	×	-124	×	-133
F ₄	SLG	-76	×	-70	×	-66	×	-65	-108	×	-115	×	-122
	LL	-91	×	-82	×	-75.5	×	-74	-124	×	-135	×	-144
	LLG	-87	×	-78.5	×	-72.5	×	-71	-119	×	-129	×	-138
F ₅	SLG	-72	×	-66.5	×	-63	×	-62	×	-61.5	-122	×	-129
	LL	-87	×	-79	×	-73	×	-71	×	-70	-138	×	-149
	LLG	-84	×	-76	×	-70.5	×	-69	×	-67.5	-133	×	-143
F ₆	SLG	-69	×	-64.5	×	-61	×	-60	×	-60	×	-59.5	-135
	LL	-84.5	×	-77	×	-71	×	-69.5	×	-68.5	×	-67.5	-151
	LLG	-81	×	-73.5	×	-68	×	-67	×	-66	×	-65	-146

B. Discussion on the Achievements

Different methodologies for fault detection in IBMGs are compared in Table I in the introduction section. In this sub-section, the proposed method is also evaluated considering the same criteria used in Table I. The achievements are listed as below.

- An analytical short circuit fault model is derived for VF-IBDERs,
- A voltage-restraint negative sequence resistance fault detection quantity is proposed which is inspired by the derived inverter short circuit model. Having known the inverter behavior under

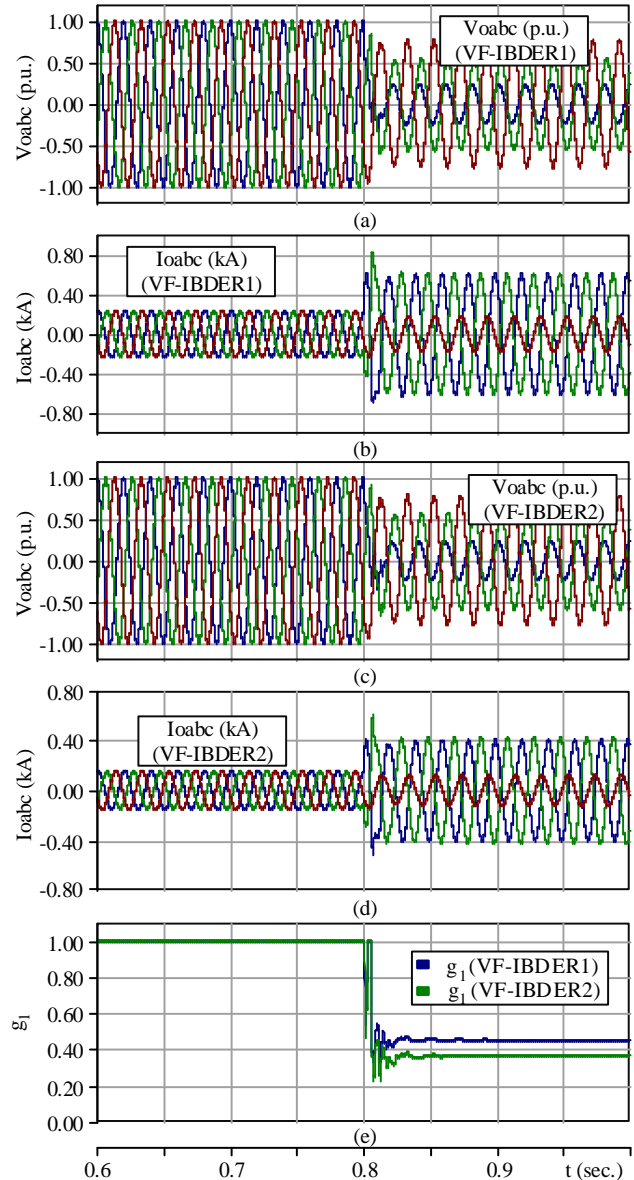


Fig. 13. Output voltages and currents of VF-IBDERs by occurrence of an SLG short circuit fault at F3, and corresponding g_1 values, (a) output voltages of VF-IBDER1, (b) output currents of VF-IBDER1, (c) output voltages of VF-IBDER2, (d) output currents of VF-IBDER2, (e) the variation of g_1 values.

short circuit conditions, this quantity provides clear discrimination between normal and short circuit conditions.

- The proposed scheme is effective considering both types of inverter control modes which are voltage/frequency (used in VF-IBDERs) and P/Q (used in PQ-IBDERs) control modes. Part “F” of section IV discusses the impact of PQ-IBDERs.
- Regarding the noise immunity of the proposed scheme, the fundamental frequency components of voltages and currents are used for negative sequence resistance calculation, therefore, the method performance cannot be affected by the system harmonics, noises, and non-fundamental components.
- As shown in Part “C” of section IV, by considering the worst possible cases for unbalanced loads, the load unbalanced condition does not impair the proposed method functionality (contrary to the methods based on negative sequence currents).
- The proposed method does not use the current amplitude as a feature for fault detection which makes it useful for fault detection in an islanded inverter-based microgrid with reduced fault current amplitudes (unlike over-current protection).
- The proposed fault detection scheme only uses the local

voltage and current waveforms. Then, the information from other points of the network is not needed. Then, the communication infrastructure is not required for fault detection. Therefore, the protection system security is increased.

- In the proposed method, the current signal is taken from the CT located in the relay busbar. Then, unlike the differential current protection, the proposed method is not sensitive to CTs mismatch, improving the protection system security.
- Further to negative sequence resistances amplitude which is used for fault occurrence detection, its sign reveals the fault direction. A negative sign corresponds to the forwards direction and vice versa. Then, by knowing both fault occurrence and its direction, the proposed quantity can be used effectively in available coordination schemes (communication-assisted coordination or time-delay based grading). The voltage-based schemes lack this feature resulting in difficulty in the protection coordination.
- The existing impedance-based scheme (namely distance protection) relies on the measurement of the positive sequence impedance which logically calculates the positive-sequence impedance of the line from the relay location to the fault point. The calculated impedance and the operation threshold (which is 80% of the protected line impedance) are very small values for microgrids with short lines, and then, the impedance-based distance relays suffer from accuracy for MG protection. Unlike conventional impedance-based relays, the proposed negative sequence quantity is zero under normal conditions, but increases considerably under short circuit conditions (0.7 p.u.~ 0.8 p.u.- the base for per unit is the converter nominal power). Therefore, it accurately discriminates the short circuit conditions from normal conditions.
- The proposed fault detection method can be used either in the time-delay based grading method or in the communication-assisted coordination strategy.
 - time-delay based grading: Using this scheme, neither for fault occurrence and direction detection nor for coordination, the communication system is not needed. Then, both detection and coordination tasks are done locally by the relays which is the most cost-effective way for implementing the protection system. However, the delayed operation is the disadvantage of this approach. Usually, this delayed operation is acceptable considering the low short circuit fault magnitudes in IBMGs, and then, less damage to the equipment. In case of requiring fast operation of the relays for sensitive loads, the second remedy should be employed.
 - communication assisted coordination strategy: In this scheme, the fault occurrence and its direction are still obtained locally by the relays using the proposed negative sequence resistance quantity. Both fault detection and its direction information are collected from all the relays in the system and sent to the MCU. Now, the MCU identifies the exact location of the fault and commands the corresponding relays for clearance. As the communication system is only used for coordination purposes, its failure does not impair the protection system if the time-delay based grading is used as a back-up. This is the advantage of the proposed protection scheme over other schemes relying on the communication systems.
- Differential protection-based methods suffer from low accuracy considering distributed loads in the system. Despite the spot loads, the distributed loads are directly connected to

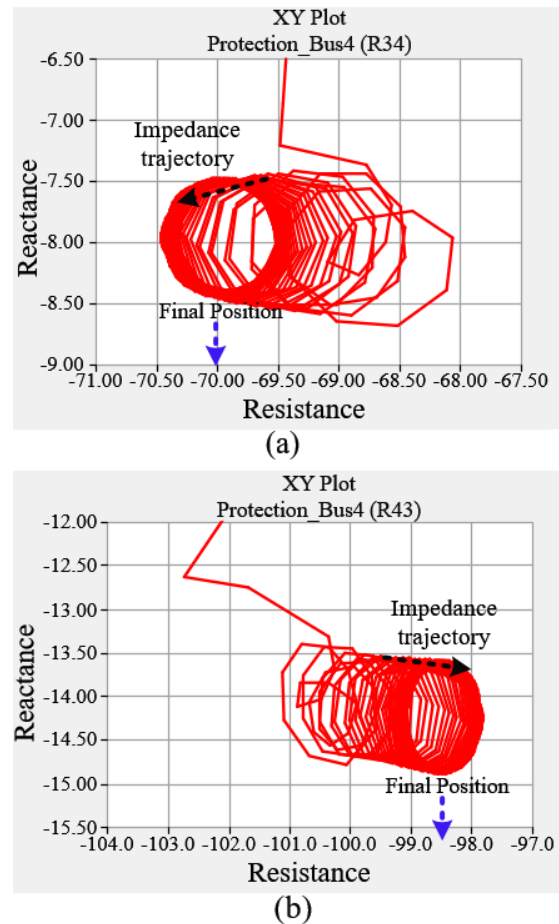


Fig. 14. The negative sequence impedance trajectory in R-X diagram for (a) relay R34, (b) relay R43 under F3 single-line-to-ground short circuit fault.

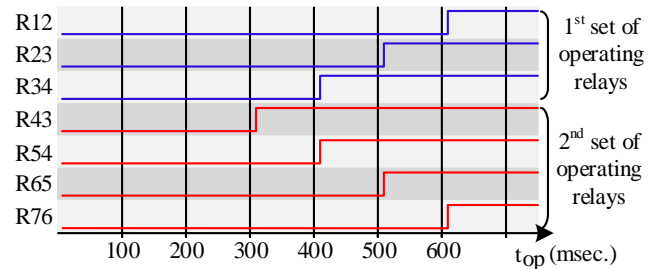


Fig. 15. The operating times of the system relays for a single-line-to-ground short circuit fault at F3.

the lines and not busbars resulting in a current mismatch even under normal conditions in the differential scheme. The proposed method only uses the local information which makes it insensitive to the distributed loads.

VII. CONCLUSION

This paper proposes a system protection strategy for islanded inverter-based micro-grids (IBMGs) containing voltage- frequency controlled inverter-based distributed energy resources (VF-IBDERs) as IBMG sources. The strategy includes *i*) short circuit fault modeling of VF-IBDERs, *ii*) a fault detection method, and *iii*) a protection coordination strategy. First, the control structure of VF-IBDERs under a short circuit condition has been presented. Then, sequence component networks are derived to specify the VF-IBDERs behavior under short circuit conditions. Next, using the sequence networks, a voltage-restrained negative-sequence resistance-based fault detection method is proposed. This method

does not rely on large fault current magnitudes, and therefore, makes it applicable to the IBMG in an islanded mode. This fault detection method does not need any communication infrastructure. Also, this method can be implemented in digital relays. Using the proposed fault detection method, a local definite time grading approach is employed for protection coordination. This remedy also does not require a communication link. However, it can be regarded as a backup coordination approach when the communication infrastructure, and consequently, the microgrid central protection unit (MCPU) performs the coordination task. Several fault conditions including SLG, LL and LLG faults at different locations are performed on a test IBMG system using time-domain simulations in PSCAD/EMTDC environment to show the performance of the proposed protection system.

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