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An Embedded Enhanced-boost Z-source Inverter Topology with Fault-Tolerant Capabilities

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Abstract—**This paper proposes an Embedded Enhanced-Boost Z-Source Inverter (EEB-ZSI) with fault tolerant capabilities for PV applications. Compared with the prior-art Embedded Source Inverters (E-ZSI) and Enhanced-boost Z-source Inverter (EB-ZSI), the proposed topology features that when one dc source like one PV panel is short circuit (SC) or open circuit (OC), the inverter can tolerate the faults and still operate with a compromised conversion ratio. However, the conversion ratio is still larger than the traditional E-ZSI. This topology can be further applied to the cascaded H-bridge inverter systems for multi-level applications with fault-handling capabilities. A detailed fault-tolerant analysis is conducted on the EEB-ZSI and simulations are provided to validate the analysis. Small signal modelling, analysis, cascading operation, and experimental verification will be provided in the final version.**

Keywords- Impedance source converter, embedded source converter, fault-tolerant circuit,

I. INTRODUCTION

Traditional Voltage Source Inverters (VSIs) are widely used in industrial applications, e.g., motor drives, distributed power systems, and hybrid electric vehicles [1], which are typically operated in the buck operation mode. Generally, a dc-dc boost converter is added to obtain a desired ac output. However, this two-stage power conversion increases the system cost and lowers the efficiency. The Z-source inverter shown in Fig. 1 [2] as a single-stage conversion effectively tackles those issues. Hence, many attempts have been made in recent years to improve the performance of Z-sources inverters through topological innovations and advanced control schemes [3]-[12].

In order to increase the boost capability, more passive components (inductors, capacitors and diodes) should be added into the classic Z-source network in Fig. 1. For instance, a switched inductor (SL) Z-source inverter [3] as shown in Fig. 2 adopts two SL cells to replace the two inductors (L_1 and L_2) in the traditional Z-source inverter, and thus leading to a higher conversion ratio. Based on the SL-ZSI topology, modified topologies were developed [4]-[10] to further increase the boost ratio. In [9], a topology with switched impedance network was introduced, as shown in Fig. 3, which can achieve an even higher boost factor due to the shorter shoot-through duration and a larger modulation index. However, the inverter volume also increases because of the extra inductors and/or capacitors.

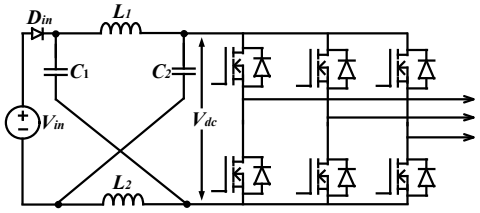

Fig. 1. Classic three-phase Z-source inverter.

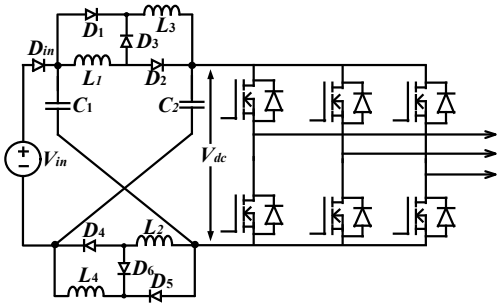

Fig. 2. Three-phase switched-inductor Z-source inverter [3].

Additionally, the dc current of Z-source inverters is normally chopped due to the shoot-through operation. To address this problem, a number of embedded Z-source inverters were proposed [11], [12], which may also achieve lower capacitor voltage ratings. A typical parallel-embedded Z-source inverter (E-ZSI) is shown in Fig. 4, where it can be observed that two dc sources (e.g., PV panels) are directly connected in series with the inductors (i.e., L_1 and L_2) of the classic ZSI in Fig. 1. This topology is especially suitable for PV or fuel cell systems.

Inspired by the above, in this digest, a new topology with fault-tolerance capabilities is proposed by modifying the embedded Z-source and switched impedance-source inverters. The proposed topology has a good capability of fault-tolerance if an open circuit or a short circuit happens in the system; however, the boost factor remains to be a relatively large value. In § II, the operation principle of the proposed topology under normal operation and fault operation is presented. Comparisons with normal operation and fault operation are performed, and the benchmarking results are

shown in § II. Simulation results are provided in § III, which verify the high performance of the proposed Z-source topology in terms of high boost factor and fault-tolerance capabilities

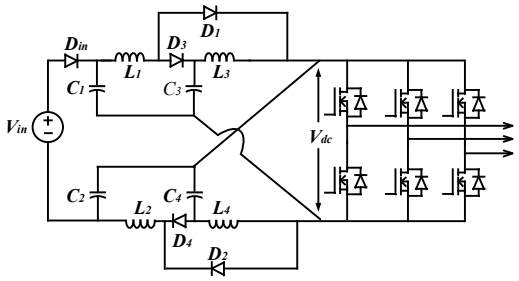

Fig. 3. Enhanced-boost Z-source inverter [8].

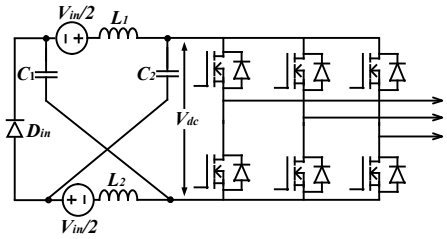

Fig. 4. Parallel-embedded Z-source inverter [11].

II. PROPOSED Z-SOURCE INVERTER

A. Operation principle of the proposed topology

Fig. 5 shows the topology of the proposed Embedded Enhanced-Boost Z-Source Inverter (EEB-ZSI), where two symmetrical Z-source networks with embedded dc sources. The operation principle of the EEB-ZSI is the same as that of the conventional ZSI: the shoot-through state and non-shoot-through state.

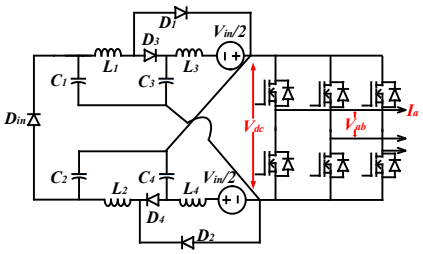

Fig. 5. Proposed three-phase embedded enhanced-boost Z-source inverter.

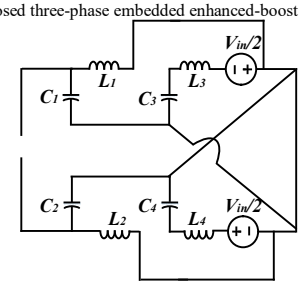

Fig. 6. Shoot-through state of the proposed Z-source inverter.

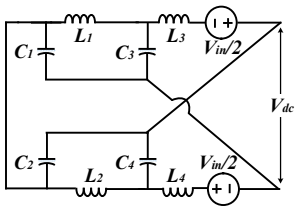

Fig. 7. Non-shoot-through state of the proposed Z-source inverter.

The equivalent circuits of the proposed Z-source converter in the shoot-through state and non-shoot-through state are shown in Figs. 6 and 7, respectively. It is assumed that all capacitors (and inductors) in the proposed topology are identical. Moreover, the dc sources in the two Z-source networks are the same. According to the topological symmetry, it can be obtained that

$$V_{C1} = V_{C2} \qquad V_{C3} = V_{C4} \tag{1}$$

in which V_{C1}, V_{C2}, V_{C3}, and V_{C4} are the corresponding voltage across the capacitor C_1, C_2, C_3, and C_4. As mentioned above, the operation can be separated into two states:

Shoot-Through State. As shown in Fig. 6, D_1 and D_2 are ON with D_3, D_4, and D_{in} are being reverse-biased in the shoot-through state. Additionally, L_1 and L_2 are in parallel with C_1 and C_2, respectively. Then, it can be obtained that

$$V_{C1} = V_{C2} = V_{L1} = V_{L2} \tag{2}$$

According to the Kirchhoff's voltage law, the voltages on the inductors L_3 and L_4 can be expressed as

$$V_{L3} = V_{C3} + 0.5V_{in} \tag{3}$$

$$V_{L3} = V_{C3} + 0.5V_{in} \tag{4}$$

with V_{L1}, V_{L2}, V_{L3}, and V_{L4} being the inductor voltages in the shoot-through state.

Non-Shoot-Through State. As shown in Fig. 7, D_3, D_4, and D_{in} are ON, and D_1 and D_2 are OFF. In one cycle, the inductor average voltage should be zero, and then applying the volt-second balance principle to all the inductors gives

$$V_{L1-NON} = -\frac{D}{1-D}V_{C1} \tag{5}$$

$$V_{L3-NON} = -\frac{D}{1-D}\left(V_{C3} + 0.5V_{in}\right) \tag{6}$$

Furthermore, according to Fig. 7, the following can be obtained by applying the Kirchhoff's voltage law:

$$V_{L1-NON} + V_{C3} - V_{C1} = 0 \tag{7}$$

$$V_{L1-NON} + V_{L3-NON} - 0.5V_{in} + V_{C2} = 0 \tag{8}$$

$$V_{L3-NON} - 0.5V_{in} + V_{dc} - V_{C3} = 0 \tag{9}$$

Accordingly, the capacitor voltage V_{C3} and the peak dc-link voltage $\hat{V}_{dc}$ can be expressed as

$$V_{C3} = \frac{0.5}{2D^2 - 4D + 1}V_{in} \tag{10}$$

$$\hat{V_{dc}} = \frac{1-D}{2D^2-4D+1}V_{in} = B \cdot V_{in} \tag{11}$$

where

$$B = \frac{1-D}{2D^2-4D+1} \tag{12}$$

is the boost factor.

The peak output voltage of the inverter is expressed by

$$\begin{cases} \hat{V_{ac}} = 0.5 \cdot M \cdot V_{dc} \\ \hat{V_{ac}} = 0.5 \cdot M \cdot B \cdot V_{dc} \\ \hat{V_{ac}} = 0.5 \cdot G \cdot V_{dc} \end{cases} \tag{13}$$

in which G is the buck-boost factor, M is the modulation index, and V_{dc} is the average dc-link voltage. The buck-boost factor can be represented in terms of modulation index M as:

$$G = M \cdot B = \frac{M^2}{2M^2-1} \tag{14}$$

B. Fault-tolerant analysis

Open circuit analysis: The open circuit condition of the proposed topology is shown in Fig. 8.

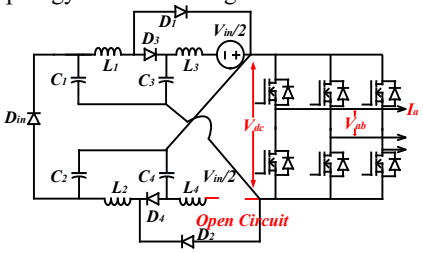

Fig. 8. Open circuit condition of the proposed EEB-ZSI.

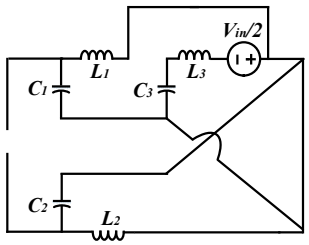

Fig. 9. Shoot-through state of the proposed Z-source inverter under open circuit condition.

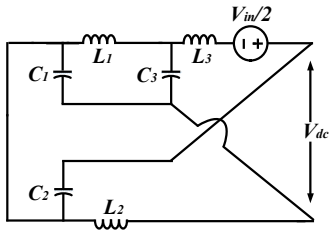

Fig. 10. Non-shoot-through state of the proposed Z-source inverter under open circuit condition.

The operation principle in this condition is different from the normal EEB-ZSI due to the open circuit. The equivalent circuits during the shoot-through state and non-shoot-through state are shown in Figs. 9 and 10, respectively.

With the previous analysis, it is known that D_2 is on and D_4 is reverse-biased in these two states and the following equations can be obtained:

$$\hat{V_{dc}} = \frac{1-D}{D^2-3D+1}V_{in} \tag{15}$$

$$G = M \cdot B = \frac{M^2}{M^2+M-1} \tag{16}$$

Short circuit analysis: When one dc source is short-circuited, the corresponding hardware schematic is shown in Figs. 11, 12 and 13.

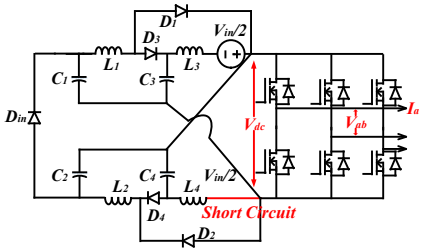

Fig. 11. Open circuit condition of the proposed EEB-ZSI.

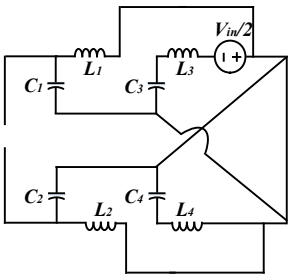

Fig. 12. Shoot-through state of the proposed Z-source inverter under short circuit

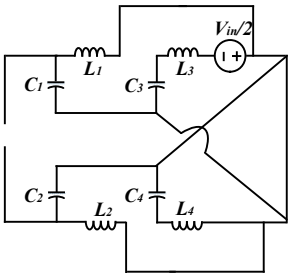

Fig. 13. Non-shoot-through state of the proposed Z-source inverter under short circuit.

The operation principle in this condition is the same as the normal EEB-ZSI. Thus, a similar analysis can be applied, and the boost factor can be derived as

$$\hat{V_{dc}} = \frac{1-D}{2D^2-4D+1} \cdot \frac{1}{2} V_{in} \tag{17}$$

$$G = M \cdot B = \frac{0.5M^2}{2M^2-1} \tag{18}$$

A detailed comparison in terms of the boost factor is shown in Table I. Fig. 14 shows the relationship between the shoot-through duty ratio and the boost factor among these topologies. Although the boost factor of the proposed EEB-ZSI during open circuit or short circuit is lower than that of the normal operation of the EEB-ZSI, it is higher than the traditional E-ZSI, as observed in Fig. 14. In addition, Fig. 15 compares the voltage gains in respect to the modulation index. It can be seen in Fig. 15 that the voltage gain of the proposed impedance-source topology under normal or fault operation is higher than the conventional E-ZSI. Moreover, the voltage gain can be maintained by controlling the modulation index to achieve fault-tolerant operation. Additionally, the topology can be extended with cascaded H-bridge converters in order to achieve multi-level voltages while maintaining the fault-tolerant capability.

	EEB-ZSI[8]	OC-EEB-ZSI	SC-EEB-ZSI	E-ZSI[11]
B	$\frac{1}{2D^2-4D+1}$	$\frac{1-D}{D^2-3D+1}$	$\frac{1-D}{D^2-3D+1}\cdot\frac{1}{2}$	$\frac{1}{1-2D}$
$G-M$	$G=\frac{M}{2M-1}$	$G=\frac{M^2}{M^2+M-1}$	$G=\frac{0.5M^2}{2M^2-1}$	$G=\frac{M}{2M-1}$

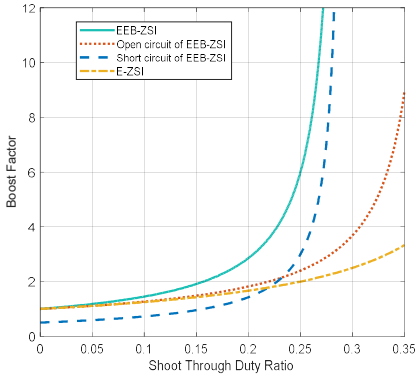

Fig. 14. Boost factor comparison between topologies.

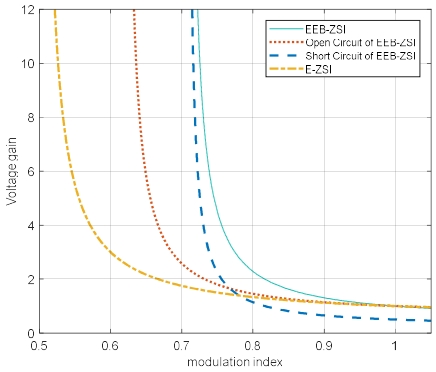

Fig. 15. Voltage gain comparison between topologies.

III. SIMULATION RESULTS

Referring to Figs. 5-13, simulations are performed in PLECS with the system parameters being $L_1=L_2=L_3=L_4=350$ μH and $C_1=C_2=C_3=C_4=250$ μF, switching frequency $f_s=10$ kHz, and three phase load L = 5 mH and R = 25 Ω. The simulation results are shown in Figs. 16-18, where M = 0.75, D = 0.25, and V_{in} = 100 V. As it can be seen from Fig. 16-18, the proposed inverter can operate normally under open circuit and short circuit conditions, and the peak dc-link voltage V_{dc} under three cases are, respectively, boosted to 600, 120, and 300 V. The simulation results are in agreement with the theoretical analysis and comparison in Table I.

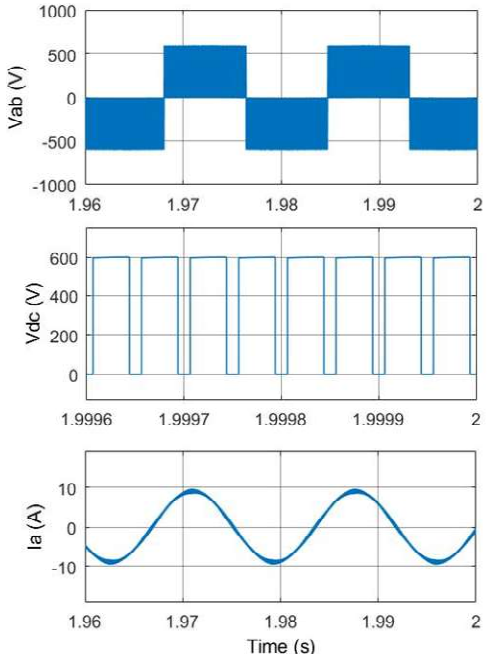

Fig. 16. Simulation results of the proposed EEB-ZSI.

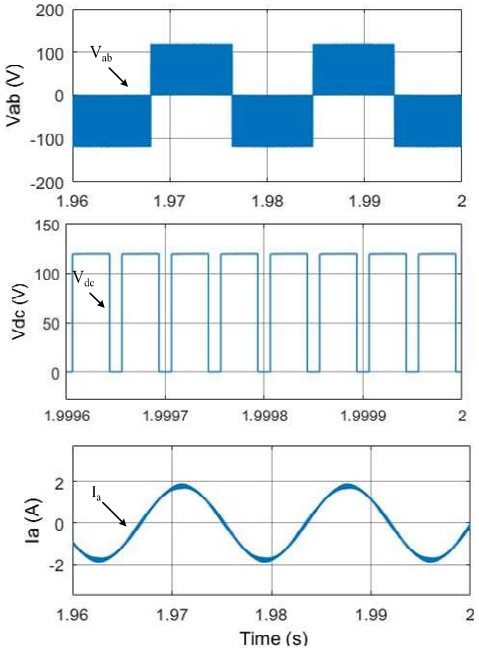

Fig. 17. Simulation results of the proposed EEB-ZSI under open circuit condition for one of the DC sources.

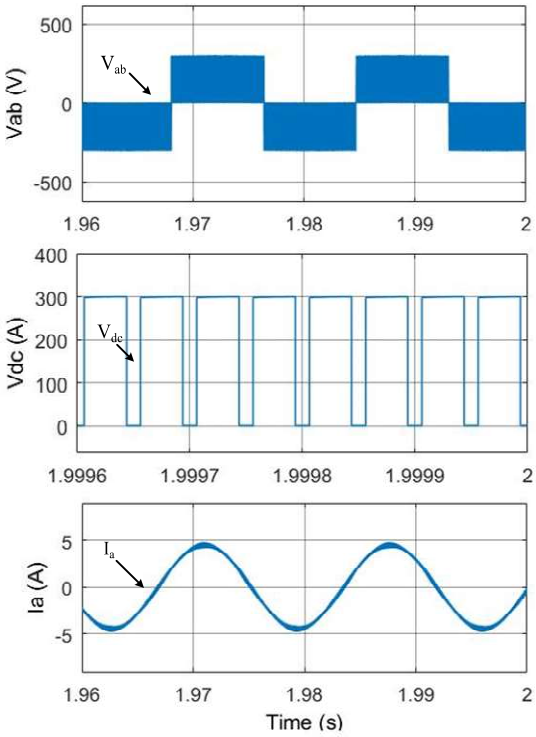

Fig. 18. Simulation results of the proposed EEB-ZSI under short circuit condition for one of the DC sources.

IV. CONCLUSION

In this paper, an embedded enhanced-boost Z-source inverter with fault-tolerant capabilities has been proposed. Compared with the traditional embedded ZSI, the boost factor of the proposed topology is much higher. Additionally, the proposed topology has a fault-tolerant capability which cannot be achieved in the conventional enhanced-boost ZSI. Simulation results have demonstrated that the proposed topology has a good boost capability compared with the traditional embedded ZSI and a good fault-tolerant capability compared with the conventional enhanced-boost ZSI. Future work includes the experimental verification and further cascaded H-bridge applications in PV systems considering the fault condition.

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