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A Multi-Structure, Multi-Mode Three-Phase Dual-Active-Bridge Converter Targeting Wide-Range High-Efficiency Performance

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***Abstract*—Three-phase dual-active-bridge (3p-DAB) converter is an attractive topology for bidirectional power conversion in high-power applications. However, conduction loss and switching loss are two main loss mechanisms that severely affect its efficiency performance, and adoption of any single modulation scheme or topology cannot minimize these losses over a wide operating range. For this purpose, a reconfigurable topology of 3p-DAB converter is proposed in this paper that utilizes a reconfigurable and tunable resonant network to offer multiple degrees-of-freedom (DoF) in minimizing conduction and switching losses over a wide range of operating conditions. The converter is designed such that for 40 $\%$ to 100 $\%$ of the rated output power, it operates as a tunable 3p-DAB resonant immittance converter with its output power controlled by varying switching frequency and tuning the resonant frequency of a resonant immittance network to track the switching frequency. Below 40 $\%$ of the rated output power, the converter transforms to a tunable 3p-DAB series resonant converter with its output power controlled by varying the impedance of a series resonant network while keeping the switching frequency and phase-shift constant. The combination of both operation modes jointly leads to wide-range zero circulating current and soft-switching of all the switches, and hence a wide-range high-efficiency performance as validated by the experimental results.**

***Index Terms*—DC-DC power conversion; immittance converters (ICs); resonant power conversion; series resonant network; unity power factor; zero-voltage switching (ZVS)**

NOMENCLATURE

3p	Three-phase
DAB	Dual-active-bridge
ZVS	Zero voltage switching
SPS	Single phase-shift
DoF	Degree-of-freedom
RMS	Root-mean-square
DABRIC	Dual-active-bridge resonant immittance converter
DABSRC	Dual-active-bridge series resonant converter
RTRN	Reconfigurable and tunable resonant network
TRIN	Tunable resonant immittance network
TSRN	Tunable series resonant network
SCC	Switch-Controlled Capacitor
DFM	Dynamic frequency matching
$D_{\rm p}$	Duty cycle of switches in the primary-bridge
$D_{\rm s}$	Duty cycle of switches in the secondary-bridge
θ	Phase-shift between primary-bridge and secondary-bridge ac voltages
ψ	Control angle of SCC
ϕ	Phase angle of port currents
$f_{\rm s}$	Switching frequency
$f_{\rm s,max}$	Maximum switching frequency
$f_{\rm s,min}$	Minimum switching frequency
$\mathbf{X_A}$	Capacitive impedance comprising L_1 and C_1
$\mathbf{X_B}$	Inductive impedance comprising L_2 and C_2
$\omega_{\rm a}$	Angular series-resonance frequency of L_1 and C_1
$\omega_{\rm b}$	Angular series-resonance frequency of L_2 and C_2
$\omega_{\rm s}$	Angular switching frequency
$\omega_{\rm r}$	Angular resonance frequency of $\mathbf{X_A}$ and $\mathbf{X_B}$
$\omega_{\rm r,max}$	Maximum angular resonance frequency of $\mathbf{X_A}$ and $\mathbf{X_B}$
$\omega_{\rm r,min}$	Minimum angular resonance frequency of $\mathbf{X_A}$ and $\mathbf{X_B}$
$S_{{\rm N}x}$	Switches $S_{\rm N1}$, $S_{\rm N2}$, and $S_{\rm N3}$ in branch $\mathbf{X_A}$ used for transformation of network
$S_{{\rm T}x{\rm A}}$	Switches $S_{\rm T1A}$, $S_{\rm T2A}$, and $S_{\rm T3A}$ in branch $\mathbf{X_B}$ used for tuning $C_{2{\rm t}}$
$S_{{\rm T}x{\rm B}}$	Switches $S_{\rm T1B}$, $S_{\rm T2B}$, and $S_{\rm T3B}$ in branch $\mathbf{X_B}$ used for tuning $C_{2{\rm t}}$
S_{j1}, S_{j2}	Complimentary switches in the primary-bridge where j = A, B, and C is used for phase-designation
Q_{j1}, Q_{j2}	Complimentary switches in the secondary-bridge where j = A, B, and C is used for phase-designation
$C_{2{\rm t}}$	Tunable capacitors comprising base capacitors C_2 and switches $S_{{\rm T}x{\rm A}}$ and $S_{{\rm T}x{\rm B}}$
$P_{\rm o,max}$	Maximum output power of 3p-DABRIC
$P_{\rm o,min}$	Minimum output power of 3p-DABRIC
$X_{\rm max}$	Maximum impedance of $\mathbf{X_A}$ and $\mathbf{X_B}$
$X_{\rm min}$	Minimum impedance of $\mathbf{X_A}$ and $\mathbf{X_B}$
n	Transformer's turn ratio
$V_{\rm in}$	Dc input voltage of the converter
$V_{\rm o}$	Dc output voltage of the converter
G	Voltage ratio $nV_{\rm o}/V_{\rm in}$

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ϵ	Ratio of $P_{\mathrm{o,max}}$ to $P_{\mathrm{o,min}}$
σ	Ratio of $f_{\mathrm{s,max}}$ to $f_{\mathrm{s,min}}$
κ	Ratio of maximum $C_{2\mathrm{t}}$ to minimum $C_{2\mathrm{t}}$

I. INTRODUCTION

THREE-phase dual-active-bridge (3p-DAB) converter has been widely researched over the past few decades due to its superiority over other bidirectional power converter topologies in terms of modularity, lower component stress, higher power density, smaller input and output current ripple, smaller size of filter elements, galvanic isolation and inherent soft-switching operation [1]. Due to these advantages, 3p-DAB converter has been successfully applied in many emerging high-power applications such as solid-state transformers (SSTs), vehicle-to-grid (V2G) operation, uninterruptible power supplies (UPS) and dc microgrids.

The conventional 3p-DAB converter comprises of two three-phase half bridges interfaced by a three-phase high-frequency isolation transformer. The simplest modulation scheme for 3p-DAB converter is the single phase-shift (SPS) modulation where two phase-shifted high-frequency ac-voltages are applied across transformer's leakage inductances for power flow control. The power flows from the leading to lagging ac-voltage with the phase-shift being used as a control variable to control the output power. However, SPS modulation suffers from the drawbacks of high circulating current and narrow zero-voltage switching (ZVS) range which is sensitive to input-to-output voltage ratio and load conditions. This makes it extremely challenging to maintain a high-efficiency operation of an SPS-controlled 3p-DAB converter for applications where the input-to-output voltage ratio is prone to wide-range variations.

To overcome the drawbacks of SPS modulation, various modulation schemes have been proposed for 3p-DAB converter that make use of additional degree-of-freedom (DoF) for more efficient power flow control at the expense of increased control complexity. The control variables available for modulating 3p-DAB converter are the duty cycles (D_{p}, D_{s}) of the complimentary switches in the primary and secondary bridge, phase-shift (θ) between the primary-bridge and secondary-bridge ac voltages, and the switching frequency (f_{s}). Simultaneous control of two control variables gives rise to a two degree-of-freedom (2-DoF) modulation scheme for 3p-DAB converter. The most popular 2-DoF modulation scheme reported for 3p-DAB converter is the duty-cycle plus phase-shift modulation where the complimentary switches in both active bridges are modulated simultaneously with the same duty cycle (i.e. $D_{\mathrm{p}} = D_{\mathrm{s}} = D$) in conjunction with the modulation of phase-shift θ [2]–[5]. The advantages of this modulation scheme stem from its ability to generate and control the pulse-width of the zero voltage levels in the phase voltages (for the duty cycle range $0<D<1/3$) that can help to minimize reactive power flow due to the zero voltage levels and improve light-load efficiency. However, with reduced load (i.e. smaller values of D), the inductor current and energy flow through the converter becomes increasingly discontinuous. Moreover, difficulty in the selection of optimal values of multiple control variables (D, θ) and high circulating current under heavy-load conditions are some of the drawbacks of this modulation scheme. Another 2-DoF modulation scheme was reported in [6], [7] that utilized phase-shift (θ) and switching frequency (f_{s}) as control variables to achieve a narrow frequency range for output power modulation and simplify close-loop implementation. However, the optimal efficiency performance of this modulation scheme remains highly sensitive to the input-to-output voltage ratio. To further enhance control flexibility, 3-DoF modulation schemes were proposed in [8], [9] that utilized three control variables D_{p}, D_{s}, and θ, where $D_{\mathrm{p}} \neq D_{\mathrm{s}}$, simultaneously for power flow control. These 3-DoF modulation schemes were reported to achieve better performances in terms of reduced conduction loss and extended ZVS range [10]; however, they produce asymmetrical voltage waveforms that lead to increased reactive current flow. In addition, the extensive computational efforts involved in the optimization of three control variables D_{p}, D_{s} and θ for different input-to-output voltage ratios render their implementation challenging.

In conjunction with the design of modulation schemes, another approach that has been widely researched for enhancing the efficiency of 3p-DAB converter is based on topological variations. In this context, multi-level 3p-DAB converters have been widely investigated that offer the advantages of symmetrical voltage waveforms containing more voltage levels that helps to reduce reactive current flow as well as to lower device stresses. For example, a T-type three-level 3p-DAB converter was proposed in [11]–[13] that was capable of producing a three-level ($+V_{\mathrm{DC}}/2$, 0, $-V_{\mathrm{DC}}/2$) symmetrical voltage waveform. The ability to control the duration of the zero-voltage state with this topology favors the minimization of reactive power flow and extension of ZVS range as compared to two-level ($+V_{\mathrm{DC}}/2$, $-V_{\mathrm{DC}}/2$) operation of 3p-DAB converter. However, the issue of circulating current remains unsolved as the phase-current continues to circulate in the converter during the zero-voltage state. For reducing the circulating current, a π-type four-level 3p-DAB converter was proposed in [14]. This topology was capable of producing a four-level ($+V_{\mathrm{DC}}/2$, $+V_{\mathrm{DC}}/6$, $-V_{\mathrm{DC}}/2$, $-V_{\mathrm{DC}}/6$) symmetrical voltage waveform leading to a more flexible output power control and wide-range zero circulating current. However, increased complexity and higher component count are some of the disadvantages of this topology. Another modified topology of 3p-DAB converter was proposed in [15]–[17] that comprises of three parallel 120$^{\mathrm{o}}$ phase-shifted H-bridges at the primary side. This topology offers the freedom to utilize the internal phase-shift between the two legs of the same H-bridge to generate a three-level ($+V_{\mathrm{DC}}$, 0, $-V_{\mathrm{DC}}$) symmetrical ac voltage with adjustable duty ratio. This topology was also proposed to limit reactive power flow and reduce conduction loss; however, it still failed to achieve wide-range ZVS operation. The concept of a modified auxiliary-resonant commutated pole was applied to 3p-DAB converter in [18] to achieve wide-range ZVS operation; however, conduction loss cannot be minimized using this approach.

In addition to the different modulation schemes and multi-level topologies, resonant-variants of 3p-DAB converter have

also been investigated extensively with the objective to enhance its efficiency performance. The insertion of different resonant networks to the high-frequency ac-link of 3p-DAB converter offers another DoF in achieving additional desirable characteristics such as dc-bias blocking capability, lower RMS phase current, extended ZVS range, and unity-power-factor operation [19]–[26]. For example, the series-capacitor in a 3p-DAB series resonant converter (3p-DABSRC) helps to remove the dc-bias in the phase-current [27], [28]. Moreover, the sinusoidal current in 3p-DABSRC gives rise to lower RMS value as compared to the piecewise linear current in non-resonant 3p-DAB converter, thus leading to a lower conduction loss. However, the conduction loss and ZVS operation of 3p-DABSRC are still sensitive to the input-to-output voltage ratio. To achieve ZVS operation independent of input-to-output voltage ratio, a 3p-DAB resonant immittance converter (3p-DABRIC) was proposed in [21] which enables a precise control of the phase current phasor and thus, leads to full-range ZVS operation independently of input-to-output voltage ratio. However, it suffers from severe circulating current under light-load conditions leading to poor light-load efficiency. A second mode of operation was proposed for 3p-DABRIC in [21] to achieve in-phase relationship between the voltages and currents at all ports of the immittance network which leads to the elimination of reactive power and minimum conduction loss. However, 33 $\%$ of the switches undergo hard-switching in this mode of operation.

From the extensive literature review conducted, it can be concluded that it is very challenging if not impossible to achieve full-range ZVS operation and wide-range zero circulating current simultaneously with any one modulation scheme or topology of 3p-DAB converter. This has motivated us to propose the idea of a reconfigurable topology and modulation scheme that can dynamically adapt to varying operating conditions while ensuring that conduction loss and switching loss are minimized simultaneously over the whole operating range. To meet this objective, a reconfigurable topology of 3p-DAB converter is proposed in this paper that utilizes a reconfigurable and tunable resonant network for achieving a multiple DoF control of the 3p-DAB converter with the objective of maximizing its efficiency under widely varying operating conditions. The converter is designed such that from 40 $\%$ to 100 $\%$ of the rated output power, it operates as a tunable 3p-DABRIC with its output power controlled by varying the switching frequency and tuning the resonant frequency of the immittance network by means of a switch-controlled capacitor (SCC). This gives rise to a unity-power-factor operation that eliminates all circulating current and reactive power flow. Moreover, all switches undergo ZVS independently of the input-to-output voltage ratio under this operation mode. This allows boosting the efficiency performance for medium-to-high output power levels. Below 40 $\%$ of the rated output power, the converter transforms to a tunable 3p-DABSRC with its output power controlled by varying the impedance of a series resonant network using SCC while keeping the switching frequency and phase-shift at the optimal values as determined by the input-to-output voltage ratio. This operation mode ensures minimum-tank-current operation that minimizes conduction loss and full-range ZVS operation is achieved for all switches leading to enhanced efficiency performance for low-to-medium output power levels. The combination of both operation modes, therefore, leads to a wide-range high-efficiency performance of the proposed converter by minimizing both the switching and conduction losses simultaneously.

The paper is organized as follows. Section II introduces the proposed three-phase reconfigurable and tunable resonant network. The proposed 3p-DAB topology is discussed in Section III. The modeling and analysis of the two operating modes of the proposed 3p-DAB topology, namely, 3p-DABRIC and 3p-DABSRC, are discussed in Sections IV and V, respectively. The prototype design and experimental results are discussed in Section VI. Finally, the concluding remarks are presented in section VII.

II. PROPOSED THREE-PHASE RECONFIGURABLE AND TUNABLE RESONANT NETWORK

The proposed three-phase reconfigurable and tunable resonant network (3p-RTRN) is a delta-connected network consisting of two types of impedances labeled as $\mathbf{X_A}$ and $\mathbf{X_B}$ as shown in Fig. 1. $\mathbf{X_A}$ consists of switch $S_{\mathrm{N}x}$, inductor L_1 and, capacitor C_1, whereas $\mathbf{X_B}$ consists of inductor L_2, capacitor C_2 and switches $S_{\mathrm{T}x\mathrm{A}}$, $S_{\mathrm{T}x\mathrm{B}}$ (where x = 1, 2, and 3). $\mathbf{X_A}$ is constrained to operate below the series resonance frequency ω_{a} of L_1 and C_1, $i.e.$ $\omega_{\mathrm{a}} > \omega_{\mathrm{s}}$, to constitute an overall capacitive impedance. On the contrary, $\mathbf{X_B}$ is constrained to operate above the series resonance frequency ω_{b} of L_2 and C_2, $i.e.$ $\omega_{\mathrm{b}} < \omega_{\mathrm{s}}$, to constitute an overall inductive impedance. The switches $S_{\mathrm{N}x}$ in $\mathbf{X_A}$ are used to connect or isolate the

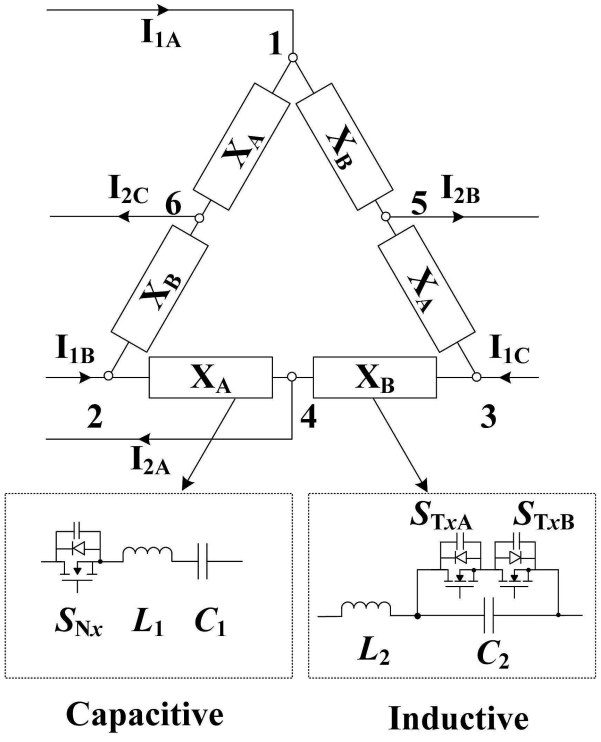

Fig. 1. Proposed reconfigurable and tunable resonant network.

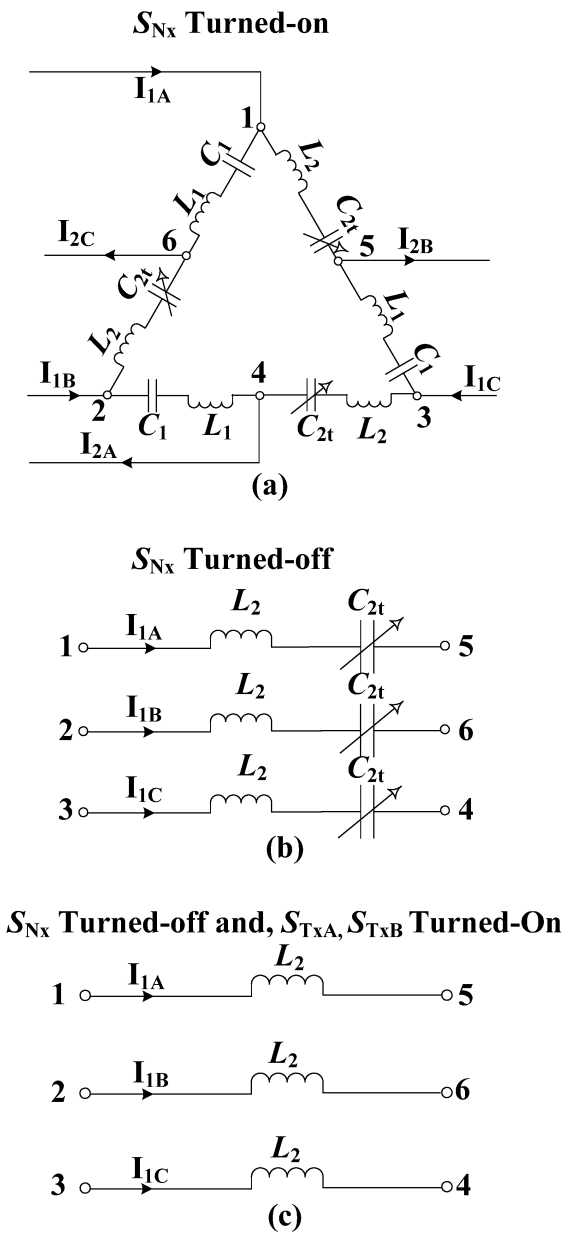

Fig. 2. (a) Three-phase tunable resonant immittance network; (b) Three-phase tunable series resonant network; and (c) Three-phase series inductors.

capacitive impedance $\mathbf{X_A}$ from the network, thus enabling the transformation of the network into different configurations. It should be noted that $\mathbf{X_A}$ can be fully isolated using only a two-quadrant switch as the body diode of $S_{\mathrm{N}x}$ is kept in a reverse biased stated by the voltage across C_1 when $S_{\mathrm{N}x}$ are turned off.

The switches $S_{\mathrm{T}x\mathrm{A}}$ and $S_{\mathrm{T}x\mathrm{B}}$ in $\mathbf{X_B}$ are used to electronically control the capacitance of C_2, thus enabling the control of the series impedance and tuning of the resonance frequency ω_{b} of L_2 and C_2. Regarding the labeling of the network terminals shown in Fig. 1, the following conventions are adopted: terminals 1, 2, and 3 represent the input ports of the network, whereas terminals 4, 5, and 6 represent the output ports of the network. Furthermore, subscripts $1j$ (where j = A, B, and C) are used to denote the parameters ($e.g.$, line currents) at the input ports of the network, whereas the subscripts $2j$ (where j = A, B, and C) are used to denote the parameters ($e.g.$, line currents) at the output ports of the network.

Depending upon the state of switches $S_{\mathrm{N}x}$, $S_{\mathrm{T}x\mathrm{A}}$ and $S_{\mathrm{T}x\mathrm{B}}$, 3p-RTRN can transform between three different network configurations. The configuration of Fig. 2(a) is obtained when $S_{\mathrm{N}x}$ are turned on. This action connects the capacitive impedance $\mathbf{X_A}$ to the network and thus transforms the network to a three-phase tunable resonant immittance network (3p-TRIN). To simpify the drawing, $S_{\mathrm{N}x}$ are not shown in Fig. 2(a) whereas $S_{\mathrm{T}x\mathrm{A}}$, $S_{\mathrm{T}x\mathrm{B}}$ and C_2 are represented by a tunable capacitor $C_{2\mathrm{t}}$. The configuration of Fig. 2(b) is obtained when $S_{\mathrm{N}x}$ are turned off. This action isolates $\mathbf{X_A}$ from the network and thus transforms the network to a three-phase tunable series resonant network (3p-TSRN). The third configuration shown in Fig. 2(c) is obtained by turning $S_{\mathrm{N}x}$ off and turning $S_{\mathrm{T}x\mathrm{A}}/S_{\mathrm{T}x\mathrm{B}}$ on. This action isolates $\mathbf{X_A}$ from the network and bypasses C_2 in $\mathbf{X_B}$. In doing so, the network transforms to a conventional three-phase series inductor network.

The reconfigurability of the proposed network highlights the flexibility that it offers to the power control of 3p-DAB converter. Since 3p-TRIN and 3p-TSRN offer the desirable characteristics of dc-bias blocking capability, lower RMS phase current, full-range ZVS, and unity-power-factor operation, the scope of present work is confined to the tunable resonant networks. The subsequent sections will discuss in detail the application of 3p-TRIN and 3p-TSRN in the 3p-DAB converter for improving its efficiency performance.

III. PROPOSED 3P-DAB CONVERTER WITH 3P-RTRN

The schematic diagram of the proposed converter is shown in Fig. 3. The proposed converter comprises of two three-phase half-bridges interfaced by three Y-Y connected high-frequency isolation transformers and the 3p-RTRN. The complimentary switch pairs S_{j1}/S_{j2} and $Q_{\mathrm{j}1}/Q_{\mathrm{j}2}$ (where j = A, B, and C) in the primary and secondary bridge are operated with a fixed duty-cycle of 0.5 and variable switching frequency $f_{\mathrm{s,\ min}} \leq f_{\mathrm{s}} \leq f_{\mathrm{s,\ max}}$. Moreover, the complimentary switch pairs in the adjacent phase legs of primary and secondary bridge are phase-shifted by 120°. ($e.g.$, S_{A1}/S_{A2} and $S_{\mathrm{B}1}/S_{\mathrm{B}2}$ have a phase-shift of 120°). In addition, there exists an external phase-shift θ between the complimentary switch pairs of the corresponding phase legs in the primary and secondary bridge ($e.g.$, S_{A1}/S_{A2} and $Q_{\mathrm{A}1}/Q_{\mathrm{A}2}$ are phase-shifted by θ). In this way, the primary bridge generates three two-level ($+V_{\mathrm{in}}/2$, $-V_{\mathrm{in}}/2$) high-frequency square-wave ac voltages $v'_{1j}(t)$ (where j = A, B, and C) having a fixed 120° phase-shift between the adjacent phase voltages. Similarly, a second set of three-phase two-level ($+V_{\mathrm{o}}/2$, $-V_{\mathrm{o}}/2$) square-wave ac voltages $v_{2j}(t)$ (where j = A, B, and C) are generated by the secondary bridge. Moreover, $v'_{1j}(t)$ and $v_{2j}(t)$ are phase-shifted by θ with θ defined as positive when $v'_{1j}(t)$ leads $v_{2j}(t)$.

For ease of analysis, the primary side voltages $v'_{1j}(t)$ and currents $i'_{1j}(t)$ are reflected to the secondary side ($i.e.$, $v_{1j}(t)$ and $i_{1j}(t)$) to obtain an equivalent circuit without transformers. The three-phase square wave ac voltages $v_{1j}(t)$ and $v_{2j}(t)$ are

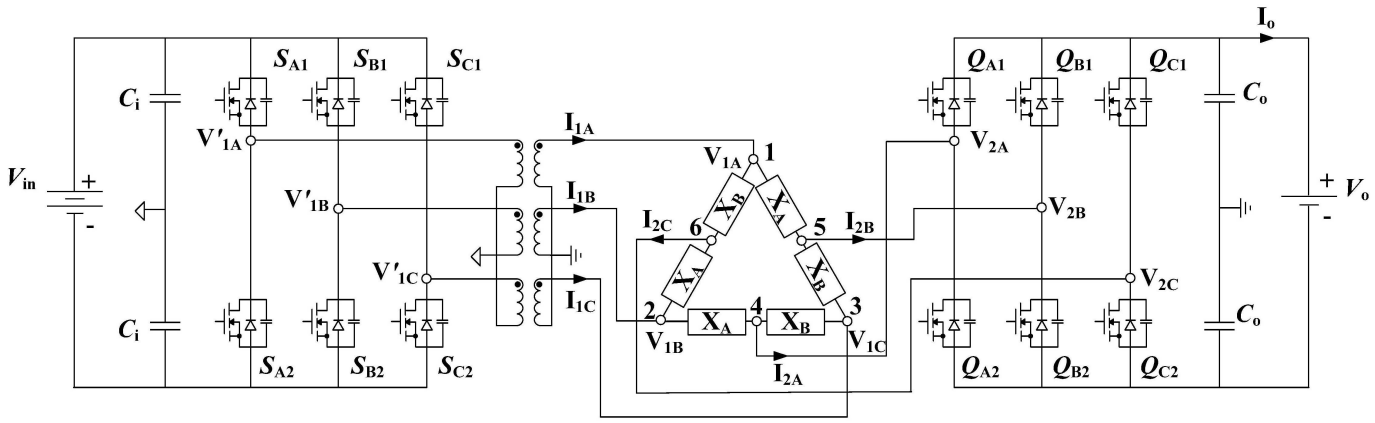

Fig. 3. Proposed 3p-DAB converter with 3p-RTRN.

subsequently represented by their Fourier series expansions as given by (1) and (2).

$$v_{1j}(t) = \frac{2V_{\rm in}}{n\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin\left(k\omega_s t + f(j)\frac{2\pi}{3}\right) \quad (1)$$

$$v_{2j}(t) = \frac{2V_{\rm o}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin\left(k\omega_s t - k\theta + f(j)\frac{2\pi}{3}\right) \quad (2)$$

where $f(j)$ = (0,+1,−1) when j = (A, B, C), ω_s=2 πf_s and $n = \frac{N_p}{N_s}$ is the transformer's turns ratio.

It is assumed that higher-order voltage and current harmonics are attenuated by the resonant network. By applying fundamental component analysis (FCA), the fundamental components of $v_{1j}(t)$ and $v_{2j}(t)$ can be represented in phasor form as $\mathbf{V}_{1j}$ and $\mathbf{V}_{2j}$ respectively. Hence, $\mathbf{V}_{1j}$ and $\mathbf{V}_{2j}$ can be written as (3) and (4).

$$\begin{aligned}\mathbf{V}_{1j} &= V_{1j}\angle(0 + f(j)\frac{2\pi}{3}) \\ &= \frac{\sqrt{2}V_{\rm in}}{n\pi}\angle(0 + f(j)\frac{2\pi}{3})\end{aligned} \quad (3)$$

$$\begin{aligned}\mathbf{V}_{2j} &= V_{2j}\angle(\theta + f(j)\frac{2\pi}{3}) \\ &= \frac{\sqrt{2}V_{\rm o}}{\pi}\angle(\theta + f(j)\frac{2\pi}{3})\end{aligned} \quad (4)$$

Depending upon the state of switches $S_{{\rm N}x}$ in the 3p-RTRN, the proposed converter can transform between a tunable 3p-DABRIC and a tunable 3p-DABSRC. The detailed discussions on the modeling and analysis for each of the two network configurations are presented in the following sections.

IV. MODELING AND ANALYSIS OF TUNABLE 3P-DABRIC

A. Power Flow Analysis

Considering the case when the switches $S_{{\rm N}x}$ in branch $\mathbf{X_A}$ are turned on, the impedances $\mathbf{X_A}$ enter into the resonant network and the converter transforms to a tunable 3p-DABRIC that can be represented by the equivalent circuit as shown in Fig. 4. The magnitude of the impedances $\mathbf{X_A}$ and $\mathbf{X_B}$ are given by (5) whereas the angular series-resonance frequencies $\omega_{\rm a}$ and $\omega_{\rm b}$ of $\mathbf{X_A}$ and $\mathbf{X_B}$ are given by (6).

$$\begin{aligned}|\mathbf{X_A}| &= X_{\rm A} = \left|\omega_{\rm s}L_1 - \frac{1}{\omega_{\rm s}C_1}\right| \\ |\mathbf{X_B}| &= X_{\rm B} = \left|\omega_{\rm s}L_2 - \frac{1}{\omega_{\rm s}C_{2\rm t}}\right|\end{aligned} \quad (5)$$

$$\begin{aligned}\omega_{\rm a} &= \frac{1}{\sqrt{L_1C_1}} \\ \omega_{\rm b} &= \frac{1}{\sqrt{L_2C_{2\rm t}}}\end{aligned} \quad (6)$$

Recall that $\mathbf{X_A}$ is constrained to operate below $\omega_{\rm a}$ ($i.e.$, $\omega_{\rm a} > \omega_{\rm s}$) to constitute an overall capacitive impedance to the network. On the contrary, $\mathbf{X_B}$ is constrained to operate above $\omega_{\rm b}$ ($i.e.$, $\omega_{\rm b} < \omega_{\rm s}$) to constitute an overall inductive impedance

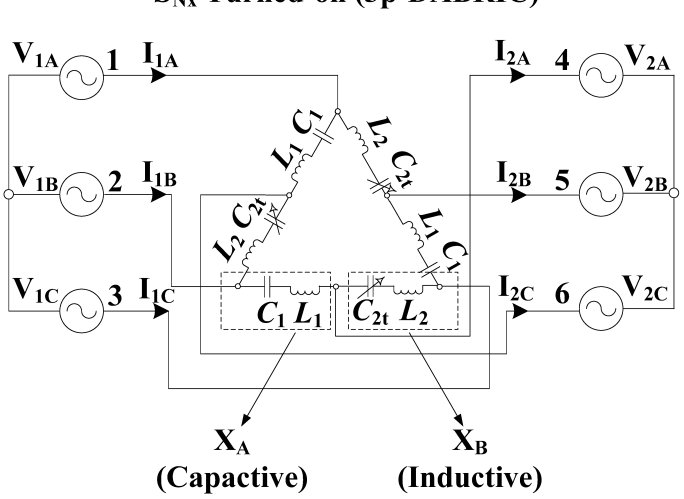

Fig. 4. Equivalent circuit of the proposed converter with 3p-TRIN.

to the network. There exists a specific frequency at which the impedances $\mathbf{X_A}$ and $\mathbf{X_B}$ are equal in magnitude and opposite in phase such that they resonate with each other. The resonance frequency at which $\mathbf{X_A}$ = - $\mathbf{X_B}$ can be found by solving $|\mathbf{X_A}|$ = $|\mathbf{X_B}|$ and the resulting expression is given by (7).

$$\omega_{\rm r} = \sqrt{\frac{(C_1 + C_{2\rm t})}{C_1 C_{2\rm t}(L_1 + L_2)}} \tag{7}$$

When operated at $\omega_{\rm r}$ ($i.e.$, $\omega_{\rm r}$ = $\omega_{\rm s}$), the resonant network exhibits immittance characteristics, and the line currents $\mathbf{I}_{1j}$ at the input ports become linearly dependent on the phase voltages $\mathbf{V}_{2j}$ at the output ports. Similarly, the line currents $\mathbf{I}_{2j}$ at the output ports become linearly dependent on the phase voltages $\mathbf{V}_{1j}$ at the input ports. In other words, source transformation occurs at $\omega_{\rm r}$ = $\omega_{\rm s}$ and the voltage sources $\mathbf{V}_{1j}$ at the input ports are transformed into current sources $\mathbf{I}_{2j}$ at the output ports. Under immittance conditions $|\mathbf{X_A}|$ = $|\mathbf{X_B}|$ = X, the expressions for the line currents $\mathbf{I}_{1j}$, $\mathbf{I}_{2j}$ at input and output ports can be found by applying nodal analysis at different nodes of the resonant network and the results are given by (8) and (9). The detailed derivation of these expressions and a detailed analysis of the effects of component tolerances on the immittance network's characteristics has been presented previously in [21] and will not be repeated here due to space constraint.

$$\begin{aligned}\mathbf{I}_{1j} &= I_{1j}\angle(\theta + f(j)\frac{2\pi}{3}) \\ &= \frac{\sqrt{6}V_{\rm o}}{\pi X}\angle(\theta + f(j)\frac{2\pi}{3})\end{aligned} \tag{8}$$

$$\begin{aligned}\mathbf{I}_{2j} &= I_{2j}\angle(0 + f(j)\frac{2\pi}{3}) \\ &= \frac{\sqrt{6}V_{\rm in}}{n\pi X}\angle(0 + f(j)\frac{2\pi}{3})\end{aligned} \tag{9}$$

where X = $\left|\omega_{\rm r}L_1 - \frac{1}{\omega_{\rm r}C_1}\right|$ = $\left|\omega_{\rm r}L_2 - \frac{1}{\omega_{\rm r}C_{2\rm t}}\right|$.

By inspecting (3), (4), (8) and (9), it can be seen that there exists a phase difference equal to the phase-shift θ between $\mathbf{V}_{1j}$, $\mathbf{I}_{1j}$ and between $\mathbf{V}_{2j}$, $\mathbf{I}_{2j}$. By setting θ = 0, in-phase relationship (i.e., unity power factor operation) can be achieved between $\mathbf{V}_{1j}$, $\mathbf{I}_{1j}$ and between $\mathbf{V}_{2j}$, $\mathbf{I}_{2j}$ at all ports of the immittance network as depicted in the phasor diagrams of Fig. 5.

Considering the converter as being lossless, the expression for the converter's output power $P_{\rm o}$ can be derived by finding the output power expression for a single phase ($e.g.$, phase A) and multiplying the resulting expression by three, as given by equation (10).

$$P_{\rm o} = 3 \times \Re[\mathbf{V_{1A}}\mathbf{I}^*_{\mathbf{1A}}] = 3 \times \Re[\mathbf{V_{2A}}\mathbf{I}^*_{\mathbf{2A}}]$$

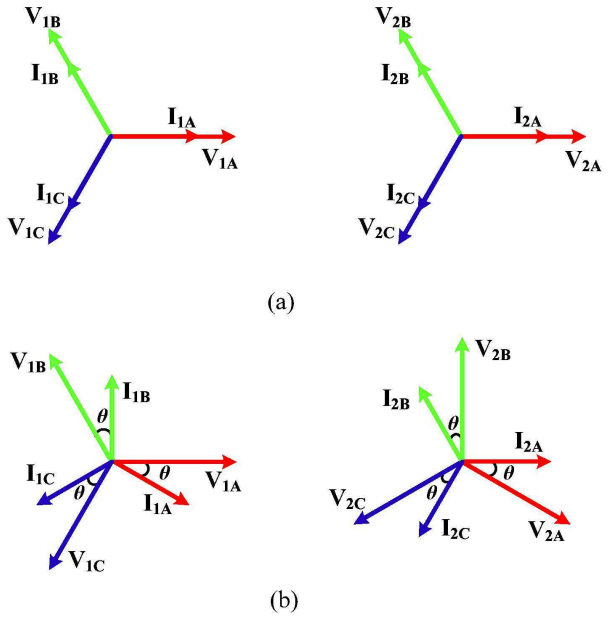

Fig. 5. (a) Phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{I}_{1j}$ and between $\mathbf{V}_{2j}$, $\mathbf{I}_{2j}$ for θ = 0; (b) Phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{I}_{1j}$ and between $\mathbf{V}_{2j}$, $\mathbf{I}_{2j}$ for $\theta \neq 0$.

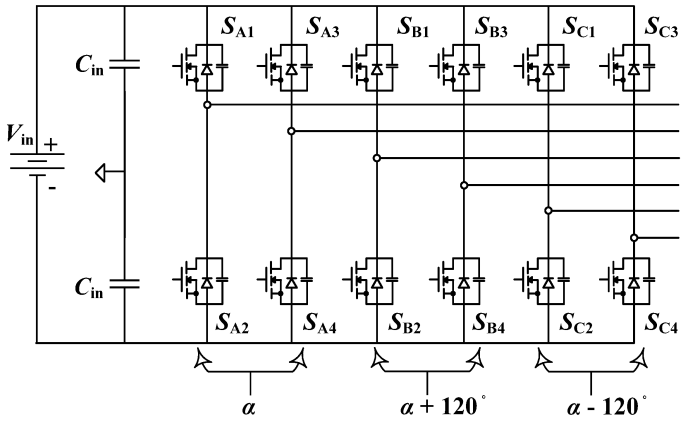

Fig. 6. Three-phase full-bridge structure proposed in [21], [26].

$$= \frac{3\sqrt{12}V_{\rm in}V_{\rm o}}{n\pi^2 X}\cos(\theta) \tag{10}$$

Inspection of (10) reveals that one of the control variables available for modulating output power of 3p-DABRIC is the phase-shift θ. However, since θ is constrained to be zero for achieving unity power factor operation, it is necessary to utilize other control variables for controlling the output power. The authors have previously proposed an application of three-phase full-bridge in 3p-DABRIC with which the internal phase-shift α between the two legs of the same full-bridge is used as a control variable for modulating output power (cf. Fig. 6) [21], [26]. By utilizing an internal phase shift between S_{j1}/S_{j2} and S_{j3}/S_{j4} in the range $0 \leq \alpha \leq 180^o$, three-phase three-level ($+V_{\rm in}$, 0, $-V_{\rm in}$) pulse-width modulated symmetrical ac voltages $\mathbf{V}_{1j}$ with variable duty ratio can be generated by this bridge structure. In this way, the converter's output power can be controlled by modulating the pulse-

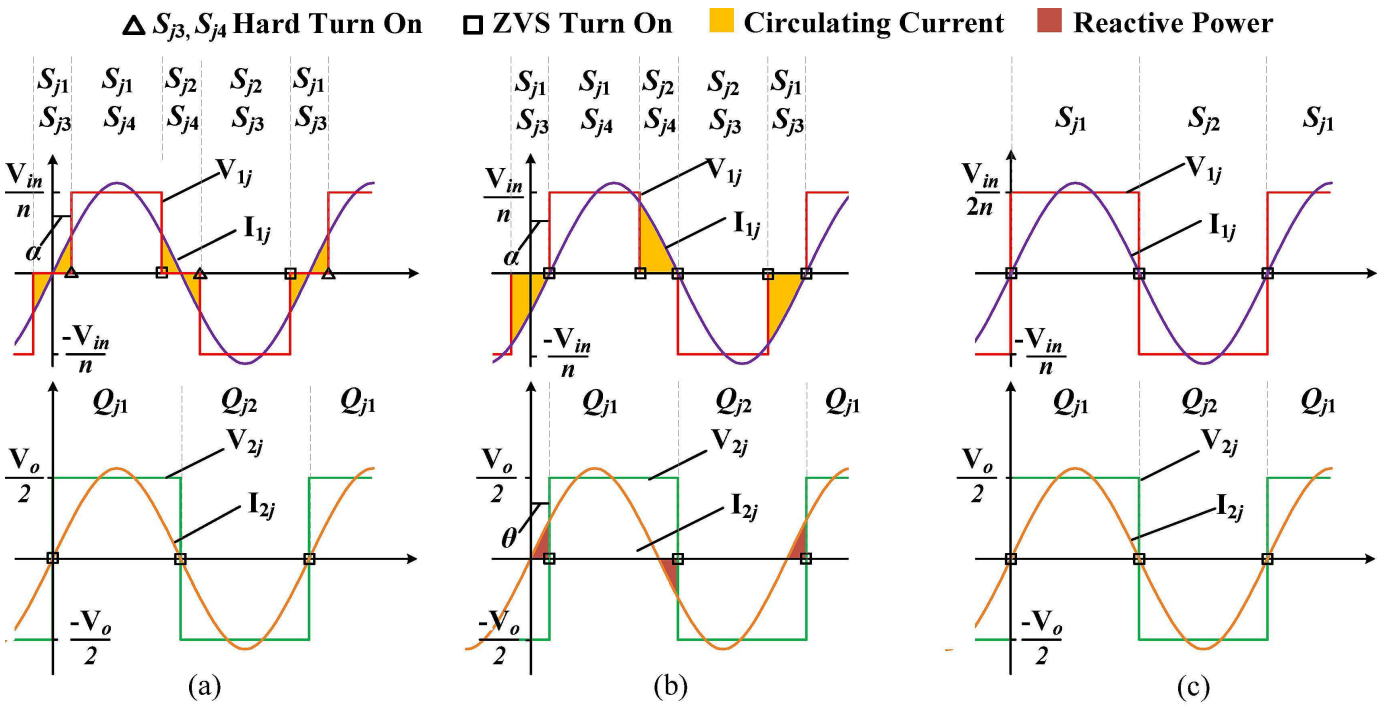

Fig. 7. (a) Port currents and port voltages for unity power factor operation; (b) Port currents and port voltages for full-range ZVS operation; and (c) Port currents and port voltages for proposed DFM modulation.

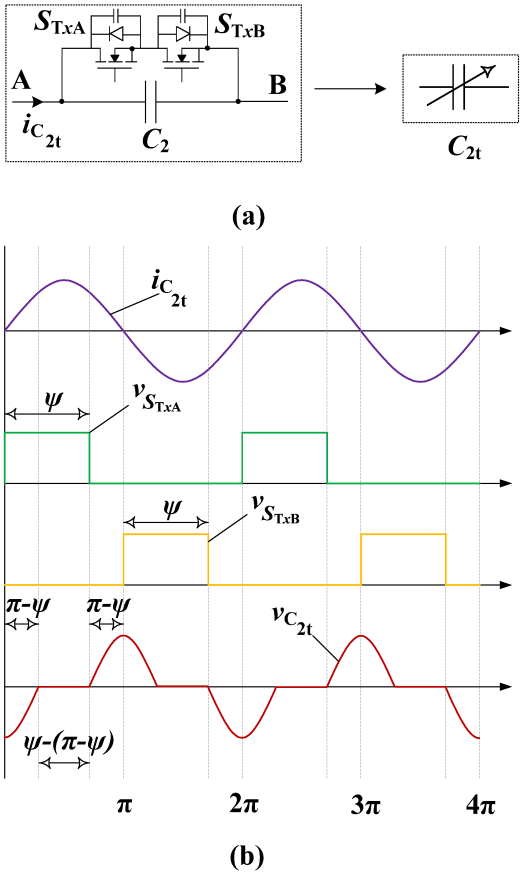

Fig. 8. (a) Schematic diagram of switch-controlled capacitor (SCC); (b) Timing diagram of switch-controlled capacitor (SCC).

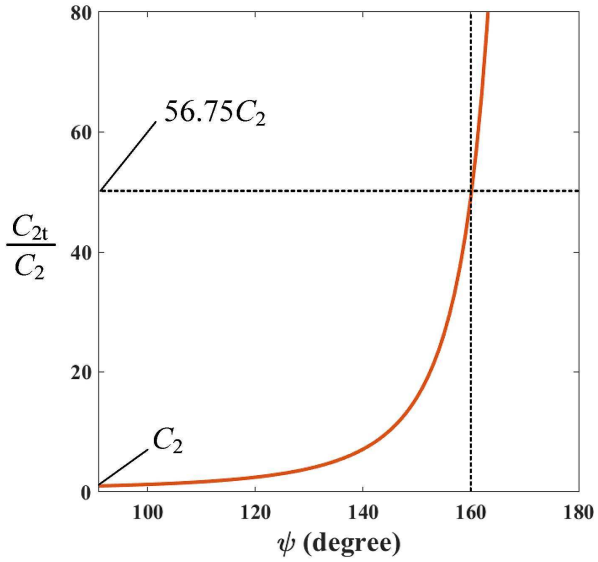

Fig. 9. Effective SCC capacitance C_{2t} versus control angle ψ.

width of the input port voltages $\mathbf{V}_{1j}$ as a function of the internal phase shift α while maintaining a unity power factor at all ports of the immittance network. Under this control scheme, $\mathbf{V}_{1j}$, $\mathbf{I}_{1j}$, and similarly for $\mathbf{V}_{2j}$, $\mathbf{I}_{2j}$, are constantly in-phase with each other (cf. Fig. 7(a)) which leads to minimum RMS port currents and conduction loss. However, the major drawback of this control method is that the complimentary switches S_{j3} and S_{j4} in the lagging leg of each phase are hard switched (cf. Fig. 7(a)) leading to increased switching loss.

In order to mitigate switching loss and achieve ZVS commutation for all switches, a 2-DoF control scheme has been proposed previously that utilizes both α and θ simultaneously ($i.e.$, $\alpha = \theta$) for controlling output power. By introducing θ between $\mathbf{V}_{1j}$ and $\mathbf{V}_{2j}$, $\mathbf{V}_{1j}$ leads $\mathbf{I}_{1j}$ at the input ports by θ and $\mathbf{V}_{2j}$ lags $\mathbf{I}_{2j}$ at the output ports by θ leading to ZVS turn-on of all the switches (cf. Fig. 5(b) and Fig. 7(b)). However, the major drawback of this control method is that high circulating current and reactive power prevails under light-load conditions (cf. highlighted by the shaded areas in Fig. 7(b)) which leads to increased conduction loss. It can be safely inferred that the existing approaches cannot concurrently minimize conduction loss and switching loss in 3p-DABRIC, therefore, it is necessary to devise a new approach that can overcome this restriction for achieving a wide-range high-efficiency performance.

B. Proposed Modulation Scheme for Tunable 3p-DABRIC

By inspection of (10), it can be observed that the switching frequency $\omega_{\rm s}$ can be used to control the output power of 3p-DABRIC. However, since $\omega_{\rm r}$ must be tuned to match with $\omega_{\rm s}$ to meet the immittance conditions ($i.e.$, $|\mathbf{X_A}| = |\mathbf{X_B}| = X$), it is necessary to modulate $\omega_{\rm r}$ in synchronism with $\omega_{\rm s}$. For modulating $\omega_{\rm r}$, switch-controlled capacitors (SCC) are used to realize electronically tunable capacitors C_{2t} in the immittance network with tunable $\omega_{\rm r}$. Thus, by modulating $\omega_{\rm s}$ and $\omega_{\rm r}$ concurrently ($i.e.$, dynamic frequency mathcing (DFM)), X can be varied and the 3p-DABRIC's output power can be controlled according to (10). The port voltages $\mathbf{V}_{1j}$, $\mathbf{V}_{2j}$ and port currents $\mathbf{I}_{1j}$, $\mathbf{I}_{2j}$ under the proposed DFM modulation are shown in Fig. 7(c)). It can be seen from Fig. 7(c) that the proposed modulation method enables a control of output power while achieving unity power factor operation and zero circulating current. Moreover, as the zero crossings of i_{1x} and i_{2x} are always aligned with the rising edges of v_{1x} and v_{2x}, all switches inherently undergo ZVS commutation. Due to the elimination of circulating current, unity power factor operation and ZVS commutation of all switches, the proposed DFM modulation scheme is anticipated to yield a wide-range high efficiency performance as will be validated by experimental results in section VI.

To derive the expression for the output power under DFM modulation and define the controllable range of P_o, X and $\omega_{\rm s}$, it is necessary to describe the operating principle of SCC. Recall that the switches $S_{\rm TxA}$, $S_{\rm TxB}$, and capacitor C_2 in branch $\mathbf{X_B}$ constitute the SCC which acts as an electronically controllable capacitor $C_{2\rm t}$ as shown in Fig. 8(a). The operating principle of SCC can be explained by referring to the timing diagram for SCC as shown in Fig. 8(b) where $i_{\rm C_{2t}}$ is the sinusoidal current flowing through $C_{2\rm t}$, $v_{\rm C_{2t}}$ is the voltage across C_2, ψ is the control angle of $S_{\rm TxA}$, $S_{\rm TxB}$, and T is the period of $i_{C_{2\rm t}}$. The gating signals for $S_{\rm TxA}$ are applied for a duration of $\frac{\psi T}{2\pi}$ at the negative to positive zero-crossing instant of $i_{C_{2\rm t}}$, while the gating signals with the same pulse-width are applied to $S_{\rm TxB}$ at the positive to negative zero-crossing instant of $i_{C_{2\rm t}}$. At ωt = π-ψ, the voltage $v_{\rm C_{2t}}$ across C_2 is zero and $i_{C_{2\rm t}}$ flows from A to B through $S_{\rm TxA}$ and the body diode of $S_{\rm TxB}$. At ωt = ψ, $S_{\rm TxA}$ is turned off and $i_{C_{2\rm t}}$ flows from A to B through C_2, thus charging it for a duration of $\frac{(\pi-\psi)T}{2\pi}$. At the positive to negative transition of $i_{C_{2\rm t}}$ ($i.e.$, ωt = π), $S_{\rm TxB}$ is turned on, $i_{C_{2\rm t}}(t)$ starts flowing in the opposite direction from B to A through C_2, thus discharging it to zero. During the next zero voltage state of $v_{\rm C2t}$, $i_{C_{2\rm t}}$ flows from B to A through $S_{\rm TxB}$ and the body diode of $S_{\rm TxA}$ until $S_{\rm TxB}$ is turned off at ωt = $(\pi + \psi)$ followed by the charging of C_2 by the negative flowing $i_{C_{2\rm t}}$.

It can be inferred from Fig. 8(b) that the control angle ψ provides a means to control the charging/discharging time ($i.e.$, $\frac{(\pi-\psi)T}{2\pi}$) of C_2 and consequently determines the magnitude of the fundamental component of $v_{\rm C2t}$ for a given $i_{C_{2\rm t}}$ [29]. By considering the fundamental component of $v_{C_{2\rm t}}$, an expression for the effective capacitance $C_{2\rm t}$ can be derived as a function of control angle ψ as given by (11). The derivation of this expression can be found in [30]. Moreover, it should also be noted that $S_{\rm TxA}$ and $S_{\rm TxB}$ turn on and off at zero voltage and thus incur negligible commutation loss.

$$C_{2\rm t}(\psi) = \frac{\pi C_2}{2\pi - 2\psi + \sin 2\psi} \tag{11}$$

C. Design Considerations for Tunable 3p-DABRIC under DFM Modulation

Based on (11), $C_{2\rm t}$ can be varied theoretically in the range $C_2 \leq C_{2\rm t} \leq \infty$ corresponding to $90^{\rm o} \leq \psi \leq 180^{\rm o}$. A plot of $C_{2\rm t}/C_2$ versus ψ is depicted in Fig. 9 where it can be seen that $C_{2\rm t}$ increases non-linearly with increasing ψ and tends to ∞ as $\psi \longrightarrow 180^{\rm o}$. To have a reasonable range of $C_{2\rm t}$ with good controllability, the values of $C_{2\rm t}$ and ψ should be restricted, for example, $C_2 \leq C_{2\rm t} \leq \kappa C_2$ and $90^{\rm o} \leq \psi \leq 160^{\rm o}$ respectively with κ = 56.75 (cf. Fig. 9). It should be noted that the value of κ is dependent on the maximum value of ψ and can be obtained from (11). Furthermore, by substituting (11) into (7), an expression for $\omega_{\rm r}$ can be obtained as a function of control angle ψ as given by (12).

$$\omega_{\rm r}(\psi) = \sqrt{\frac{2\pi C_1 + \pi C_2 - 2C_1\psi + C1\sin(2\psi)}{\pi C_1 C_2 (L_1 + L_2)}} \tag{12}$$

By inspection of (12), it can be observed that $\omega_{\rm r}$ can be tuned to match with $\omega_{\rm s}$ by means of varying ψ in the range of $160^{\rm o} \geq \psi \geq 90^{\rm o}$ to give $\omega_{\rm r,min} \leq \omega_{\rm r} \leq \omega_{\rm r,max}$. An expression for $\omega_{\rm r,min}$ and $\omega_{\rm r,max}$ can be obtained by substituting the extreme values of ψ ($i.e.$, ψ = $160^{\rm o}$ and ψ = $90^{\rm o}$ respectively) into (12). The resulting expressions for $\omega_{\rm r,min}$ and $\omega_{\rm r,max}$ are given by (13).

$$\omega_{\rm r,min} = \sqrt{\frac{(C_1 + \kappa C_2)}{C_1 \kappa C_2 (L_1 + L_2)}}$$

$$\omega_{\rm r,max} = \sqrt{\frac{(C_1 + C_2)}{C_1 C_2 (L_1 + L_2)}} = \sigma \omega_{\rm r,min} \tag{13}$$

By setting $\theta = 0^{\circ}$ in (10), an expression for the output power as a function of ψ can be obtained as given by (14).

$$P_o(\psi) = \frac{3\sqrt{12}V_{\rm in}V_{\rm o}}{n\pi^2 X(\psi)} \tag{14}$$

where $X(\psi) = \left|\omega_{\rm r}L_1 - \frac{1}{\omega_{\rm r}C_1}\right| = \left|\omega_{\rm r}L_2 - \frac{1}{\omega_{\rm r}C_{2\rm t}}\right|$.

By dividing (14) with $V_{\rm o}$, the expression for the output current of 3p-DABRIC can be obtained as given by (15).

$$I_o(\psi) = \frac{3\sqrt{12}V_{\rm in}}{n\pi^2 X(\psi)} \tag{15}$$

The expressions for $P_{\rm o,min}$ and $P_{\rm o,max}$ corresponding to $\omega_{\rm r,min}$ and $\omega_{\rm r,max}$ respectively can be obtained by substituting (13) into (14). The results are given by (16) and (17).

$$P_{\rm o,min} = \frac{3\sqrt{12}V_{\rm in}V_{\rm o}}{n\pi^2 X_{\max}} \tag{16}$$

where

$X_{\max} = \left|\omega_{\rm r,min}L_1 - \frac{1}{\omega_{\rm r,min}C_1}\right| = \left|\omega_{\rm r,min}L_2 - \frac{1}{\omega_{\rm r,min}\kappa C_2}\right|$.

$$P_{\rm o,max} = \frac{3\sqrt{12}V_{\rm in}V_{\rm o}}{n\pi^2 X_{\min}} \;=\; \epsilon P_{\rm o,min} \tag{17}$$

where

$X_{\min} = \left|\omega_{\rm r,max}L_1 - \frac{1}{\omega_{\rm r,max}C_1}\right| = \left|\omega_{\rm r,max}L_2 - \frac{1}{\omega_{\rm r,max}C_2}\right|$.

By inspection of (16) and (17), it can be observed that there is a certain range of output power $P_{\rm o}$ ($i.e.$, medium-to-high output power levels) that can be attained by the proposed DFM modulation. Moreover, $P_{\rm o}$ is directly proportional to $\omega_{\rm r}$ and to reduce output power, $\omega_{\rm r}$ needs to be reduced by increasing ψ. Nevertheless, below $P_{\rm o,min}$ the output power cannot be reduced further by DFM modulation as ψ reaches its maximum value. Therefore, below $P_{\rm o,min}$ corresponding to $\omega_{\rm r,min}$, it is proposed to reconfigure the converter to a tunable 3p-DABSRC for operation in low power range. The detailed analysis and the proposed modulation scheme for the tunable 3p-DABSRC is presented in the next section. As the desired ranges of P_o and $\omega_{\rm r}$ (cf. (12)−(17)) depend on the selection of passive component values, the key design equations for L_1, L_2, C_1, and C_2 as a function of the multiplier terms (ϵ, σ, and κ) can be obtained by simultaneously solving (16) and (17). The results are given by (18) - (21).

$$L_1 = \frac{X_{\min}\sigma(\epsilon-\sigma)}{\omega_{\rm r,max}(\sigma^2-1)} \tag{18}$$

$$L_2 = \frac{X_{\min}\sigma(\kappa\epsilon-\sigma)}{\omega_{\rm r,max}(\kappa-\sigma^2)} \tag{19}$$

$$C_1 = \frac{\sigma^2-1}{X_{\min}\omega_{\rm r,max}(\sigma\epsilon-1)} \tag{20}$$

$$C_2 = \frac{\kappa-\sigma^2}{\kappa X_{\min}\omega_{\rm r,max}(\kappa\sigma\epsilon-1)} \tag{21}$$

By inspection of (18)−(21), it can be observed that while selecting the values of the multiplier terms ($i.e.$, ϵ, σ and κ) for a given $P_{\rm o,max}$ and $\omega_{\rm r,max}$, the constraints $\epsilon > \sigma$, $\sigma > 1$, $\kappa\epsilon > 1/\sigma$, and $\kappa > \sigma^2$ must be adhered to. Furthermore, by substituting (18)−(21) into (6), the new expressions for $\omega_{\rm a}$ and $\omega_{\rm b}$ can be obtained in terms of ψ, σ and κ as given by (22).

$$\omega_{\rm a} = \sqrt{\frac{\omega_{\rm r,max}^2(\sigma\epsilon-1)}{\sigma(\epsilon-\sigma)}}$$

$$\omega_{\rm b}(\psi) = \sqrt{\frac{\kappa\omega_{\rm r,max}^2(\sigma\epsilon-1)}{{\rm A}\sigma(\epsilon\kappa-\sigma)}} \tag{22}$$

where ${\rm A} = \frac{\pi}{2\pi - 2\psi + 2\sin(2\psi)}$.

By dividing (22) with (12), the ratios $\frac{\omega_{\rm a}}{\omega_{\rm r}(\psi)}$ and $\frac{\omega_{\rm b}(\psi)}{\omega_{\rm r}(\psi)}$ can be obtained as given by (23). These ratios are important design parameters as they determine the voltage stress across the passive components in the immittance network and the shape of the network's current waveforms. Moreover, these ratios describe how far the branch impedances $\mathbf{X_A}$ and $\mathbf{X_B}$ are operating from their series-resonance frequencies $\omega_{\rm a}$ and $\omega_{\rm b}$. A value closer to unity for these ratios implies stronger resonance, higher voltage stress and more sinusoidal current waveforms, and vice-versa.

$$\frac{\omega_{\rm a}}{\omega_{\rm r}(\psi)} = \sqrt{\frac{{\rm A}\sigma^2\omega_{\rm r,max}^2(\sigma\varepsilon-1)(\kappa-1)}{\sigma\omega_{\rm r,max}^2(\sigma-\varepsilon)\left(\kappa+{\rm A}\sigma^2-\sigma^2\kappa-{\rm A}\kappa\right)}}$$

$$\frac{\omega_{\rm b}(\psi)}{\omega_{\rm r}(\psi)} = \sqrt{\frac{{\rm A}\sigma^2\kappa\omega_{\rm r,max}^2(\sigma\epsilon-1)(\kappa-1)}{{\rm A}\sigma\omega_{\rm r,max}^2(\sigma-\kappa\epsilon)\left(\kappa+{\rm A}\sigma^2-\sigma^2\kappa-{\rm A}\kappa\right)}} \tag{23}$$

By utilizing (18)−(23), the range of controllable output power, switching frequency, and control angle for the DFM-modulated 3p-DABRIC can be selected appropriately to have adequate voltage stress across the SCC, good sinusoidal current waveforms and a narrow switching frequency range.

V. MODELING AND ANALYSIS OF TUNABLE 3P-DABSRC

Recall that the proposed DFM modulation scheme should not be used for modulating output power below $P_{\rm o,min}$. Although the DFM modulation scheme completely eliminates circulating current and achieves full-range ZVS operation, its implementation is constrained by the minimum allowable switching frequency. Therefore, below $P_{\rm o,min}$ which is associated with $\omega_{\rm r,min}$, it is proposed to reconfigure the converter to a tunable 3p-DABSRC and use impedance modulation for modulating output power while keeping the switching frequency constant. In addition, the phase-shift θ is kept constant

as determined by the input-to-output voltage ratio to achieve full-range ZVS operation and maintain minimum-tank-current operation simultaneously for minimizing switching loss and conduction loss respectively [29]. As a result, the proposed reconfiguration will enable high-efficiency performance for light-load operation as well.

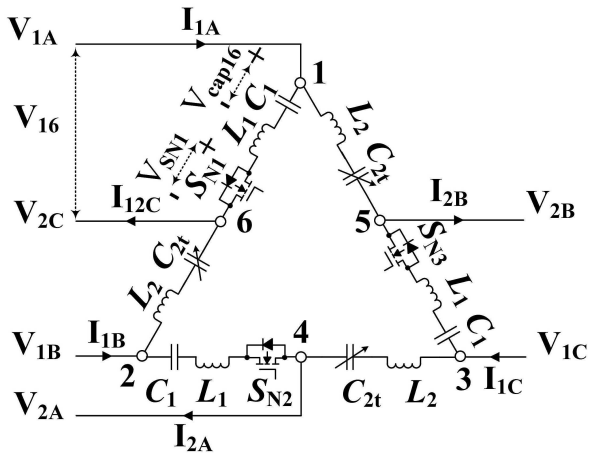

Fig. 10. Voltage distribution across branch $\mathbf{X_A}$.

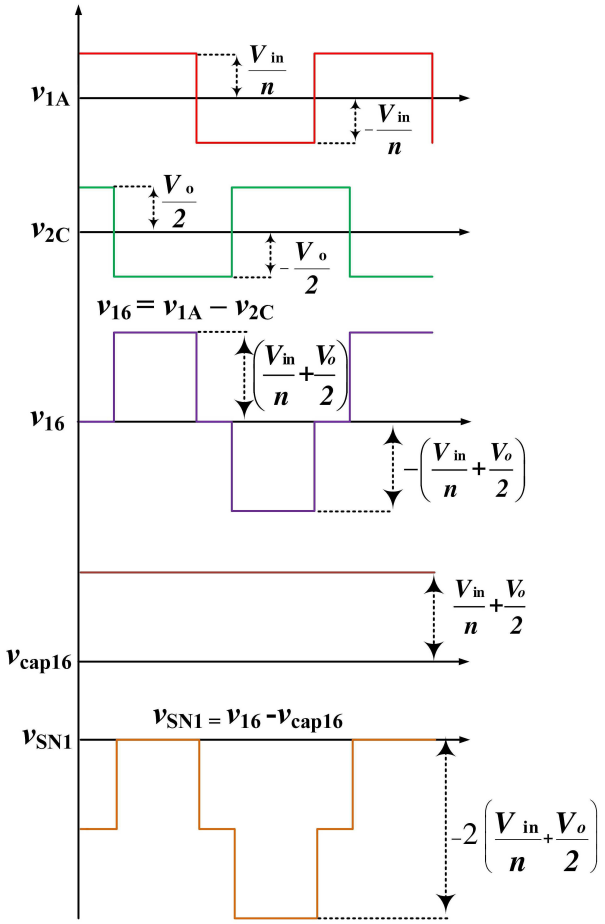

Fig. 11. Voltage waveforms across capacitor C_1 and switch $S_{\rm N1}$ for 3p-DABSRC.

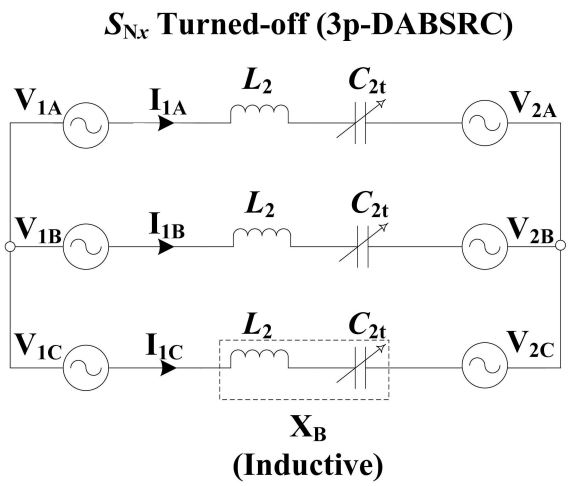

Fig. 12. Equivalent circuit of the proposed converter with 3p-TSRN.

A. Power Flow Analysis

For reconfiguration to a tunable 3p-DABSRC, the switches $S_{{\rm N}x}$ in branch $\mathbf{X_A}$ are turned off (cf. Fig. 10). This action isolates the impedances $\mathbf{X_A}$ from the resonant network and only impedances $\mathbf{X_B}$ are active. Referring to Fig. 10, when $S_{\rm N1}$ (the same argument applies to $S_{\rm N2}$ and $S_{\rm N3}$) is turned off, the capacitor C_1 in $\mathbf{X_A}$ is charged to the maximum voltage $(\frac{V_{in}}{n}+\frac{V_o}{2})$ by the voltage difference $v_{\rm 1A}-v_{\rm 2C}$ (cf. Fig. 11). As a result, the voltage seen by $S_{\rm N1}$, i.e. $v_{\rm 1A}-v_{\rm 2C}-v_{\rm cap16}$ will vary between 0 and $-2(\frac{V_{in}}{n}+\frac{V_o}{2})$ which will always keep the body diode of $S_{\rm N1}$ in a reverse biased state. Therefore, $\mathbf{X_A}$ can be fully isolated by using only a two-quadrant switch. Furthermore, to operate the converter as a tunable 3p-DABSRC, phase transposition must be applied at the output ports of the network $i.e.$, $\mathbf{V}_{2j}$ are to be phase-shifted by 120° so that the voltages at the input and output ports of the network correspond with each other. The effects of these two operations ($i.e.$, $S_{{\rm N}x}$ are turned off and phase transposition is applied at the output ports), are to transform the converter to a tunable 3p-DABSRC as depicted by the equivalent circuit shown in Fig. 12. Considering the case where power is transfered from $\mathbf{V}_{1j}$ to $\mathbf{V}_{2j}$ ($i.e.$, $\mathbf{V}_{1j}$ leads $\mathbf{V}_{2j}$), the port currents $\mathbf{I}_{1j}$ can be obtained by applying Ohm's law as given by (24). By using (3) and (24), an expression for the output power of 3p-DABSRC can be obtained as given by (25). By dividing (25) with $V_{\rm o}$, the expression for the output current of 3p-DABSRC can be obtained as given by (26).

$$\mathbf{I}_{1j} = \frac{\mathbf{V}_{1j}-\mathbf{V}_{2j}}{\mathbf{X}_{\rm B}} = I_{1j}\angle(\phi + f(j)\frac{2\pi}{3})$$

$$I_{1j} = \frac{\sqrt{2}\ V_{\rm in}\sqrt{1-2\ G\cos(\theta)+G^{\ 2}}}{n\pi X_{\rm B}}$$

$$\phi = (\tan^{-1}(\frac{1-G\cos(\theta)}{G\sin(\theta)}) \qquad (24)$$

where $G = nV_{\rm o}/V_{\rm in}$.

$$P_{\rm o} = 3 \times \Re[\mathbf{V_{1A}}\mathbf{I}^*_{\mathbf{1A}}]$$

$$= \frac{6V_{\rm in}V_{\rm o}}{n\pi^2 X_{\rm B}}\sin(\theta) \tag{25}$$

$$I_{\rm o} = \frac{6V_{\rm in}}{n\pi^2 X_{\rm B}}\sin(\theta) \tag{26}$$

By inspection of (24), it can be observed that unlike 3p-DABRIC, the phase angle ϕ of $\mathbf{I}_{1j}$ of 3p-DABSRC is dependent on the voltage ratio G. For ZVS operation of 3p-DABSRC, the value of ϕ should be in the range $0 \leq \phi \leq \theta$ so that $\mathbf{I}_{1j}$ lags $\mathbf{V}_{1j}$ and leads $\mathbf{V}_{2j}$. This implies that the instantaneous current should be negative at the turn-on instants of the primary-side switches S_{j1} (and positive for S_{j2}) and positive at the turn-on instants of the secondary-side switches Q_{j1} (and negative for Q_{j2}) (cf. Fig. 3) so that the switches parasitic capacitances are discharged and their body diodes conduct before the gate signals are applied. Based on (24), when G is unity, the value of ϕ will be $\theta/2$ and 3p-DABSRC will achieve ZVS operation independent of output power. However, deviation of G from unity causes ϕ to violate the constraint $0 \leq \phi \leq \theta$ resulting in hard switching and increased circulating current. Therefore, it is proposed to calculate θ based on the value of G such that ϕ resides in the range $0 \leq \phi \leq \theta$ and modulate output power by varying $X_{\rm B}$ (cf. 25).

B. Criteria for ZVS and Minimum-Tank-Current Operation

Recall that for ZVS operation of all switches, ϕ should reside between 0 and θ *i.e.*, $0 \leq \phi \leq \theta$. Therefore, by evaluating $\phi \geq 0$ and $\phi \leq \theta$, the ZVS conditions for the primary-side and secondary-side switches can be derived in terms of G and θ. The results are given by (27) and (28).

$$\theta \geq \cos^{-1}\left(\ G\ \right) \quad \text{for} \quad G < 1 \tag{27}$$

$$\theta \geq \cos^{-1}\left(\ \frac{1}{G}\ \right) \quad \text{for} \quad G > 1 \tag{28}$$

Thus, θ can be selected as a function of G according to (27)$-$(28) to ensure ZVS operation of the 3p-DABSRC.

To determine the criteria for minimum-tank-current operation of 3p-DABSRC, the port currents I_{1j} given by (24) are divided by the output current given by (26) to obtain a load independent and normalized expression for port current that is independent of $X_{\rm B}$. The resulting expression is given by (29).

$$I_{\rm N1j} = \frac{I_{1j}}{I_{\rm o}} \ = \ \frac{\sqrt{2}\ \pi\sqrt{1 - 2\ G\cos(\theta) + G^{\ 2}}}{6\sin(\theta)} \tag{29}$$

By inspection of (29), it can be seen that the normalized port currents $I_{\rm N1j}$ are function of G and θ only. To achieve minimum-tank-current operation, the minimum value of $I_{\rm N1j}$ is found by taking its first derivative (with respect to θ) and setting it to zero [29]. The results are given by (30).

$$\frac{\rm d}{{\rm d}\theta}\left(I_{\rm N1j}\right) = 0 \Rightarrow \theta = \begin{cases} \cos^{-1}(G) & \forall \quad G < 1 \\ \cos^{-1}\left(\ \frac{1}{G}\ \right) & \forall \quad G > 1 \end{cases} \tag{30}$$

The conditions given by (30) (*i.e.*, $\theta = \cos^{-1}(G)$ for $G < 1$ and $\theta = \cos^{-1}(1/G)$ for $G > 1$) form the criteria for minimum-tank-current operation of 3p-DABSRC. To determine the phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{V}_{2j}$ and $\mathbf{I}_{1j}$ under minimum-tank-current operation, the values of θ as determined by (30) are substituted in (24) to obtain ϕ for different values of G. The resulting expression is given by (31).

$$\phi = \begin{cases} \theta & \forall \quad G < 1 \ \ \& \ \ \theta = \cos^{-1}\left(G\right) \\ \frac{\theta}{2} & \forall \quad G = 1 \ \ \& \ \ \theta = \theta_{min} \\ 0 & \forall \quad G > 1 \ \ \& \ \ \theta = \cos^{-1}\left(\ \frac{1}{G}\ \right) \end{cases} \tag{31}$$

According to (31), under minimum-tank-current-operation, $\mathbf{I}_{1j}$ should be in phase with $\mathbf{V}_{2j}$ for $G < 1$ (cf. Fig. 13 (a), (d)), and in phase with $\mathbf{V}_{1j}$ for $G > 1$ (cf. Fig. 13 (c), (f)). Thus, it can be concluded that by selecting θ corresponding to (30) for different values of G, full-range ZVS and minimum-tank-current operation can be achieved for 3p-DABSRC to minimize switching loss and conduction loss simultaneously.

C. Impedance Modulation and Design Considerations for Tunable 3p-DABSRC

After determining θ for a given G, the output power of 3p-DABSRC can be controlled by modulating impedance $X_{\rm B}$ as a function of ψ. By substituting (30) into (25), the expression for the output power of 3p-DABSRC can be obtained as given by (32).

$$P_{\rm o}(\psi) = \begin{cases} = \frac{6V_{\rm in}V_{\rm o}}{n\pi^2 X_{\rm B}(\psi)}\sin(\cos^{-1}\left(G\right)) & \forall \quad G < 1 \\ = \frac{6V_{\rm in}V_{\rm o}}{n\pi^2 X_{\rm B}(\psi)}\sin(\theta_{min}) & \forall \quad G = 1 \\ = \frac{6V_{\rm in}V_{\rm o}}{n\pi^2 X_{\rm B}(\psi)}\sin(\cos^{-1}\left(\ \frac{1}{G}\ \right)) & \forall \quad G > 1 \end{cases} \tag{32}$$

Since the maximum output power for 3p-DABSRC is equal to the minimum output power for 3p-DABRIC, the minimum series impedance $X_{\rm B_{SRC(min)}}$ can be obtained from (16) and (32). The result is given by (33). By using (16) and (33), the switching frequency for 3p-DABSRC can be obtained as given by (34).

$$X_{\rm B_{SRC(min)}} = \frac{6\epsilon V_{\rm o}V_{\rm in}\sin(\theta_{\rm min})}{n\pi^2 P_{\rm o,max}} \tag{33}$$

$$\omega_{\rm s} = \frac{\sqrt{(C_2 X_{\rm B_{SRC(min)}})^2 + 4L_2C_2} + C_2 X_{\rm B_{SRC(min)}}}{2L_2C_2} \tag{34}$$

Thus, for a tunable 3p-DABSRC, the converter is operated with a constant switching frequency as given by (34) and the

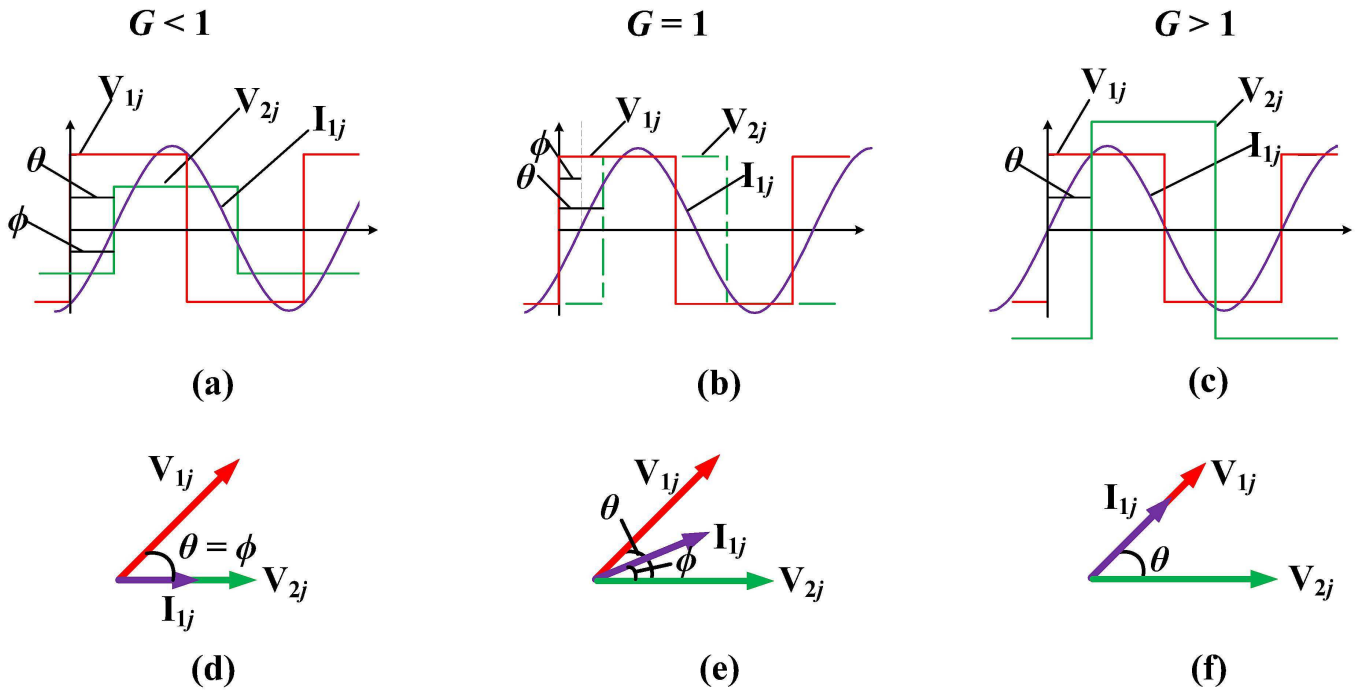

Fig. 13. Port currents and voltages of a tunable 3p-DABSRC using impedance modulation scheme for different voltage ratios G (a) $G < 1$; (b) $G = 1$; (c) $G > 1$ (d) Phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{V}_{2j}$ and $\mathbf{I}_{1j}$ for $G < 1$; (e) Phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{V}_{2j}$ and $\mathbf{I}_{1j}$ for $G = 1$; and (f) Phasor relationship between $\mathbf{V}_{1j}$, $\mathbf{V}_{2j}$ and $\mathbf{I}_{1j}$ for $G > 1$.

output power is varied by modulating impedance X_{B} as a function of ψ.

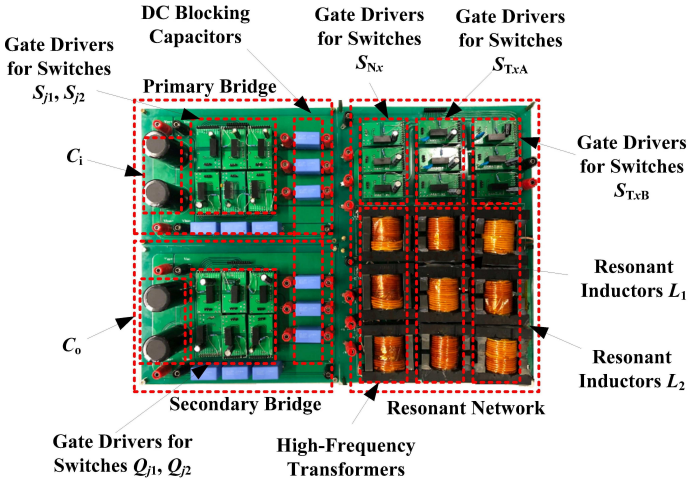

Fig. 14. Photo of constructed laboratory prototype of 1.5 kW.

TABLE I
DESIGN SPECIFICATIONS OF PROPOSED 3P-DAB CONVERTER

Input voltage V_{in}	300 V
Nominal output voltage V_{o}	150 V
Output voltage range	75-225 V
Maximum output power $P_{\mathrm{o,max}}$	1500 W
Resonant inductor L_1	73.9 μH
Resonant inductor L_2	184.4 μH
Resonant capacitor C_1	81.5 nF
Resonant capacitor C_2	73.5 nF
Switching frequency f_{s} (3p-DABRIC)	35−50 kHz
Switching frequency f_{s} (3p-DABSRC)	46 kHz
Control angle of SCC ψ	$90^{\mathrm{o}} - 160^{\mathrm{o}}$
Transformer's Turns ratio n	2
Core Type	ETD-54 Core
Core Material	N87 Ferrite
Power gain ϵ	2.5
Frequency gain σ	1.4
Capacitance gain κ	56.7
MOSFETs	UJC06505K
Controller	TMS320F28379D

VI. PROTOTYPE DESIGN AND THE EXPERIMENTAL RESULTS

To validate the effectiveness of the proposed converter and benchmark its performance, a laboratory prototype shown in Fig. 14 has been designed and built with the specifications listed in Table I. A flowchart depicting the detailed design procedure is shown in Fig. 15. The prototype has been designed to operate as a tunable 3p-DABRIC from 40 % to 100 % of the rated output power with variable switching frequency such that the switching frequency varies from 35 kHz at 40 % to 50 kHz at 100% of the rated output power. The variation of f_{s} and ψ versus P_{o} is plotted in Fig. 16a by using (14). It can be seen from Fig. 16a that P_{o} varies from 40 % to 100 % of the rated output power as f_{s} varies from 35 kHz to 50 kHz and ψ varies from 160° to 90 °. It is reminded that under the proposed DFM modulation for 3p-DABRIC, f_{s}

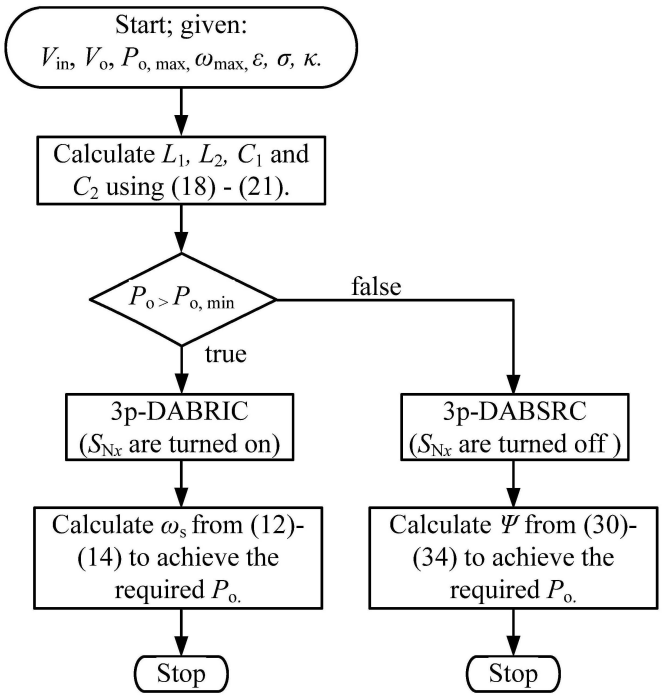

Fig. 15. Flowchart for design and operation of proposed converter.

and ψ are varied synchronously to maintain the immittance condition ($i.e.$, $\omega_r = \omega_s$). Below 40 % of the rated output power ($i.e.$, $P_o \leq P_{o,max}/\sigma$), the converter is reconfigured to a tunable 3p-DABSRC. The output power for the tunable 3p-DABSRC is controlled by impedance modulation method where the impedance of the series LC network is modulated by varying ψ from 90° to 160 °. Regarding the selection of the multiplier terms ϵ, σ, and κ they are selected to limit the voltage stress across the SCC and keep a narrow range of frequency variation. The voltage stress across the SCC for the selected converter specifications is plotted using (35) and is shown in Fig. 16b. The derivation of this expression can be found in [29].

$$V_{C2,peak} = \frac{\sqrt{2}I_{C2}}{\omega C_{2t}} = \frac{\sqrt{2}(2\pi - 2\psi + \sin 2\psi)I_{C2}}{\omega\pi C_2} \quad (35)$$

To characterize the performance of the proposed converter, the constructed prototype has been extensively tested under both configurations and its power conversion efficiency has been measured over a wide range of G ($i.e.$, 0.5≤G≤1.5). Moreover, for better benchmarking its efficiency performance, the port currents and efficiency of the proposed converter has been compared to conventional 3p-DABRIC operating in UPF and ZVS modes and 3p-DABSRC under SPS modulation.

A. Experimental Results for Tunable 3p-DABRIC under DFM Modulation

The prototype was operated as a tunable 3p-DABRIC from 40 % to 100 % of the rated output power with the proposed DFM modulation, under which f_s and ψ were modulated simultaneously to maintain the immittance condition ($i.e.$, $\omega_r = \omega_s$) through-out the entire power range. The corresponding experimental results are shown in Fig. 17 for three different power levels $i.e.$, 100 %, 75 % and 50 % of the rated output power. By inspection of the experimental waveforms shown in Fig. 17, it can be observed that v_{1j}, i_{1j} at the input ports (cf. Fig. 17 (a), (c) and (e)) and v_{2j}, i_{2j} at the output ports (cf. Fig. 17 (b), (d) and (f)) maintain an in-phase relationship for all the three output power levels. Moreover, it can also be observed that as the immittance condition is maintained under switching frequency variation, circulating current and reactive power are completely eliminated. The in-phase relationship between the current and voltage waveforms at all ports and the elimination of circulating current have

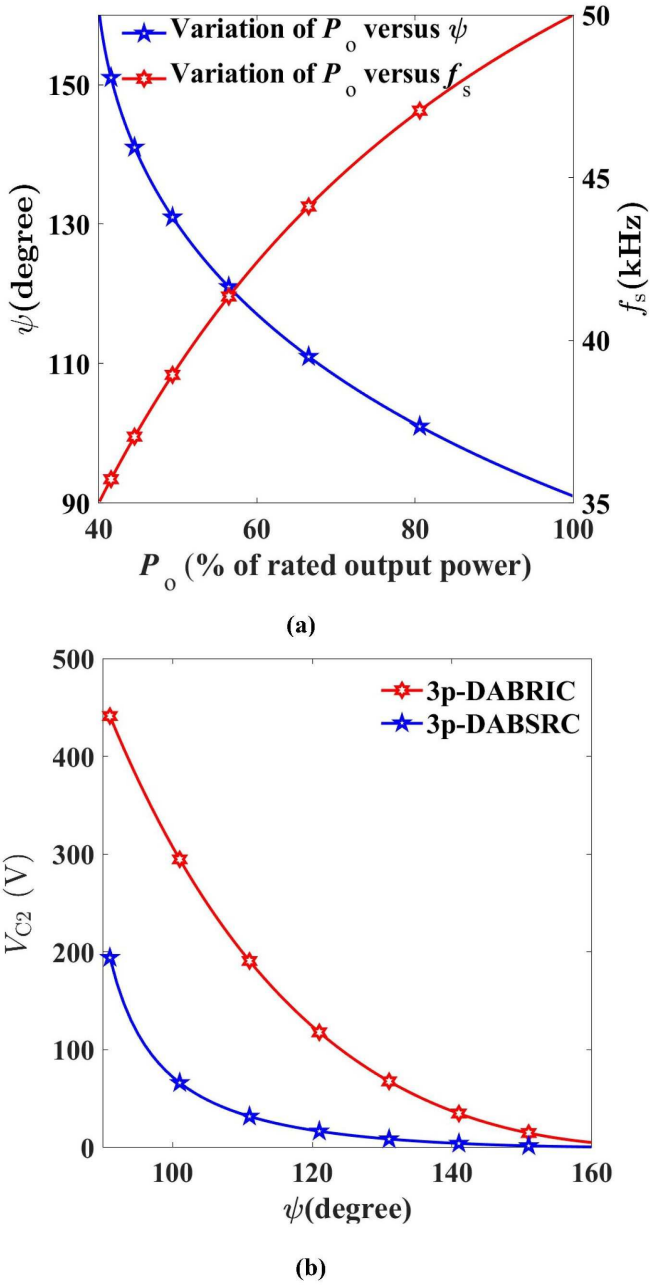

Fig. 16. (a) Variation of f_s and ψ versus P_o for 3p-DABRIC; (b) Variation of V_{2t} versus ψ for 3p-DABRIC and 3p-DABSRC.

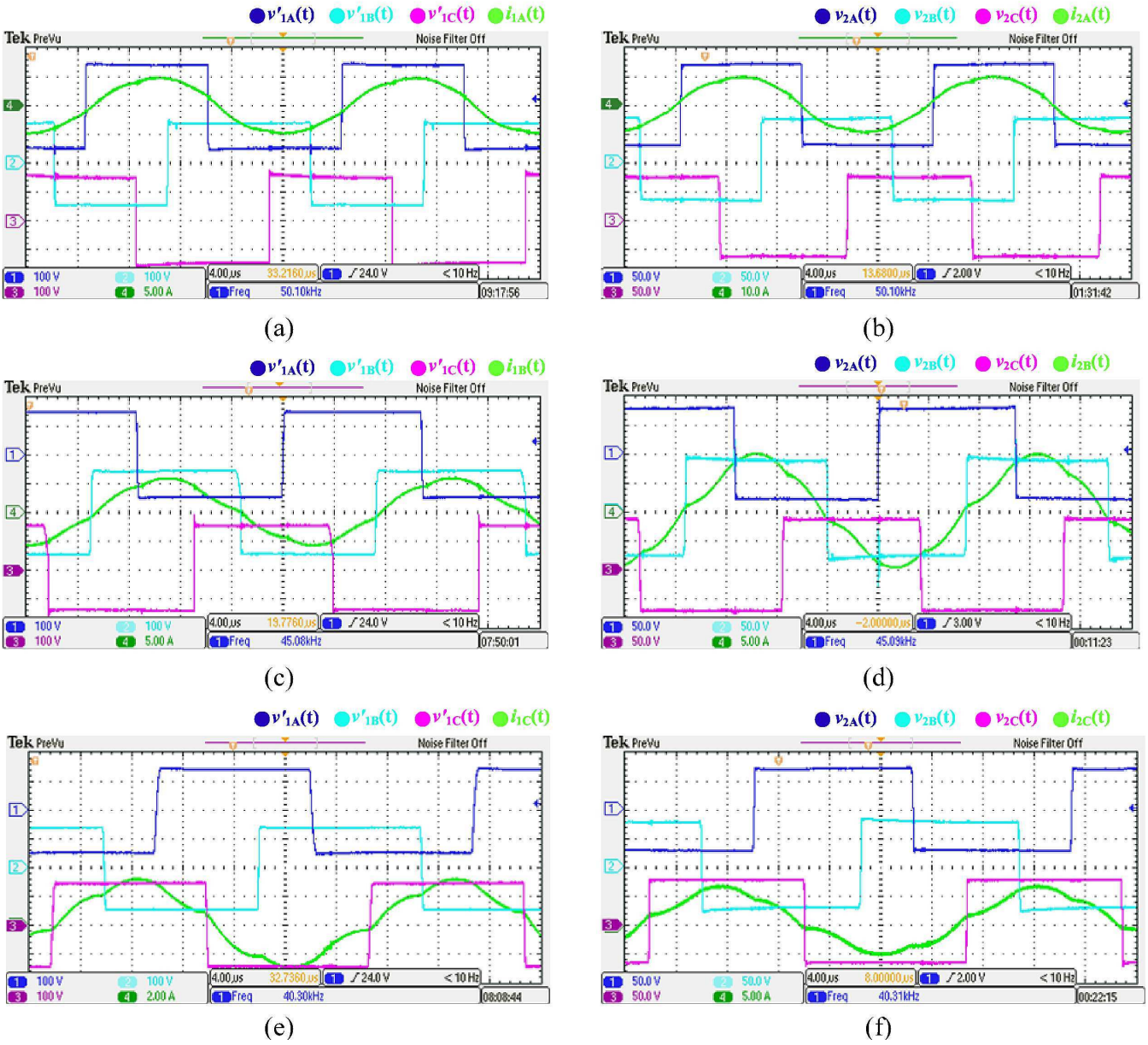

Fig. 17. Measured port voltages v'_{1j}, v_{2j} and currents i_{1j}, i_{2j} for 3p-DABRIC under DFM at (a)−(b) 100% of the rated output power with f_s = 50 kHz, and ψ = 90°; (c)−(d) 75% of the rated output power with f_s = 45 kHz, and ψ = 104.7°; (e)−(f) 50% of the rated output power with f_s = 40 kHz, and ψ = 123.9°.

led to significantly reduced RMS port currents i_{1j}, i_{2j} and conduction loss. Furthermore, judging from the direction of i_{1j}, i_{2j} during the voltage transitions of v_{1j}, v_{2j}, it can be observed that all switches undergo ZVS commutation leading to mitigation of switching loss. Overall, the elimination of circulating current and achievement of ZVS operation in all switches have contributed to the achievement of wide-range high-efficiency performance.

B. Experimental Results for Tunable 3p-DABSRC Under Impedance Modulation

Below 40% of the rated output power, the prototype was operated as a tunable 3p-DABSRC with impedance modulation. Under this modulation method, switching frequency f_s and phase-shift θ were kept constant and the output power was controlled by modulating the impedance of the series LC resonant network by means of varying the SCC control angle ψ. The corresponding experimental are shown in Fig. 18 corresponding to three different output power levels $i.e.$, 40 %, 25 %, and 10 % of the rated output power. By inspection of Fig. 18, it can be observed that unlike SPS modulation where circulating current increases with the increase of θ, the proposed modulation method constantly operates the converter at the minimum tank current for the entire power range as θ is kept constant at the optimal value as determined from (30), and ψ is used to modulate output power. Moreover, it can be observed from Fig. 18 that i_{1j} lags v_{1j} and leads v_{2j} leading to the ZVS operation of all switches. The waveforms

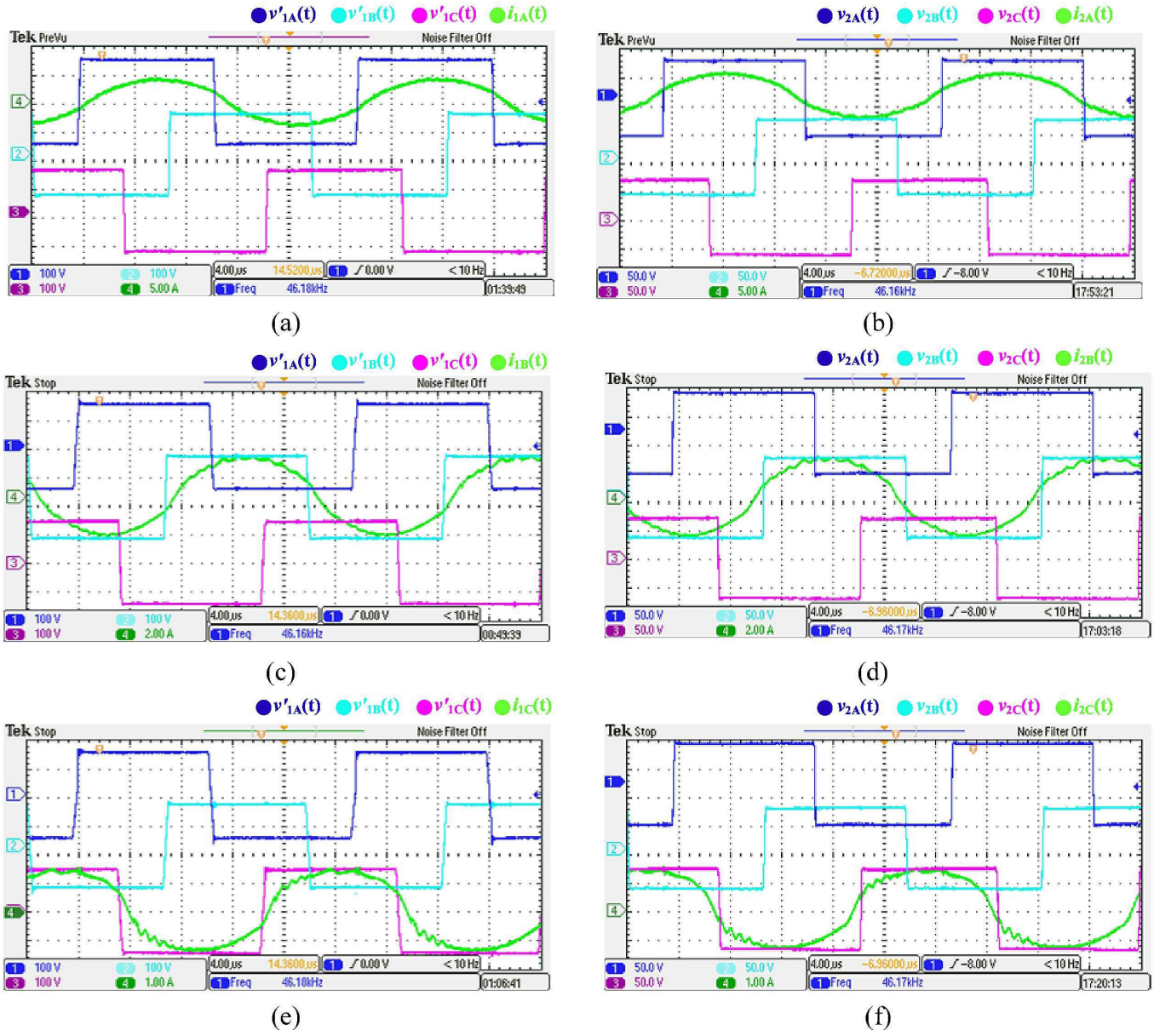

Fig. 18. Measured port voltages v'_{1j}, v_{2j} and currents i_{1j}, i_{2j} for 3p-DABSRC under impedance modulation at (a)−(b) 40% of the rated output power with ψ = 90°; (c)−(d) 25% of the rated output power with ψ = 95.8°; (e)−(f) 10% of the rated output power with ψ = 105.7°.

depicting the ZVS operation of the primary-side switches S_{A1}, S_{A2} and secondary-side switches Q_{A1}, Q_{A2} are shown in Fig. 19(a)−(b) respectively, and the voltage waveforms of SCC are shown in Fig. 19(c). Hence, it can be concluded that under this operation mode, attenuation of the circulating current in conjunction with ZVS operation of all switches have contributed to the realization of high-efficiency performance at low-to-medium output power levels.

C. Closed-Loop Voltage-Mode Control Transient Performance Under Mode Switching

To demonstrate the transient performance of the proposed converter under fast load transitions and mode switching, the simulated closed-loop transient response of the proposed converter with voltage-mode control under step load changes of 1A→7.5A→1A are shown in Fig. 20. The converter is designed to operate as a tunable 3p-DABSRC for load current below 4 A and a tunable 3p-DABRIC for load current above 4A, the load current is sensed continuously and mode transition occurs seamlessly as the load current exceeds/fall below the threshold value of 4A. The block diagram representing the closed-loop voltage-mode control strategy of the proposed converter is depicted in Fig. 21. The feedback loop comprises of a mode selection block which selects between two different proportional-integral (PI) controllers (designed for each operation mode) on the basis of the load current, and a compensation block which contains the two PI controllers that generate the appropriate control signals for output voltage regulation under each operation mode. A hysteresis band is designed in the mode selection block to reduce sensitivity at the threshold

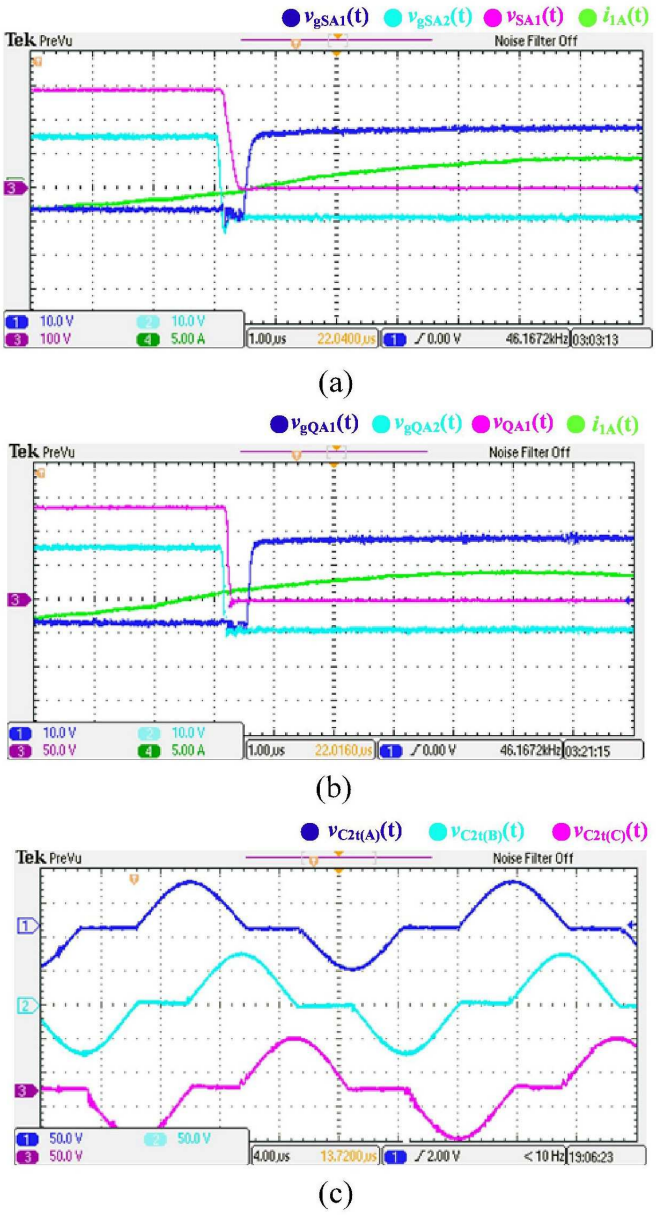

Fig. 19. (a) ZVS operation of S_{A1}, S_{A2}; (b) ZVS operation of Q_{A1}, Q_{A2}; (c) Measured waveforms of $v_{2\mathrm{Ct(A)}}$, $v_{2\mathrm{Ct(B)}}$ and $v_{2\mathrm{Ct(C)}}$ at ψ = 115.3°.

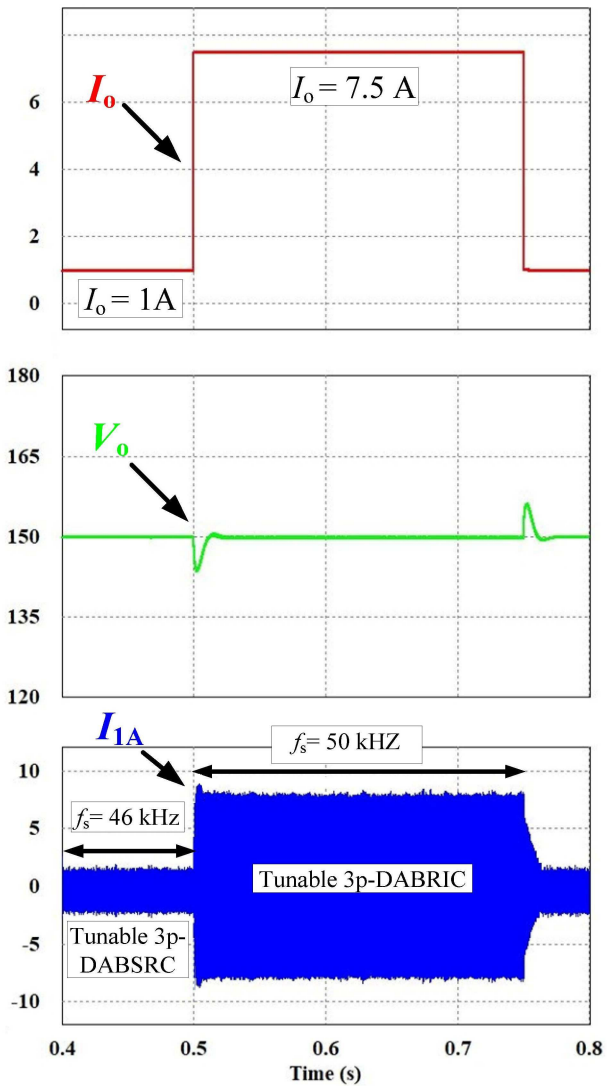

Fig. 20. Closed-loop transient response under step load changes of 1A→7.5A→1A accompanied by mode transitions between 3p-DABSRC and 3p-DABRIC.

value of 4 A. Based on the simplified small-signal model of the proposed converter as shown in Fig. 22, the PI controllers are designed with a crossover frequency of 500 Hz and a phase margin of 70°. The expressions for the small-signal value of the output current $\widetilde{i}_{\mathrm{o\_mode},avg}$ for 3p-DABRIC and 3p-DABSRC can be obtained by taking the partial derivative of (14) and (26) with respect to f_{s} and ψ, respectively. The resulting expressions are given by (36) and (37). For tunable 3p-DABRIC, as f_{s} is varied, the corresponding value of ψ required to maintain the immitance condition is taken from a look-up-table. The Bode plots of the compensated loop gain for each operation mode are shown in Fig. 23. It can be seen from Fig. 20 and Fig. 23 that with suitably designed PI controllers, the converter's output voltage is well regulated during fast load transients and the converter is able to operate

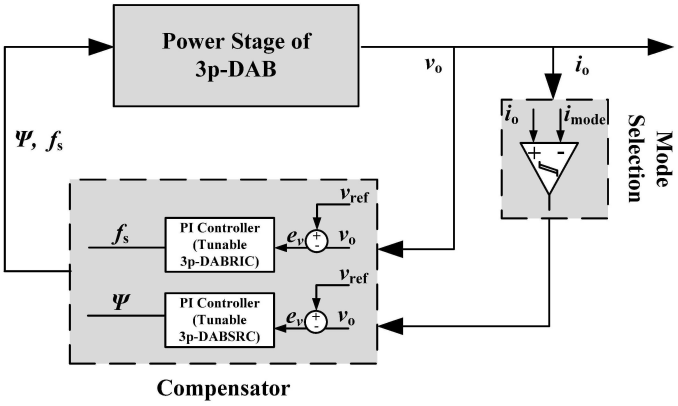

Fig. 21. Block diagram of the closed-loop implementation of the proposed converter.

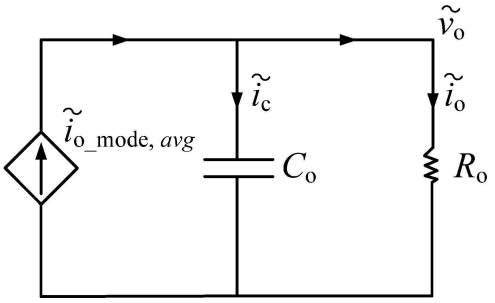

Fig. 22. Simplified small-signal model of the proposed converter.

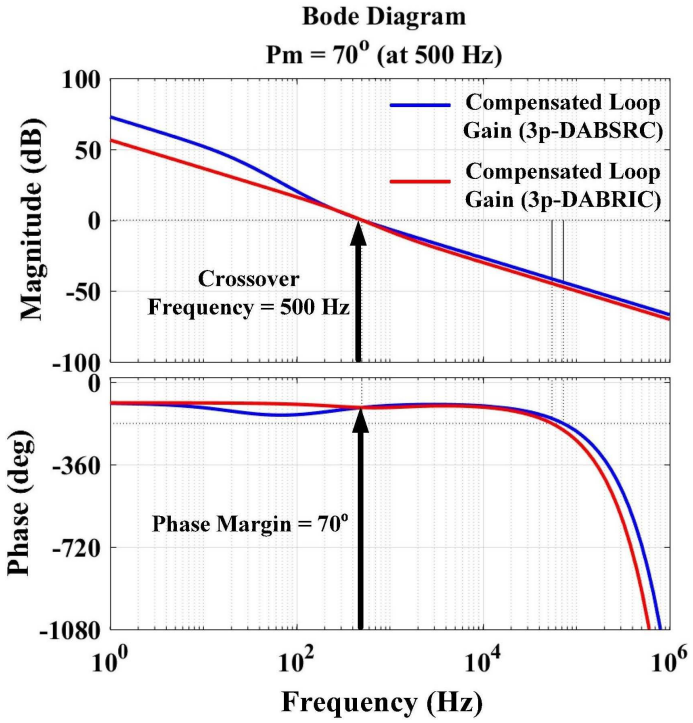

Fig. 23. Bode plots of the compensated loop gain for each operation mode.

stably during mode transition.

$$\tilde{i}_{o\_3p-DABRIC,avg} = \frac{12\sqrt{3}C_1V_{in}\left(4\pi^2C_1L_1f_s^2+1\right)}{n\pi\left(4\pi^2C_1L_1f_s^2-1\right)^2}\tilde{f}_s \quad (36)$$

$$\tilde{i}_{o\_3p-DABSRC,avg} = \frac{48C_2V_{in}f_s\sin(\theta)\left(\cos(\psi)^2-1\right)}{n\left(2\pi-4\pi^3C_2L_2f_s^2-2\psi+\sin(2\psi)\right)^2}\tilde{\psi} \quad (37)$$

D. Performance Comparison with Conventional 3p-DABRIC and 3p-DABSRC

To demonstrate the merits of the proposed topology and modulation schemes, the performance of the proposed converter was evaluated and compared (in terms of RMS port currents, ZVS range and power conversion efficiency) with the conventional 3p-DABRIC and 3p-DABSRC with fixed resonant networks. The conventional 3p-DABRIC with a fixed immittance network operating with unity power factor and full-range ZVS modes, and 3p-DABSRC operating with SPS modulation were included in the comparison. For a more comprehensive comparison, wide-range variations in G ($i.e.$, 0.5 $\leq G \leq$1.5) are considered. The simulated RMS port currents ($i.e.$, $\mathbf{I}_{N,rms}$= ($\mathbf{I}_{1j}$+$\mathbf{I}_{2j}$)/2) of the proposed converter, conventional 3p-DABRIC and 3p-DABSRC for the selected converter specifications are plotted in Fig. 24(a)−(c) for G = 0.5, G = 1 and G = 1.5 respectively. By inspection of Fig. 24(a)−(c), it can be observed that the proposed converter offers significantly lower RMS port currents under wide-range variations in G as compared to the other two topologies. The lower RMS port currents of the proposed converter is attributed to the achievement of wide-range zero circulating current which favorably leads to lower conduction loss. Moreover, as the proposed converter is capable of achieving full-range ZVS operation for all switches irrespective of variations in G, the proposed converter incurs lower switching loss in comparison to the other two topologies. The ZVS range comparison of the proposed converter with the other two topologies is presented in Fig. 25. It can be seen from Fig. 25 that unlike UPF operation of 3p-DABRIC (cf. Fig. 25(a) where switches S_{j3}, S_{j4} are hard-switched) and SPS operation of 3p-DABSRC (cf. Fig. 25(b) where switches Q_{j1}, Q_{j2} are hard-switched for G < 1 and switches S_{j1}, S_{j2} are hard-switched for $G > 1$), the proposed converter achieves ZVS operation for all the switches independent of output power level and input-to-output voltage ratio (cf. Fig. 25(c)).

The measured power conversion efficiency of the proposed converter, conventional 3p-DABRIC and 3p-DABSRC are plotted in Figs. 26(a)−(c) for G = 0.5, G = 1 and G = 1.5 respectively. It can be observed from Figs. 26(a)−(c) that due to reconfiguration flexibility, attenuation of circulating current and full-range ZVS operation, the proposed converter offers a wide-range high-efficiency performance as compared to the other two topologies. For the conventional 3p-DABSRC, it achieved a better efficiency performance at low-to-medium output power levels for G = 1 but suffered from high circulating current and hard-switching under $G \neq 1$ leading to a deterioration of efficiency performance. For the conventional 3p-DABRIC operating with unity power factor, 33% of the switches suffered from hard-switching and high circulating current prevails under light-load condition. The worst efficiency performance resulted from the conventional 3p-DABRIC operating with full-range ZVS mode due to excessive conduction loss caused by the high circulating current needed to realize the ZVS operation. For the proposed converter, switching loss is negligible due to full-range ZVS operation of all switches and the dominant loss mechanism is conduction loss. The increase in conduction loss with increasing load leads to a decrease in efficiency. However due to wide-range zero circulating current, unity power factor operation and ZVS operation of all switches, the loss in efficiency with increasing load is quite small and the proposed converter offers relatively flat (i.e; weak dependence on load) efficiency curves as compared to the other two topologies.

E. Power Loss Model

The power loss breakdown of the proposed converter for both operation modes over wide output voltage and power

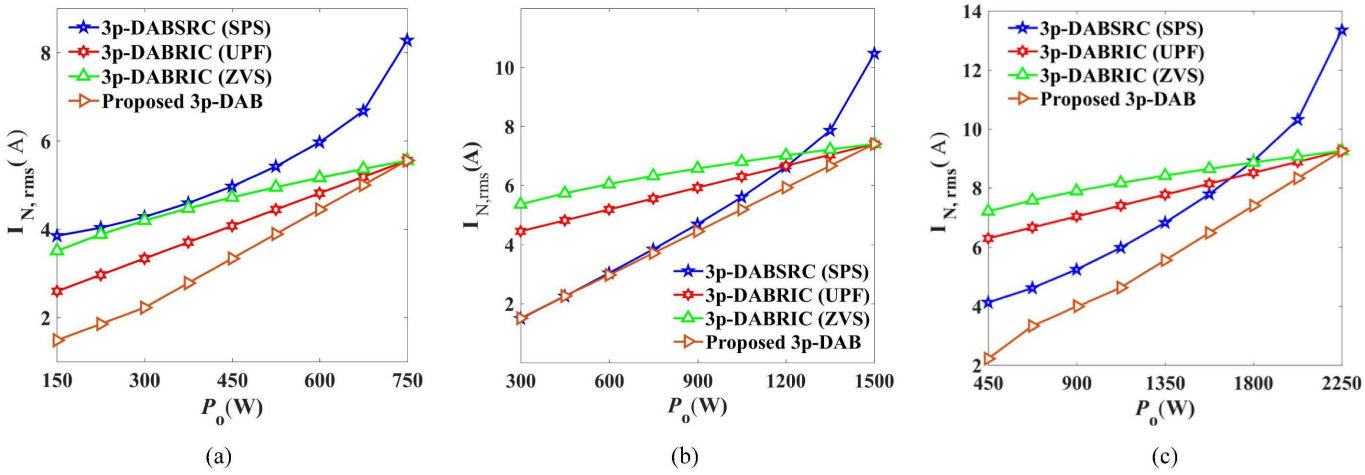

Fig. 24. Normalized simulated port currents $I_{\mathrm{N,rms}}$ comparison between the proposed converter and conventional 3p-DABRIC (UPF and ZVS modes) and 3p-DABSRC (SPS modulation) for (a) G = 0.5; (b) G = 1; (c) G = 1.5.

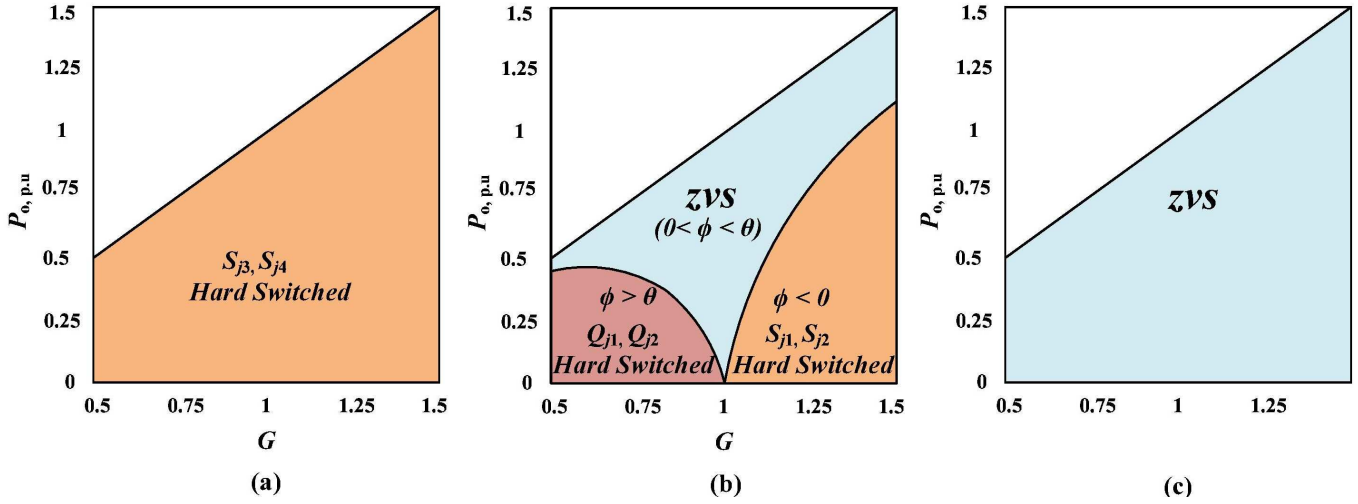

Fig. 25. (a) ZVS range of 3p-DABRIC (UPF mode); (b) ZVS range of SPS controlled 3p-DABSRC; (c) ZVS range of the proposed converter.

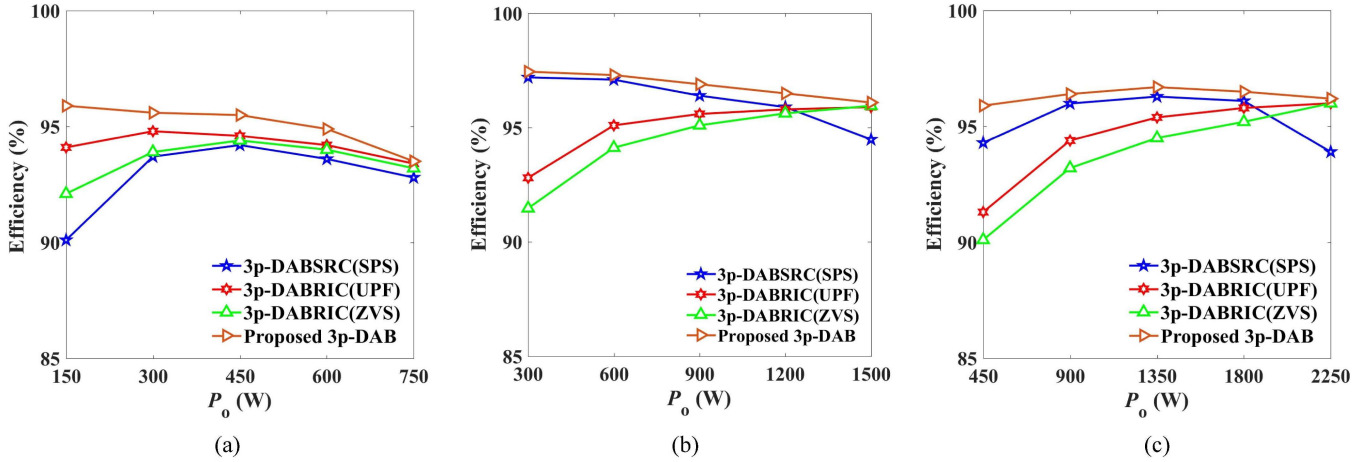

Fig. 26. Comparison of measured power conversion efficiency between the proposed converter and conventional 3p-DABRIC (UPF and ZVS modes) and 3p-DABSRC (SPS modulation) for (a) G = 0.5; (b) G = 1; (c) G = 1.5.

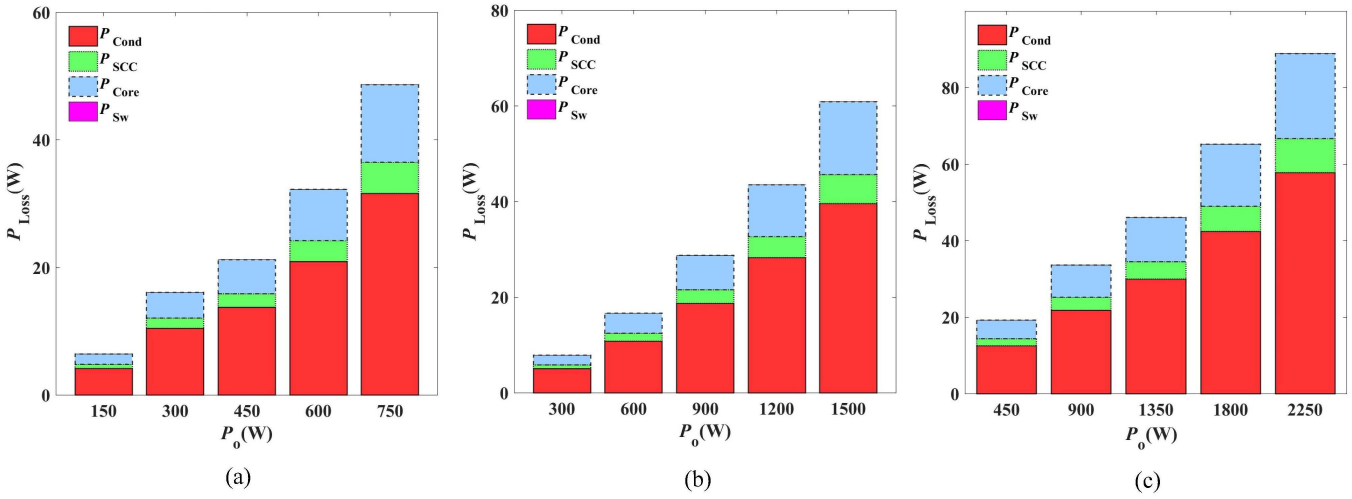

Fig. 27. Power loss breakdown of the proposed converter for (a) G = 0.5; (b) G = 1; (c) G = 1.5.

range has been calculated by adopting and extending the power loss models proposed in [31], [32]. The developed power loss model (cf. (38)) considers the following losses:

$$P_{\mathrm{L}} = P_{\mathrm{Cond}} + P_{\mathrm{SCC}} + P_{\mathrm{Core}} + P_{\mathrm{Sw}} \tag{38}$$

1) Conduction Loss: The conduction loss P_{Cond} is calculated using (39) and is contributed by the on-state resistance $R_{\mathrm{ON,p}}$, $R_{\mathrm{ON,s}}$ of the MOSFETs in the primary and secondary bridges respectively, AC resistances R_{L1}, R_{L2} of the resonant inductors L_1, L_2 respectively, and AC resistance R_{T} (secondary-reflected) of the HF transformers windings.

$$P_{\mathrm{cond}} = 6 \times \left(\left(\frac{I_{\mathrm{1j,rms}}}{n\sqrt{2}} \right)^2 R_{\mathrm{ON,p}} + \left(\frac{I_{\mathrm{2j,rms}}}{\sqrt{2}} \right)^2 R_{\mathrm{ON,s}} \right) + 3 \times \left(\left(I_{\mathrm{L1,rms}}\right)^2 R_{\mathrm{L1}} + \left(I_{\mathrm{L2,rms}}\right)^2 R_{\mathrm{L2}} + \left(I_{\mathrm{2j,rms}}\right)^2 R_{\mathrm{T}} \right) \tag{39}$$

2) Power Loss in SCC: The power loss in SCC is calculated using (40) and is contributed by the on-state resistance $R_{\mathrm{ON,SCC}}$ of the SCC MOSFETs and the forward voltage drop V_f of the SCC body diodes [29].

$$P_{\mathrm{SCC}} = 3 \times \left(\left(I_{\mathrm{SCC,rms}}\right)^2 R_{\mathrm{ON,SCC}} + V_f I_{\mathrm{SCC,rms}} \right) \tag{40}$$

3) Core Loss: The total core loss incurred in the resonant inductors L_1, L_2 and HF transformers is calculated by applying the modified Steinmetz equation as given by (41).

$$P_{\mathrm{core}} = 3 \times \left(K_{fe} A_c l_m \left(\Delta B_{\mathrm{T}}^{\beta} + \Delta B_{L1}^{\beta} + \Delta B_{L2}^{\beta} \right) \right) \tag{41}$$

where K_{fe}, $A_c l_m$, and β are the loss coefficient, volume, and loss exponent of the magnetic core respectively, while ΔB_T, ΔB_{L1}, and ΔB_{L2} are the flux densities of the HF transformer, resonant inductor L_1, and resonant inductor L_2, respectively.

4) Switching Loss: The total switching loss is given by (42) and is caused by the voltage and current overlap during the switching transitions of MOSFETs.

$$P_{\mathrm{Sw}} = \left(6 \times \left| \frac{i_{1j}(0)}{n} \right| V'_{1j} \left(t_{\mathrm{rip}} + t_{\mathrm{rvp}} + t_{\mathrm{fip}} + t_{\mathrm{rvp}} \right) f_{\mathrm{s}} \right) + \left(6 \times \left| i_{2j}(\theta) \right| V_{2j} \left(t_{\mathrm{ris}} + t_{\mathrm{rvs}} + t_{\mathrm{fis}} + t_{\mathrm{rvs}} \right) f_{\mathrm{s}} \right) \tag{42}$$

where $\left| \frac{i_{1j}(0)}{n} \right|$, $|i_{2j}(\theta)|$ are the instantaneous current values at the turn-on instants of primary and secondary-bridge MOSFETs, t_{rip}, t_{rvp}, t_{fip}, and t_{rvp} are the rise and fall time of the current and voltage of the primary-bridge MOSFETs while t_{ris}, t_{rvs}, t_{fis}, and t_{rvs} are the same for secondary-bridge MOSFETs.

By using (38)-(42), the power loss breakdown of the proposed converter is calculated and shown in Figs. 27(a)−(c) for G = 0.5, G = 1, and G = 1.5, respectively. Since ZVS operation is achieved for the entire operating range, the switching loss P_{Sw} of the MOSFETs in the primary and secondary bridges is negligible and is not shown in Fig. 27. It can be seen from Fig. 27 that the major source of power loss of the proposed converter is attributed to conduction loss for the entire operating range.

Finally, a comprehensive comparison of the proposed 3p-DAB topology with the existing 3p-DAB topologies is presented in Table II to conclude the paper.

VII. Conclusion

A flexible and reconfigurable topology of three-phase DAB converter utilizing a reconfigurable and tunable resonant network has been proposed in this paper. The proposed converter offers multiple degrees-of-freedom in terms of the availability of multiple control parameters and topological variations to achieve wide-range high efficiency performance. The proposed converter has been designed to switch between two different network configurations that are controlled with two different modulation schemes to optimize its efficiency performance in both low and medium-to-high power operation. For medium-to-high output power levels, the converter operates as a tunable 3p-DABRIC with dynamic frequency matching modulation.

TABLE II
COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND EXISTING TOPOLOGIES.

S. No.	Ref	No. of Switches	Additional Resonant Components	Full-Range ZVS	Unity Power Factor Operation	Zero Circulating Current	Zero Backflow Power	Minimum Tank Current
1	[11]–[13]	24	0	✓	X	X	X	X
2	[15], [16]	21	0	✓	X	X	X	X
3	[19], [20]	12	9	✓	X	X	X	X
4	[21]	18	12	X	✓	X	✓	X
5	[26]	21	12	✓	✓	X	✓	X
6	Proposed Topology	21	12	✓	✓	✓	✓	✓

Under this mode of operation, the converter's output power is modulated by synchronously varying the resonance frequency of the immittance network and the switching frequency by using an SCC. For low-to-medium output power levels, the converter operates as a tunable 3p-DABSRC with impedance modulation. Under this mode of operation, the converter's output power is modulated by varying the impedance of a series LC resonant network with the aid of SCC while keeping the switching frequency and phase-shift constant. The combination of both operation modes have led to the realization of wide-range zero circulating current and full-range ZVS operation of all switches for a wide-range of output power and input-to-output voltage ratio. The presented theoretical analysis has been validated by the experimental results obtained from a 1.5 kW laboratory prototype yielding wide-range high-efficiency performance.

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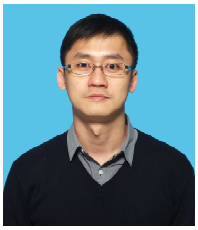

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