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An Overview of Condition Monitoring Techniques for Capacitors in DC-Link Applications

Zhaoyang Zhao, *Student Member, IEEE*, Pooya Davari, *Senior Member, IEEE*, Weiguo Lu, *Member, IEEE*, Huai Wang, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

Abstract—Capacitors are widely used in dc links of power electronic converters to balance power, suppress voltage ripple, and store short-term energy. Condition monitoring (CM) of dc-link capacitors has great significance in enhancing the reliability of power converter systems. Over the past few years, many efforts have been made to realize CM of dc-link capacitors. This paper gives an overview and a comprehensive comparative evaluation of them with emphasis on the application objectives, implementation methods, and monitoring accuracy when being used. First, the design procedure for the condition monitoring of capacitors is introduced. Second, the main capacitor parameters estimation principles are summarized. According to these principles, various possible CM methods are derived in a step-by-step manner. On this basis, a comprehensive review and comparison of CM schemes for different types of dc-link applications are provided. Finally, application recommendations and future research trends are presented.

Index Terms—Condition monitoring, ceramic capacitors, dc link, electrolytic capacitors, film capacitors, reliability.

I. INTRODUCTION

DC-LINK capacitors are an important part in the majority of electronic converters, which contribute to suppressing dc-link voltage ripple, absorbing harmonics, and balance the instantaneous power difference between the front-end and rear-end of converter systems [1], [2]. In some applications, they are also served to provide sufficient energy for transient and abnormal operations [3], [4]. However, capacitors are sensitive to thermal and electrical stresses and have the main disadvantage of finite lifespan and high degradation failure rate [6]–[8]. As reported in [8], about 30% of the faults in converters are caused by the degradation of capacitors, which makes them to be considered as the weakest link in power electronic systems [8]. With regard to this, monitoring the

degradation state of capacitors and scheduling maintenance before serious degradation or break down occurs have great significance for ensuring the reliable operation of dc-link applications and preventing possible catastrophic failures [9], [10].

In the last two decades, many efforts [11]–[101] have been made to realize the condition monitoring (CM) for capacitors in dc-link applications. Some of them are designed for capacitors dismantled from converters, i.e., offline schemes [11]–[24]. Others are implemented on-site in a real system, i.e., real-online and quasi-online schemes. Here, different types of dc-link applications are considered, such as adjustable speed drive (ASD) systems [25]–[47], photovoltaic (PV) grid-connected inverters [48]–[55], power factor correction (PFC) converters [56]–[61], and dc/dc buck and boost converters [62]–[101]. Moreover, the implementation methods are various. Some schemes monitor the dc-link capacitors using the existing voltage and current information, which can be obtained directly from controllers. Others are based on the signals sampled from additional hardware circuits and sensors. Generally, the research objective and implementation methods of condition monitoring are various. It is of great necessity to review these CM techniques for the following purposes.

- 1) Summarize the existing CM techniques and provide a reference for the researchers in this field.
- 2) Benchmark different CM schemes and identify the advantages and limitations of them, in order to provide suggestions for industrial application.
- 3) Analyze the existing challenges and explore future research opportunities.

Recently, some overview papers have been published to review the CM techniques for dc-link capacitors. In [102], Wang *et al.* reviewed the reliability of dc-link capacitors. However, their work mainly focuses on the reliability-oriented design. Only a brief discussion on the condition monitoring of dc-link capacitors is given. On this basis, Soliman *et al.* [103] give a review of the condition monitoring of capacitors in power electronic converters. Their work mainly focuses on the classification of the CM techniques. Based on three-category classification methods, the CM techniques are reviewed. Although the above-mentioned review papers give a comparison and analysis for CM techniques of capacitors, there are the following limitations.

- 1) A large amount of latest CM techniques for dc-link capacitors have emerged in recent years, which are not

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Z. Zhao is with the State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing 400044, China, and also with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: zhaoyang.z@foxmail.com).

P. Davari, H. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: pda@et.aau.dk; hwa@et.aau.dk; fbl@et.aau.dk).

W. Lu is with the State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing 400044, China (e-mail: luweiguo@cqu.edu.cn).

considered in [102], [103]. Thereby, it is worth to investigate and discuss on the feasibility of the new state-of-the-art techniques.

- 2) A comprehensive design procedure of condition monitoring for capacitors is not given in [102], [103], which is important for industry application and academic research.
- 3) There is a lack of summarizing of monitoring principles and how to obtain the possible CM methods based on the basic principles.
- 4) No assessment of CM schemes for different types of dc-link applications is provided. For a certain type of converter, such as ASD systems, PV inverters, it is difficult to compare the existing CM schemes.

Therefore, the main goal of this paper is to provide a better understanding of both industry and academia on the suitability, feasibility, and implementation of CM schemes by answering the following: 1) What are the possible methods for the condition monitoring of capacitors and how to implement them? 2) For a given dc-link application (e.g., ASD systems), what is the difference between the existing CM schemes and how to choose the best one? To answer these questions, this paper gives an overview with emphasis on the derivation of CM methods and the discussion of different types of dc-link applications. The main contribution is given as follows.

- 1) A comprehensive design procedure of condition monitoring for capacitors is presented.
- 2) Summarizes the main capacitor parameters estimation principles and derives the various possible CM methods in a step-by-step manner.
- 3) Discussion and comparison of the existing CM schemes for main dc-link applications including ASD systems, PV inverters, PFC converters, and dc/dc converters. Based on this, giving suggested solutions for industrial applications.

This paper is organized as follows: Section II presents the design procedure of condition monitoring for capacitors. The derivation of CM methods is introduced in Section III. Section IV to Section VII are dedicated to suitability investigation of CM techniques for different types of dc-link applications. Finally, the suggested solutions for industrial applications, future challenges, and opportunities are drawn in Section VIII.

II. DESIGN PROCEDURE FOR CONDITION MONITORING OF DC-LINK CAPACITORS

A. Capacitors for DC-Link Applications

The typical structure of power electronic systems with dc-link capacitors is shown in Fig. 1. Based on the ripple current limitation of capacitors, a capacitor bank is usually placed at dc link based on series-parallel configuration. Generally, three types of capacitors are used in dc-link applications, which are the Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF-Caps), and Multi-Layer Ceramic Capacitors (MLC-Caps) [102]. Fig. 2(a) shows a simplified model of the three types of capacitors, where C is the capacitance, R_{ESR} and L_{ESL} represent the equivalent series resistance (ESR) and the equivalent series inductance (ESL), R_p denotes the insulation

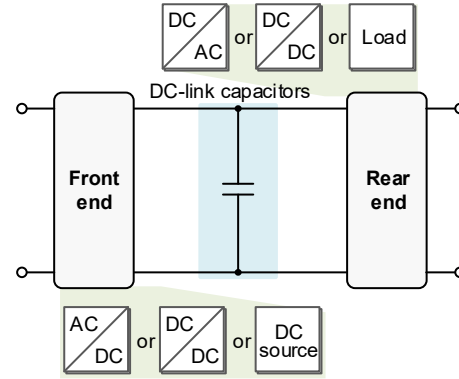


Fig. 1. Typical structure of power electronic systems with dc-link capacitors.

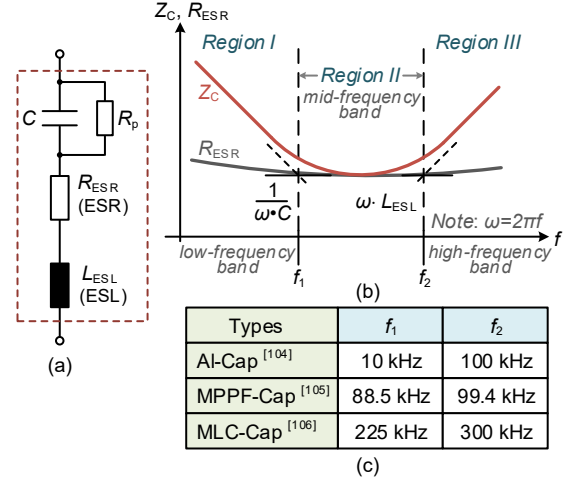


Fig. 2. Equivalent circuit model and impedance characteristics of capacitors. (a) Equivalent circuit model. (b) Impedance characteristics. (c) Typical values of f_1 , f_2 , where the types of Al-Cap, MPPF-Cap, and MLC-Cap are SLPX [104] (470 $\mu\text{F}/450\text{ V}$), B32778-JX [105] (480 $\mu\text{F}/450\text{ V}$) and KCM55WC71E107MH13 [106] (100 $\mu\text{F}/25\text{ V}$) respectively.

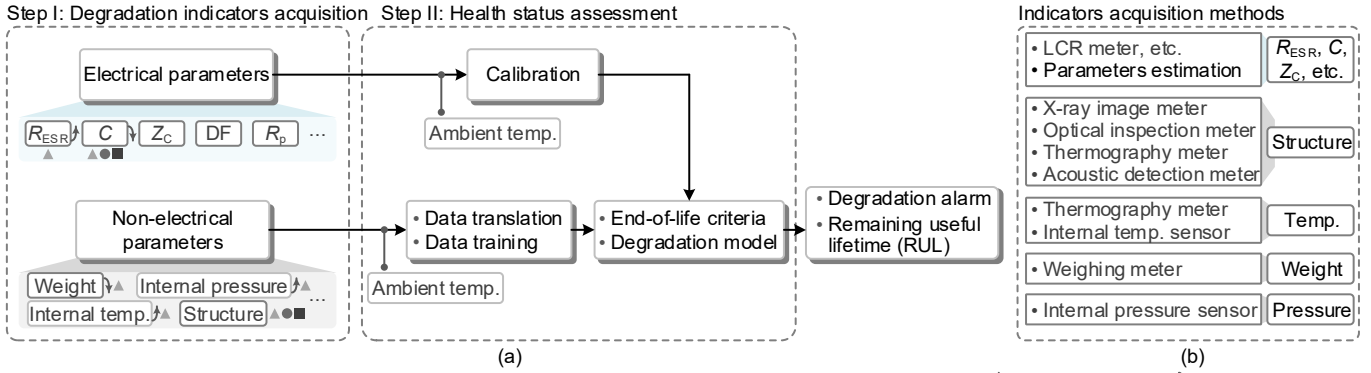
resistance. According to the model, the dissipation factor (DF) is defined as $\tan\delta = \omega \cdot R_{ESR} \cdot C$. The impedance Z_C of capacitors is expressed as

$$Z_C = \sqrt{R_{ESR}^2 + \left(2\pi f \cdot L_{ESL} - \frac{1}{2\pi f \cdot C}\right)^2}. \quad (1)$$

Using (1), Fig. 2(b) shows the impedance characteristics of capacitors [103]. It is found that the impedance is dominated by the capacitance C in Region I (i.e., low-frequency band, $f \leq f_1$), R_{ESR} in Region II (i.e., mid-frequency band, $f_1 \leq f \leq f_2$), and L_{ESL} in Region III (i.e., high-frequency band, $f \geq f_2$). Taking an Al-Cap, an MPPF-Cap and an MLC-Cap as examples, Fig. 2(c) gives the typical values of f_1 and f_2 at 25 $^\circ\text{C}$ [104]–[106], where the types of capacitor are SLPX (Al-Cap, 470 $\mu\text{F}/450\text{ V}$), B32778-JX (MPPF-Cap, 480 $\mu\text{F}/450\text{ V}$) and KCM55WC71E107MH13 (MLC-Cap, 100 $\mu\text{F}/25\text{ V}$), respectively. Notice that C and R_{ESR} are the main degradation indicators of capacitors. Thereby, Region I and Region II (i.e., low-frequency and mid-frequency bands) are considered for CM, which is discussed in the following.

B. Design Procedure for Condition Monitoring

With the degradation of dc-link capacitors, a series of physical and chemical changes occur in the inside of capacitors,



Note: ▲ Suitable indicators for Al-Caps, ● suitable indicators for MPPF-Caps, ■ suitable indicators for MLC-Caps, ↑ indicator increases, ↓ indicator decreases

Fig. 3. Condition monitoring procedure for dc-link capacitors. (a) Condition monitoring procedure. (b) Degradation indicators acquisition methods.

TABLE I TYPICAL END-OF-LIFE CRITERIA OF CAPACITORS

	Al-Caps	MPPF-Caps	MLC-Caps
End-of-life criteria	$C/C_0 < 80\%$ $R_{ESR}/R_{ESR0} > 2$	$C/C_0 < 95\%$	$C/C_0 < 90\%$

C - capacitance, R_{ESR} - equivalent series resistance, C_0 -initial capacitance, R_{ESR0} -initial equivalent series resistance.

which will cause electrical parameters (e.g., R_{ESR} , C , Z_c , DF , R_p), and non-electrical parameters (e.g., weight, structure, internal temperature, internal pressure) to be changed [107]. Generally, these parameters can be chosen as the degradation indicators of capacitors. Based on this, Fig. 3(a) presents a condition monitoring procedure for dc-link capacitors. It mainly includes two steps, i.e., degradation indicators acquisition (Step I) and capacitor health status assessment (Step II). For Step I, Fig. 3(b) lists some commonly used parameter acquisition methods. It is found that industrial instruments including weighting meters [108], [109], X-ray image meters [110], optical inspection meter [111], acoustic detection meter [112], thermography meter [113], etc., are widely used to obtain non-electrical parameters. Moreover, internal temperature sensors [114] and internal pressure sensors [115] are employed to obtain the internal temperature and pressure of capacitors. Due to the electrical parameters and non-electrical parameters of capacitors are easily influenced by the ambient temperature, which should be considered in Step II.

Considering the electrical characteristics of capacitors, the preferred indicators and their change trends for different types of capacitors are given in Fig. 3. Notice that some electrical parameters, such as Z_c , DF , and R_p can indicate the degradation of capacitors, however, it is difficult to measure them or use them to define the degradation level of capacitors. they are not the best lifetime indicators for CM. Similarly, the suitable non-electrical indicators are shown in Fig. 3. For Al-Caps, MPPF-Caps, and MLC-Caps, the change of internal structure can be used for condition monitoring. However, the changes in weight, internal pressure, and internal temperature are more suitable for Al-Caps.

Generally, electrical parameters can be measured using LCR meter, impedance analyzer, etc. However, parameter estimation based methods are widely used to estimate the electrical parameters of dc-link capacitors due to the capacitors are not

needed to be dismantled from converters in most cases, which will be detailed discussed in Section III.

1) End-of-Life Criteria

As mentioned above, R_{ESR} and C are the preferred electrical indicators for the condition monitoring of capacitors. In [102], the typical end-of-life criteria for Al-Caps, MPPF-Caps, and MLC-Caps have been summarized, as shown in Table I. Different from the electrical parameters, the non-electrical parameters of capacitors are dependent on capacity, materials, rated voltages and currents. Hence, there are no uniform end-of-life criteria for capacitors when choosing the non-electrical parameters as the degradation indicators. Generally, two categories of methods are applied to define the end-of-life criteria of capacitors.

One category is to construct the relationship between electrical parameters and non-electrical parameters, i.e., data translation method. For Al-Caps, capacitor weight, internal pressure, and internal temperature are suitable non-electrical indicators. Taking weight loss as an example, Fig. 4(a) shows the average weight loss of an Al-Cap (Nichicon PW series, 450 V/68 μ F), Fig. 4(b) gives the relationship between weight loss and R_{ESR} changes [108]. It is found that the weight of capacitors decreases with the degradation of capacitors, the critical weight loss can be defined at a 200% increase in R_{ESR} . However, the weight change is in milligrams, which requires high-accuracy measurement devices.

Another non-electrical parameter based method is to identify the failure status of capacitors using the structure change of capacitors. Taking the X-ray image based method as an example, Fig. 4(c) shows the X-ray images of a healthy Al-Cap and a failure Al-Cap. However, due to the uncertainty of structure change, it is difficult to construct the relationship between the electrical parameters and structure change. Similarly, the main physical degradation indicator of MLC-Caps and MPPF-Caps is the structure change of capacitors [e.g., internal crack of MLC-Caps, as shown in Fig. 4(d)], which is difficult to construct the relationship between the electrical parameters and non-electrical parameters. Usually, some data training algorithms are used to distinguish the damaged and undamaged capacitors. In [112], an acoustics detection based method is applied to detect the micro-crack of capacitors, as shown in Fig. 4(e).

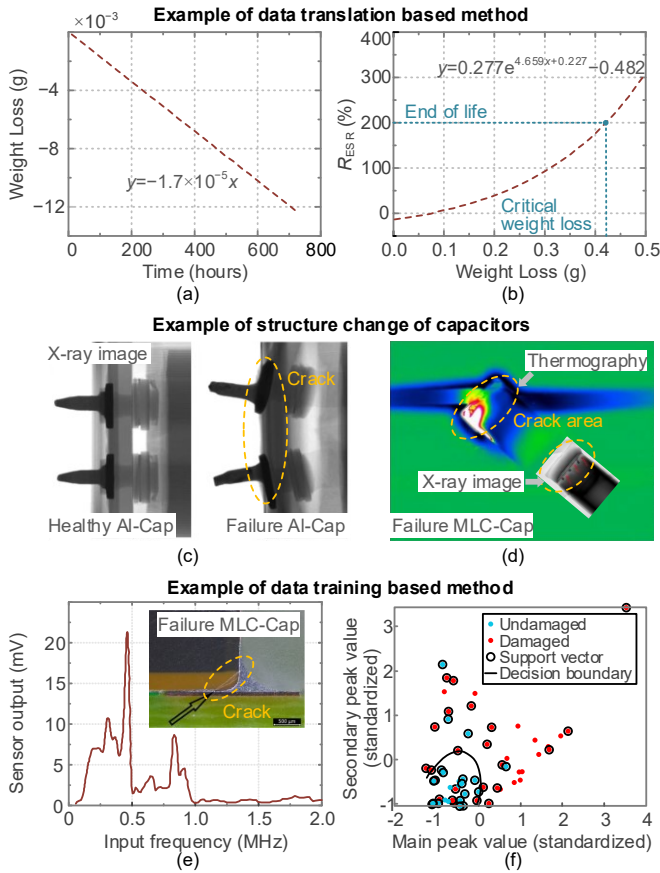


Fig. 4. Example of CM methods based on non-electrical parameters. (a) Average weight loss of a type of Al-Cap (Nichicon PW series, 450 V/68 μ F) [108]. (b) Weight loss versus R_{ESR} changes of this type of Al-Cap [108]. (c) X-ray images of a healthy Al-Cap and a failure Al-Cap [109]. (d) Thermography and X-ray image of a failure MLC-Cap [113]. (e) Acoustic response of a failure MLC-Cap [112]. (f) SVM classifier fitted into observed MLC-Cap features [112].

Based on the acoustic response of MLC-Caps, the damaged and undamaged capacitors can be distinguished using a support vector machine (SVM) classifier, as shown in Fig. 4(f).

In summary, non-electrical parameters based CM schemes generally required high-cost measurement instruments. Moreover, there are no uniform end-of-life criteria, which are not the best schemes for condition monitoring.

2) Degradation Models

Degradation models are used to calculate the remaining useful lifetime (RUL) of capacitors, which are generally based on electrical parameters. A simple degradation model of Al-Caps is described as [116], [117]

$$\begin{cases} C(t) = C_0 \cdot (1 + A_{Al} \cdot t) \\ R_{ESR}(t) = R_{ESR0} \cdot e^{\beta_{Al} \cdot t} \end{cases} \quad (2)$$

where t represents the operation time, C_0 and R_{ESR0} are the initial capacitance and ESR, respectively. A_{Al} and β_{Al} describe temperature-dependent degradation rates, which can be determined experimentally. For MPPF-Caps, the degradation model based on C is defined as [118]

$$C(t) = A_{MPPF} + \lambda_1 \cdot \lambda_2 \cdot e^{-(\lambda_1 \cdot t)} \quad (3)$$

where A_{MPPF} is a parameter which depends on C_0 , and λ_1 , λ_2 depend on the component characteristics and the applied

TABLE II EXPERIMENTAL PARAMETERS OF DEGRADATION MODELS

Cap. types	Experimental parameters	Test condition
Al-Cap [116]	$A_{Al} = -4.899 \times 10^{-6}$, $B_{Al} = 9.547 \times 10^{-5}$	300 kHz @ 54.85–126.85 °C
MPPF-Cap [118]	$\lambda_1 = 4.91 \times 10^{-8}$, $\lambda_2 = 0.001$	Rated voltage @ 85 °C
MLC-Cap [119]	k equals to 0 (for COG-type), 2.5 (for X7R-type), 7 (for Y5V-type).	2 times rated voltage @ 125 °C

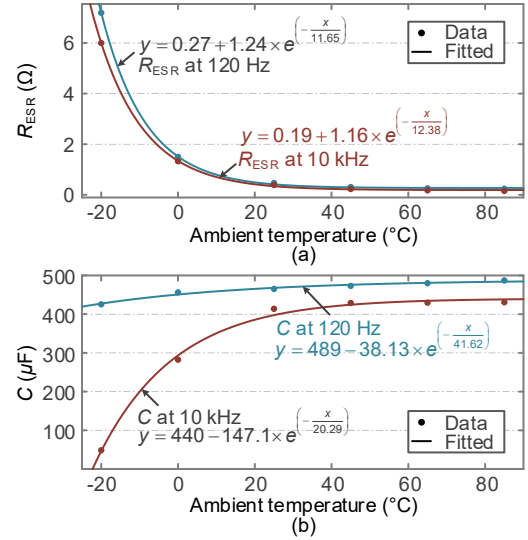


Fig. 5. R_{ESR} and C variations versus temperature of a new capacitor (Type: SLPX 470 μ F/ 450 V, datasheet [104]). (a) R_{ESR} versus temperature. (b) C versus temperature.

stresses. Similarly, the degradation model of MLC-Caps is [119]

$$C(t) = C_0 (1 - k \cdot \log t) \quad (4)$$

where k represents the maximum percent capacitance loss per decade hour, which is changed with the materials of capacitors. Taking the experimental results in [116], [118], and [119] as examples, Table II lists the experimental parameters of degradation models.

3) Electrical Parameters Calibration

It is noticed that the electrical parameters of capacitors are easily influenced by the operating frequency, ambient temperature, which needs to be calibrated in condition monitoring systems [120], [121]. Usually, the operating frequency of capacitors in converters is dependent on the known switching frequency, however, the ambient temperature is changing. Taking the Al-Cap (Type: SLPX 470 μ F/ 450 V) as an example, Figs. 5(a) and 5(b) show R_{ESR} and C variations versus temperature, respectively [104], which are given from a manufacturer datasheet. It is found that C increases as the ambient temperature T_a increases and R_{ESR} decreases as T_a increases. The relationship between R_{ESR} , C of a new capacitor and ambient temperature is given as [59]

$$\begin{cases} R_{ESR}(T_a) = \alpha_{Al} + \beta_{Al} e^{-T_a/\gamma_{Al}} \\ C(T_a) = \chi_{Al} + \lambda_{Al} e^{-T_a/\nu_{Al}} \end{cases}, T_{min} < T_a < T_{max} \quad (5)$$

where α_{Al} , β_{Al} , γ_{Al} , χ_{Al} , λ_{Al} , and ν_{Al} are characteristics coefficients of capacitors, which are determined experimentally. T_{min} and T_{max} represent the minimum and maximum operating

temperatures of capacitors respectively, which are defined by the manufactures. For SLPX-type capacitors, T_{\min} and T_{\max} are $-40\text{ }^{\circ}\text{C}$ and $+85\text{ }^{\circ}\text{C}$, respectively. Referring to Fig. 5, the variations of R_{ESR} and C at different frequencies are different. Therefore, it is needed to define the estimation frequency to establish the relationships in (5) before condition monitoring. Assuming the estimation frequencies of R_{ESR} and C are 10 kHz and 120 Hz respectively, $\alpha_{\text{Al}}, \beta_{\text{Al}}, \gamma_{\text{Al}}, \chi_{\text{Al}}, \lambda_{\text{Al}}$, and ν_{Al} of this type of capacitor are 0.19, 1.16, 12.38, 489, -38.13 , and 41.62, respectively. Notice that the relationship between C and T_a in (5) is based on the physical meaning of capacitors. It also can be written as $C(T_a) = \chi_{\text{Al}} + \lambda_{\text{Al}} \times T_a + \nu_{\text{Al}} \times T_a^2$ [56], which is based on the polynomial fitting. Here, $\chi_{\text{Al}}, \lambda_{\text{Al}}$, and ν_{Al} are 448.5, 0.84, and -0.0049 , respectively. Although the relationship between R_{ESR} , C , and T_a can be constructed, it is recommended to monitor the capacitors at a relatively low temperature (e.g. $25\text{ }^{\circ}\text{C}$) due to the influence of degradation on R_{ESR} and C is not significant at high temperatures [31].

The capacitance C of MPPF-Caps and MLC-Caps are also influenced by the temperature. For MPPF-Caps, the effects of temperature on C are dependent on the capacitor materials. For polypropylene (PP) capacitors, C decreases as the ambient temperature increases. For polyethylene terephthalate (PET) and Polyethylene naphthalate (PEN) capacitors, C increases as the ambient temperature increases. Generally, the relationship between ambient temperature T_a and capacitance is [122]

$$C(T_a) = \alpha_{\text{MPPF}} \cdot C_{20^{\circ}\text{C}} (T_a - T_{\text{test}}) + C_{\text{test}} \quad (6)$$

where C_{test} and T_{test} are the capacitance and temperature under the testing condition, $C_{20^{\circ}\text{C}}$ is the reference capacitance at $20\text{ }^{\circ}\text{C}$. α_{MPPF} is the temperature coefficient, α_{MPPF} of PP, PET, and PEN capacitors are $-250 \times 10^{-6}/\text{K}$, $600 \times 10^{-6}/\text{K}$, and $200 \times 10^{-6}/\text{K}$ respectively. Similarly, the relationships between ambient temperature T_a and capacitance of MLC-Caps can be constructed. Taking Class I MLC-Caps as an example, the relationship is [123]

$$C(T_a) = \alpha_{\text{MLC}} \cdot C_{\text{test}} (T_a - T_{\text{test}}) + C_{\text{test}} \quad (7)$$

where C_{test} represents the capacitance at T_{test} (i.e., $25\text{ }^{\circ}\text{C}$). According to the result of data fitting [124], α_{MLC} is defined as 0.001629. For Class II and Class III ceramic capacitors, the relationship between C and T_a can also be constructed in the same way.

III. DERIVATION OF CM METHODS FOR DC-LINK CAPACITORS

Comparing with industrial instruments measurement based methods, the parameters estimation based methods are more economic, which can be implemented without impairing the power converter operation. Fig. 6 presents a derivation procedure for parameters estimation methods of dc-link capacitors. The key steps are discussed as follows.

A. Parameters Estimation Principles

According to the dependence on the capacitor model, two main categories of principles are generally used to estimate the electrical parameters of dc-link capacitors. One is to estimate the parameters based on the capacitor impedance model, another is independent of the capacitor model. Furthermore,

according to the type of needed electrical signals, the first category principle includes two sub-types, i.e., periodic small-signal ripples based principle (Principle I) and non-periodic large-signal charging/discharging profiles based principle (Principle II). The second category principle treats the power electronic system as a black box, which does not need the specific capacitor model and converter model. Here, we define it as Principle III (i.e., black-box model).

Fig. 6(a) shows the equivalent circuit of dc-link capacitors, where v_{CAP} and i_{C} denote the voltage and current of capacitors respectively. Based on Ohm's law, the capacitor voltage ripple Δv_{CAP} and capacitor current ripple Δi_{C} having the following relationship

$$\Delta v_{\text{CAP}}(t) = \frac{1}{C} \int_0^t i_{\text{C}}(t) dt + R_{\text{ESR}} \cdot \Delta i_{\text{C}}(t) + L_{\text{ESL}} \cdot \frac{di_{\text{C}}(t)}{dt}. \quad (8)$$

Considering that L_{ESL} is very small (on the order of 10–100 nH [41]) at the working frequency of converters (i.e., low-and mid-frequency bands in Fig. 2), which can be ignored in dc-link capacitors. Hence, (8) can be written as

$$\Delta v_{\text{CAP}}(t) = \frac{1}{C} \int_0^t i_{\text{C}}(t) dt + R_{\text{ESR}} \cdot \Delta i_{\text{C}}(t). \quad (9)$$

Furthermore, Δv_{CAP} at low-frequency band and mid-frequency band can be simplified as

$$\Delta v_{\text{CAP_LF}}(t) \approx \frac{1}{C} \int_0^t i_{\text{C_LF}}(t) dt \quad (10)$$

$$\Delta v_{\text{CAP_MF}}(t) \approx R_{\text{ESR}} \cdot \Delta i_{\text{C_MF}}(t) \quad (11)$$

where $\Delta v_{\text{CAP_LF}}, \Delta i_{\text{C_LF}}$ denote the ripples at low-frequency band, and $\Delta v_{\text{CAP_MF}}, \Delta i_{\text{C_MF}}$ indicate them at mid-frequency band. From (10) and (11), C and R_{ESR} can be estimated as

$$C \approx \frac{1}{\Delta v_{\text{CAP_LF}}(t)} \int_0^t i_{\text{C_LF}}(t) dt \quad (12)$$

$$R_{\text{ESR}} \approx \frac{\Delta v_{\text{CAP_MF}}(t)}{\Delta i_{\text{C_MF}}(t)}. \quad (13)$$

From (12) and (13), it is easily found that C is inversely proportional to the voltage ripple Δv_{CAP} and R_{ESR} is proportional to Δv_{CAP} for a given i_{C} . Hence, (12) and (13) can be simplified as (14) and (15) when i_{C} is given.

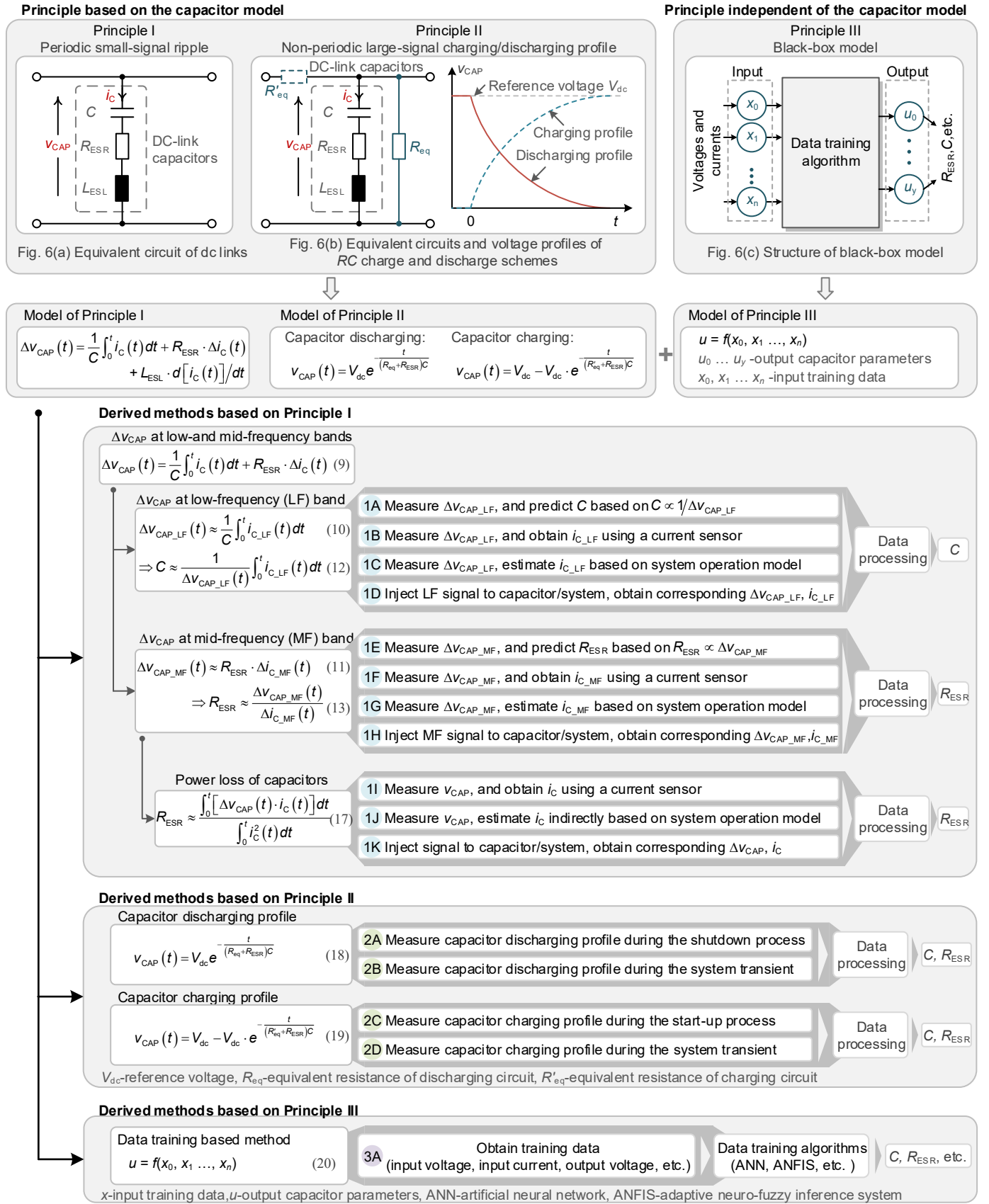
$$C \propto 1/\Delta v_{\text{CAP_LF}} \quad (14)$$

$$R_{\text{ESR}} \propto \Delta v_{\text{CAP_MF}}. \quad (15)$$

Referring to (11), the main power loss of capacitors is caused by R_{ESR} . Considering different harmonic frequencies, the total power loss P_{loss} of capacitors is

$$P_{\text{loss}} = \sum_{k=1}^n R_{\text{ESR},k} I_{\text{C_RMS},k}^2 \quad (16)$$

where $R_{\text{ESR},k}$ and $I_{\text{C_RMS},k}$ represent the ESR and the root mean square (RMS) current for each harmonic k [126]. Although (16) can be used to calculate ESR, it is difficult to determine $R_{\text{ESR},k}$ for each harmonic k . Moreover, the end-of-life criteria (e.g., $R_{\text{ESR}}/R_{\text{ESR}0} > 2$) provided by manufacturers are usually based on a frequency region (i.e., mid-frequency band) without considering a specified frequency. As discussed in [38], R_{ESR} calculated by the average power loss \bar{P}_{loss} and the total RMS current $I_{\text{C_RMS}}$ can approximately represent the actual ESR of



Note: 1) The methods 1A and 1E, 1B and 1F, 1C and 1G, 1D and 1H can be grouped together respectively when using (9). Here, C and R_{ESR} are approximately estimated under the same frequency, such as low frequency or mid frequency.

2) Fig. 6(b), Eqs. (17) and (18) are examples of Principle II. For different charging or discharging modes, the profiles and equations are different

Fig. 6. Derivation procedure for parameters estimation methods of dc-link capacitors.

capacitors in power electronic converters. Therefore, R_{ESR} is approximately calculated as

$$R_{ESR} \approx \frac{\bar{P}_{loss}}{I_{C_RMS}^2} = \frac{\int_0^t [\Delta v_{CAP}(t) \cdot i_C(t)] dt}{\int_0^t i_C^2(t) dt}. \quad (17)$$

Principle II is based on the large-signal discharging/charging profile, as shown in Fig. 6(b). The left part of Fig. 6(b) shows the equivalent circuit of capacitor discharging and charging schemes, where R_{eq} and R'_{eq} represent the equivalent resistances of discharging circuits and charging circuits respectively. The right part gives the discharging and charging profiles, where, V_{dc} denotes the reference value of capacitor voltage. During the discharging period, the capacitor voltage is expressed as

$$v_{CAP}(t) = V_{dc} e^{-\frac{t}{(R_{eq} + R_{ESR})C}}. \quad (18)$$

During the charging period, the capacitor voltage is

$$v_{CAP}(t) = V_{dc} - V_{dc} \cdot e^{-\frac{t}{(R'_{eq} + R_{ESR})C}}. \quad (19)$$

By solving (17) and (18), R_{ESR} and C can be estimated.

Principle III is based on the black-box model, as shown in Fig. 6(c). Here, the power electronic system to be monitored is treated as a black box. Taking the voltage and current signals of systems as input data, the capacitor parameters can be estimated using data training algorithms (e.g., artificial neural network) without considering the specific capacitor model and converter model. The relationship between capacitor parameters and input signals can be obtained using training algorithms, i.e.,

$$u = f(x_0, x_1, \dots, x_n) \quad (20)$$

where $u_0 \dots u_y$ denote the output capacitor parameters, and x_0, x_1, \dots, x_n are the input training data.

B. Derivation of Condition Monitoring Methods

Based on the three key principles, the condition monitoring methods for dc-link capacitors can be derived in a step by step manner. There exist 16 derived methods, as shown in Fig. 6.

1) Derived Methods based on Principle I

There exist 11 derived methods based on Principle I, where methods 1A and 1E use the voltage ripple to approximately estimate the capacitor parameters without dependency on the capacitor current. The methods 1B–1D, 1F–1H and 1I–1K utilize sampled or estimated capacitor current to calculate R_{ESR} or C , which are illustrated using the examples in Fig. 7.

Fig. 7(a) shows an implementation example of methods 1B and 1F. Here, the capacitor current is directly sampled by a current sensor. To accurately obtain R_{ESR} or C , a band-pass filter and a low-pass filter are required respectively. To avoid using capacitor current sensors, the methods 1C and 1G utilize the circuit operation model to indirectly obtain i_C . Referring to Fig. 7(b), taking a buck converter as an example, it is easily found that $i_C = i_L - i_o$, where i_L and i_o are inductor current and load current respectively.

The implementation of schemes 1D and 1H can be divided into two categories. One is to inject current into the tested capacitor directly, as shown in Fig. 7(d). Here, a signal generation circuit including a signal generator and a power amplifier is employed to inject current signals at given frequencies to the tested capacitor. The injected signal can be sinusoidal waves, square waves, triangle waves, etc. Another is to inject a perturbation signal into the power electronic systems. Taking a photovoltaic (PV) grid-connected inverter as an example, Fig. 7(e) gives the implementation scheme. Here, a current at h th harmonic frequency is injected into the grid, which causes $(h-1)$ th and $(h+1)$ th voltage and current ripples to appear on the dc-link capacitors. Then, R_{ESR} and C can be estimated using the voltage and current ripples at $(h-1)$ th or $(h+1)$ th.

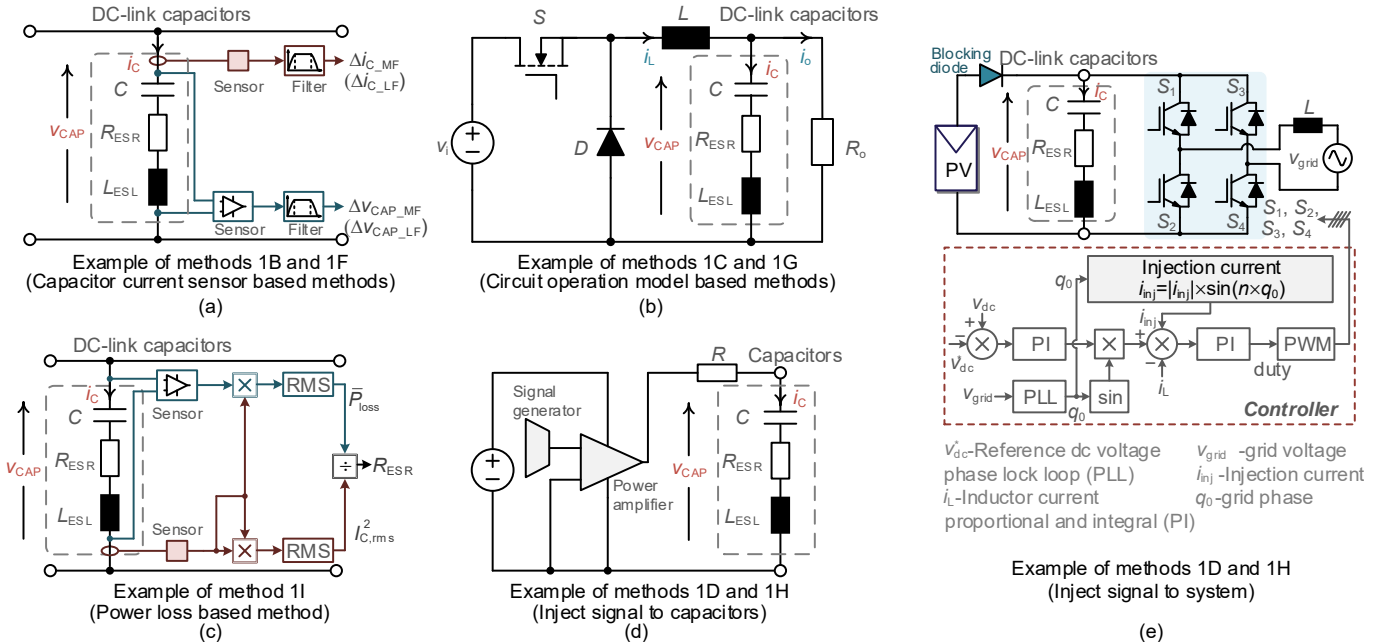


Fig. 7. Implementation examples of derived methods based on Principle I. (a) Example of methods 1B and 1F. (b) Example of methods 1C and 1G based on a buck converter. (c) Examples of methods 1I. (d) Example of method 1D and 1H, here, extra signals are injected to capacitors. (e) Example of method 1D and 1H based on a PV inverter, here, extra signals are injected to systems.

TABLE III DESCRIPTION OF DERIVED METHODS 1A–1H

Derived methods	Description
1A, 1E	Capacitor voltage based methods
1B, 1F	Capacitor current sensor based methods
1C, 1G	Circuit operation model based methods
1D, 1H	External signal injection based methods

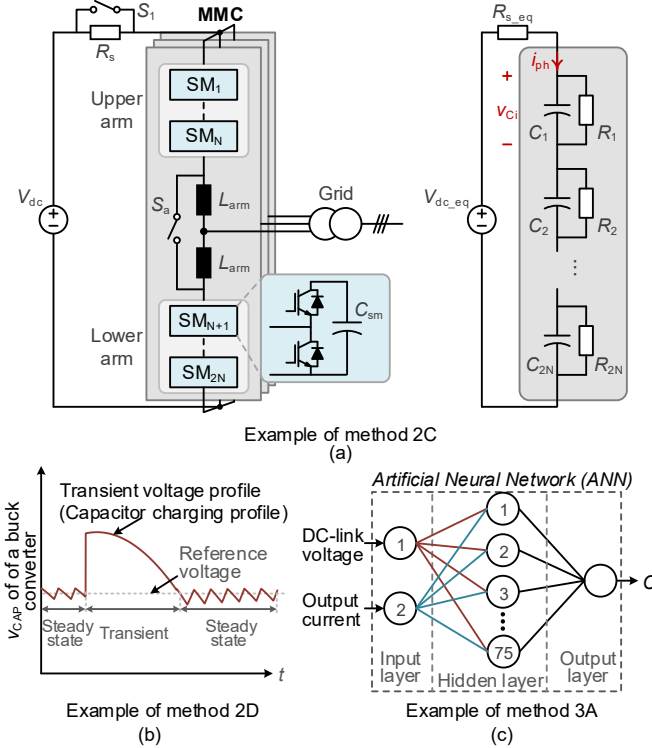


Fig. 8. Implementation examples of derived methods based on Principles II and III. (a) Example of method 2C based on an MMC. (b) Example of method 2D based on a buck converter. (c) Example of method 3A.

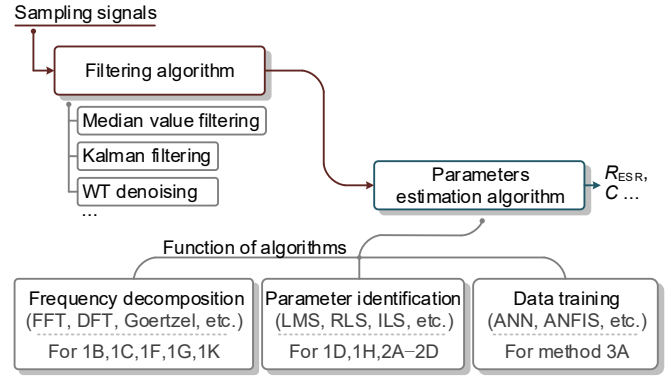
Notice that the methods 1A and 1E, 1B and 1F, 1C and 1G, 1D and 1H can be grouped together respectively when using (9). The description is listed in Table III. Here, C and R_{ESR} are approximately estimated under the same frequency, such as low frequency or mid frequency.

According to (17), R_{ESR} can be calculated using power losses of capacitors. Fig. 7(c) shows the implementation of the method 1I. It is similar to the method 1B, however, a band-pass filter is not required. The implementation of method 1J and 1K are similar to 1G and 1H, respectively.

2) Derived Methods based on Principles II and III

There exist 4 derived methods based on Principle II, where 2A, 2B are based on the discharging profile, and 2C, 2D are based on the charging profile.

The methods 2A and 2C obtain the discharging or charging profiles during the shutdown process or start-up process of converters. Referring to Fig. 6(b), during the shutdown process of converter, the dc-link capacitors discharge through the equivalent resistor R_{eq} . The capacitor parameters can be estimated based on the discharging profile and (18). During the start-up process of converter, the capacitors charge through R'_{eq} . The capacitor parameters can be estimated based on the



Note: FFT-fast Fourier transform, DFT-discrete Fourier transform, LMS-least mean squares, RLS-recursive least squares, ILS-iterative least squares, ANN-artificial neural network, ANFIS-adaptive neuro fuzzy inference system, WT-wavelet transform.

Fig. 9. Data processing procedure for condition monitoring.

charging profile and (19). Taking modular multilevel converters (MMCs) as an example, the left part of Fig. 8(a) shows the circuit of a three-phase MMC, which including the detailed circuit of a sub-module (SM) [127]. During the DC-side start-up process, the power switches S_1 turns OFF and S_a turns ON, the equivalent circuit of a signal-phase MMC is given in the right part of Fig. 8(a). Here, R_s and R_{s_eq} represent the equivalent start-up resistance with/without considering the resistance of diodes, N denotes the number of SM in each arm, C_i and R_i are the capacitance and resistance of the i -th SM. Referring to the right part of Fig. 8(a), the capacitors are charged through R_{s_eq} during this start-up process. Assuming each SM has the same phase current i_{ph} and the same capacitor voltage v_{Ci} , the capacitances can be estimated using the equivalent DC voltage V_{dc_eq} , R_{s_eq} and the charging profile [see Fig. 6(b)].

Similar to the shutdown and start-up processes, the capacitors will be discharged or charged during transients. Taking buck converters as examples, Fig. 8(b) shows the voltage profile (i.e., capacitor charging profile) during an unloading transient. Based on the relationship between charging profile and capacitor parameters, R_{ESR} and C can be estimated [99].

The method 3A is based on Principle III, an implementation example is shown in Fig. 8(c). Here, an artificial neural network (ANN) algorithm is used to estimate the capacitance for an ac/dc/ac system. Taking dc-link voltage and output current as training data, the capacitance can be estimated based on the data training algorithm.

C. Data Processing

Referring to Fig. 6, data processing is a key link of the condition monitoring for dc-link capacitors. Fig. 9 shows the general procedure of data processing for condition monitoring. First, the sampling signals are filtered using filtering algorithms including median value filtering, Kalman filtering, wavelet transform denoising, etc. Then parameter estimation algorithms are employed to obtain capacitor parameters. For methods 1B, 1C, 1F, 1G, and 1K, the key issue is to obtain the low-frequency or mid-frequency components of capacitor voltage and capacitor current. Usually, frequency decomposition

algorithms including fast Fourier transform (FFT) algorithm, discrete Fourier transform (DFT) algorithm, Goertzel algorithm, etc., are used to extract the low-frequency or mid-frequency components of v_{CAP} and i_C .

For methods 1D, 1H, and 2A–2D, adaptive filter algorithms including least mean squares (LMS) algorithm, recursive least squares (RLS) algorithm, iterative least squares (ILS) algorithm, etc. are widely used to identify R_{ESR} and C in equations (9)–(11), (18) and (19). Moreover, some optimization algorithms, such as particle swarm optimization (PSO) algorithm, genetic algorithm (GA) can be used to identify capacitor parameters.

For method 3A, data training algorithms including artificial neural network (ANN) algorithm, adaptive neuro-fuzzy inference system (ANFIS) algorithm, support vector regression (SVR) algorithm, etc., are widely used for condition monitoring.

IV. APPLICATION OF DERIVED CONDITION MONITORING METHODS

A. Overview of the Application of CM Methods

Based on the derived methods, various condition monitoring techniques for dc-link capacitors have been proposed in [11]–[109]. Fig. 10 gives the development history of these techniques. It is found that the research on the condition monitoring techniques for dc-link capacitors started at the end of the 1990s, and it has become a hot issue in the past decade. Fig. 11(a) shows a statistical analysis of CM techniques for different types of dc-link applications, where the offline

schemes estimate the capacitor parameters under the case that the capacitors are dismantled from converters, which can be applied for all types of converters. Different from offline schemes, real-online or quasi-online schemes (CM under special test conditions, such as start-up and shutdown process) can be implemented on-site in a real system, which are widely used for condition monitoring of capacitors in adjustable speed drive (ASD) systems, photovoltaic (PV) inverters, power factor correction (PFC) converters, dc/dc converters, etc.

From Fig. 11(a), it is found that the dc/dc converters and ac/dc/ac or dc/ac ASD systems are the most popular research objectives. More than 60% of CM techniques are proposed for these two types of applications. For different dc-link applications, Fig. 11(b) gives the distribution of CM methods, where the ordinate shows the number of applied methods. Taking ASD systems and dc/dc converters as examples, it is found the signal injection based method (1D, 1H) and circuit operation model based method (1C, 1G) are widely used respectively. Moreover, from the perspective of availability, Fig. 11(b) illustrates that the real-online scheme is the most popular one for CM.

For different types of dc-link applications, the detailed discussions of CM methods are given in Section V to Section VII. Offline monitoring techniques are independent of topologies of converters, which are investigated in the following part.

B. Offline Monitoring Techniques

1) Implementation of offline monitoring schemes

Generally, industrial instruments including LCR meter,

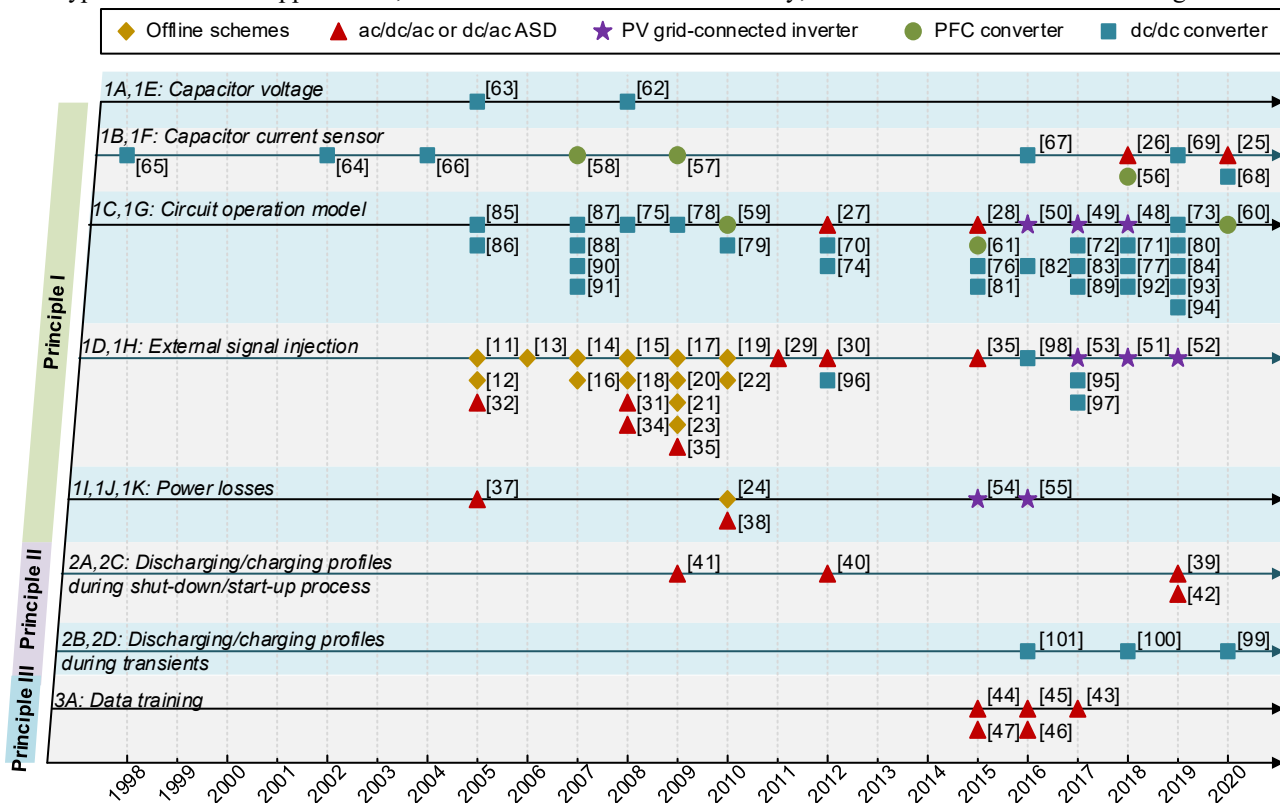


Fig. 10. Development history of the condition monitoring techniques for dc-link capacitors.

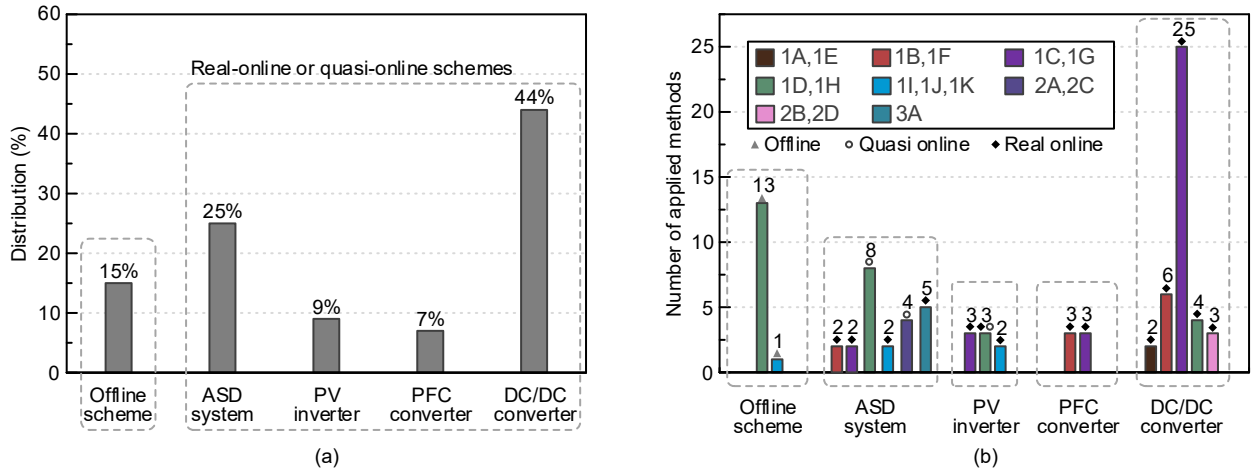


Fig. 11. Statistics of condition monitoring techniques for dc-link applications. (a) Statistics of research objects. (b) Condition monitoring schemes for different types of dc-link applications.

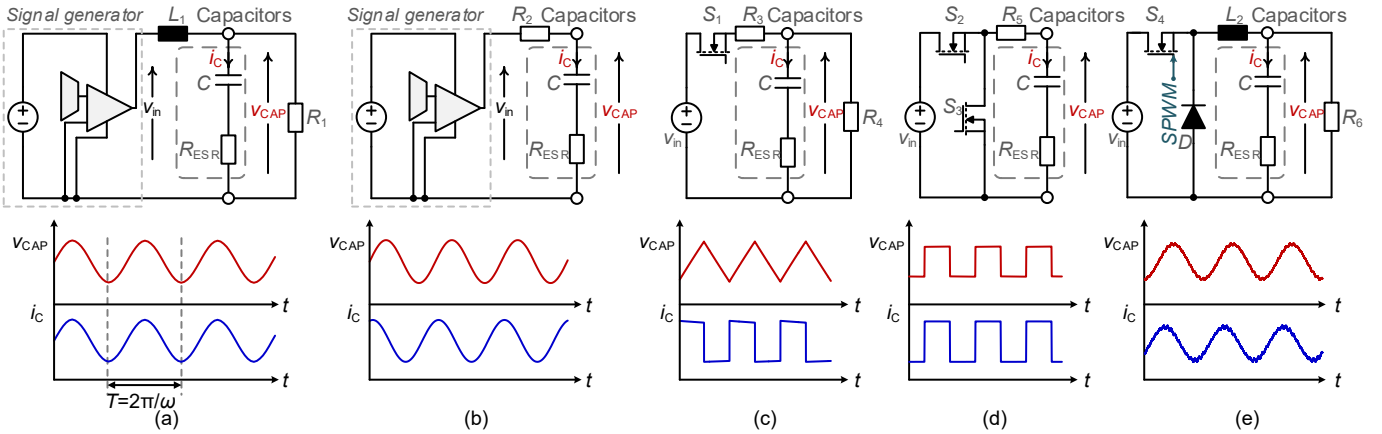


Fig. 12. Schematics of CM schemes for dismantled capacitors, here, L_{ESL} is ignored. (a) LC circuit with sinusoidal signal injection scheme. [12]. (b) RC circuit with sinusoidal signal injection scheme [13]–[19]. (c) Charge-discharge circuit scheme [19], [20]. (d) Square wave signal injection scheme [21], [22]. (e) Buck converter scheme [23].

impedance analyzer, etc., can be used for the offline measurement of R_{ESR} and C of capacitors. Considering the high price of these instruments, various low-cost offline measurement techniques have been presented in [11]–[24]. Ignoring L_{ESL} , a simple offline scheme is shown in Fig. 12 (a). Here, a sinusoidal signal is injected into an LC circuit, then R_{ESR} near the resonance frequency ω of an Al-Cap is estimated as [11], [12]

$$R_{ESR} = \sqrt{\left(\frac{v_{CAP} L_1 C \omega}{v_{in}}\right)^2 - \frac{1}{\omega^2}} / C \quad (21)$$

where v_{in} is the injected sinusoidal signal. However, this scheme ignores the effect of frequency on R_{ESR} and C .

To overcome the aforementioned shortcomings, [13]–[19] use an RC circuit to estimate the capacitor parameters. Referring to Fig. 12(b), a modulated sinusoidal signal is injected to the RC circuit, which causes sinusoidal voltage v_{CAP} and current i_C on the capacitor. According to the relationship between v_{CAP} and i_C , R_{ESR} and C can be estimated by using analysis algorithms, such as Laplace transform [13], Newton-Raphson (NR) algorithm [14], [15], discrete Fourier transform (DFT) [16], [17], and least mean square (LMS) algorithm [18]–[19].

Besides the sinusoidal signal generation circuit, a charge-discharge circuit is proposed in [19], [20], as shown in Fig. 12(c). Using the LMS algorithm, the capacitor parameters are calculated based on the relationship between v_{CAP} and i_C . In [21], [22], another RC circuit scheme is proposed, as shown in Fig. 12(d). Here, the injection signal is a square wave, which is different from that of Fig. 12(b). Using v_{CAP} and v_{in} , C and R_{ESR} are estimated at low-frequency and high-frequency bands respectively. Referring to Fig. 12(e), a buck converter with a sinusoidal pulse width modulator (SPWM) is also proposed for offline measurement of capacitors [23]. Using DFT, R_{ESR} and C are calculated based on the analysis of v_{CAP} and i_C .

All of the above-mentioned schemes are implemented based on methods 1D and 1H. Different from that, [24] utilizes the power loss on capacitors to estimate capacitor parameters. Referring to Fig. 12(b), a low-frequency sinusoidal current is injected into the capacitor, then R_{ESR} and C are calculated as

$$\begin{cases} R_{ESR} = \bar{P}T / \int_0^T i_C^2(t) dt \\ C = T / 2\pi \sqrt{\left(\int_0^T v_{CAP}^2(t) dt\right) / \left(\int_0^T i_C^2(t) dt\right) - R_{ESR}^2} \end{cases} \quad (22)$$

TABLE IV ESTIMATION ERROR OF SINUSOIDAL WAVE INJECTION CIRCUIT WITH DIFFERENT ALGORITHM

Injection signal	Methods	Algorithms	Error of C δ_C	Error of R_{ESR} δ_R	Ref.
Sinusoidal wave circuit [Fig. 12(b)]	1D, 1H	Laplace	$\delta_C_{120\text{Hz}}=17.6\%$	$\delta_R_{750\text{Hz}}=18\%$	[13]
		NR	$\delta_C_{120\text{Hz}}=1.5\%$	$\delta_R_{120\text{Hz}}=19.8\%$	[14]
		DFT	$\delta_C_{120\text{Hz}}=1.5\%$	$\delta_R_{1\text{kHz}}=5.9\%$	[17]
	LMS	$\delta_C_{120\text{Hz}}=0.8\%$	$\delta_R_{1\text{kHz}}=0.3\%$	[19]	
	1K	N/A	$\delta_C_{50\text{Hz}}=4.7\%$	$\delta_R_{50\text{Hz}}=3.5\%$	[24]

NR-Newton Raphson algorithm, DFT-discrete Fourier transform algorithm, LMS-least mean square algorithm.

TABLE V ESTIMATION ERROR FOR DIFFERENT TYPES OF SIGNAL-INJECTION CIRCUIT

Signal injection circuit	Algorithms	Error of C δ_C	Error of R_{ESR} δ_R	Ref.
Sinusoidal wave circuit [Fig. 12(b)]	LMS	$\delta_C_{120\text{Hz}}=0.8\%$ $\delta_C_{1\text{kHz}}=0.3\%$	$\delta_R_{120\text{Hz}}=1.6\%$ $\delta_R_{1\text{kHz}}=9.7\%$	[19]
Charge-discharge circuit [Fig. 12(c)]	LMS	$\delta_C_{120\text{Hz}}=1.9\%$ $\delta_C_{1\text{kHz}}=1\%$	$\delta_R_{120\text{Hz}}=4.1\%$ $\delta_R_{1\text{kHz}}=0.4\%$	[19]
Square-wave circuit [Fig. 12(d)]	N/A	$\delta_C_{1\text{kHz}}=4.9\%$	$\delta_R_{150\text{kHz}}=8.8\%$	[22]
Buck converter [Fig. 12(e)]	DFT	N/A	$\delta_R_{1\text{kHz}}=3\%$	[23]

LMS-least mean square algorithm, DFT-discrete Fourier transform algorithm.

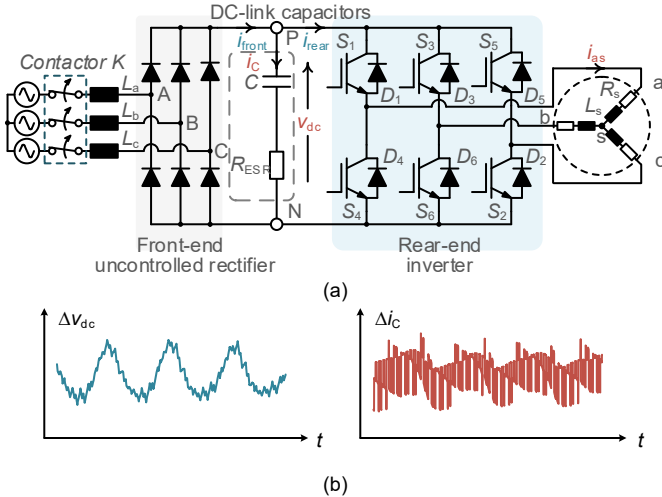


Fig. 13. Adjustable speed drive (ASD) system with a front-end diode rectifier [26], here, L_{ESL} is ignored. (a) System structure. (b) Capacitor voltage ripple and current ripple.

where T is the period of the sinusoidal signal and \bar{P} is the capacitor average power.

2) Discussion of offline monitoring schemes

As mentioned above, the offline schemes are mainly based on methods 1D, 1H and 1K (i.e., signal injection scheme). Various data processing algorithms including Laplace transform, DFT, LMS, etc., are used. To compare the estimation accuracy of these algorithms, Table IV lists the estimation errors of C and R_{ESR} . Here, sinusoidal signal injection scheme [see Fig. 12(b)] is taken as examples. It illustrates that the estimation errors of the Laplace transform and NR algorithm are relatively high. And, the NR algorithm is not suitable for the estimation of R_{ESR} . For the DFT algorithm and LMS algorithm, their estimation errors are relatively low and the error of the LMS algorithm is minimum.

To compare the estimation accuracy of different types of signal injection circuit, Table V summarize the estimation error

of these schemes. Due to the lack of data processing algorithms, the estimation accuracy of square-wave circuit [see Fig. 12(d)] is relatively low. For capacitance estimation, the estimation accuracy of sinusoidal wave circuit [see Fig. 12(b)] is larger than that for charge-discharge circuit [see Fig. 12(c)]. And the estimation accuracy decreases as the injection-signal frequency increases. For ESR estimation, the charge-discharge circuit [see Fig. 12(c)] has a relatively high estimation accuracy. And the estimation error decreases as the injection-signal frequency increases.

In summary, a low-frequency sinusoidal current injection based scheme is more suitable for capacitance estimation. A square-wave current with relatively high frequency is more suitable for ESR estimation.

V. CM FOR CAPACITORS IN AC/DC/AC OR DC/AC ASD SYSTEMS

Adjustable speed drive (ASD) systems are widely used in industrial and residential applications. Various CM schemes for capacitors in ASD systems have been presented in [25]–[47].

A. Implementation of CM Schemes based on Principle 1

1) Capacitor current sensor based methods (1B, 1F)

A generic structure of two-stage ASD systems with a front-end diode rectifier is shown in Fig. 13(a). The corresponding dc-link voltage waveform and capacitor current waveform are shown in Fig. 13(b). In [25], [26], a CM scheme based on 1B and 1F is proposed to estimate the capacitor parameters of this system. Firstly, the capacitor voltage ripple and current ripple are directly measured by sensors, as shown in Fig. 7(a). Then data processing algorithms, such as the Goertzel algorithm [25] and fast Fourier transform (FFT) [26] are applied to analyze the sampled waveforms. Based on equations (12) and (13), C and R_{ESR} are estimated using the extracted mid-frequency and low-frequency components of capacitor current ripple Δi_c and voltage ripple ΔV_{CAP} .

2) Circuit operation model based methods (1C, 1G)

To avoid using a capacitor current sensor, [27], [28] indirectly obtain capacitor current using $i_c = i_{front} - i_{rear}$, where i_{front} and i_{rear} represent the front-end current and rear-end current respectively. Referring to Fig. 13(a), when $i_{rear} = 0$, i_c equals i_{front} . Based on the estimated capacitor current, R_{ESR} and C can be calculated using equations (12) and (13).

3) External signal injection based methods (1D, 1H)

In [29], [30], a signal injection scheme is proposed to estimate the capacitor parameters of ASD systems. Referring to Fig. 13(a), condition monitoring is taken when the motor is stopped. Here, the contactor K is keeping ON. When S_6 is turned ON and S_1 is controlled by a constant-duty constant-frequency PWM, the charge on the capacitor can be discharged through the phase a and phase b windings, which causes voltage and current ripples on the dc link. The equivalent circuit and corresponding waveforms are given in Fig. 14(a) and Fig. 14(b) respectively. Using ripples ΔV_{dc} and Δi_c , C and R_{ESR} can be estimated based on equations (10) and (11). The flowchart is shown in Fig. 14(c). In [31], the same method is used for a single-phase motor drive system.

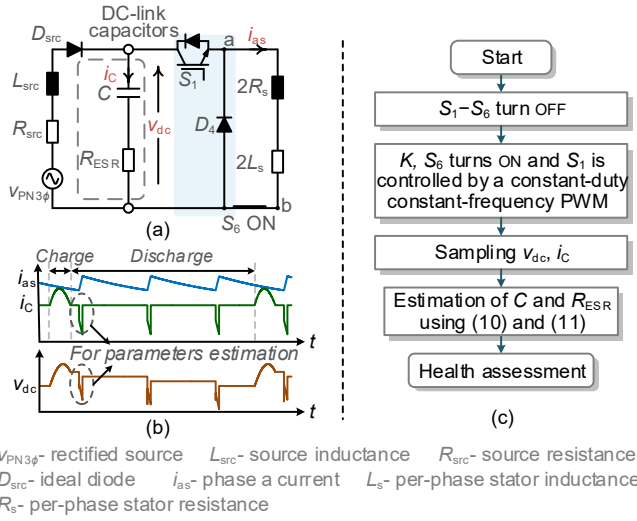


Fig. 14. Current injection based scheme [29], here, L_{ESL} is ignored. (a) Equivalent circuit under CM condition. (b) Key waveforms. (c) Flowchart of the monitoring scheme.

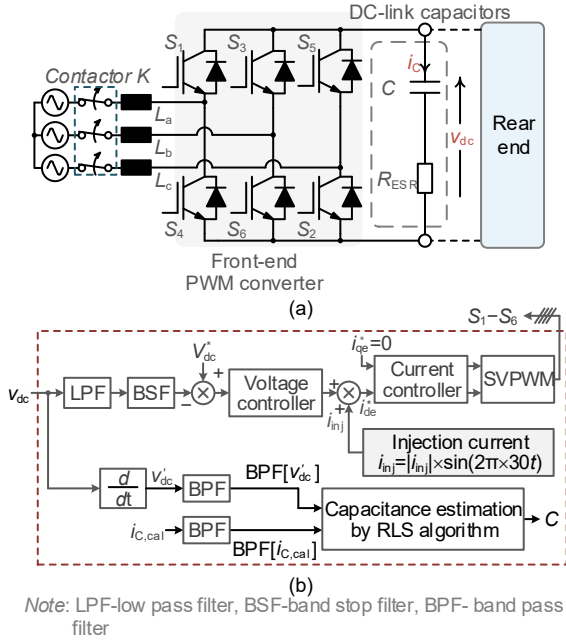


Fig. 15. Block diagram for monitoring capacitors in a PWM converter [32], here, L_{ESL} is ignored. (a) Structure of a PWM converter. (b) Block diagram of a signal injection based scheme.

Besides a diode rectifier, a pulse-width modulation (PWM) converter is widely used as the first stage of two-stage ASD systems, as shown in Fig. 15(a). In [32]–[35], Dong-Choon *et al.* utilize current injection-based schemes to estimate the capacitor parameters of PWM converters [front end of Fig. 15(a)] and two-stage ac/dc/ac converters. Referring to Fig. 15(b), at no-load condition, a controlled AC current i_{inj} with a lower frequency (30 Hz) than the line frequency is injected into the front-end PWM converter, which induces voltage ripples on the dc link. Using (10) as well as the extracted v_{dc} and i_{dc} at 30 Hz, C is estimated based on the recursive least square (RLS) algorithm [32], i.e.,

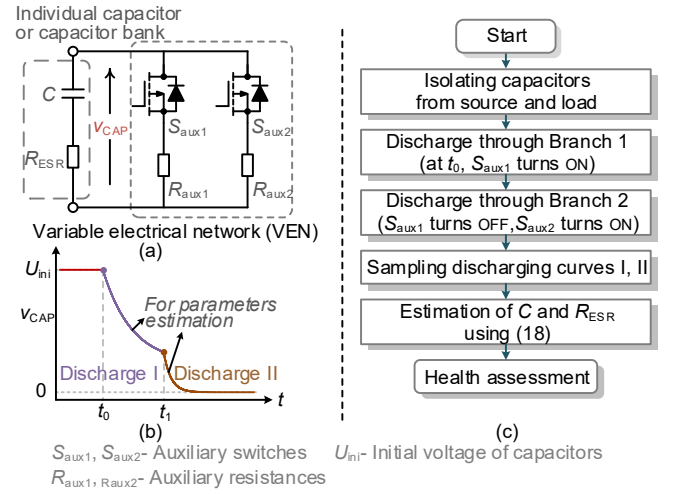


Fig. 16. Variable resistance network based capacitor discharge scheme [39], here, L_{ESL} is ignored. (a) Variable resistance network. (b) Discharge profile. (c) Flowchart of the monitoring scheme.

$$C = \frac{\text{BPF}[i_{C,cal}]}{\text{BPF}[v'_{dc}]} \quad (23)$$

where $\text{BPF}[\cdot]$ represents the band-pass filter quantity, $i_{C,cal}$ is the derived capacitor current based on the system operation mode.

Utilizing the similar schemes, the capacitor parameters of three-phase systems or single-phase systems are estimated in [33]–[35], where [33] is based on current injection and [34], [35] are based on voltage injection. Notice that for an ASD system with a front-end uncontrolled rectifier, it is impossible to inject current signals into the front end at no-load condition. Therefore, [36] injects the AC current signal into the rear-end inverter when the motor operates in the regenerative model.

4) Power losses based method (II)

Based on the estimated method in Fig. 7(d), [37], [38] calculated R_{ESR} using $R_{ESR} = P_{dc,rms} / I_{C,rms}^2$. In [37], the RMS values $P_{dc,rms}$, $I_{C,rms}$ are obtained using analog RMS converters. In [38], the RMS values are calculated in a microcontroller.

B. Implementation of CM Schemes based on Principle II

Usually, the capacitor discharging profile is obtained during the shutdown process of systems. In [39], an auxiliary capacitor-discharge network is proposed for two-stage ac/dc/ac converters. Referring to Fig. 16 (a), a variable electric network (VEN) consisting of auxiliary switches and resistors is connected in parallel with dc-link capacitors (individual capacitor or capacitor bank). After the converter shuts down, the dc-link capacitors are isolated from the power source and load. The charge in capacitors can be released through the auxiliary resistor net. By controlling the switching of auxiliary switches S_{aux1} and S_{aux2} , a two-period discharge trajectory is formulated, as shown in Fig. 16(b). Sampling the discharge profile, C and R_{ESR} can be estimated based on (18). The flowchart is shown in Fig. 16(c).

Besides the additional discharging path, motor windings and impedance networks in the converter systems are used to form a discharge path. In [40], a constant-current discharge scheme is

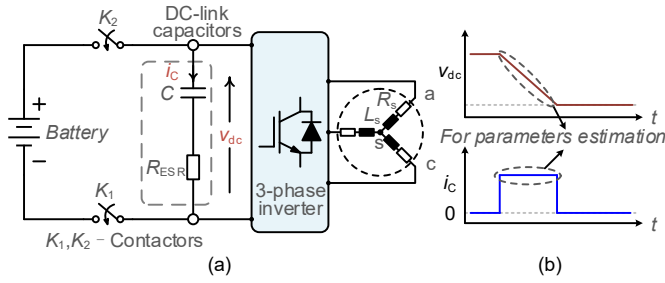


Fig. 17. Constant-current discharge based scheme [40], here, L_{ESL} is ignored. (a) Electrical configuration of an electric vehicle. (b) Constant-current discharge profiles.

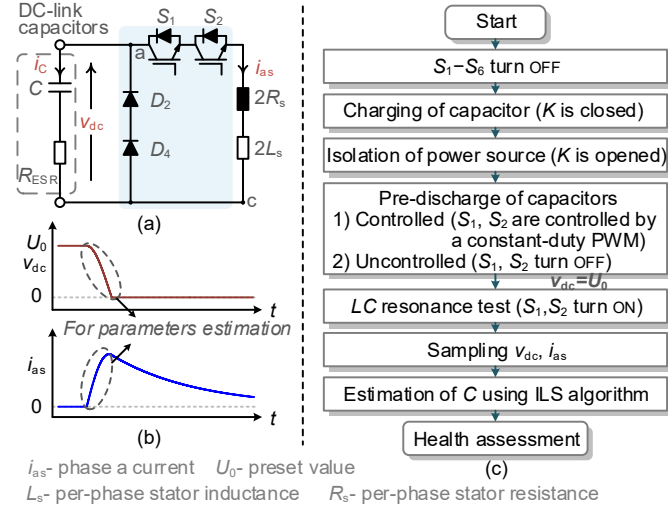


Fig. 18. LC-resonance based capacitor-charge scheme [41], here, L_{ESL} is ignored. (a) Equivalent circuit under CM condition. (b) Capacitor discharging profile. (c) Flowchart of the monitoring scheme.

proposed to monitoring the capacitors in ASD system for electric vehicles. Referring to Fig. 17(a), when the motor is stopped, capacitors and inverter are isolated from the power source (K_1 and K_2 are opened). Here, the capacitors start to discharge through the windings. By controlling the inverter, the capacitors can discharge at a constant current, as shown in Fig. 17(b). Using the discharge profiles v_{dc} and i_c , the capacitance can be estimated using (18). In [41], an LC-resonance capacitor-discharge profile based scheme is proposed for an ASD system [see Fig. 13(a)]. The condition monitoring is taken when the system is before start up. Fig. 18(a) shows the equivalent circuit of the rear-end inverter under the capacitor monitoring condition. By turning on S_1 and S_2 , the capacitor, phase a and phase c windings can form an LC-resonant circuit during the capacitor discharging period. The discharging profile is shown in Fig. 18(b). By sampling the discharge trajectories v_{dc} and i_{as} , the capacitance can be calculated by iterative least squares (ILS) algorithm. The detailed monitoring flowchart is shown in Fig. 18(c).

Considering the impedance networks in the converter systems, a discharging profile based scheme is proposed for ASD systems in railway power trains [42], as shown in Fig. 19(a). When the motor is stopped, the dc-link is isolated from the source and motor. By controlling the switch S_{break} , a C-LC-R-type discharge path is formed, as shown in Fig. 19(b).

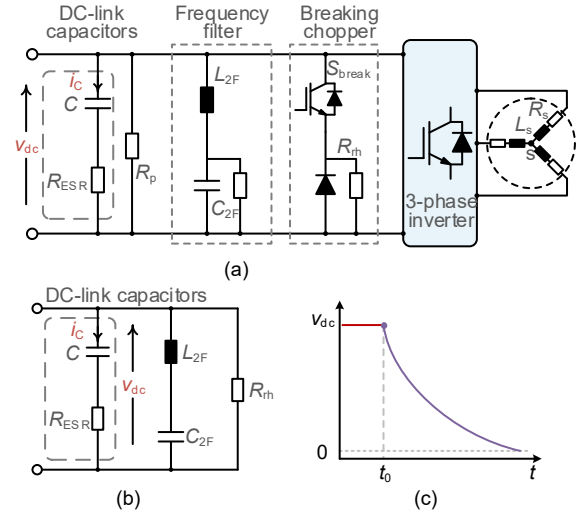


Fig. 19. Capacitor discharge through impedance networks in an ASD system for railway power trains [42], here, L_{ESL} is ignored. (a) Structure of a general traction scheme. (b) Equivalent circuit under CM condition. (c) Discharging profile.

According to the discharging profile in Fig. 19(c), C is estimated using LMS algorithm.

C. Implementation of CM Schemes based on Principle III

In [43]–[46], artificial neural network (ANN) algorithm based schemes are proposed to estimate the capacitor parameters of ASD system. An implementation example is given in Fig. 8(c). The key issue of these schemes is to obtain and define a suitable training data set. To accurately obtain the relationship between capacitor parameters and input training data (such as input current, input voltage, dc-link voltage, output current, output voltage), different capacitance and load conditions must be considered in the training process. Besides the ANN algorithm, an adaptive neuro-fuzzy inference system (ANFIS) algorithm is employed to train data to monitor the capacitor health state in [47].

D. Discussions of CM Schemes for Capacitors in ASD Systems

Table VI summarizes the CM schemes for capacitors in ASD systems. Brief remarks are given as follows.

- 1) The derived schemes based on 1B, 1F, and 1I can real-online estimate capacitor parameters, however, capacitor current sensors, additional signal processing circuits, and complex algorithms are required [25], [26], [37], [38].
- 2) The derived schemes based on 1C and 1G can real-online estimate capacitor parameters without a capacitor current sensor. However, the estimation accuracy is relative low [27], [28].
- 3) The derived schemes based on 3A are real-online estimate schemes, which have relatively estimation accuracy. Additional sensors and hardware circuits are not required. However, complexly training algorithms and a large amount of training data are required, which is the maximum challenge [43]–[47].
- 4) The derived schemes in [29]–[36] (based on 1D, 1H) and [40]–[42] (based on 2A) are quasi-online schemes,

without additional current sensors and hardware circuits. The estimation accuracy is relatively high, however, some complex control of systems needs to be considered.

In summary, from the perspective of estimation accuracy and hardware cost, the schemes based on signal injection (1D, 1H), discharging profile (2A), and data training (3A) are recommended for condition monitoring of capacitors in ASD systems.

VI. CM FOR CAPACITORS IN PV GRID-CONNECTED INVERTERS AND PFC CONVERTERS

A. CM for Capacitors in PV Grid-connected Inverters

Single-phase inverters are widely used in photovoltaic (PV) systems to feed power from energy sources to the grid. Some condition monitoring schemes of capacitors in single-phase inverters are presented in [48]–[55]. All of these schemes are derived based on Principle I.

1) Circuit Operation Model based Methods (1C, 1G)

In [48] a derived scheme based method 1C is proposed to estimate C of the input capacitor in a single-phase grid-connected PV H4 inverter, as shown in Fig. 20(a). Here, the average capacitor current i_C is calculated as $i_C = i_{pv} - i_{inv} = i_{pv} - i_L(S_1S_4 - S_2S_3)$, where $S_1 - S_4$ are the state of the switches. The estimated capacitor current and capacitor voltage waveform are shown in Fig. 20(b). The dc-link voltage is sampled at two special instants t_1 and t_2 , where average capacitor current equals to 0, i.e., $i_C(t_1) = i_C(t_2) = 0$. Thus, the capacitance is calculated using (12), i.e.,

$$C = \frac{\int_{t_1}^{t_2} i_C(t) dt}{v_{dc}(t_2) - v_{dc}(t_1)}. \quad (24)$$

Using the same capacitor current reconstruction method, [49] estimates the capacitor impedance at 2nd harmonic frequency of a PV inverter as $Z_2 = V_{dc,2}/I_{C,2}$, where $V_{dc,2}$ and $I_{C,2}$ represent the RMS values at 2nd harmonic frequency.

In [50], a condition monitoring scheme is proposed for a PV H5 inverter, as shown in Fig. 20(c), the capacitance is calculated during the zero state, i.e., the power switch S_5 is turned OFF, as shown in Fig. 20(d). Using (10), C is calculated as $C = (i_{pv,1} \times \Delta t) / (v_{dc,2} - v_{dc,1})$.

2) External Signal Injection based Methods (1D, 1H)

In [51], a current injection scheme is proposed for a grid-connected PV inverter, as shown in Fig. 7(e). Here, the condition monitoring of capacitors is taken during the night. At night, there is no voltage on the PV panel/string. Here, a current at h th harmonic frequency is injected into the grid, which causes $(h-1)$ th and $(h+1)$ th voltage and current ripples to appear on the dc-link capacitors. Using (9), R_{ESR} and C can be estimated using the voltage and current ripples at $(h-1)$ th or $(h+1)$ th based on the LMS algorithm. Utilizing the same monitoring scheme, [52] further proposes a health estimation method for individual capacitors in a capacitor bank.

In [53], a short-circuit test scheme is introduced to a dc/ac converter to estimate R_{ESR} of capacitors, as shown in Fig. 21. Before the short-test, the converter operates in a normal state.

TABLE VI SUMMARY OF CM SCHEMES FOR CAPACITORS IN ASD SYSTEMS

Method	Working principle	Experimental error	Advantages	Limitations
Capacitor current directly measurement (1B, 1F)	[25]: A current sensor is used to sample capacitor current. Then use the Goertzel algorithm to extract low-frequency (300 Hz) and switching-frequency (2.5 kHz) ripples.	R_{ESR} : <3% C : <1%	Real-online estimation.	Additional current sensors and filter circuits, complex algorithms.
	[26]: A current sensor is used to sample capacitor current. Then use fast Fourier transform (FFT) algorithm is used to analyze mid-frequency (15 kHz) ripples.	R_{ESR} : <3.86%		
System operation model (1C, 1G)	[27], [28]: Utilizing the operation mode of converters to indirectly acquire capacitor current ripple and sampled voltage ripple to estimate C .	C : <5.2% [27]	Real-online estimation, no additional hardware circuit and current sensors.	Small-amplitude ripple measurement, estimated i_C .
Signal injection (1D, 1H)	[29]–[31]: The power switches are controlled to realize the charge and discharge (through the motor windings) of capacitors, then sample the constructed waveforms to estimate parameters.	R_{ESR} : <2% [31] C : <5% [31]	No additional hardware circuits and current sensors.	Quasi-online estimation, motor is stopped, additional control of switches, small-amplitude ripple measurement.
	[32]–[36]: Low-frequency ac current or voltage are injected to the front-end ac/dc converter [32]–[35] or rear-end dc/ac converter [36], then use the recursive least squares (RLS) algorithm or support vector regression (SVR) to analyze the corresponding voltage ripple to estimate parameters.	R_{ESR} : <3.2% [33] C : <0.4% [34]	No additional hardware circuits and current sensors.	Quasi-online estimation, external signal injection, operation in no load condition [32]–[35] or regenerative mode [36].
Power losses (1I)	[37], [38]: R_{ESR} is calculated using average power losses of capacitors. Analog circuits [37] and an MCU [38] are used to calculate the power losses.	R_{ESR} : <1.8% [38]	Real-online estimation, no need for specific band-pass filter.	Additional capacitor current sensor [37], [38], extra power loss calculation circuit [38].
Discharging profile (2A)	[39]: Control capacitors discharge through a variable electric network (VEN), then estimate R_{ESR} and C using the discharging profile.	R_{ESR} : <1.3% C : <0.047%	High estimation accuracy.	Quasi-online estimation, additional VEN on dc link, which introduces reliability risks, during shutdown process, need control of switches.
	[40]–[42]: Control capacitors discharge through the motor windings [40],[41] and electric network [42] in the converter, then estimate C using the discharging profile.	C : <2.1% [41]	No additional hardware circuits and current sensors.	Quasi-online estimation, motor is stopped, need control of switches [40], [41], electric vehicles application [40], railway trains application [42].
Data training (3A)	[43]–[46]: Using the artificial neural network (ANN) network to train data such as input voltage/current, output input voltage/current, and dc-link voltage to obtain C .	C : <2% [46]	Real-online estimation, no additional hardware circuit and current sensors.	Need a large amount of training data and complexly algorithms.
	[47]: Using adaptive neuro-fuzzy inference system (ANIS) algorithm to train voltage data to obtain the capacitor health state.	N/A		

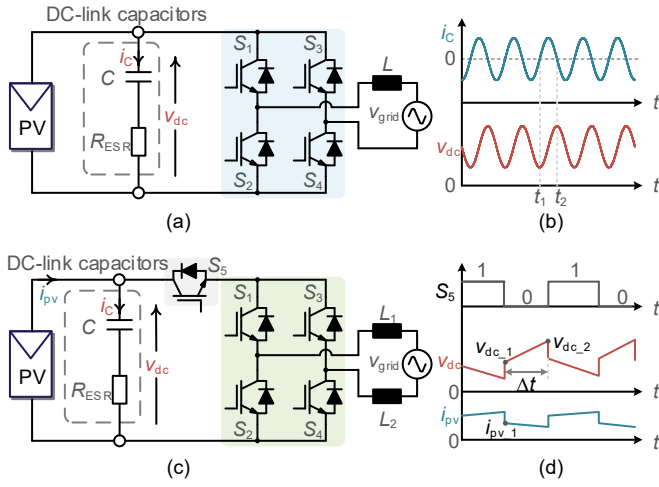


Fig. 20. Single-phase grid-connected PV H4 inverter [48] and H5 inverter [50]. (a) Structure of H4 inverter, here, L_{ESL} is ignored. (b) Average capacitor current and voltage waveforms. (c) Structure of H5 inverter. (d) Typical waveform of PV voltage and PV current in active and zero state.

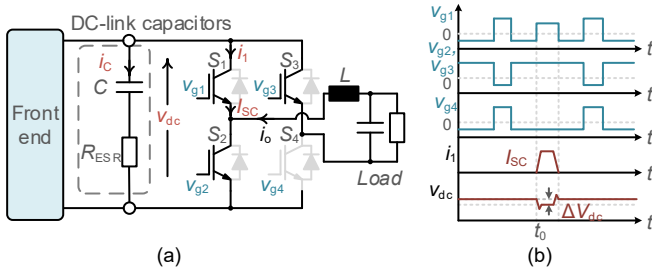


Fig. 21. Short-circuit current perturbation for capacitor monitoring in a single-phase inverter [53], here, L_{ESL} is ignored. (a) Equivalent circuit of a single-phase inverter during short-circuit test. (b) Short-circuit test waveforms.

Here, S_2, S_3 are ON and S_1, S_4 are OFF. At t_0 , S_1 turns on, a very short time short-circuit test occurs, which causes a capacitor voltage step ΔV_{dc} . According to (11), R_{ESR} is calculated as $R_{ESR} = \Delta V_{dc} / I_{sc}$, where I_{sc} is the short circuit current.

3) Power Losses based Method (1J)

Based on the idea of power losses (i.e., method 1J), [54], [55] proposed a power extraction efficiency (PEE) method to monitor the health state of capacitors. The PEE is defined as $PEE = P_{av} / P_{max}$, where P_{av} and P_{max} represent the average PV power and maximum PV power. By sampling the PV voltage and current, the PEE is calculated to estimate the health state of capacitors.

4) Discussions of CM Schemes for Capacitors in PV Inverter

Table VII summarizes the CM schemes for capacitors in PV inverters, the remarks are given as follows.

- The CM schemes for capacitors in PV inverters are all based on Principle I.
- The signal injection scheme in [51] (based on 1D, 1H) is a quasi-online scheme, which has a relatively high estimation accuracy. However, the CM is implemented during the night and an additional power diode is required. Another injection scheme in [53] is a real-online scheme, which has high applicability. However, the estimation accuracy of R_{ESR} is relatively low, and high-frequency sampling of short-circuit current is required.

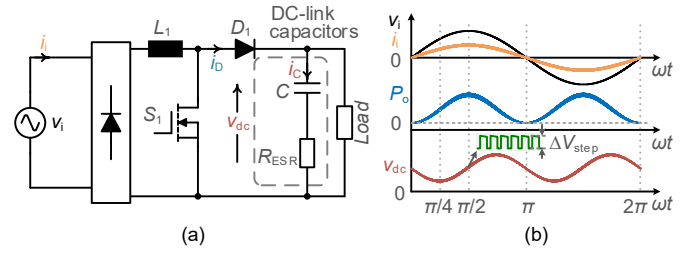


Fig. 22. Topology structure and key waveforms of boost PFC converters, here, L_{ESL} is ignored [60]. (a) Topology structure. (b) Key waveforms.

- The power losses schemes in [54], [55] (based on 1J) and capacitor current estimation scheme in [49] (based on 1C, 1G) can real-online monitoring the health status of capacitors without additional hardware circuits and current sensors. However, specially defined failure criteria are required.
- The capacitor current estimation scheme in [49], [50] (based on 1C, 1G) are real-online schemes without additional hardware circuits and current sensors. However, [50] is only suitable for PV H5 inverter, which has a low applicability.

In summary, from the perspective of estimation accuracy and hardware cost, the scheme in [48] is recommended for condition monitoring of capacitors in PV inverters.

B. CM for Capacitors in PFC converter

Power factor correction (PFC) converters are widely used in ac/dc conversion to improve power factor (PF) and reduce total harmonic correction (THD). The condition monitoring schemes in [56]–[61] are designed for PFC converters, which are derived based on Principle I.

1) Capacitor Current Sensor based Methods (1B, 1F)

Taking a boost PFC converter as an example, Fig. 22(a) shows its topology structure and key waveforms. In [56], C and R_{ESR} of capacitors are estimated using equations (10) and (11). Here, Prony's algorithm is used to process the sampled voltage and current data. Similar, discrete Fourier transform (DFT) is used in [57]. Moreover, according to (11), [58] calculates R_{ESR} using $R_{ESR} = V_{dc,RMS} / I_{C,RMS}$, where $V_{dc,RMS}$, $I_{C,RMS}$ are the Root-Mean-Square (RMS) values of ΔV_{CAP} and Δi_C .

2) Circuit Operation model based Methods (1C, 1G)

Referring to Fig. 22(a), the capacitor current can be approximately calculated as $i_C = i_D - I_D \approx i_L \times PWM - \text{avg}(i_L \times PWM)$, where I_D is the average diode current. Based on this, [59] used Kalman filter algorithm and (10), (11) to estimate C and R_{ESR} . Referring to Fig. 22(b), at $\pi/2$ in a half-line cycle, the peak value of the capacitor current is maximum, which causes the peak value of the voltage ripple to be maximum. According to (11), the ripple voltage step value ΔV_{step} is determined by R_{ESR} when the switch S_3 turns OFF. Therefore, [60] estimated R_{ESR} using $R_{ESR} \approx \Delta V_{step} / \Delta i_{L,max}$, where $\Delta i_{L,max}$ is the maximum value of inductor current ripple. Here, wavelet transform (WT) algorithms are used to calculate R_{ESR} .

TABLE VII SUMMARY OF CM SCHEMES FOR CAPACITORS IN PV GRID-CONNECTED INVERTERS AND PFC CONVERTERS

Topology	Method	Working principle	Experimental error	Advantages	Limitations
PV inverter	System operation model (1C, 1G)	[48]: Using estimated i_C and capacitor voltage to calculate C . The capacitor voltage is sampled in particular instants ($i_C=0$).	$C: <2.56\%$	Real-online estimation, no additional hardware circuits and current sensors.	Estimated i_C .
		[49]: Using the second harmonic voltage and current to calculate capacitor impedance.	$Z: <17.2\%$		Estimated i_C , low estimation accuracy, no specific values of R_{ESR} and C , specially defined failure criterion.
		[50]: Sampling capacitor voltage and PV current to calculate C when H5 inverter is worked in zero states, here, the capacitor is disconnected with the inverter.	N/A		Small-amplitude ripple, only suitable for H5 inverter.
	Signal injection (1D, 1H)	[51]: A low-frequency current harmonic is injected into the grid, which causes corresponding-frequency voltage ripple on capacitors. Using the least mean square (LMS) algorithm to analyze the ripple to estimate capacitor parameters.	$R_{ESR}: <3.65\%$ $C: <1.88\%$	No additional sensors.	Quasi-online estimation, no input source (at night), additional diode, external signal injection.
		[53]: Using the voltage step caused by a short-circuit test to estimate R_{ESR} .	$R_{ESR}: <6\%$	Real-online estimation, no additional hardware circuits and current sensors, high applicability.	Causing switches in short-circuiting status, high-frequency sampling during the short test.
Power losses (1J)	[54],[55]: Sampling PV voltage and current to calculate power extraction efficiency (PEE) to assess the health state of capacitors.	N/A	Real-online estimation, no additional hardware circuits and current sensors.	No specific values of R_{ESR} and C , specially defined failure criterion.	
PFC converter	Capacitor current directly measurement (1B, 1F)	[56],[57]: Using a current sensor to sample capacitor current. The use Prony's algorithm [56], discrete Fourier transform (DFT) algorithm [57] to analyze voltage and current ripples at low frequency and mid frequency.	$R_{ESR}: <6.01\%$ [56] $C: <2.51\%$ [56]	Real-online estimation.	Additional hardware circuits and sensors, high-frequency sampling.
		[58]: Using a current sensor to sample capacitor current. Then use the root mean square (RMS) values of capacitor voltage and current to calculate R_{ESR} .	$R_{ESR}: <5.5\%$		
	System operation model (1C, 1G)	[59]: Reconstruction of the capacitor current using diode current, then estimate capacitor parameters using Kalman filter.	$R_{ESR}: <5\%$ $C: <10\%$	Real-online estimation, no additional capacitor current sensor.	Low estimation accuracy, high-frequency sampling ($f_{sw}/f_{sw}=16$).
		[60]: Using the ripple voltage step value at switch turn-off moment to estimate R_{ESR} . Wavelet transform (WT) algorithm is used to calculate the parameter.	$R_{ESR}: <9.5\%$		Low estimation accuracy, additional hardware circuits, high-frequency sampling ($f_{sw}/f_{sw}\approx 53$).
		[61]: Sampling of two values of the capacitor voltage in particular instants within a line cycle.	$R_{ESR}: <3.7\%$ $C: <1.9\%$		Additional hardware circuit.

The scheme in [60] analyzes the steady-state waveforms on the switching-frequency scale. Considering the line-frequency scale of a boost PFC, [61] uses the capacitor voltage at 0 and $\pi/4$ instants to estimate capacitor parameters. According to the input and output power balance, R_{ESR} and C are calculated as (25), where V_{dc} is the average capacitor voltage.

$$\begin{cases} R_{ESR} = -V_{dc} \times \Delta v_{dc}(0) / P_o \\ C = \frac{-P_o}{2\omega V_{dc} \Delta v_{dc}(\pi/4)} \end{cases} \quad (25)$$

3) Discussions of CM Schemes for Capacitors in PFC Converters

Table VII also summarizes the CM schemes for capacitors in PFC converters, the remarks are given as follows.

- The schemes are all real-online schemes, which are based on Principle I.
- The capacitor current directly measurement schemes in [56]–[58] (based on 1B, 1F) and capacitor current estimation schemes in [60], [61] (based on 1C, 1G) required additional current sensors or hardware circuits to obtain capacitor current. Moreover, the schemes in [56]–[58], [60] require high-frequency sampling to achieve ripple signals.
- The capacitor current estimation schemes in [59] does not

require additional current sensors, however, the estimation accuracy is relatively low.

VII. CM FOR CAPACITORS IN DC/DC CONVERTERS

Different from the ac/dc converters or dc/ac inverters, dc/dc converters have a relatively high switching frequency, which are widely used in low-power applications. In [62]–[101], a lot of condition monitoring schemes are proposed to assess the health status of capacitors in dc/dc converters.

A. Implementation of CM Schemes based on Principle I

1) Capacitor Voltage based Methods (1A, 1E)

Fig. 23(a) shows the main circuit and key waveforms of a buck converter. It illustrates that the output voltage waveform v_{dc} is similar to the capacitor current waveform i_C , which demonstrates that voltage ripple v_{dc} is proportional to R_{ESR} in (15). Based on this, [62] presents an analog circuit to extract the peak-to-peak value of voltage ripple, so as to predict the failure of capacitors in buck converters. In [63], a similar scheme is applied for a boost converter, as shown in Fig. 23(b).

2) Capacitor Current Sensor based Methods (1B, 1F)

In [64]–[69], the schemes based 1B and 1F are proposed to monitoring capacitors in forward converters [64],[65], flyback converters [66], buck converters [67] and PV boost converters [68],[69]. Here, C and R_{ESR} are calculated using equations (10) and (11), the implementation is shown in Fig. 7(a).

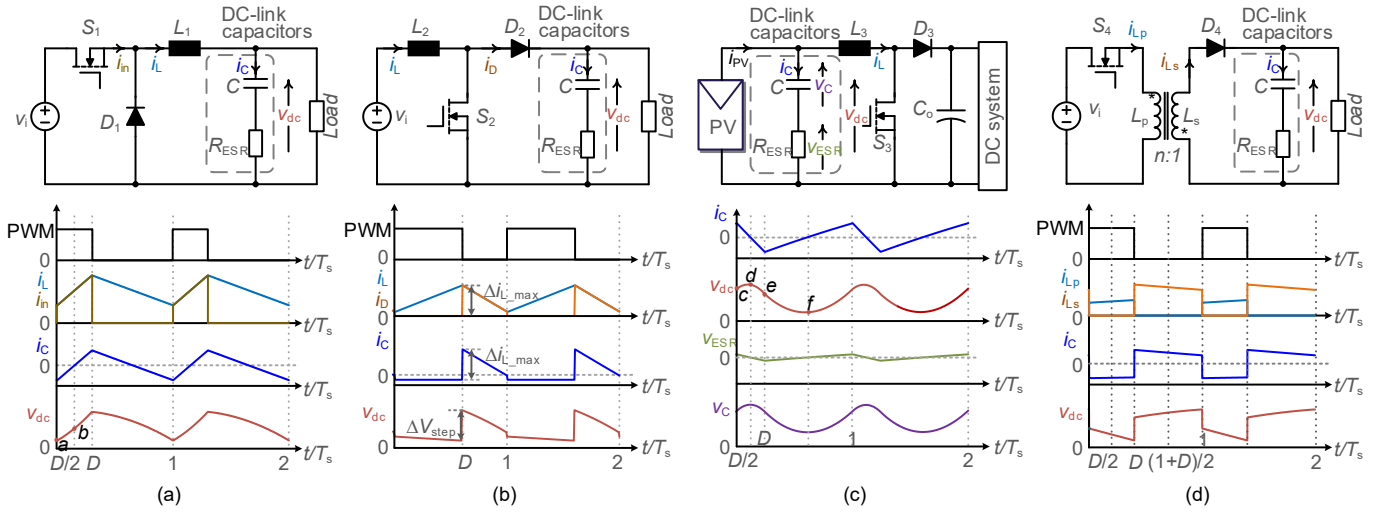


Fig. 23. Topology structure and steady-state waveforms of dc/dc converters, here, L_{ESL} is ignored. (a) Buck converter. (b) Boost converter. (c) PV boost converter. (d) Flyback converter.

There are three types of current sensor are used to obtain capacitor current, i.e., the classical current sensor including shunt resistor and Hall sensor [64]–[66], printed circuit board Rogowski coil (PCBRC) sensor [67], tunnel magnetoresistive (TMR) sensor [68], [69], where the classical current sensor is invasive type, the PCBRC sensor and TMR sensor are non-invasive type.

3) Circuit Operation Model based Methods (IC, IG)

In [70]–[94], circuit operation model based schemes are proposed for dc/dc converters. Generally, they can be divided into two categories. One is based on the converter operation model, here, the capacitor current is derived from inductor current, output current, and output voltage, etc. These signals are directly measured by sensors. Another is based on converter parameters model, here, the signals are estimated from converter parameters by using circuit model.

a) *Based on the operation model of converters:* Referring to the waveforms of buck converters in Fig. 23(a), it is easily found that the inductor current ripple Δi_L equals to the capacitor current ripple Δi_C . Based on this, [70]–[73] estimate R_{ESR} using (13), i.e.,

$$R_{ESR} \approx \frac{\Delta v_{dc}}{\Delta i_C} = \frac{\Delta v_{dc}}{\Delta i_L}. \quad (26)$$

From Fig. 23(a), it is also found that the inductor current is related to the input current i_{in} . Therefore, [74], [75] use i_{in} to estimate R_{ESR} . To avoid using current sensors, [76], [77] sample the capacitor voltage at two particular instants (points *a* and *b*) of one switching cycle to estimate R_{ESR} and C . As shown in Fig. 23(a), the difference between the capacitor voltages sampled at points *a* and *b* is due to R_{ESR} and C . Using (9), the estimation model is calculated as (27), where T_s and D represent the switching cycle and duty cycle respectively. Here, to sample the voltage at points *a* and *b*, pulse width modulation signal is needed.

$$\begin{cases} R_{ESR} = \frac{2L_1 f_s \left[\Delta v_{dc}(0) + 2 \frac{2(D-1)}{(2-D)} \times \Delta v_{dc} \left(\frac{DT_s}{2} \right) \right]}{V_{dc}(D-1)} \\ C = \frac{V_o(2-D)(D-1)}{24L_1 f_s^2 \Delta v_{dc} \left(\frac{DT_s}{2} \right)} \end{cases}. \quad (27)$$

Referring to the waveforms of boost converters in Fig. 23(b), the inductor current i_L is proportional to the capacitor current i_C . Therefore, [78]–[80] use inductor current to estimate capacitor parameters. In [79], [80], the least mean squares (LMS) and the wavelet transform denoising (WTD) algorithms are employed respectively.

According to the steady-state waveforms of a continuous conduction mode (CCM) PV boost converter in Fig. 23(c), the difference between the capacitor voltages sampled at points *c* and *e* are due to R_{ESR} . And, the voltage difference at points *d* and *f* is only due to C . Using (9), R_{ESR} and C are calculated as (28), where V_{dc} is the average capacitor voltage [81].

$$\begin{cases} R_{ESR} = \left[v_{dc}(0) - v_{dc}(DT_s) \right] L_2 / (V_{dc} DT_s) \\ C = \frac{V_{dc} DT_s^2}{8L_2 \{ v_{dc}(DT_s/2) - v_{dc}[(1+D)T_s/2] \}} \end{cases}. \quad (28)$$

Based on this, [82] further proposed an improved estimation scheme to monitor the capacitors for a converter operated in discontinuous conduction mode (DCM). In [83], a similar scheme is proposed for a CCM flyback converter, as shown in Fig. 23(d). Based on the derivation of (9), the capacitor parameters are calculated using the output voltage at 0, $DT_s/2$ and $(1+D)T_s/2$. In [84], an improved multiple-spot sampling method is proposed for a discontinuous conduction mode (DCM) flyback converter.

b) *Based on the circuit parameters model of converters:* Since a power electronic circuit is a hybrid dynamic system, its operation can be described by a state-space model. In [85], [86] a circuit model based method is proposed to estimate the

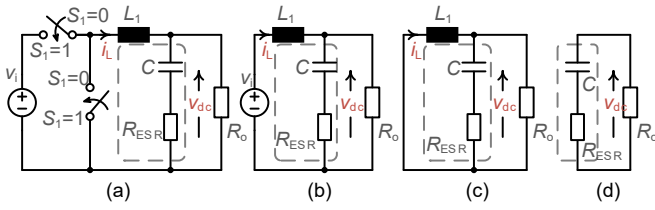


Fig. 24. Equivalent circuits of buck converter [85]. (a) Main circuit. (b) State 1. (c) State 2. (d) State 3.

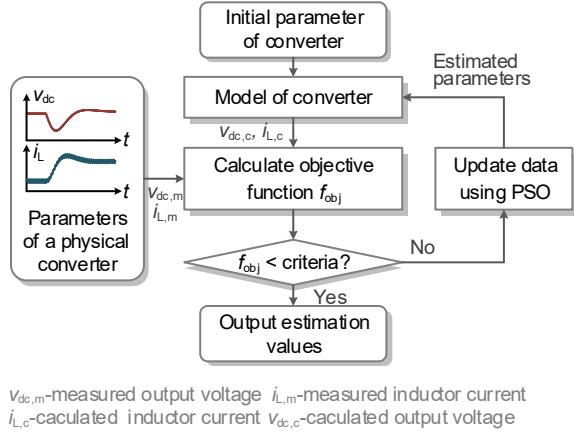


Fig. 25. Flow chart of circuit model based PSO algorithm [93].

capacitor parameters of a buck converter. Ignoring the ESL, Fig. 24(a) shows the equivalent circuit of the converter. The buck converter has two discrete states in CCM with (S_1, S_2) in the set $\{(1,0), (0,1)\}$, and three states in DCM with (S_1, S_2) in the set $\{(1,0), (0,1), (0,0)\}$ as shown in Fig. 24(b), (c) and (d). Synthesizing these states with different values of switches, we have

$$\begin{bmatrix} i_L(t) \\ v_{dc}(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 - \frac{T}{(R_{ESR} + R_o)C} \end{bmatrix} \begin{bmatrix} i_L(t-1) \\ v_{dc}(t-1) \end{bmatrix} + S_1(t-1) \begin{bmatrix} v_i/L \\ \frac{R_{ESR} R_o v_i T}{(R_{ESR} + R_o)L} \end{bmatrix} + [S_1(t-1) + S_2(t-1)] \begin{bmatrix} 0 & -T/L \\ \frac{R_o T}{(R_{ESR} + R_o)C} & -\frac{R_{ESR} R_o T}{(R_{ESR} + R_o)L} \end{bmatrix} \begin{bmatrix} i_L(t-1) \\ v_{dc}(t-1) \end{bmatrix} \quad (29)$$

where T is the sampling period. Using variables to represent the elements in the parameter matrixes in (29), it can be rewritten as

$$\begin{bmatrix} i_L(t) \\ v_{dc}(t) \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} i_L(t-1) \\ v_{dc}(t-1) \end{bmatrix} + S_1(t-1) \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} + [S_1(t-1) + S_2(t-1)] \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_L(t-1) \\ v_{dc}(t-1) \end{bmatrix} \quad (30)$$

According to equations (29), (30), the capacitor parameters can be calculated as

$$\begin{cases} \hat{C} = (T \times \hat{R}_o - \hat{b}_2 \times \hat{L}_1 / v_i) / [(\hat{a}_{21} + \hat{h}_{21}) \times \hat{R}_o] \\ \hat{R}_{ESR} = \hat{b}_2 \times \hat{L}_1 / [v_i \times \hat{C} \times (\hat{a}_{21} + \hat{h}_{21})] \end{cases} \quad (31)$$

Using LMS algorithm, the coefficients a_{11} – a_{22} , h_{11} – h_{22} , b_1 , b_2 and capacitor parameters can be calculated.

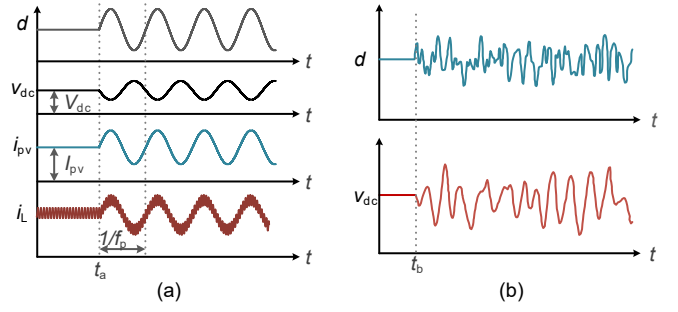


Fig. 26. Representative waveforms of duty cycle perturbation based schemes. (a) Waveforms of a PV boost converter [95]. (b) Waveforms of a buck converter [97].

The similar methods are proposed for buck converters [87]–[90], and boost converters [91], [92].

Based on the circuit model, a particle swarm optimization (PSO) algorithm is used to estimate the circuit parameters include L , C , R_{ESR} , etc., as shown in Fig. 25 [93], [94]. Here, the output voltage $v_{dc,m}$ and inductor $i_{L,m}$ during load transient are target values of the PSO algorithm. If the calculated values $v_{dc,c}$ and $i_{L,c}$ are matched with the target values, the estimated converter parameters are consistent with the non-electrical parameters. Based on this, the capacitor parameters can be obtained.

4) External Signal Injection based Methods (1D, 1H)

In [95], a signal injection method is proposed for a PV boost converter [See Fig. 23(c)]. Referring to Fig. 26(a), at t_a , a small perturbation signal of low frequency f_p is added to the original duty cycle d , which causes low-frequency oscillations on the voltage v_{dc} and current i_{pv} , i_L . Using (9), the low-frequency impedance of the capacitor is calculated as

$$Z_C(f_p) = V_{dc,rms}^{f_p} / I_{C,rms}^{f_p} \quad (32)$$

where $V_{dc,rms}^{f_p}$, $I_{C,rms}^{f_p}$ are the RMS values of capacitor voltage and current at f_p . Here, the capacitor current i_C is calculated as $i_C = i_{pv} - i_L$. Similar duty-cycle perturbation methods and Principle IV are utilized for a buck converter [See Fig. 23(a)] in [96]–[98], where the discrete transfer function of the buck converter is given as

$$G_{dv}(z) = \frac{b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad (33)$$

Referring to the duty cycle and output voltage waveforms in Fig. 26(b), before t_b , the converter works in steady state. At t_b , a pseudo-random binary sequence (PRBS) perturbation is injected into the duty cycle, which causes an oscillation on the voltage v_{dc} . Using signal processing algorithms include infinite impulse response (IIR) filter [96], self-tuned Kalman filter [97], and biogeography-based optimization (BBO) [98] to analyze the duty cycle and voltage waveforms during perturbation period, the coefficients a_1 , a_2 , b_1 , b_2 as well as capacitor parameters are identified.

B. Implementation of CM Schemes based on Principle II

During transients, the capacitor will charge or discharge, which forms a charging or discharging profile. In [99], a load transient trajectory analysis based scheme is proposed for

TABLE VIII SUMMARY OF CM SCHEMES FOR CAPACITORS IN DC/DC CONVERTERS

Method	Topology	Working principle	Experimental error	Advantages	Limitations
Capacitor voltage based method (1A,1E)	buck	[62]: Using analog circuits to extract the dc value of ripple voltage, which can represent the change of R_{ESR} .	N/A	Real-online prediction, simple.	Additional ripple processing circuits, no specific values of R_{ESR} and C .
	buck	[63]: Fast Fourier transform (FFT) is used to analyze the estimated voltage ripple. Then, judge the parameter change of capacitors.	N/A		
Capacitor current directly measurement (1B,1F)	forward [64], [65] Flyback [66]	[64]–[66]: Using a current sensor to sample capacitor current, then calculate R_{ESR} based on switching-frequency voltage ripple and current ripple.	$R_{ESR} < 2.77\%$ [66]	Real-online estimation.	Additional capacitor current sensor, high-frequency sampling.
	buck	[67]: PCB Rogowski coil (RC) sensor is designed to capture capacitor current to estimate R_{ESR} .	$R_{ESR} < 5.56\%$	Real-online estimation, switch fault diagnosis.	Specially designed PCBRC sensor, high-frequency sampling.
	PV boost	[68], [69]: Magnetoresistive sensors are used to sample capacitor current to calculate R_{ESR} and C .	$R_{ESR} < 4.9\%$ [68] $C < 5.4\%$ [68]	Real-online monitor of input/output capacitors.	Special current sensor, high-frequency sampling.
Operation model of converters (1C,1G)	buck	[70]: Empirical mode decomposition (EMD) algorithm on capacitor voltage and inductor current.	N/A	Real-online estimation, no capacitor current sensor.	High-frequency sampling, complex algorithm.
	buck	[71]: Wavelet transform denoising (WTD) algorithm on ripple voltage and inductor current.	$R_{ESR} < 3.89\%$	Real-online estimation, consider DCM model, no additional capacitor current sensor.	High-frequency sampling ($f_{sa}/f_{sw}=2247$), complex algorithm.
	buck	[72],[73]: Calculation of R_{ESR} utilizing capacitor voltage and inductor current, where ripple current is extracted using Rogowski Coil (RC) sensor.	$R_{ESR} < 6\%$ [72]	Real-online estimation, switch fault diagnosis, no capacitor current sensor.	Specially designed RC sensor, high-frequency sampling.
	buck	[74],[75]: Utilizing the input current and the output voltage to estimate R_{ESR} , discrete Fourier transform (DFT) and least mean square (LMS) algorithms are used to compute the best values.	$R_{ESR} < 4.9\%$ [74]	Real-online estimation, no capacitor current sensor.	High-frequency sampling ($f_{sa}/f_{sw}=100$).
	buck	[76],[77]: Sampling voltage ripple at two particular instants of one switching cycle, calculation of R_{ESR} and C using pulse width modulation signal and voltage ripple.	$R_{ESR} < 7.6\%$ [76] $C < 6.37\%$ [76]	Real-online estimation, low-frequency sampling, no capacitor current sensor.	Addition hardware circuit.
	boost	[78],[79]: Capacitor current is indirectly obtained based on inductor current. Least mean square (LMS) algorithm is used.	$R_{ESR} < 10.5\%$ [79] $C < 15.8\%$ [79]	Real-online estimation, no capacitor current sensor.	High-frequency sampling ($f_{sa}/f_{sw}=100$ [79]), low estimation accuracy.
	boost	[80]: Capacitor current is indirectly obtained based on inductor current. Wavelet transform denoising (WTD) algorithm is employed.	$R_{ESR} < 3.06\%$	Real-online estimation, no capacitor current sensor.	High-frequency sampling ($f_{sa}/f_{sw}=333$).
	PV boost	[81],[82]: Using capacitor voltages of particular instants to calculate R_{ESR} and C .	$R_{ESR} < 6.2\%$ [82]	Real-online estimation, low-frequency sampling, no capacitor current sensor.	Addition hardware circuit.
	flyback	[83], [84]: Sampling voltage ripple at particular instants of one switching cycle, calculation of R_{ESR} and C using pulse width modulation signal and voltage ripple.	$R_{ESR} < 5.83\%$ [83] $C < 9.5\%$ [83]	Real-online estimation, low-frequency sampling, no capacitor current sensor.	Addition hardware circuit.
Circuit parameters model of converters (1C,1G)	buck	[85]–[88]: Using hybrid model as well as recursive least squares (RLS) algorithm and least mean square (LMS) algorithm to estimate capacitor parameters.	$R_{ESR} < 6.5\%$ [88] $C < 5.5\%$ [88]	Real-online estimation, no capacitor current sensor, full parameters monitoring.	High-frequency sampling ($f_{sa}/f_{sw}=25$), complex calculation model.
	PV buck	[89]: Using an adaptive model observe method to estimate C .	$C < 5\%$	Real-online estimation, no capacitor current sensor, full parameters monitoring.	High-frequency sampling ($f_{sa}/f_{sw}=666$), complex calculation model.
	boost	[90],[91]: Using hybrid model and least mean square (LMS) algorithm to estimate capacitor parameters.	$R_{ESR} < 13.3\%$ [91] $C < 7.5\%$ [91]	Real-online estimation, no capacitor current sensor, full parameters monitoring.	High-frequency sampling ($f_{sa}/f_{sw}=200$), complex calculation model.
	boost	[92]: Using modified hybrid model and wavelet transform denoising (WTD) algorithm to estimate capacitor parameters.	$R_{ESR} < 11.7\%$ $C < 9.2\%$	Real-online estimation, no capacitor current sensor, full parameters monitoring.	High-frequency sampling, complex calculation model.
	buck	[93],[94]: Taking the transient voltage and current as the target values, using particle swarm optimization (PSO) algorithm and circuit model to estimate the circuit parameters.	$C < 9.2\%$ [94]	Real-online estimation, no capacitor current sensor, full parameters monitoring.	Complex algorithm, estimation during transient.
Signal injection (1D, 1H)	PV boost	[95]: Injecting low-frequency perturbation signal (120 Hz) to duty cycle, then calculate the low-frequency impedance.	$Z < 0.64\%$	Real-online monitor, no capacitor current sensor.	External signal injection, additional circuits, no specific values of R_{ESR} and C .
	buck	[96]–[98]: Pseudo-random binary sequence (PRBS) is injected into the duty cycle, then estimate circuit parameters using infinite impulse response (IIR) filter [96], Kalman filter [97], and biogeography-based optimization (BBO) [98].	$R_{ESR} < 10.9\%$ [98] $C < 18.6\%$ [98]	Real-online estimation, no additional hardware, full parameters monitoring.	Complex algorithm, not suitable for high-frequency converter.
Discharging/charging profiles during transients (2B,2D)	buck	[99]: Using the large-signal load transient trajectory to estimate R_{ESR} and C .	$R_{ESR} < 7.4\%$ $C < 9.6\%$	Real-online estimation, low-frequency sampling.	Estimation during transient, additional hardware circuit.
	full-bridge converter	[100]: Using the maximum voltage deviation during load transient to estimate R_{ESR} .	N/A	Real-online estimation, low-frequency sampling.	Estimation during transient, no specific values of R_{ESR} and C .
	full-bridge converter	[101]: Modifying the reference voltage to introduce a voltage step, then estimate C using the voltage step.	N/A	Real-online estimation.	External signal perturbation, need offline training of data.

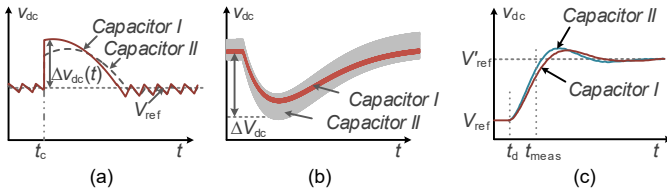


Fig. 27. Capacitor charging/discharging profiles during transients. (a) Transient waveforms of a buck converter [99]. (b) Transient waveforms of a full-bridge converter [100]. (c) Transient waveforms of a phase-shifted ZVS converter [101].

TABLE IX COMPARISON OF CM SCHEMES FOR CAPACITORS IN BUCK CONVERTERS

Method	Additional circuits/sampling devices	f_{sw} (N)	Algorithm (complexity)	Experimental error
Capacitor voltage based method (1A)	Simple hardware circuits	50 kHz (N/A)	N/A	N/A [62]
Capacitor current measurement (1B, 1F)	Current sensor, oscilloscope	100 kHz (N=100)	N/A	R_{ESR} : <5.56% [67]
System operation model (1C, 1G)	Oscilloscope	44.5 kHz (N=2247)	WTD (++)	R_{ESR} : <3.89% [71]
	Oscilloscope	20 kHz (N=100)	LMS (+)	R_{ESR} : <4.9% [74]
	Simple circuits	100 kHz (N=2)	N/A	R_{ESR} : <7.6% [76] C: <6.37% [76]
System circuit model (1C, 1G)	Acquisition card	20 kHz (N=150)	LMS (+)	R_{ESR} : <6.7% [85] C: <6% [85]
	Acquisition card	300 kHz (N=666)	N/A	C: <5% [89]
Signal injection (1D, 1H)	N/A	20 kHz (N=1)	BBO (++++)	R_{ESR} : <10.9% [98] C: <18.6% [98]
Charging profiles (2D)	Simple hardware circuits	200 kHz (N=1)	N/A	R_{ESR} : <7.4% [104] C: <9.6% [104]

monitoring the output capacitor of a buck converter. Taking an unloading transient as an example, Fig. 27(a) shows the transient trajectories of capacitor voltage. Here, two capacitors with different parameters are used. It is found that the output voltage trajectory ΔV_{dc} is changed as the output capacitor parameters change when the load current step ΔI_o is the same. Based on the charging profile, R_{ESR} and C are calculated as

$$\begin{cases} R_{ESR} = \Delta V_{dc}(t_c) / \Delta I_o \\ \Delta V_{dc}(t) = \frac{\Delta I_o}{C} t - \frac{1}{2} \frac{C}{k} t^2 + \Delta I_o \cdot R_{ESR} - R_{ESR} \cdot kt \end{cases} \quad (34)$$

where t_c is the initial instant of load step, k is the inductor current slew rate, and $k \approx V_{ref} / L_1$. In this scheme, an RC differential circuit is used to detect the load transient [125]. In [100], a similar method is proposed for a full-bridge converter. But the accurate mathematical relation between capacitor parameters and transient trajectory is not given, R_{ESR} is estimated as $R_{ESR} \approx \Delta V_{dc} / \Delta I_o$, where ΔV_{dc} is the voltage deviation, as shown in Fig. 27(b).

Besides the load transient, a reference voltage perturbation scheme is proposed for a phase-shifted full-bridge converter in [101]. Referring to Fig. 27(c), at t_d , the reference voltage is modified as V'_{ref} , which causes a voltage step. For different capacitors, the voltage values at t_{meas} are different. By fitting the

measurement data, C is estimated as

$$C = \frac{148.2 - S + 0.1687I_o}{27960} \quad (35)$$

where I_o is the load current, S represents the step slope and it is related to the measurement value at t_{meas} .

C. Discussions of CM Schemes for Capacitors in DC/DC Converters

Table VIII summarizes the CM schemes for capacitors in dc/dc converters. It is found that the derived schemes are all real-online schemes, which are based on Principle I and Principle II. The remarks are given as follows.

1) It is known that dc/dc converters usually work with a relatively high switching frequency, which introduces high-frequency small-amplitude ripples. For the schemes based Principle I, high-frequency and high-precision sampling devices are generally required to obtain steady-state ripples. And powerful data processing tools are needed for filtering and analysis of sampling signals.

a) The derived schemes based on 1A and 1E (i.e., capacitor voltage based schemes) can predict the health status of capacitors without capacitor current sensors [62], [63]. However, there are no specific values of R_{ESR} and C , which is difficult to calculate RUL of capacitors. Moreover, [62] uses analog circuit to judge the parameter change of capacitors, which does not need high-frequency sampling.

b) The derived schemes based on 1B and 1F in [64]–[69] have relatively high estimation accuracy (the estimation error is about 5%), however, capacitor current sensors and high-frequency sampling devices are required.

c) The converters operation model schemes (based on 1C, 1G) estimate R_{ESR} and C using the relationship between voltage ripple and current ripple. In [70]–[75], [80], high-frequency sampling devices are required. The schemes in [76]–[77] and [81]–[84] do not need high-frequency sampling devices, and the calculation model is simple. However, additional hardware circuits are required.

d) The circuit model schemes (based on 1C, 1G) in [85]–[92] also need high-frequency sampling to accurately obtain the circuit parameters model. Besides capacitor parameters, these schemes can estimate other key parameters, such as inductance. However, the calculation algorithm is complex and the estimation accuracy is relatively low. The schemes in [93], [94] avoided high-frequency sampling, however, the estimation algorithm is also complex.

e) The calculation model of the signal injection scheme (based on 1D, 1H) in [95] is simple and the sampling frequency is low. However, a simple ripple extraction circuit is required, and there are no specific values of R_{ESR} and C . The schemes in [96]–[98] can implement full parameters monitoring of converters. But complex algorithms limit their application in high-frequency converters.

2) The discharging/charging profiles schemes (based on 2B, 2D) avoid the high-frequency sampling of ripples. However, there is no data processing algorithms, which causes a relatively low estimation accuracy.

3) Taking a buck converter as an example, Table IX shows the comparison results of these derived schemes, where f_{sw} is the switching frequency and N represents the number of sampling points during one switching cycle. It illustrates that the derived schemes based on capacitor current direct measurement (1B, 1F) and circuit operation model (1C, 1G) generally require high-cost sampling devices, such as data acquisition card, which limits their application in industrial systems. Moreover, complex algorithms of signal injection (1D, 1H) based scheme limit their application for high-frequency dc/dc converters.

In summary, from the perspective of implementation, the charging/discharging profiles based schemes with low sampling frequency and data are recommended for CM of capacitors in dc/dc converters. Simple data processing algorithms can be considered to improve estimation accuracy.

VIII. CONCLUSION

Condition monitoring (CM) of dc-link capacitors has great significance in enhancing the reliability of the power electronics converters with dc link. In this paper, an overview of condition monitoring techniques for dc-link capacitors is presented. 1) The wear-out failure characteristics of capacitors including degradation models and end-of-life criteria are summarized. Based on this, the design procedure of CM for dc-link capacitors is presented. 2) The main estimation principles of capacitor parameters are reviewed. Accordingly, the CM methods for dc-link capacitors are derived in a step by step manner. 3) The existing CM methods for dc-link capacitors are reviewed and discussed according to different types of dc-link applications including ASD systems, PV inverters, PFC converters, and dc/dc converters. Based on this literature review, Table X summarizes the existing CM schemes without additional hardware circuits, sensors, and high-frequency sampling devices. Moreover, the suggested feasible solutions for industrial applications are listed in the following. Future research challenges and research opportunities are summarized from the authors' point of view.

A. Suggested Feasible Solutions

The key goal of employing a CM scheme in industrial applications is to accurately estimate capacitor parameters without additional cost and reliability risk, i.e., without additional hardware circuits and sensors. For the application with charging or discharging paths, such as ASD systems (motor windings as discharging paths). The best solution for CM of capacitors is to construct discharging or charging profile during shutdown or start-up processes (i.e, schemes based on 2A, 2C). Then to analyze the charging/discharging profile to estimate capacitor parameters.

1) For the application without charging or discharging paths, such as PV inverters, and PFC converters, circuit operation model based schemes (i.e., schemes based on

1C, 1G) and signal injection based schemes (i.e., schemes based on 1D, 1H) are recommended.

- 2) For high-frequency dc/dc converters, capacitor charging/discharging profiles during transients (i.e., schemes based on 2B, 2D) are recommended for parameters estimation. Although low-cost signal processing circuits are required, high-precision and high-frequency sampling devices are avoided.
- 3) Data training schemes without additional hardware circuits, sensors and external interference are attractive for all types of dc-link applications.

B. Challenges

For CM schemes based on non-electrical parameters, i.e., industrial instruments measurement based schemes, the main challenge is the lack of uniform end-of-life criteria for capacitors. For CM schemes based on electrical parameter estimation, the challenges are given in the following.

- 1) Lack of accurate measurement or estimation of the internal temperature of capacitors, which is essential for parameter calibration.
- 2) Additional hardware costs, software costs or external interference for condition monitoring.
- 3) Measurement noise of voltage and current in harsh electromagnetic interference (EMI) environment, which introduces inaccurate estimation of R_{ESR} or C .
- 4) A large amount of sampling data or complex processing data are used to improve estimation accuracy.
- 5) Inaccurate estimation of capacitor parameters when systems parameters are varied.
- 6) One condition monitoring scheme is difficult to extend to other types of dc-link applications

C. Opportunities

- 1) Further research in wear-out mechanisms of capacitors to obtain accurate degradation model and end-of-life criteria based on non-electrical parameters.
- 2) Designing of accurate CM schemes for real industrial applications (working in harsh EMI environment) without additional hardware cost and reliability risk. Future studies need to improve estimation accuracy while reducing the complexity of sampling data and algorithms.
- 3) Monitoring of capacitors' status while monitoring other key components in converters, such as semiconductor switches.
- 4) Designing of low-cost and high-accuracy CM schemes that are suitable for all types of dc-link applications.
- 5) Research of CM schemes for other types of power electronic applications such as the sub-module capacitors in modular multilevel converters (MMC).
- 6) Designing of emerging capacitors with built-in monitoring components such as internal thermal sensors and pressure sensors.
- 7) Applying the emerging artificial intelligence (AI) technology to condition monitoring of capacitors.

TABLE X SUMMARY OF THE CM SCHEMES WITHOUT ADDITIONAL CIRCUITS, SENSORS, AND HIGH-FREQUENCY SAMPLING DEVICES

DC-Link application	CM method	Implementation	Experimental error	Ref.
AC/DC/AC or DC/DC ASD system	System operation model (1C, 1G)	Real online	$C < 5.2\%$	[27]
	Signal injection (1D, 1H)	Quasi online	$R_{ESR}: < 2\%$ [31] $C: < 0.4\%$ [34]	[29]–[36]
	Discharging profile (2A)	Quasi online	$C: < 2.1\%$ [41]	[40]–[42]
	Data training (3A)	Real online	$C: < 2\%$ [46]	[43]–[47]
PV inverter	System operation model (1C, 1G)	Real online	$C: < 2.56\%$	[48]
PFC converter	System operation model (1C, 1G)	Real online	$R_{ESR}: < 5\%$ $C: < 10\%$	[59]
DC/DC converter	Circuit parameters model of converters (1C, 1G)	Real online	$C: < 9.2\%$ [94]	[93], [94]
	Signal injection (1D, 1H)	Real online	$R_{ESR}: < 10.9\%$ [98] $C: < 18.6\%$ [98]	[96]–[98]

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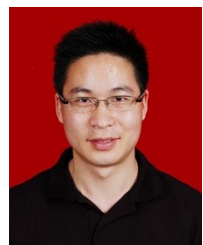
Zhaoyang Zhao (S’20) received the B.S. and M.S. degrees in electrical engineering from Northeast Agricultural University, Harbin, China, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree in electrical engineering in the School of Electrical Engineering, Chongqing University, Chongqing, China. From 2019 to 2020, he was a Visiting Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark.

His research interests include condition monitoring, reliability assessment, and control of power electronic converters.



Pooya Davari (S’11–M’13–SM’19) received the B.Sc. and M.Sc. degrees in electronic engineering in 2004 and 2008, respectively, and the Ph.D. degree in power electronics from QUT, Australia, in 2013. From 2005 to 2010, he was involved in several electronics and power electronics projects as a Development Engineer. From 2013 to 2014, he was with QUT, as a Lecturer. He joined Aalborg University, in 2014, as a Postdoc, where he is currently an Associate Professor. He has been focusing on EMI, power quality and harmonic mitigation analysis and control in power electronic systems. He has published more than 100 technical papers. He is the recipient of a research grant from the Danish Council of Independent Research (DFF-FTP) in 2016.

Dr. Davari served as a Guest Associate Editor of IET journal of Power Electronics, IEEE Access Journal, Journal of Electronics and Journal of Applied Sciences. He is an Associate Editor of Journal of Power Electronics, Associate Editor of IET Electronics, Editorial board member of EPE journal and Journal of Applied Sciences. He is member of the International Scientific Committee (ISC) of EPE (ECCE Europe). Currently, he is a member of Joint Working Group six and Working Group eight at the IEC standardization TC77A.



Weiguo Lu (M’14) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Chongqing University, Chongqing, China, in 2000, 2003, and 2008, respectively.

He is currently a Professor in the School of Electrical Engineering, Chongqing University, Chongqing. He is the author or coauthor of more than 20 papers in journal or conference proceedings. His current research interests include the stability analysis and control strategies of switching power converters, and magnetic-resonance wireless power

transfer.



Huai Wang (M’12–SM’17) received the B.E. degree in electrical engineering, from Huazhong University of Science and Technology, Wuhan, China, in 2007 and the Ph.D. degree in power electronics, from the City University of Hong Kong, Hong Kong, in 2012. He is currently Professor with the Center of Reliable Power Electronics (CORPE), Department of Energy Technology at Aalborg University, Denmark. He was a Visiting Scientist with the ETH Zurich, Switzerland, from Aug. to Sep. 2014, and with the Massachusetts Institute of Technology (MIT), USA, from Sep. to

Nov. 2013. He was with the ABB Corporate Research Center, Switzerland, in 2009. His research addresses the fundamental challenges in modelling and validation of power electronic component failure mechanisms, and application

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issues in system-level predictability, condition monitoring, circuit architecture, and robustness design.

Dr. Wang received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016, and the Green Talents Award from the German Federal Ministry of Education and Research in 2014. He is currently the Chair of IEEE PELS/IAS/IES Chapter in Denmark. He serves as an Associate Editor of IET Electronics Letters, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and IEEE TRANSACTIONS ON POWER ELECTRONICS.



Frede Blaabjerg (S’86–M’88–SM’97–F’03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications. He has received 30 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves as President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too. He is nominated in 2014-2018 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.