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Keywords

<<DC power supply>>, << Pulse width modulation (PWM)>>,<< Frequency-Domain Analysis >>, <<Reliability>>,<< Voltage Source Inverters (VSI)>>

Abstract

This paper explores the impact of different modulation techniques on the lifetime of DC-link capacitors for different modulation indices and varying operating power of voltage source inverter system. The conducted analysis show that the capacitor lifetime improves when using unipolar Sinusoidal pulse-width modulation (SPWM), which introduces the highest lifetime for DC-link capacitors when a single unit voltage source inverter is used. Likewise, for two paralleled voltage source inverter unit' topology, both units using unipolar SPWM, having the same switching frequency produces the least thermal stress on the capacitor and consequently giving the highest lifetime.

Introduction

DC-link capacitor, also known as an intermediate circuit capacitor is one of the most crucial power conversion stages for several industrial applications such as adjustable speed motor drives, wind power systems, photovoltaic systems, and electric vehicles [1], [2]. The main functions of DC-link capacitors are to compensate the instantaneous power difference between the source (usually a rectifier bridge) and output load (usually an inverter whose mean value is constant in steady-state operation), absorb the high-frequency currents generated by inverter modulation technique, thereby preventing the flow of switching frequency current harmonics into the source and to smoothen voltage ripple superimposed on the DC-link voltage [3], [4]. Aluminum electrolytic capacitors (El-caps) are one of the most commonly used DC-link capacitors, due to their advantage of providing a high capacitance per unit volume at low costs compared to other types of capacitors. However, recent studies show that capacitors, in general, contribute to 30% of the total failure root causes in the power electronic systems [5] and they are considered as the most fragile components in a power electronic system [3]–[6].

Many studies [3], [7] have shown that for different pulse width modulation (PWM) techniques, the root means square (RMS) value of DC-link capacitor current only depends on the fundamental output current, modulation amplitude index and load power factor. This might be true from the analytical point of view. However, different modulation techniques affect the switching characteristics of semiconductor devices, resulting in a change of the harmonic spectrum of the DC-link capacitor [8]. Similarly, connecting multiple converters onto one common DC-bus affects the DC-link capacitor's harmonic spectrum. These research gaps are not well discussed in the existing literature. The capacitor's full current spectrum, which affects its lifetime is of paramount importance. Firstly, it affects the hotspot temperature (core temperature increases with increase in capacitor current) of the capacitor, which contributes to self-heating and thereby, decreasing the lifetime of capacitors [9]. Secondly, the power loss of the capacitor, which is a function of the current harmonic spectrum and its Equivalent Series Resistance (ESR) increases as the capacitor current increases. To have a more accurate representation

of the actual current flowing through the capacitor, the harmonic spectrum of capacitor, which includes the DC component, carrier frequency, and all other harmonic currents are used in this paper to accurately size the DC-link capacitors of a power converter operating with a specific modulation method. Furthermore, the lifetime of DC-link capacitors is also evaluated using the capacitor current value calculated based on the entire capacitor current harmonic spectrum.

In this paper, the lifetime of DC-link capacitors is analysed with different modulation schemes such as unipolar and bipolar SPWM for a single inverter and then for two inverter systems sharing a common DC-bus, in order to find which of the modulation techniques produce the least capacitor ripple current at different output power levels and different values of the modulation amplitude index. The key feature of this paper is the lifetime estimation of the DC-link capacitor considering the DC-link capacitor ripple term, which includes the entire range of harmonic ripple currents. Based on the findings, this paper proposes modulation schemes that can improve the lifetime of the DC-link capacitor in multi converter systems.

System Description

To analyse the effect of using unipolar and bipolar SPWM technique on the lifetime of DC-link capacitor, a single-phase full-bridge, commonly known as H-bridge voltage source inverter (VSI) shown in Fig.1 is considered in this paper. The four switches *Q1, Q2, Q3, Q4* of the VSI are controlled using the SPWM technique (explained in detail in [10]).

The specifications of the VSI are listed in Table I and output filter information is provided in Table II and the DC-link capacitor used in this study is obtained from the capacitor datasheet [11]. Fig. 1(a) shows the first topology, where a single VSI is connected to a DC-bus and Fig. 1(b) presents the second topology containing two VSI units connected to a common DC-bus. Both the topologies have a large DC-link bank ($C_{dc\ bank}$) with El-caps to limit the DC-link voltage fluctuation. In Fig 1(a), two parallel electrolytic capacitors are implemented in the $C_{dc\ bank,}$ and in Fig 1(b), it contains four parallel capacitors. In this way, the RMS value of the high-frequency ripple current (I_{cap}) flowing through the DC-link bank is distributed within the capacitors, which reduces the ripple current stress on the individual DC-link capacitor. Hence, the heating and power losses within the DC-link capacitor reduces, which improve the lifetime of C_{dc} (single DC-link capacitor). In this power converter topology, a Proportional – Integral (PI) controller is employed to regulate the DC-link voltage (V_{dc}) at a rated value of 400V as shown in Fig. 1(c). A Proportional-Resonant (PR) controller in Fig. 1(d) is used to ensure that the output voltage is the rated 400V_o. The specifications of PI and PR controller are given in Table III and Table IV.

Table I: Specifications of the output load

Parameter	Symbol	Value
Rated Power (kW)	P_o	2.5
Load (Ω)	R_L	20
Rated RMS Load Voltage (V)	$V_{o\text{-}rated}$	230
Load Frequency (Hz)	f_o	50
Rated DC-link Volatge (V)	$V_{dc\text{-}rated}$	400

Table II: Specifications of the output filter

Parameter	Symbol	Value
Inductor (H)	L_f	$1*10^{-3}$
Capacitor (F)	C_f	$1*10^{-6}$
Resistor (Ω)	R_f	0.1

Table III: Specifications of the PI-controller in Fig. 1c

Parameter	Symbol	Value
Propotional Parameter	K_P	2
Integrator Parameter	K_I	100

Table IV: Specifications of the PR- controller in Fig. 1d.

Parameter	Symbol	Value
Propotional Parameter	K_P	1
Resonant frequency	ω	$2\pi(50)$
Resonant Coefficient	K_R	50

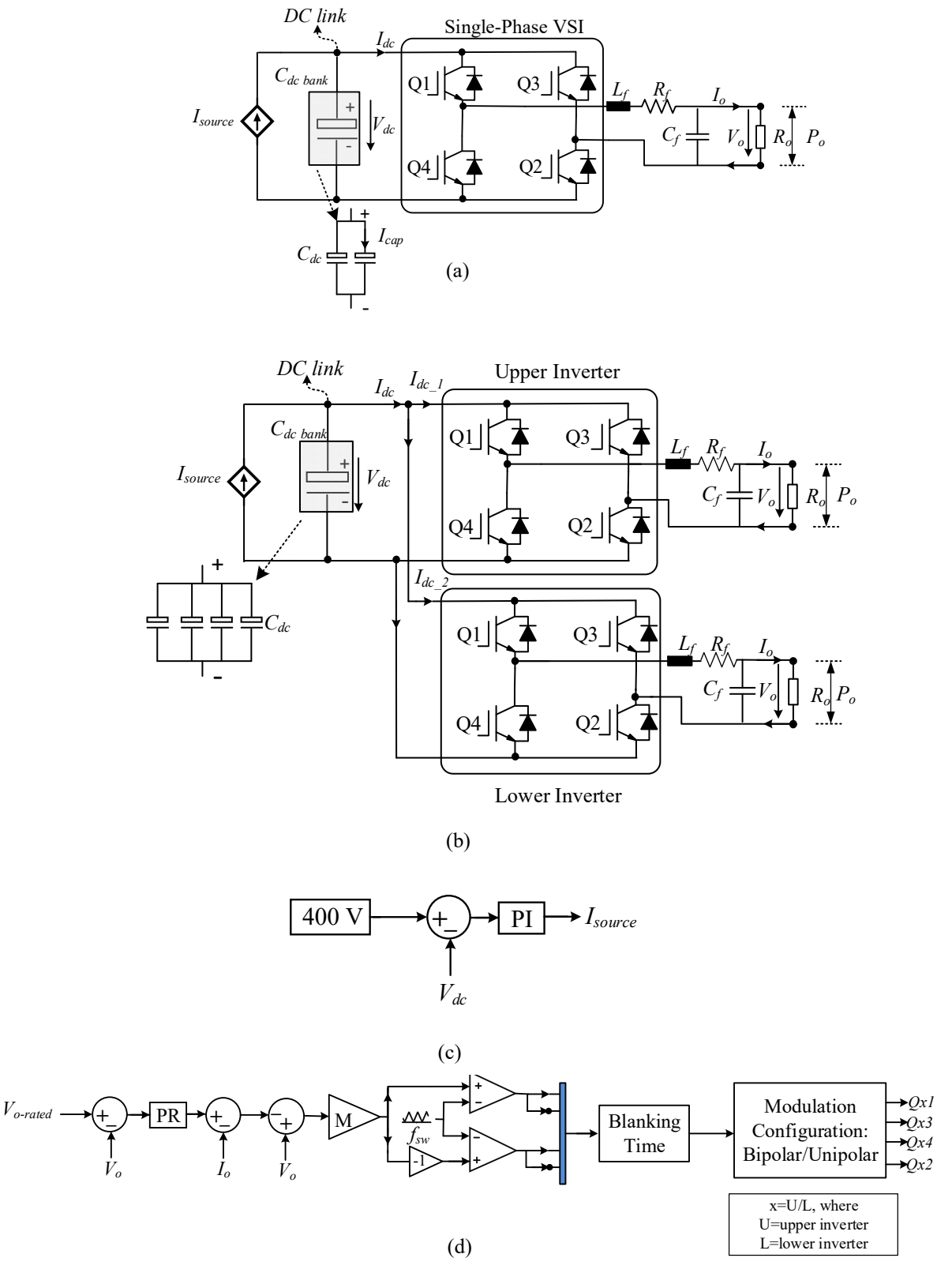


Fig. 1: Block diagram of (a) single phase VSI (b) two parallel VSI units connected to a common DC-bus (c) PI controller unit for input DC-link voltage (V_{dc}) control (d) PR controller unit for output voltage control using the different modulation techniques (Specifications: M=1/400).

Reliability Analysis of the DC-link Capacitor

The first step is to choose the C_{dc} based on the DC-link specifications (V_{dc}) and maximum allowed I_{cap}. The rated voltage and rated ripple current of chosen capacitor should be greater than the specified DC-link voltage and maximum $I_{cap.}$ The next important step, while designing the DC-link capacitor bank is to determine if multiple capacitors are needed rather than connecting a single capacitor based on the required voltage rating and also to reduce the current stress on the C_{dc}. Finally, the electrical and thermal stress should be carefully evaluated for a precise capacitor lifetime estimation. In a VSI, high capacitance at the DC-link is required to suppress the high-frequency harmonic ripples from the switching of the inverters as well as the double-line frequency ripples. Electrical stress analysis and thermal stress analysis are given below [12].

Electrical Stress Analysis

The equivalent electrical circuit model and the thermal model of El-caps are shown in Fig.2(a). It consists of the ESR, ESL (Equivalent Series Inductance), and $R_{leakage}$ (connected in parallel with C_{dc} to provide a path for the flow of $I_{leakage}$). The ESL is not considered in this paper for calculations because the simulations are operated below the resonance frequency of the capacitor, where the inductive resistance of the winding and its terminals ($X_L = \omega ESL$) is considered to be very small and constant. Similarly, according to the datasheet [9], $I_{leakage}$ for the selected capacitor is very small (in values of μA).

$$ESR = R_o + R_d + R_e \tag{1}$$

As explained in (1), the ESR of a capacitor, which is a sum of R_o (constant ohmic resistance of foil, connecting legs of capacitors, etc), R_d (frequency-dependent resistance of dielectric layer) and R_e (temperature-dependent resistance of electrolytic solution) varies with the frequency of ripple current (I_{cap}) as well the hot-spot (core temperature) of the capacitor. Therefore, it is necessary to consider the ESR to calculate the capacitor current ripple, which is a limiting factor of the capacitor lifetime as shown in (2)-(3).

$$I_{cap} = \sqrt{\left(I_{f1} \times K_{f1}\right)^2 + \left(I_{f2} \times K_{f2}\right)^2 + ... + \left(I_{fi} \times K_{fi}\right)^2} \tag{2}$$

$$K_{fi} = \sqrt{\frac{ESR(f_i)}{ESR(f_{double})}} \tag{3}$$

where I_{fi} is the RMS value of harmonic ripple current (calculated from the current harmonic spectrum) at frequency f_i. K_{fi} is the correction factor for I_{fi} at the respective frequency, which can be obtained from the datasheet of the specific capacitor used in this study. In (3), f_{double} represents the double-frequency or second harmonic. $ESR\ (f_i)$ and $ESR\ (f_{double})$ are the ESR of the i^{th} frequency and at 100 Hz. For the capacitor chosen in this paper, the line fundamental frequency is 50 Hz. Hence, f_{double} =100Hz, from capacitor datasheet [11].

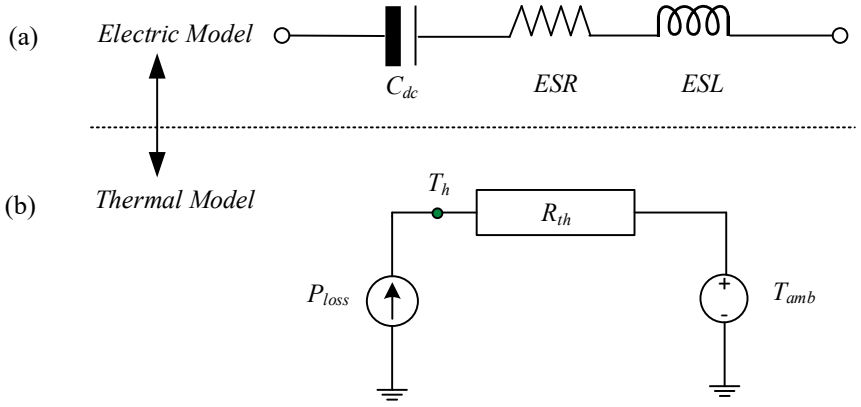


Fig. 2: Aluminium Electrolytic Capacitor (a) Electrical Model and (b)Thermal Model [13]

Thermal Stress Analysis

Besides the electrical stress, the thermal stress analysis is an equally critical stressor to capacitor wear out [14]. The thermal model of an electrolytic capacitor is shown in Fig. 2(b) and the thermal parameters, obtained from the datasheets are summarized in Table V. The core temperature is also known as the hot-spot temperature T_h which is determined by three factors [9] as shown in (4): T_a (operational temperature), P_{loss} (the power dissipation in the capacitor as shown in (5)), and the overall thermal resistance R_{th} between the capacitor core and the ambient air.

$$T_h = T_a - \left(P_{loss} \times R_{th}\right) \tag{4}$$

$$P_{loss} = \sum_{i=1}^{n} \left(I_{fi}\right)^2 \times ESR(f_i) \tag{5}$$

$$\Delta T_h = \left(P_{loss} \times R_{th}\right) \tag{6}$$

where ΔT_h is the rise in the core temperature of the capacitor. The above three equations show that an increase in the capacitor current increases both the power losses and capacitor core temperature within the capacitor. This will eventually degrade the capacitor reliability due to the loss of electrolyte, as described in previous sections.

Lifetime Estimation of the DC-link Capacitor

The lifetime of the El-caps, which includes the actual ripple current I_{cap} flowing through the capacitor can be estimated by using the (7) [15].

$$L_x = L_o \times \underbrace{2^{\left(\frac{T_r - T_a}{10}\right)}}_{K_T} \times \underbrace{\left(\frac{V_a}{V_r}\right)^{-p}}_{K_V} \times \underbrace{K_c^{\left[1-\left(\frac{I_{cap}}{I_r}\right)^2\right]\times\frac{\Delta T_h}{10}}}_{K_{CR}} \tag{7}$$

where L_x and L_o are the estimated and rated lifetime of the capacitor. L_x depends upon the temperature factor K_T, voltage ripple factor K_V, and the current ripple factor K_{CR}. T_r is the rated upper category temperature, ΔT_h is the rated rise in the core temperature of the capacitor and T_a refers to the operating temperature. V_a and V_r are the actual operating voltage and rated voltage. Exponent p is a constant and depends on the ratio between V_a and V_r whereas parameter K_C is a temperature T_r dependent constant. In this paper, as discussed in [12], the values are taken as $p=5$ and $K_C=4$. According to (7), an increase in the capacitor current decreases the lifetime of the capacitor. The parameters of the chosen capacitor for this study, obtained from the capacitor's datasheet [11] are shown in Table V. I_r is the rated RMS value of capacitor current and I_{cap} is calculated using (2-3) [12].

Table V: Parameters of a Single DC-link Capacitor (BDK4345)

Parameter	Values
Single Capacitance	460 uF
ESR(f_{double})	0.18 Ω @ 100 Hz
ESL	20 nH
Thermal Resistance (R_{th})	5.74 ºC /W
Rated Lifetime (L_o)	5000 hours @ T_r and I_r
Rated Upper Category Temperature (T_r)	105 ºC
Rated Ripple Current (I_r)	2.54 A
Rated Voltage (V_r)	500 V
Operating Temperature (T_a)	55 ºC
Rated core temperature increase (ΔT_h)	5 ºC

Results and Discussion

To study the effect of the unipolar and bipolar SPWM technique on the lifetime of the DC-link capacitor, two scenarios are analysed in this paper. In the first scenario, the two topologies shown in Fig.1 (a) and Fig.1 (b) are studied under different output loading conditions, and in the second scenario, different modulation indices are considered. First, one single-phase VSI unit, as shown in Fig. 1(a) is simulated using different modulations for three cases (explained in Table VI). Next, two parallel single-phase VSI units connected to a common DC-bus as shown in Fig. 1(b) are simulated under four cases (as explained in Table VI). In the two-units system, both units are operated at the same loading conditions and are assumed to be synchronous. The modelling and simulations are carried out in *PLECS* to obtain the I_{cap} spectrum corresponding to each case. It is then exported to *MATLAB*, where the actual I_{cap} is calculated as explained in [6] from its spectrum. Finally, the L_x of the capacitor is estimated using (7) and the results are shown in Fig. 3 (a)-(d). It can be observed from Fig. 3 (a)-(b) that the lifetime of C_{dc} decreases with the increasing output power of the system. Furthermore, the lifetime of the C_{dc} increases with increasing M_a as it is shown in Fig.3 (c)-(d). The time-domain waveforms of the DC-link capacitor current are shown in Fig. 4, which illustrates the effect of different modulations on the I_{cap} ripples in a single unit and parallel-connected VSI system. The results from the simulations can be summarised as follows:

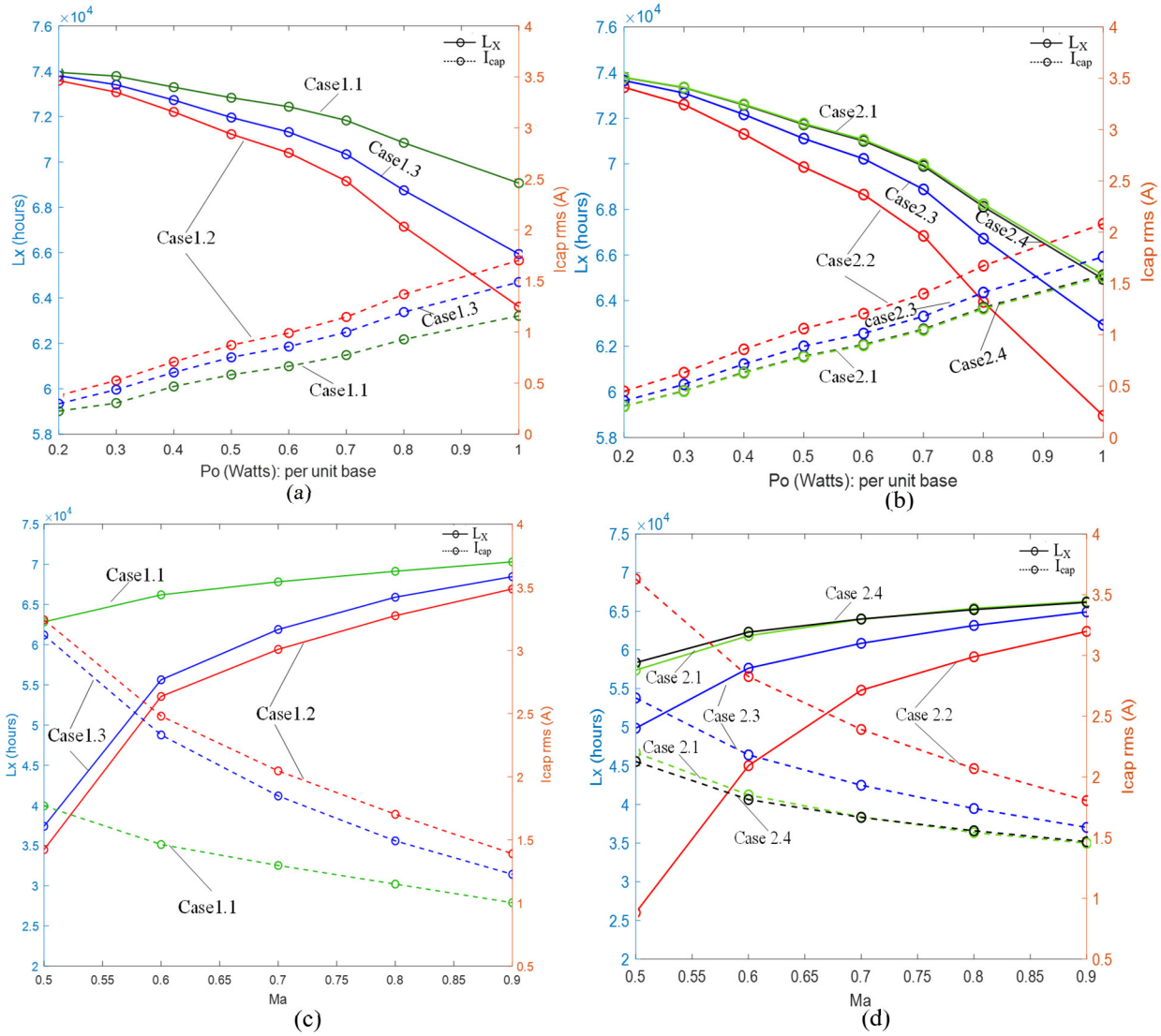


Fig. 3: Effect of modulation techniques on the lifetime of single DC-link El-cap, *under different output power conditions in*: (a) single VSI unit (Fig. 1(a)) (b) two parallel VSI units connected to a common DC-bus (Fig. 1(b)), and *under varying values of modulation index* M_a in : (c) single VSI unit (d) two parallel VSI units.

Table VI: Simulation case studies of systems in Fig. 1

Case	No. of Units	Modulation Type	
		Unipolar SPWM (unit #1)	Bipolar SPWM (unit #2)
1.1	1	✓ f_{sw} = 20 kHz	×
1.2	1	×	✓ f_{sw} = 20 kHz
1.3	1	×	✓ f_{sw} = 40 kHz
2.1	2	✓ f_{sw} = 20 kHz	×
2.2	2	×	✓ f_{sw} = 20 kHz
2.3	2	✓ f_{sw} = 20 kHz	✓ f_{sw} = 20 kHz
2.4	2	✓ f_{sw} = 20 kHz	✓ f_{sw} = 40 kHz

Results of scenario 1-Different output power (P_o) conditions:

From the graphs in Fig. 3(a)-(b), it is observed that the current flowing through the DC-link capacitor increases with the increase in output power, thereby decreasing the lifetime of C_{dc}. Comparing the three cases shown in Fig. 3(a), the L_x of the DC-link capacitor is the highest in Case 1.1 when unipolar SPWM (with switching frequency f_{sw} = 20 kHz) is applied to a single unit VSI. The L_x of the capacitor in Case 1.2 and Case 1.3, which uses bipolar SPWM is less compared to when using unipolar modulation. This is because, as seen from the right y-axis of Fig. 3(a), I_{cap} flowing into the capacitor is less for unipolar SPWM, resulting in lower the electro-thermal stress on the capacitor than when using bipolar SPWM. Besides, it is visible from Fig. 3(a) that even though both Case 1.2 and Case 1.3 use bipolar SPWM, the L_x in case 1.3 (having f_{sw} = 40 kHz) is higher than in Case 1.2 (having f_{sw} = 20 kHz). The increase in the lifetime is because increasing the f_{sw} decreases the high-frequency current ripple components flowing into the capacitor, thus reducing the electro-thermal stress on C_{dc}.

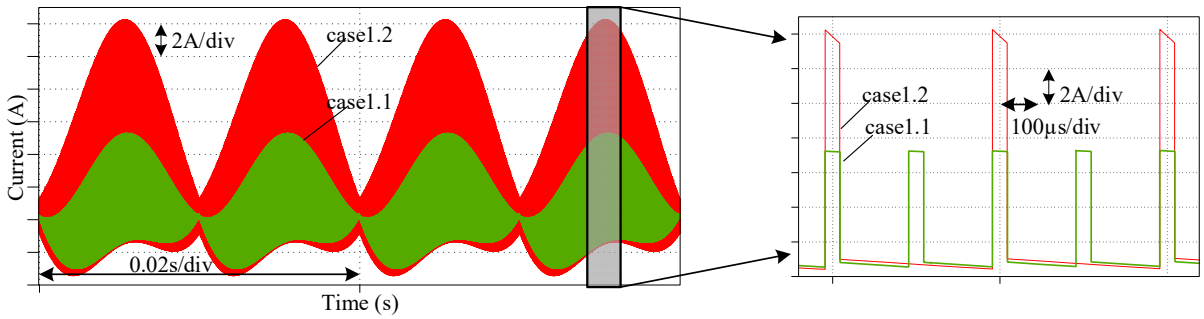
Now, when two VSI units are implemented, it is expected from the results of single-unit topology that when both upper and lower units use unipolar SPWM modulation (at same f_{sw}), the L_x of C_{dc} will be the highest. Whereas, employing bipolar SPWM for both lower and upper VSI units will result in the lowest L_x. From the four cases shown in Fig. 3(b), it can be seen that the results match the expectation where Case 2.1 results in the highest L_x and Case 2.2 results in the lowest L_x of the DC-link capacitor. It is interesting to note that, Case 2.1 and case 2.4 results have almost the same lifetime for the C_{dc}. However, comparing Case 2.1 and Case 2.4, it is better to use Case 2.1 because of the lower switching frequency capacitor current ripple as shown in Fig. 4(c)-(d). This is due to the differences in the electro-thermal stresses on the capacitor which are a result of the current flowing into the capacitor.

Results of scenario 2-Different modulation amplitude indices (M_a):

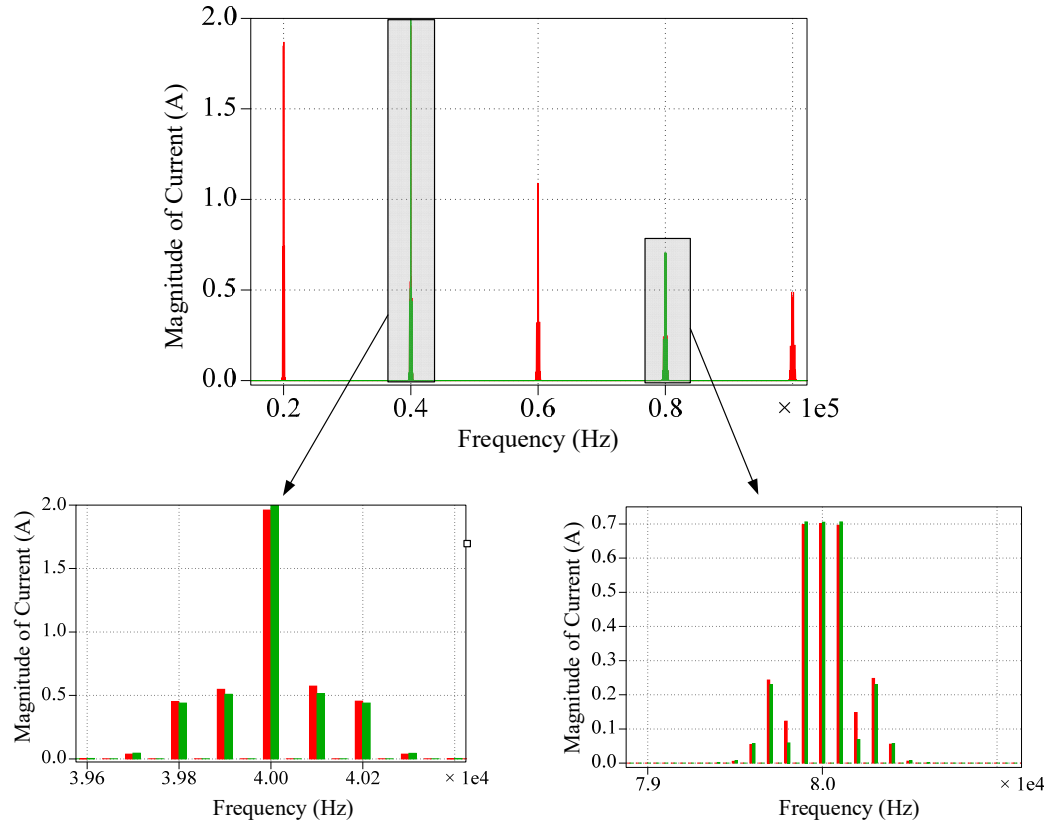
For scenario-2 in Fig. 3(c)-(d), it is seen that the current flowing through the DC-link capacitor decreases with the increase in the modulation amplitude index. This is because the output voltage increases with the increase in modulation amplitude index, thereby decreasing the output current. Eventually, the I_{cap} decreases with the decrease in the output current, which increases the lifetime of C_{dc}. As the modulation amplitude index increases, for a single unit VSI (three cases implemented) it can be seen from the result in Fig. 3(c) that unipolar SPWM gives the highest lifetime for DC-link capacitors whereas bipolar SPWM produces the lowest L_x, as expected from the analysis of the scenario-1 results. Similarly, for the two VSI unit's topology, using Case 2.1 (both units having unipolar SPWM, having the same switching frequency) results in the highest lifetime for the C_{dc} as shown in Fig. 3(d). In contrast, the lowest L_x is observed when implementing Case 2.2.

Finally, as shown in Fig. 4(a)-(b), it can be concluded that unipolar SPWM gives the highest lifetime for DC-link capacitors when a single unit VSI is implemented. Likewise, for two paralleled VSI unit's topology, both units using unipolar SPWM, having the same switching frequency produces the least thermal stress on the capacitor and consequently giving the highest lifetime as shown in Fig. 4(c)-(d).

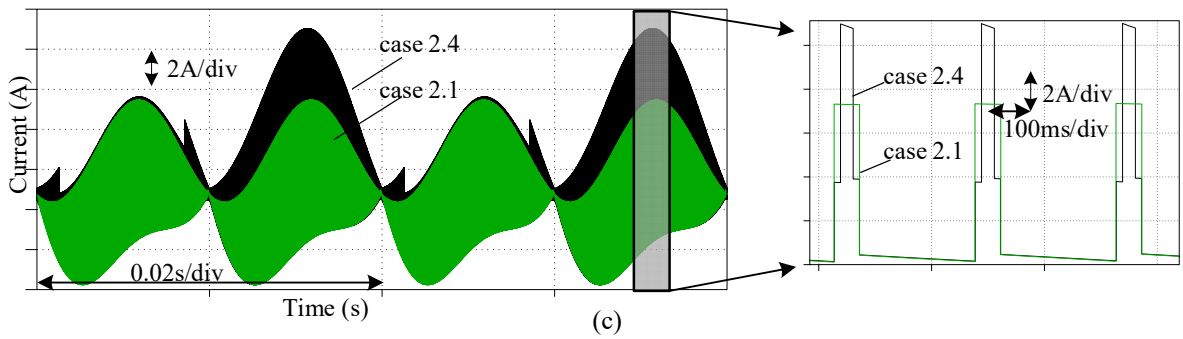
Furthermore, increasing the number of VSI units connected onto a common DC-bus increase the I_{cap}, thereby lowering the L_x of C_{dc}.



(a)



(b)



(c)

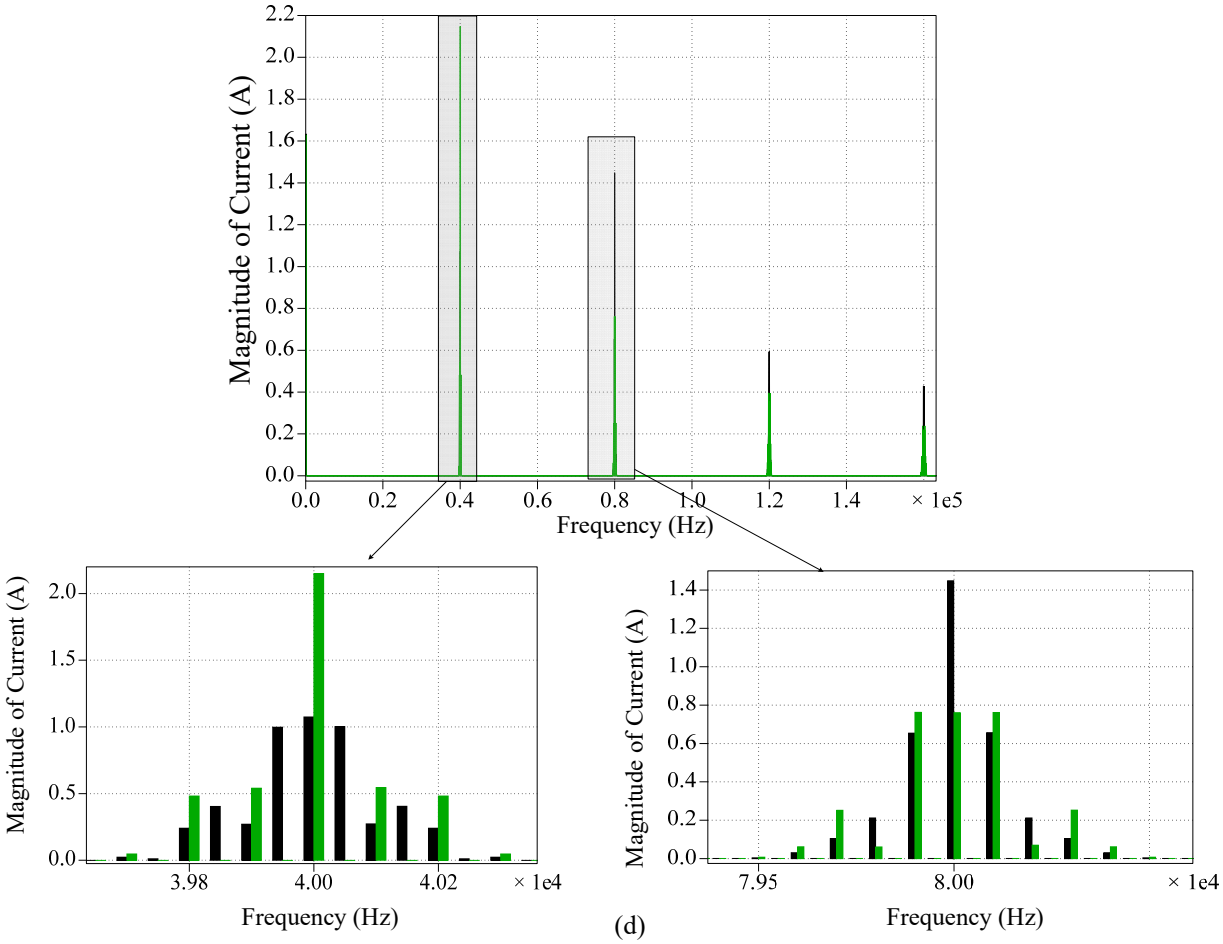


Fig. 4: At rated P_o = 2.5 kW and M_a=0.8 : (a) Time-domain waveforms of I_{cap} for Case 1.1 and Case 1.2 in a single unit VSI (b) FFT of I_{cap} for Case 1.1 and Case 1.2 in a single unit VSI (c) Time-domain waveforms of I_{cap} for Case 2.1 and Case 2.4 in parallel connected VSI units (d) FFT of I_{cap} for Case 2.1 and Case 2.4 in parallel connected VSI units.

Conclusion

This paper has explored the impact of different modulation techniques on the lifetime of the DC-link capacitor in a single voltage source inverter unit and two paralleled voltage source inverter unit topology. Two converter topologies having the same power ratings such as the same DC-link input voltage and rated output power were analysed for different cases. The obtained results indicate that the ripple/switching current components contained in the capacitor current depend on the number of VSI units implemented and the switching characteristics of the semiconductor switches in the inverter, which is controlled by the modulation technique and switching frequency. Hence, using different modulation techniques produces different harmonic currents in the I_{cap}, consequently having different impacts on the lifetime of the capacitors. The higher the value of I_{cap} is, the lower is the lifespan of the capacitor due to an increase in the core-temperature and power-losses within the capacitor. Therefore, in a power converter system, for an appropriate sizing and thermal design of the capacitor and thereby a more accurate estimation of the lifetime of a capacitor, the following factors are of equal paramount importance: the actual current (containing all harmonic ripple currents) flowing through the capacitor, the number of inverter units, switching frequency and the modulation technique which produces the lowest capacitor current ripple.

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