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A Novel Direct Power Control for DFIG with Parallel Compensator under Unbalanced Grid Condition

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Abstract—This paper presents a Voltage-Modulated Direct Power Control (VM-DPC) with an additional parallel compensator for the Doubly Fed Induction Generator (DFIG) under unbalanced grid conditions. The proposed method not only guarantees a satisfying steady-state performance but provides also a regulating property of the negative-sequence output currents through designed negative-sequence parallel compensator. It can provide symmetrical stator currents and suppress the ripples in both active and reactive powers under unbalanced grid conditions. The performance of the proposed method are verified by comparing it with three different control strategies in simulations carried out in Matlab/Simulink SimScape Power System. Finally, the effectiveness of the proposed method is evaluated in an experimental prototype, which proves the proposed VM-DPC with the additional compensator has a satisfactory steady-state performance and a fast power transient response under unbalanced grid conditions.

Index Terms—Direct power control (DPC), doubly fed induction generator (DFIG), rotor side converter (RSC), unbalanced voltage condition.

I. INTRODUCTION

WIND power has experienced rapid growth in recent decade and has become one of the most competitive renewable energy sources [1]. The Doubly-Fed Induction Generator (DFIG) is the dominant onshore wind power generation topology due to the advantages including flexible power regulating capability and low cost of the back-to-back converter. Due to the increasing penetration level, the wind turbines are now required to withstand grid faults and disturbances as well as contributing to the grid recovery [2]. The DFIG system, however, is sensitive to the stator voltage disturbances due

to the direct connection between the stator and the grid [3]. The Vector Oriented Control (VOC) is the most well-known control strategy for DFIG. But the Phase-Locked Loop (PLL) is required in VOC, which may be disturbed by the voltage distortion [4], [5].

The Direct Power Control (DPC) techniques have been widely discussed in the last decades and proved to be feasible in DFIG control applications [6]–[12]. Conventional Look-Up-Table (LUT) based DPC technique enables DFIGs with faster transient power dynamics than VOC [6], [7]. The main drawback of LUT-DPC is the time-varying switching frequency, which results in unexpected fluctuations in stator current and power. To solve the problem, numbers of improved DPC methods have been proposed such as Model Predictive Control (MPC)-DPC, Sliding Model Control (SMC)-DPC, and Voltage Modulated (VM)-DPC. The MPC-DPC can select the optimal voltage vector by minimizing the cost function, which is more effective and accurate than traditional DPC [10]. However, the MPC-DPC is relatively complex, the evaluation of the optimal voltage vector requires a lot of computation time. SMC-DPC is a robust control strategy [8], but it is a nonlinear control and has a potential chattering problem, which may introduce instability to the control system. The VM-DPC combined with Pulse-Width-Modulation (PWM) has recently been proposed [13]–[16], which provides a linear-time-invariant characteristic. It has been applied in voltage source converter and has been experimentally proved to be well-performed with a small-level of current fluctuations in steady-state [14], [15]. However, it has not been applied to wind power generation. Besides, the limitations and improvements of VM-DPC under unbalanced voltage conditions have not been thoroughly discussed.

Most of the control strategies are sensitive to the grid disturbance and unbalanced grid faults [8], [17]. A flexible current selector based on VOC is designed for the distributed power generation system under the unbalanced voltage conditions [18]. For the DPC based control, several efforts have been addressed to improve the performance under unbalanced grid conditions by adding compensation terms, which works well for the LUT-DPC and SMC-DPC strategies [8], [17], [19]. An improved MPC-DPC with unified power compensation is proposed in [10], which can reduce the current harmonic and restrain power ripples under unbalanced voltage conditions. However, it requires a PLL to obtain synchronous phase posi-

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tion. An improved DPC design with a frequency estimation algorithm is proposed in [20] to deal with the frequency deviation and harmonic distortion problems. However, the design requests a frequency estimation unit to provide the phase signal of the stator voltage. A resonant based back-stepping DPC is proposed in [21], which can provide satisfying performance under unbalanced conditions without the need of sequence decomposition, but a PLL is needed for the compensation block. An improved SMC-DPC method using extended active power is presented in [5], which restrains the ripple of stator current and electromagnetic torque effectively under unbalanced conditions. However it provides a stator current with relatively large harmonics under balanced grid conditions. A four-leg stator side converter configuration is proposed for a stand-alone DFIG-based generation system, which largely improves the system performance when connected to an unbalanced load [22]. However, the application for grid-connected DFIG system is not mentioned.

The purpose of this paper is to present a simple yet efficient control strategy for Rotor Side Converter (RSC) to improve the performance of DFIG under both balanced and unbalanced grid conditions. The VM-DPC is designed as the control basis to obtain an improved steady-state performance and a fast transient response of DFIG under balanced grid conditions. Besides, a Parallel Compensator (PC) is designed to operate along with the VM-DPC and control the negative-sequence current through a closed-loop structure, which can balance the stator current and reduce the ripples in active and reactive powers under unbalanced grid conditions. The merits of the proposed method are as follows:

- Guaranteed steady-state performance under unbalanced voltage conditions by the elimination of the negative-sequence stator current and reduction of the third-order harmonics. The active and reactive power fluctuations having twice the fundamental frequency and the electromagnetic torque ripples under unbalanced grid conditions are also significantly suppressed.
- The proposed VM-DPC with PC provides a fast and smooth power transient response under unbalanced voltage condition, which indicates a potential application of the proposed method for quick dynamic response scenarios under unbalanced grid conditions.
- The proposed control design has a simple structure, which does not require a PLL or measurement of the rotor side current.

Although the idea for voltage source converters was firstly introduced in [23], in this paper, the VM-DPC with compensator is applied in DFIG rather than voltage source converter. The simulation results are compared with three different control strategies, including two with targeted improvements under unbalanced voltage conditions and as well as the pure VM-DPC. Moreover, the effectiveness of the proposed method applied in DFIG is tested through an experimental prototype.

II. BASIC KNOWLEDGE OF VM-DPC AND DESIGN OF PARALLEL COMPENSATOR

In order to investigate the proposed control strategy, the basic mathematical modeling of the DFIG is firstly presented

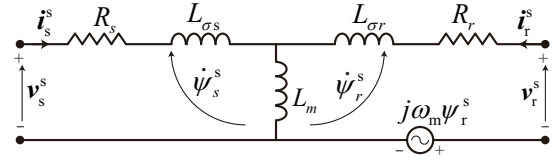


Fig. 1. Equivalent circuit of the DFIG in the stator stationary ($\alpha\beta$) reference frame.

in subsection A. The derivation of the PC designed for the unbalanced grid conditions is presented in subsection B.

A. Design of VM-DPC for Rotor Side Converter

The equivalent circuit of the DFIG in the $\alpha\beta$ reference frame is presented in Fig. 1, where the space vectors of the stator side and rotor side voltages can be expressed as follows,

$$\begin{aligned} v_s^s &= R_s i_s^s + \frac{d\psi_s^s}{dt} \\ v_r^s &= R_r i_r^s + \frac{d\psi_r^s}{dt} - j\omega_m \psi_r^s \end{aligned} \quad (1)$$

where $v_s^s = v_{s\alpha} + jv_{s\beta}$ and $v_r^s = v_{r\alpha} + jv_{r\beta}$ are the space vector of the stator voltages. Note that the superscript 's' of the vectors indicates the $\alpha\beta$ reference frames, which is omitted in the rest of this paper for simplicity. Besides, i_s , i_r , ψ_s , and ψ_r represent the space vectors of the stator and rotor side currents, the stator and rotor side fluxes, respectively, ω_m represents the electrical angular frequency of the rotor, R_s and R_r represent stator and rotor resistances, respectively. The stator and rotor side flux linkages can be expressed as $\psi_s = L_s i_s + L_m i_r$ and $\psi_r = L_r i_r + L_m i_s$, where the self inductances of the stator and rotor windings are $L_s = L_{\sigma s} + L_m$ and $L_r = L_{\sigma r} + L_m$, respectively, L_m denotes the mutual inductance. Note that (1) can be rearranged as follows,

$$\begin{aligned} v_r - \frac{L_r}{L_m} v_s &= R_r i_r + \sigma L_m \frac{di_s}{dt} - j\omega_m (\sigma L_m i_s \\ &\quad + \frac{L_r}{L_m} \psi_s) - \frac{R_s L_r}{L_m} i_s \end{aligned} \quad (2)$$

where $\sigma \triangleq 1 - \frac{L_s L_r}{L_m^2}$ is the leakage factor. According to (2), the instantaneous variation of the stator currents can be derived as follows,

$$\begin{cases} \frac{di_{s\alpha}}{dt} = \frac{1}{\sigma L_m} (v_{r\alpha} - \frac{L_r}{L_m} v_{s\alpha} - R_r i_{r\alpha} + \frac{R_s L_r}{L_m} i_{s\alpha} \\ \quad - \omega_m \frac{L_r}{L_m} \psi_{s\beta} - \sigma \omega_m L_m i_{s\beta}) \\ \frac{di_{s\beta}}{dt} = \frac{1}{\sigma L_m} (v_{r\beta} - \frac{L_r}{L_m} v_{s\beta} - R_r i_{r\beta} + \frac{R_s L_r}{L_m} i_{s\beta} \\ \quad + \omega_m \frac{L_r}{L_m} \psi_{s\alpha} + \sigma \omega_m L_m i_{s\alpha}) \end{cases} \quad (3)$$

The stator active and reactive powers are calculated as,

$$P_s + jQ_s = -\frac{3}{2} v_s \cdot i_s^* \quad (4)$$

According to (4), the instantaneous variations of the stator active and reactive powers can be derived as,

$$\begin{cases} \frac{dP_s}{dt} = -\frac{3}{2} \left(\frac{dv_{s\alpha}}{dt} i_{s\alpha} + \frac{di_{s\alpha}}{dt} v_{s\alpha} + \frac{dv_{s\beta}}{dt} i_{s\beta} + \frac{di_{s\beta}}{dt} v_{s\beta} \right) \\ \frac{dQ_s}{dt} = -\frac{3}{2} \left(\frac{dv_{s\beta}}{dt} i_{s\alpha} + \frac{di_{s\alpha}}{dt} v_{s\beta} - \frac{dv_{s\alpha}}{dt} i_{s\beta} - \frac{di_{s\beta}}{dt} v_{s\alpha} \right). \end{cases} \quad (5)$$

As expressed in (5), the instantaneous grid voltage variation is required. Note that the VM-DPC is designed based on an ideal grid condition with the voltage angular frequency of ω_s . The stator side voltage can be expressed as, $v_{s\alpha} = |v_s| \cos(\omega_s t + \theta_0)$, $v_{s\beta} = |v_s| \sin(\omega_s t + \theta_0)$. Therefore, the instantaneous grid voltage variation can be expressed as $dv_{s\alpha}/dt = -\omega_s v_{s\beta}$, $dv_{s\beta}/dt = \omega_s v_{s\alpha}$. Since the stator resistance is small, which can be neglected, the stator flux can be approximated as,

$$\psi_s \approx -j \frac{1}{\omega_s} v_s. \quad (6)$$

It is noted that the rotor resistance R_r is relatively small in the DFIG with a large capacity, therefore, by neglecting the terms with R_r and manipulating (3), (5), and (6), the dynamics of the instantaneous active and reactive powers are carried out as,

$$\begin{cases} \frac{dP_s}{dt} = -\omega_r Q_s + \frac{L_r R_s}{\sigma L_m^2} P_s \\ \quad - \frac{3}{2L_m \sigma} \underbrace{(v_{r\alpha} v_{s\alpha} + v_{r\beta} v_{s\beta} - \frac{L_r \omega_r}{L_m \omega_s} |v_s|^2)}_{U_{rP}} \\ \frac{dQ_s}{dt} = \omega_r P_s + \frac{L_r R_s}{\sigma L_m^2} Q_s - \frac{3}{2L_m \sigma} \underbrace{(v_{r\alpha} v_{s\beta} - v_{r\beta} v_{s\alpha})}_{U_{rQ}} \end{cases}, \quad (7)$$

where U_{rP} and U_{rQ} are defined as Voltage Modulated Regulation (VMR) terms, which represent the coupling terms between the stator voltage and the rotor voltage. According to (7), the VMR terms can be rearranged as follows,

$$\begin{cases} U_{rP} = K_s \nu_{rp} + K_s \omega_r Q_s + \frac{L_r \omega_r}{L_m \omega_s} |v_s|^2 \\ U_{rQ} = K_s \nu_{rq} - K_s \omega_r P_s \end{cases}, \quad (8)$$

where $K_s = -2\sigma L_m/3$ is the gain of the power compensation, ν_{rp} and ν_{rq} are the power regulating variables of the active and reactive powers, respectively,

$$\begin{cases} \nu_{rp} = \frac{dP_s}{dt} - \frac{L_r R_s}{\sigma L_m^2} P_s \\ \nu_{rq} = \frac{dQ_s}{dt} - \frac{L_r R_s}{\sigma L_m^2} Q_s \end{cases}. \quad (9)$$

Note that various control methods can be used to generate ν_{rp} and ν_{rq} , for the sake of simplicity, a simple Proportional-Integral (PI) control is chosen to design the VM-DPC in this paper as follows,

$$\begin{cases} \nu_{rp} = K_{rp}(P_s^* - P_s) + K_{ri} \int (P_s^* - P_s) dt \\ \nu_{rq} = K_{rp}(Q_s^* - Q_s) + K_{ri} \int (Q_s^* - Q_s) dt \end{cases}, \quad (10)$$

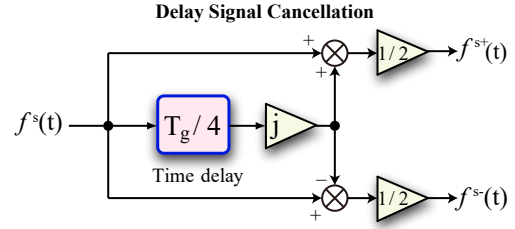


Fig. 2. Control block diagram of a delay signal cancellation (DSC) [25].

where P_s^* and Q_s^* are the references of stator active and reactive powers, respectively. K_{rp} and K_{ri} are the control parameters of the rotor side VM-DPC. By using the differential expression of (10) and (9) and applying the Laplace transform, the control system can be transformed into a single-input, single-output system. The guaranteed global exponential stability of the system can be proved [13].

The controlled RSC terminal voltage signals in the $\alpha\beta$ reference frame can be calculated by the definition of VMR inputs U_P and U_Q as,

$$\begin{cases} v_{r\alpha} = \frac{v_{s\alpha} U_{rP} + v_{s\beta} U_{rQ}}{|v_s|^2} + \frac{L_r \omega_r}{L_m \omega_s} v_{s\alpha} \\ v_{r\beta} = \frac{v_{s\beta} U_{rP} - v_{s\alpha} U_{rQ}}{|v_s|^2} + \frac{L_r \omega_r}{L_m \omega_s} v_{s\beta} \end{cases}. \quad (11)$$

B. Parallel Compensator (PC) Designed for DFIG Under Unbalanced Voltage Conditions

The proposed VM-DPC is built based on an ideal grid condition. The performance will be strongly deteriorated under unbalanced grid conditions. To improve the performance of VM-DPC under unbalanced grid conditions, the PC is introduced in this subsection.

To further explain the mechanism of the proposed parallel compensator, the mathematical modeling of the DFIG under unbalanced grid conditions is presented. The positive and negative sequences of the stator voltage v_s , can be further expressed as follows,

$$\begin{aligned} v_s^s &= v_s^{s+} + v_s^{s-} \\ &= |v_s^+| e^{j(\omega_s t + \phi_{vs}^+)} + |v_s^-| e^{j(-\omega_s t + \phi_{vs}^-)}, \end{aligned} \quad (12)$$

where superscript 's' denotes the $\alpha\beta$ reference frame. It is omitted in the later of this paper for simplicity as vectors are implemented in the same $\alpha\beta$ reference frame. It is noted that the DPC usually excites the third-order harmonic components in the stator current under unbalanced conditions [8], [17], [24]. Therefore, the stator current vector can be presented in detail as follows,

$$\begin{aligned} i_s &= i_s^+ + i_s^- + i_s^{3+} = |i_s^+| e^{j(\omega_s t + \phi_{is}^+)} \\ &\quad + |i_s^-| e^{j(-\omega_s t + \phi_{is}^-)} + |i_s^{3+}| e^{j(3\omega_s t + \phi_{is}^{3+})}, \end{aligned} \quad (13)$$

The relationship between the vectors v_s and i_s is presented as shown in Fig. 3. In order to eliminate the negative-sequence current and reduce the power ripples, the sequence separation should be considered in the first place. The traditional sequence separation method requires the coordinate

transformation of the signals and using band-trap filter [26]. In this paper, a Delay Signal Cancellation (DSC) technique is used to extract the negative-sequence components. The DSC allows extracting the positive and negative sequence with a time delay of $1/4$ of the signal period without a coordinate transformation, but it is sensitive to frequency variations [25]. It has been widely used to improve PLL or DFIG control under unbalanced grid conditions [19], [27], [28]. The DSC of the stator voltage can be designed according to the following equations,

$$\begin{aligned} v^+(t) &= \frac{1}{2}[v^s(t) + jv^s(t - \frac{T_g}{4})] \\ v^-(t) &= \frac{1}{2}[v^s(t) - jv^s(t - \frac{T_g}{4})] \end{aligned} \quad (14)$$

where T_g is the period of the grid voltage. The control block diagram of the DSC is shown in Fig. 2. It is noted that the negative-sequence components with the fundamental frequency and the positive-sequence of the third-order harmonics will be output through the same port of DSC designed for stator currents as follows,

$$\begin{aligned} i^+(t) &= \frac{1}{2}[i(t) + ji^s(t - \frac{T_g}{4})] \\ i^-(t) + i^{s3+}(t) &= \frac{1}{2}[i^s(t) - ji(t - \frac{T_g}{4})] \end{aligned} \quad (15)$$

Then, P_s and Q_s can be separated into different components as follows,

$$\begin{cases} P_s = P_{s11} + P_{s12} + P_{s21} + P_{s22} + P_{s13} + P_{s23} \\ Q_s = Q_{s11} + Q_{s12} + Q_{s21} + Q_{s22} + Q_{s13} + Q_{s23} \end{cases} \quad (16)$$

The detailed expression of each power component can be written as

$$\begin{aligned} P_{s11} &= -\frac{3}{2}(v_{s\alpha}^+ i_{s\alpha}^+ + v_{s\beta}^+ i_{s\beta}^+), & P_{s12} &= -\frac{3}{2}(v_{s\alpha}^+ i_{s\alpha}^- + v_{s\beta}^+ i_{s\beta}^-) \\ P_{s21} &= -\frac{3}{2}(v_{s\alpha}^- i_{s\alpha}^+ + v_{s\beta}^- i_{s\beta}^+), & P_{s22} &= -\frac{3}{2}(v_{s\alpha}^- i_{s\alpha}^- + v_{s\beta}^- i_{s\beta}^-) \\ P_{s13} &= -\frac{3}{2}(v_{s\alpha}^+ i_{s\alpha}^{3+} + v_{s\beta}^+ i_{s\beta}^{3+}), & P_{s23} &= -\frac{3}{2}(v_{s\alpha}^- i_{s\alpha}^{3+} + v_{s\beta}^- i_{s\beta}^{3+}) \\ Q_{s11} &= -\frac{3}{2}(v_{s\beta}^+ i_{s\alpha}^+ - v_{s\alpha}^+ i_{s\beta}^+), & Q_{s12} &= -\frac{3}{2}(v_{s\beta}^+ i_{s\alpha}^- - v_{s\alpha}^+ i_{s\beta}^-) \\ Q_{s21} &= -\frac{3}{2}(v_{s\beta}^- i_{s\alpha}^+ - v_{s\alpha}^- i_{s\beta}^+), & Q_{s22} &= -\frac{3}{2}(v_{s\beta}^- i_{s\alpha}^- - v_{s\alpha}^- i_{s\beta}^-) \\ Q_{s13} &= -\frac{3}{2}(v_{s\beta}^+ i_{s\alpha}^{3+} - v_{s\alpha}^+ i_{s\beta}^{3+}), & Q_{s23} &= -\frac{3}{2}(v_{s\beta}^- i_{s\alpha}^{3+} - v_{s\alpha}^- i_{s\beta}^{3+}) \end{aligned} \quad (17)$$

Here, (P_{s11}, Q_{s11}) , (P_{s22}, Q_{s22}) are the dc values, which are composed by the components with the same sequence. (P_{s12}, Q_{s12}) , (P_{s21}, Q_{s21}) , and (P_{s13}, Q_{s13}) are the values with twice the fundamental frequency, which are generated by the coupling between the different sequence components. (P_{s23}, Q_{s23}) with four times of the fundamental frequency, is generated by the coupling between v_s^- and i_s^{3+} . It has already been proved that the ac components cannot be eliminated simultaneously [8]. Normally, there are three control schemes to choose from, e.g., maintaining the sinusoidal stator currents, keeping constant active power, or removing the ripples of reactive power. The unbalanced stator currents will cause electromagnetic torque ripples as well as power fluctuations

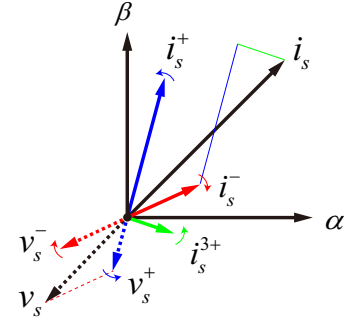


Fig. 3. Relationship of the vectors i_s and v_s with different sequence components.

and deteriorate the grid stability [29], [30]. The main purpose of the designed compensator is to realize how to balance the stator current, which is to eliminate the negative sequence of stator current i_s^- and to reduce the ripples in P_s and Q_s under unbalanced conditions.

According to (17), there are six power coupling pairs, i.e. (P_{s11}, Q_{s11}) , (P_{s12}, Q_{s12}) , (P_{s21}, Q_{s21}) , (P_{s22}, Q_{s22}) , (P_{s13}, Q_{s13}) , and (P_{s23}, Q_{s23}) . Among them, only (P_{s11}, Q_{s11}) and (P_{s22}, Q_{s22}) are the dc components, which can be simply controlled by PI control technique. Since (P_{s22}, Q_{s22}) is only related to v_s^- and i_s^- , the term i_s^- can be eliminated by controlling (P_{s22}, Q_{s22}) to be zero. Once $i_s^- = 0$, the ac component (P_{s12}, Q_{s12}) is also eliminated. Therefore, the fluctuation of the powers, as well as the third order harmonics i_s^{3+} in the stator currents, which are induced by the power components of twice the fundamental frequency, can be restrained [31]. Consequently, in this paper, a PC is designed to dynamically regulate (P_{s22}, Q_{s22}) through a closed-loop structure. By regulating (P_{s22}, Q_{s22}) to zero, the PC is capable of eliminating i_s^- in the stator currents and reducing the power ripples as well as i_s^{3+} . The compensator only operates under unbalanced conditions. In the balanced condition, the DFIG is automatically controlled by the conventional VM-DPC. Another potential application of PC is to provide a negative-sequence reactive current to overcome the voltage rise and voltage distortion under unbalanced conditions [32]. It is noted that $i^-(t)$ and $i^+(t)$ are both outputs from the same port of the DSC. Therefore, the active and reactive power inputs of the PC are $P_{sn} = P_{s22} + P_{s23}$, $Q_{sn} = Q_{s22} + Q_{s23}$, separately. The PC is mainly designed to control the dc components P_{s22} and Q_{s22} . The basic control scheme of the VM-DPC combined with PC is shown in Fig. 4. According to (17), the derivations of P_{s22} and Q_{s22} can be derived as,

$$\begin{cases} \frac{dP_{s22}}{dt} = -\frac{3}{2}(\frac{dv_{s\alpha}^-}{dt} i_{s\alpha}^- + \frac{di_{s\alpha}^-}{dt} v_{s\alpha}^- + \frac{dv_{s\beta}^-}{dt} i_{s\beta}^- + \frac{di_{s\beta}^-}{dt} v_{s\beta}^-) \\ \frac{dQ_{s22}}{dt} = -\frac{3}{2}(\frac{dv_{s\beta}^-}{dt} i_{s\alpha}^- + \frac{di_{s\alpha}^-}{dt} v_{s\beta}^- - \frac{dv_{s\alpha}^-}{dt} i_{s\beta}^- - \frac{di_{s\beta}^-}{dt} v_{s\alpha}^-) \end{cases} \quad (18)$$

The angular frequency of negative-sequence stator voltage

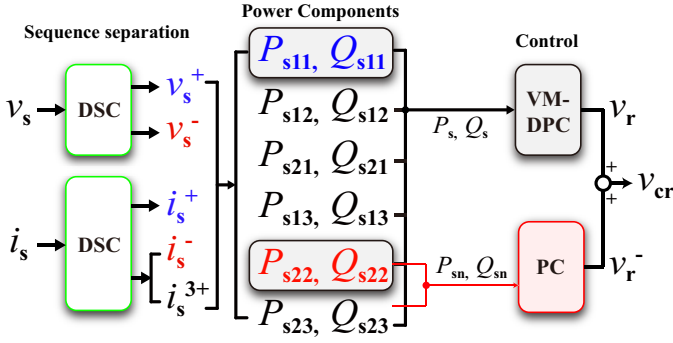


Fig. 4. Basic control scheme of VM-DPC combined with a parallel compensator (PC).

is $-\omega_s$, thus v_s^- can be described as follows,

$$\begin{cases} v_{s\alpha}^- = |v_s^-| \cos(-\omega_s t + \theta_0^-) \\ v_{s\beta}^- = |v_s^-| \sin(-\omega_s t + \theta_0^-) \end{cases} \quad (19)$$

The derivations of v_s^- can be obtained as,

$$\frac{dv_s^-}{dt} = -j\omega_s v_s^- \quad (20)$$

If R_s is small enough to be neglected, then ψ_s can also be expressed as,

$$\psi_s^- = j \frac{1}{\omega_s} v_s^- \quad (21)$$

Based on (3), (18), (20), and (21), the dynamics of P_{s22} , Q_{s22} can be written as,

$$\begin{cases} \frac{dP_{s22}}{dt} = \omega_r Q_{s22} + \frac{L_r R_s}{\sigma L_m^2} P_{s22} - \frac{3}{2L_m \sigma} [U_{rP}^- \\ - R_r (i_{r\alpha}^- v_{s\alpha}^- + i_{r\beta}^- v_{s\beta}^-)] \\ \frac{dQ_{s22}}{dt} = -\omega_r P_{s22} + \frac{L_r R_s}{\sigma L_m^2} Q_{s22} \\ - \frac{3}{2L_m \sigma} [U_{rQ}^- + R_r (i_{r\beta}^- v_{s\alpha}^- - i_{r\alpha}^- v_{s\beta}^-)] \end{cases} \quad (22)$$

Similar to the VM-DPC strategy, U_{rP}^- and U_{rQ}^- are designed as the VMR terms of the compensator. By neglecting the rotor side resistance, (22) can be simplified as,

$$\begin{cases} U_{rP}^- = K_s \nu_{rP}^- - K_s \omega_r Q_{s22} + \frac{L_r (\omega_m + \omega_s)}{L_m \omega_s} |v_s^-|^2 \\ U_{rQ}^- = K_s \nu_{rQ}^- + K_s \omega_r P_{s22} \end{cases} \quad (23)$$

where ν_{rP}^- and ν_{rQ}^- are the intermediate power regulating variables. By substituting (23) into (22), ν_{rP}^- and ν_{rQ}^- can be deduced as,

$$\begin{cases} \nu_{rP}^- = \frac{dP_{s22}}{dt} - \frac{L_r R_s}{\sigma L_m^2} P_{s22} \\ \nu_{rQ}^- = \frac{dQ_{s22}}{dt} - \frac{L_r R_s}{\sigma L_m^2} Q_{s22} \end{cases} \quad (24)$$

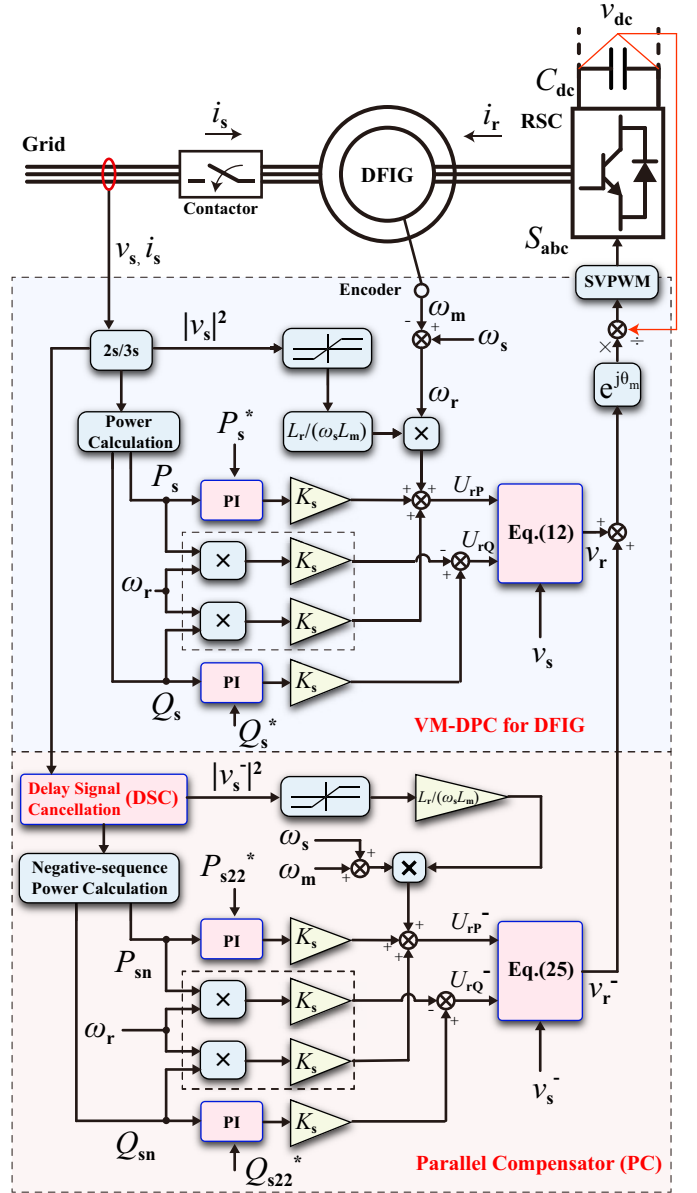


Fig. 5. Complete control block diagram of the proposed VM-DPC with parallel compensator for the rotor side converter (RSC).

The structure of the additional compensator is designed as PI control,

$$\begin{cases} \nu_{rP}^- = K_{rp,n} (P_{s22}^* - P_{s22}) + K_{ri,n} \int (P_{s22}^* - P_{s22}) dt \\ \nu_{rQ}^- = K_{rp,n} (Q_{s22}^* - Q_{s22}) + K_{ri,n} \int (Q_{s22}^* - Q_{s22}) dt \end{cases} \quad (25)$$

where P_{s22}^* and Q_{s22}^* are the power references inputs corresponding to P_{s22} and Q_{s22} , respectively. If the control target is to minimize the negative-sequence of the output current, the active and reactive power reference values can be set as $P_{s22}^* = 0$ and $Q_{s22}^* = 0$, respectively. $K_{rp,n}$ and $K_{ri,n}$ are the control parameters of the parallel compensator.

By using the definition of VMR inputs U_{rP}^- and U_{rQ}^- in (22), the negative-sequence voltage control signals of the RSC can

finally be calculated as,

$$\begin{cases} v_{r\alpha}^- = \frac{v_{s\alpha}^- U_{rP}^- + v_{s\beta}^- U_{rQ}^-}{|\mathbf{v}_s^-|^2} + \frac{L_r(\omega_m + \omega_s)}{L_m \omega_s} v_{s\alpha}^- \\ v_{r\beta}^- = \frac{v_{s\beta}^- U_{rP}^- - v_{s\alpha}^- U_{rQ}^-}{|\mathbf{v}_s^-|^2} + \frac{L_r(\omega_m + \omega_s)}{L_m \omega_s} v_{s\beta}^- \end{cases} \quad (26)$$

Since the system is linear and follows the superposition theorem, the control signals of rotor voltage in the $\alpha\beta$ reference frame can be calculated as the sum of control inputs \mathbf{v}_r in (11) and \mathbf{v}_r^- in (26) as,

$$\begin{cases} v_{cr\alpha} = v_{r\alpha} + v_{r\alpha}^- \\ v_{cr\beta} = v_{r\beta} + v_{r\beta}^- \end{cases} \quad (27)$$

The complete control block diagram of the proposed control strategy is shown in Fig. 5.

TABLE I
PARAMETERS OF SIMULATED 2 MW DFIG SYSTEM AND CONTROL

Parameter	Symbol	Value	Unit
Rated power	P_{ref}	1.5	MW
Sampling frequency	f_a	4	kHz
Switching frequency	f_w	4	kHz
Line-to-line Voltage	$v_{s,rms}$	690	V
DC voltage	v_{dc}	1150	V
Dc Capacitor	C_{dc}	0.08	F
System frequency	f	50	Hz
Stator resistance	R_s	0.0026	Ω
Stator inductance	L_s	6	mH
Rotor resistance	R_r	0.0029	Ω
Rotor inductance	L_r	2.6	mH
Mutual inductance	L_m	2.5	mH
Turns ratio	u	3	
Control Parameters			
Parameter	Value	Parameter	Value
K_{rp}	1000	K_{ri}	20000
$K_{rp,n}$	4000	$K_{ri,n}$	40000
K_s	0.00012		

III. SIMULATION RESULTS

A simulation is carried out in Matlab/Simulink, Simscape Power System to verify the effectiveness of the proposed method under unbalanced grid conditions. The sampling frequency is set to 4 kHz. The switching signal is generated by the SVPWM with a 4 kHz switching frequency. The rotor speed of DFIG is set to operate at a constant rotor speed (122.5 rad/s). The parameters of the model and controllers are presented in Table I.

A. Comparative study

In order to verify the proposed VM-DPC with PC, a comparison study is carried out with the proposed VM-DPC with compensator and other three different control strategies, including the pure VM-DPC and two improved control strategies under unbalanced grid condition: the Dual-loop VOC (D-VOC) [26] and the improved SMC-DPC with power compensation (C-SMC-DPC) [8]. The control bandwidths of the conventional VM-DPC and the PC are 175 Hz and 635

Hz, respectively. The control bandwidth of the inner-loop of D-VOC is chosen as the same value of the VM-DPC with PC. The system is directly connected with a programmed unbalanced grid voltage source with a single-phase voltage drop fault ($v_{s,a} = 0.9$ p.u.) and two-phase voltage drop ($v_{s,b} = 0.8$ p.u., $v_{s,c} = 0.8$ p.u.) set at 3 s and 3.8 s, respectively. It can be observed that both D-VOC and C-SMC-DPC are capable of keeping the stator currents symmetrical with phase-A stator current ($i_{s,A}$) THD = 1.3% and THD = 2.5% under single-phase voltage dip, respectively. These two methods also perform well under a two-phase voltage drop with $i_{s,A}$ THD of 1.4% and 1.5%, respectively. By comparing Fig. 6(c) with Fig. 6(d), it is observed that the pure VM-DPC has the same level of steady-state performance as the conventional VOC under balanced condition, which is better than the SMC-DPC. However, the performance of the original VM-DPC is seriously deteriorated by the unbalanced grid conditions. A single-phase voltage drop is set at 3 s (0.9 p.u.), which generates a negative-sequence component i_s^- , and increases the $i_{s,A}$ THD to 3.4%. By using the proposed VM-DPC with PC, the stator currents are balanced and the corresponding THD of $i_{s,A}$ is reduced from 3.4% to 1.3% under single-phase voltage drop conditions. In addition, the $i_{s,A}$ THD is reduced from 8% to 1.8% under the two-phase voltage drop conditions.

For better illustrations, the peak-to-peak values of the ripples in P_s , Q_s , T_e of four different control strategies under the unbalanced voltage dip conditions, are compared as shown in Fig. 8. The percentages of the ripples are measured based on the peak-to-peak values normalized to their respective values under the standard operating condition. It can be seen that compared to the pure VM-DPC, the proposed method can significantly reduce the ripples in P_s , Q_s , T_e . When the pure VM-DPC is applied, the maximum peak-to-peak value of the ripples in P_s , Q_s and T_e are 0.37 p.u., 0.34 p.u. and 0.66 p.u., respectively under two-phase voltage drop conditions. After the proposed method is employed, the corresponding values drop to 0.14 p.u., 0.14 p.u. and 0.27 p.u., respectively. The results indicate that the proposed method has the same level of steady-state performance as the D-VOC method under unbalanced voltage conditions, but better than the C-SMC-DPC method. The Current Unbalance Factor ($CUF = |i_s^-|/|i_s^+|$) of the four different control strategies are compared as shown in Fig. 7. The results indicate that the proposed method can maintain a symmetrical stator current similar to the D-VOC method, with the lowest CUF value of around 0.02. Fig. 9 shows a comparison of transient response between different control strategies under single-phase voltage drop (0.9 p.u.), which manifest that the VM-DPC with PC provides a smooth active power output with the smallest ripples, and the convergence time is less than 0.05 s. Besides, the C-SMC-DPC has the fastest transient response. Since the D-VOC requires PLL and an outer power loop, the transient response is slower than the other three methods.

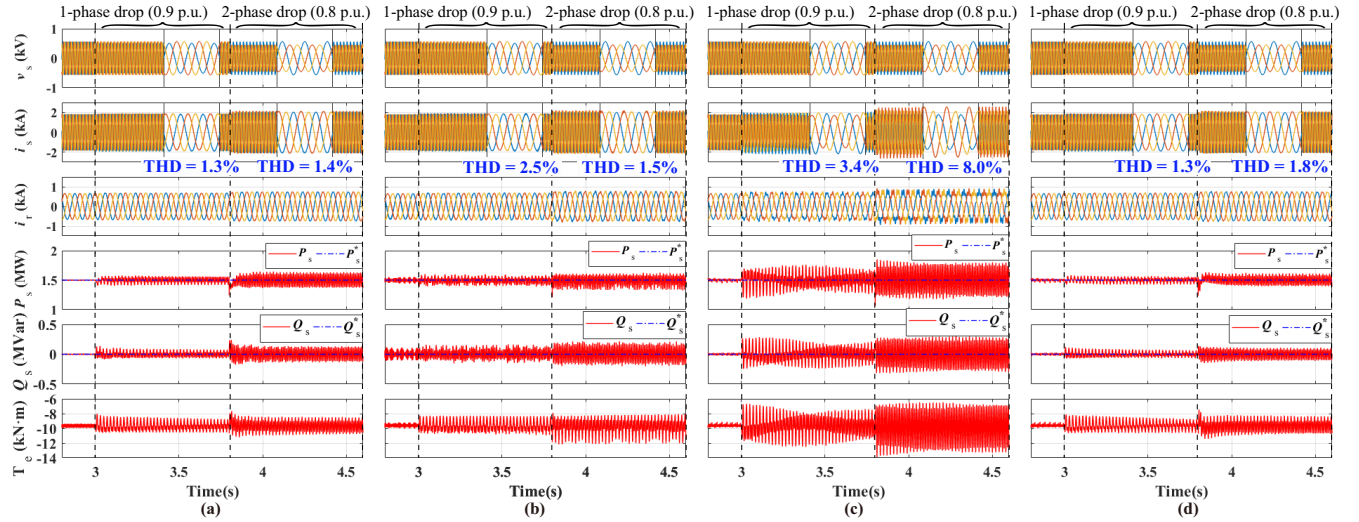


Fig. 6. Comparison of the DFIG performance controlled by four control strategies under unbalanced grid conditions. (a) D-VOC. (b) C-SMC-DPC. (c) Pure VM-DPC. (d) VM-DPC with PC.

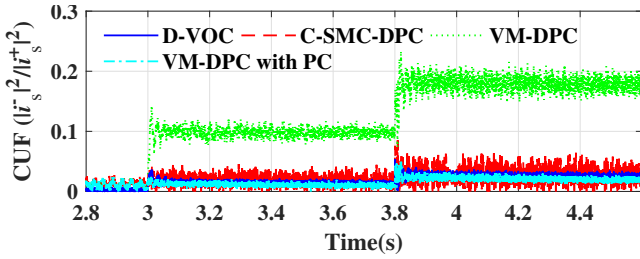


Fig. 7. Comparison of the current unbalanced factor (CUF) using different control techniques under unbalanced grid conditions

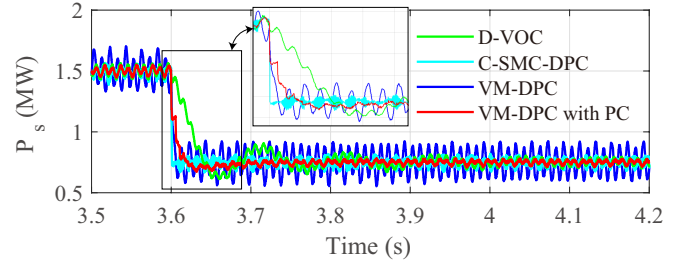


Fig. 9. Comparison of the active power transient performance under single-phase voltage drop (0.9 p.u.) conditions among the four control strategies.

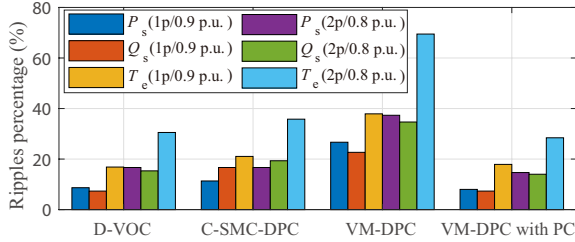


Fig. 8. Comparison of the ripples in P_s , Q_s and T_e under unbalanced grid conditions among the four control strategies.

B. Performance Under Parameter Mismatch and Harmonic Distorted Condition

As described in (9)-(12), the value of generator inductance L_m is required for the VM-DPC. Hence, it is necessary to test the robustness of the proposed method against the generator parameter mismatches. In addition, the DFIG is generally operating under non-ideal harmonic distorted voltage conditions. Therefore, in this subsection, the performance of the proposed method under parameter mismatches and distorted voltage conditions is tested as presented in Fig. 10. At 3.5 s, a phase-A voltage drop (0.7 p.u.) is set. It can be observed that the proposed method is capable of regulating the P_{s22} and Q_{s22} introduced by the unbalanced voltage at 3.5 s, to be zero

within 0.5 s. Since the negative-sequence current is eliminated, the ripples in the powers and the electromagnetic torque T_e , are also largely reduced. Then, the mutual inductance L_m and rotor resistance R_r of the control parameters in the proposed method are increased by 30% at 4 s. It can be seen that there is almost no effect on the control performance. At 4.5 s, the harmonic components are injected into the stator voltages, which increases the stator current THD from 2.7% to 3.6%. However, it is still below the range of the grid requirement [33]. Consequently, the robustness of the proposed method against parameter mismatches and harmonic distortion is verified.

C. Comparison between compensation strategy and PC

In this subsection, the PC performance of regulating the power components P_{s22} and Q_{s22} are discussed in detail. The proposed method is compared to the VM-DPC with a compensation strategy (VM-DPC + C), in which the power reference values are added with the compensation terms, i.e., $P_{s,add}^* = P_s^* + P_{s21}^*$, $Q_{s,add}^* = Q_s^* + Q_{s21}^*$. This improved technique has been widely applied in SMC-DPC and LUT-DPC based techniques [8], [10], [17], [19]. As shown in Fig. 11, a phase-A voltage drop (0.7 p.u.) is set at 3.5 s, which induces large ripples in the stator active and reactive

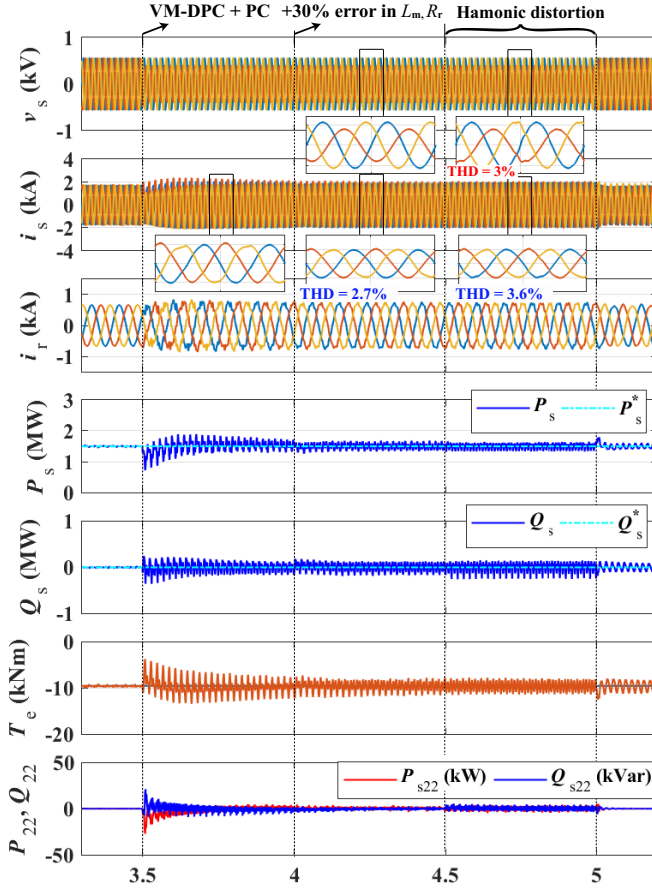


Fig. 10. Robustness of VM-DPC with PC against parameter mismatches and distorted voltage conditions.

powers. Moreover, the negative-sequence component i_s^- and the third-order harmonics i_s^{3+} are also introduced in the stator currents. It can be observed from the bottom of Fig. 11 that the coupling between v_s^+ and i_s^- induces dc components (P_{s22}, Q_{s22}), whereas the coupling between v_s^+ and i_s^- induces (P_{s23}, Q_{s23}) with a frequency of $4\omega_s$. At 4 s, the compensation terms P_{s21} and Q_{s21} are added into the power reference values, which effectively eliminate i_s^{3+} and reduce the current THD from 8.8% to 1.6%. It can be seen that the P_{s23} and Q_{s23} are also largely reduced. However, the VM-DPC with compensation strategy has less influence on (P_{s22}, Q_{s22}), and i_s^- is not reduced, which still introduce (P_{s12}, Q_{s12}) and cause the power fluctuations. At 4.5 s, the proposed method is employed, which balances the stator current by regulating P_{s22} and Q_{s22} to be zero. Since i_s^- is eliminated, the ripples of active and reactive powers are also significantly reduced. However, i_s^{3+} still partially left when using the proposed strategy. The THD of $i_{s,A}$ is 2.6%, which is higher than the compensation strategy, but much lower than the conventional VM-DPC. After 5 s, the PC and compensation strategy are employed simultaneously, which further eliminate i_s^{3+} , but slightly increase the fluctuation of the active and reactive power. Consequently, it can be concluded that the VM-DPC with PC achieves a good balance in the aspects of balancing

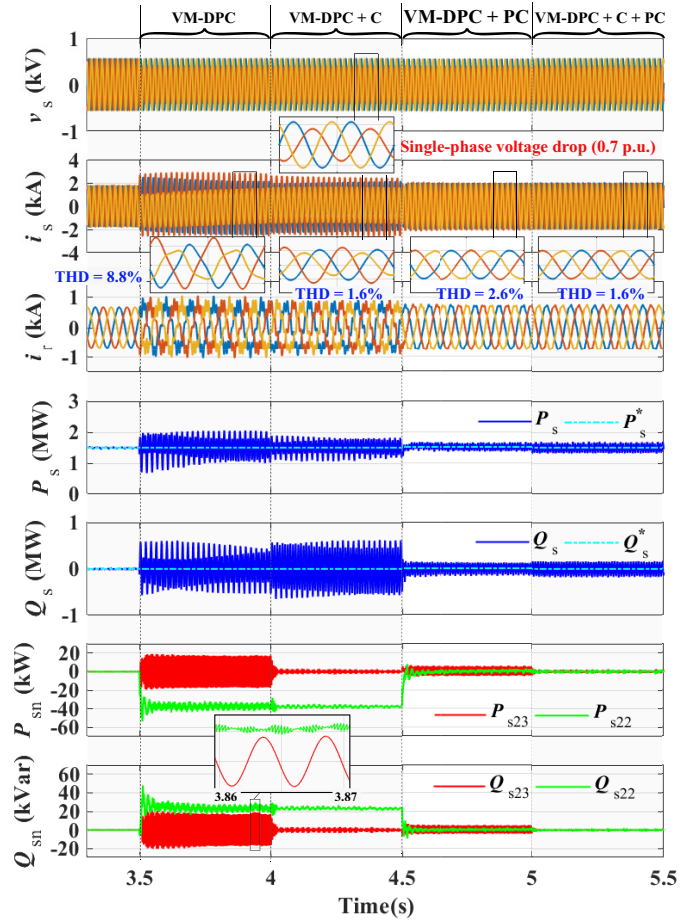


Fig. 11. Performance of the pure VM-DPC, VM-DPC with compensation strategy (VM-DPC + C), VM-DPC with PC (VM-DPC + PC), and the strategy combines two strategies (VM-DPC + C + PC) under phase-A voltage drop (0.7 p.u.) conditions.

the stator current as well as reducing the ripples in active and reactive powers. The potential application of the proposed method with compensation strategy will be studied in future research work.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed control method, an experimental prototype of a 7.5 kW DFIG is tested. The DFIG is connected with a speed-controlled induction machine operating at 1200 rpm (sub-synchronous speed). The control strategies of RSC and the Grid Side Converter (GSC) of the DFIG are implemented in a dSPACE 1006 system. The GSC is controlled as a typical VOC, which is used to support a constant DC-link voltage at 650 V. The sampling frequency is set to 10 kHz, which corresponds to 10 kHz switching frequency of the SVPWM technique. The switching signal of the GSC and RSC are generated by using the DS5101 digital waveform output board. The experimental setup and generic system architecture are shown in Fig. 12. The pure VM-DPC is chosen to be compared with the proposed method in the test platform. The unbalanced grid voltage is generated by the grid simulator. The grid condition with a single-phase voltage drop

TABLE II
 PARAMETERS OF EXPERIMENTAL DFIG PROTOTYPE

Parameter	Symbol	Value	Unit
Rated power	P_{ref}	7.5	kW
Line-to-line Voltage	$v_{s,rms}$	380	V
Dc voltage	v_{dc}^*	650	V
Dc Capacitor	C_{dc}	600	μF
System frequency	f	50	Hz
Sampling frequency	f_a	10	kHz
Switching frequency	f_w	10	kHz
Stator resistance	R_s	0.44	Ω
Stator inductance	L_s	82.7	mH
Rotor resistance	R_r	0.64	Ω
Rotor inductance	L_r	84.6	mH
Mutual inductance	L_m	79.3	mH
Control Parameters			
Parameter	Value	Parameter	Value
K_{rp}	4000	K_{ri}	20000
$K_{rp,n}$	100	$K_{ri,n}$	5000
K_s	0.0059		

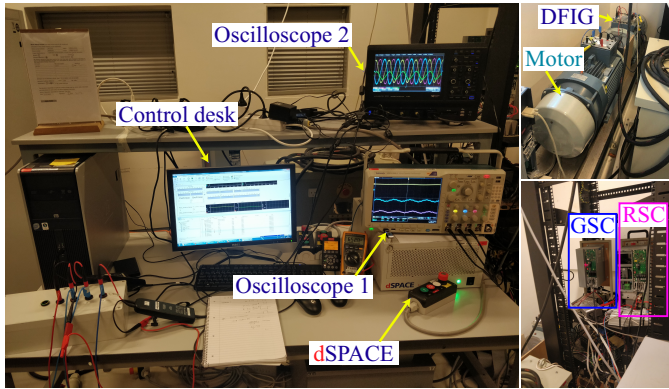


Fig. 12. (a) Experimental setup to test DFIG with the proposed control method using dSPACE. (b) Generic system architecture.

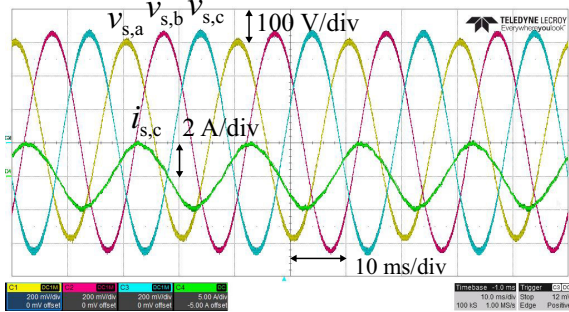
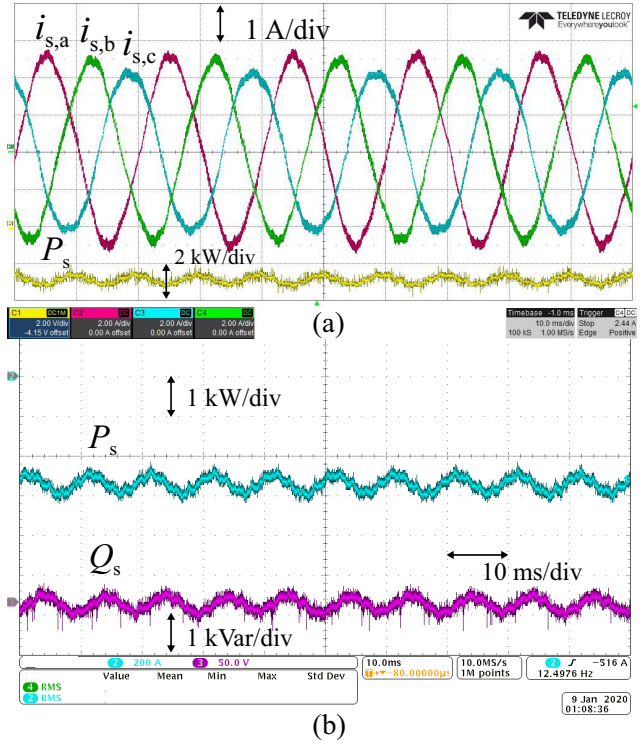

 Fig. 13. Voltage generated by the grid simulator with single-phase voltage drop ($v_{s,a} = 0.9$ pu) and the phase-C current behavior of the pure VM-DPC.


Fig. 14. The steady-state performance of the pure VM-DPC under 10% single-phase voltage drop condition. (a) Stator currents and active power performance. (b) Active and reactive power performance.

(0.9 pu), and the phase-C current behavior of the pure VM-DPC, are shown in Fig. 13. The results are presented as two parts, i.e. part.A is to illustrate the improvements of the steady-state performance of the VM-DPC with parallel compensator compared to the pure VM-DPC under unbalanced grid condition; part.B is to present the power transient response of the proposed control method under unbalanced grid conditions.

A. Steady-State Performance Under Unbalanced Grid Condition

In order to test the steady-state performance of the two control strategies, the active and reactive power reference values are set to $P_s^* = 2.3$ kW and $Q_s^* = 0$ kVar, respectively. Fig. 14 shows the stator currents of the system using the pure VM-DPC is sinusoidal but asymmetrical. There are also ripples having twice the fundamental frequency in both active and reactive powers with the peak-to-peak values of about 0.6 kW.

The improvements of the VM-DPC with PC under unbalanced voltage condition are confirmed as shown in Fig. 15. The CUF values carried out with two strategies are compared, as shown in Fig. 16, which indicates the VM-DPC with PC successfully reduces the unbalance of the stator currents and decreases the CUF value from about 0.08 to 0.02. The ripples in the active and reactive powers are significantly reduced, which are in accordance with the simulation results. Besides, the THD value of the stator currents has been reduced from 4.67% to 4.22% as shown in Fig. 17. Therefore, it can be concluded that the improvements by adding the compensator

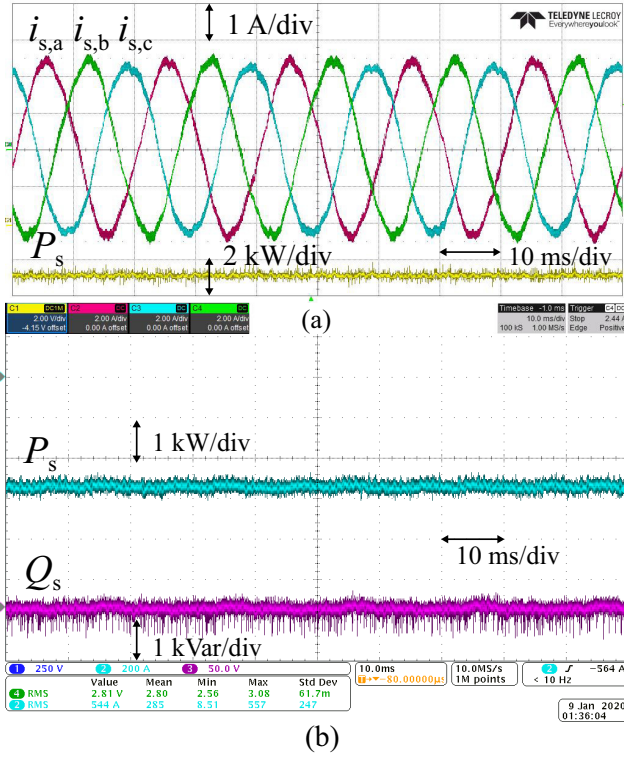


Fig. 15. The steady-state performance of the VM-DPC with parallel compensator under 10% single-phase voltage drop condition. (a) Stator currents and active power performance. (b) Active and reactive power performance.

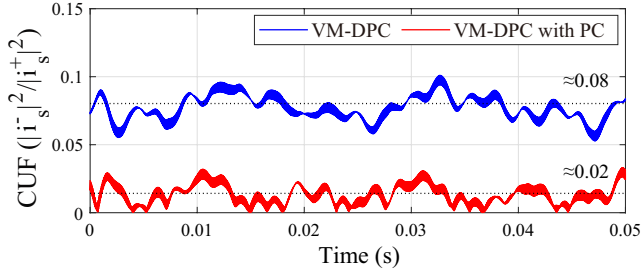


Fig. 16. Comparison of the current unbalanced factor (CUF) using VM-DPC and VM-DPC with PC under unbalanced grid conditions at 2.3 kW operation.

compared to the pure VM-DPC under unbalanced grid condition are obtained.

B. Transient Response Under Unbalanced Grid Condition

When an unbalanced grid fault occurs, the DFIG should respond and regulate its output active and reactive power in terms of the grid requirements. For that purpose, the control strategy should provoke the power responds of DFIG in a fast and smooth manner. Therefore, the power transient response of the proposed control method under unbalanced voltage condition is tested in this section. The output power of DFIG is zero at the beginning. Fig. 18 shows that when the active power reference P_s^* changes to 2.3 kW, the proposed VM-DPC with PC reaches steady-state within 10 ms with a small

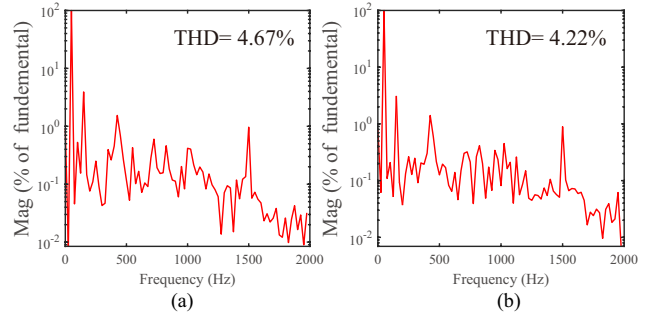


Fig. 17. Stator current harmonic spectrum at 2.3 kW operation. (a) VM-DPC. (b) VM-DPC with PC.

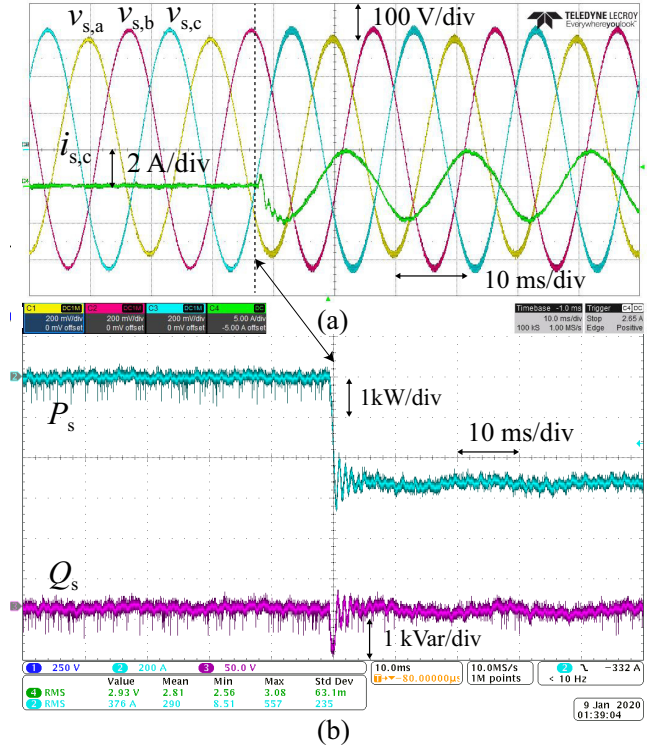


Fig. 18. The transient performance of the proposed VM-DPC with parallel compensator under 10% single-phase voltage drop condition. (a) Voltage conditions and phase-C stator current performance. (b) Active and reactive power performance.

overshoot and small ripples. Consequently, it can be concluded that the proposed control method is suitable for quick dynamic response in DFIG under unbalanced voltage condition.

V. CONCLUSION

In this paper, a newly-designed VM-DPC with PC for RSC was presented. The method has a simple structure, which does not require PLL or measurements of the rotor side currents. The pure VM-DPC guarantees a satisfying transient and steady-state performance under balanced grid conditions, while the newly-designed additional compensator considerably enhances the control performance of the pure VM-DPC under unbalanced grid conditions by dynamically regulating the negative-sequence current in a closed-loop

structure. Simulation results show that the proposed method is capable of ensuring the balanced and sinusoidal stator currents as well as reducing the ripples in both the powers and the electromagnetic torque. The robustness of the proposed method against generator parameter mismatches and harmonic distorted voltage conditions are also verified. A comparison between the proposed method and the compensation strategy shows that the VM-DPC with PC achieves a good balance between reducing the stator current unbalance and restraining the power ripples. The experimental results further verify the obvious improvements of the proposed method compared to the pure VM-DPC. Moreover, the experimental results show the system using the proposed method still obtains a fast and smooth power transient response under unbalanced grid conditions. The results indicate the application of the proposed control method for quick dynamic response scenarios under unbalanced grid conditions as well as in steady-state. Our future perspective includes further investigation on the improvements of the sequence components separation techniques under frequency variation conditions and a combination of the proposed method with the compensation strategies.

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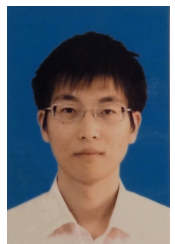


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