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SINGLE STAGE GRID CONVERTERS FOR BATTERY ENERGY STORAGE

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Abstract

Integration of renewable energy systems in the power system network such as wind and solar is still a challenge in our days. Energy storage systems (ESS) can overcome the disadvantage of volatile generation of the renewable energy sources. This paper presents power converters for battery energy storage systems (BESS) which can interface medium-voltage batteries to the grid. Converter topologies comparison is performed in terms of efficiency, common mode voltage and redundancy for a 6kV series connected medium voltage batteries with a nominal power of 5MVA to act as a battery charger/discharger.

1 Introduction

The increase of solar and wind systems in the recent years is exponential. The disadvantage of these energy sources, especially for wind farms, is the wide fluctuation of output power depending on the weather conditions. This power variation is reflected in voltage fluctuations on the load bus [1]. To overcome this, storage systems connected to the electricity grid can smooth the output power of wind farms by acting as a load/generator improving the grid stability and power quality. BESS represent a versatile solution for storage with high efficiency, high power, long energy demands and fast response.

In order to connect BESS to the grid, different power converter topologies are available. Basically the classification can be done in two main groups: single-stage and two-stage. Two-stage topologies with intermediary DC/DC converter, shown in Fig.2, decouple the batteries from the DC/AC conversion stage and this brings benefits to batteries. However, the conversion efficiency is decreased due to the losses in the DC/DC converter. Therefore using single stage topologies, shown in Fig.1, where the batteries are directly connected to the inverter DC-Link, the efficiency can be increased. This improvement in efficiency brings the disadvantage of having a floating voltage in the inverter DC-Link dependent on the batteries characteristic. As a consequence, the battery pack nominal voltage must be dimensioned somewhat higher to be able to inject current in the grid until the batteries are completely discharged.

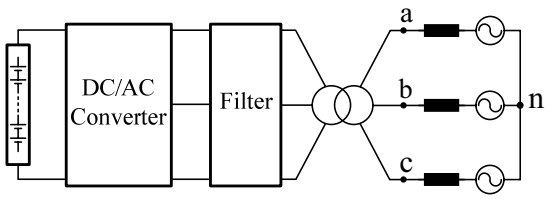

Fig.1. Single stage grid converter topology

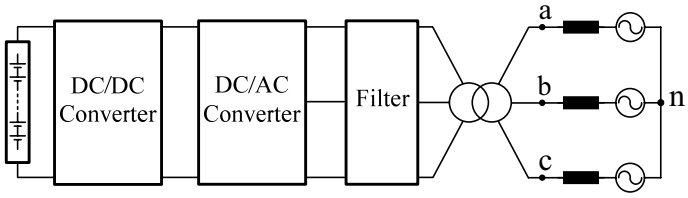

Fig.2. Two stage grid converter topology

For low voltage storage applications, the classical two-level converter is the most efficient and the most used topology [2]. Its control simplicity it's outstanding but has important drawbacks like: common mode voltage up to half of the DC-Link voltage, high switching frequency operation to comply with harmonic standards. When the operating voltage is increased, this topology requires series connected power semiconductors and the topology is not interesting anymore. For medium voltage, the multilevel converters are the key technology.

Multilevel converters represent a smart way to connect power semiconductors in series, decreasing the voltage ripple and the output harmonic distortion as well as the common mode voltage. To achieve equivalent voltage spectrum with the two-level converter the switching frequency is decreased, therefore these converters are more suitable for applications where high currents are switched. The first two topologies were introduced by Baker in 1975 the Cascaded H-Bridge (CHB) converter [3], followed by Neutral Point Clamped (NPC) converter in 1980 [4]. On the same principle but clamping capacitors in stead of diodes the Flying Capacitor (FC) converter was introduced in 1992 [5]. An improved version of NPC converter was introduced in 2001, Active Neutral Point Clamped (ANPC) converter [6]. Various hybrid topologies were lately introduced, based on the main concepts presented above one of the most important ones being the five-level ANPC [7]. This paper is focused on the CHB, NPC, ANPC and FC converters.

2 Converters Specifications

Table 1 summarizes the number of components and their voltage ratings for a converter designed to achieve the line voltage of V_{DC} for the considered converter topologies. The voltage ratings for transistors and diodes represent their nominal blocking voltage.

For the next design steps, 3L-NPC, 3L-ANPC, 3L-FC and the 5L-CHB topologies will be considered, see Fig.3-7. The choice is justified considering the number of passive and active components, capacitors voltage balancing, silicon utilization and control complexity [8].

Considering the imposed parameters from Table 2, the converter necessary dc-link voltage has to be established.

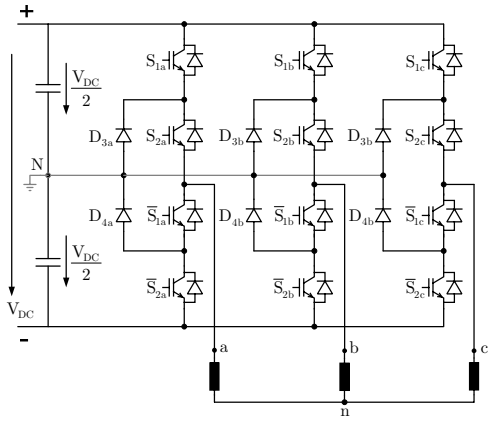

Fig.3. Three-level NPC converter (3L-NPC)

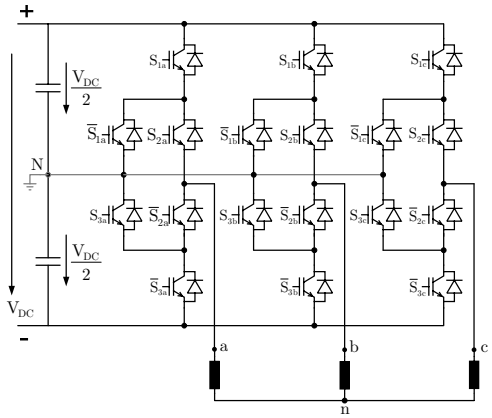

Fig.4. Three-level ANPC converter (3L-ANPC)

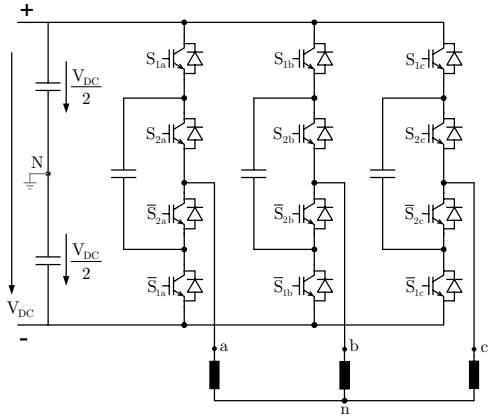

Fig.5. Three-level FC converter (3L-FC)

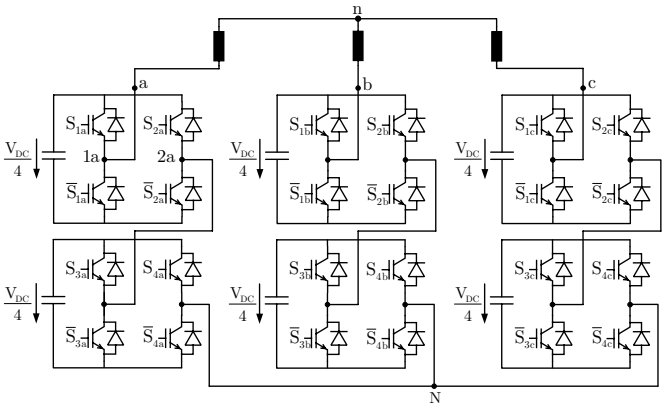

Fig.6. Five-level CHB converter (5L-CHB)

Converter Type and Levels		*Switches*	*Clamped Diodes /Flying Capacitors*	*DC-link Capacitors*	*Isolated DC Sources*
CHB	3L	12-V_{dc}/2	-	3-V_{dc}/2	3-V_{dc}/2
	5L	24-V_{dc}/4	-	6-V_{dc}/4	6-V_{dc}/4
	7L	36-V_{dc}/6	-	9-V_{dc}/6	9-V_{dc}/6
NPC	3L	12-V_{dc}/2	6-V_{dc}/2	2-V_{dc}/2	1-V_{dc}
	4L	18-V_{dc}/3	12-2V_{dc}/3	3-V_{dc}/3	1-V_{dc}
	5L	24-V_{dc}/4	36-V_{dc}/4	4-V_{dc}/4	1-V_{dc}
ANPC	3L	18-V_{dc}/2	-	2-V_{dc}/2	1-V_{dc}
	5L	12-V_{dc}/4 12-V_{dc}/2	3-V_{dc}/4	2-V_{dc}/2	1-V_{dc}
FC	3L	12-V_{dc}/2	3-V_{dc}/2	2-V_{dc}/2	1-V_{dc}
	4L	18-V_{dc}/3	3-V_{dc}/3 3-2V_{dc}/3	2-V_{dc}/2	1-V_{dc}
	5L	24-V_{dc}/4	3-V_{dc}/4 3-V_{dc}/2 3-3V_{dc}/4	2-V_{dc}/2	1-V_{dc}

Table 1: Multilevel converters necessary components

Nominal grid line voltage	10/20 kV
Nominal line frequency	50 Hz
Output transformer	10/20 kV to 4.16 kV
Nominal converter line voltage	4.16 kV
Power rating	5 MVA
Nominal converter line current	694 A
Power factor	$0.95_{leading} - 0.95_{lagging}$
Harmonics according to	EN 61000

Table 2: Converter imposed basic parameters

In single stage topologies the converter dc-link voltage has to withstand the batteries voltage variations and has to adapt the charging and discharging voltage according to the battery state of discharge. The voltage charge and discharge characteristics depend on the battery technology.

Lead-acid batteries will be considered, this being a mature technology presenting satisfactory performances for a low price. For this battery technology the voltage variation is

about 15% per cell depending on the state of charge [9]. Thus, the battery voltage taken when the discharge is completed will define the number of batteries in the system in order to be able to inject the nominal power in grid, this being given by:

$$V_{bat,min} = \sqrt{2} \cdot V_{LL,PCC} = \sqrt{2} \cdot 4.16 = 5.88\,kV \quad (1)$$

The voltage drop on the grid impedance, this will not be considered for now since the HV to MV transformers introduced impedance is around 1mΩ [10]. The sum of the transformers introduced impedance, which is mostly inductive, will be further considered to determine the necessary filtering to comply with the considered standard harmonic distortion limits.

Considering an increased voltage at full charge of about 15%, and a necessary safety margin of 10%, results the maximum dc-link voltage:

$$V_{DC,max} = 1.25 \cdot \sqrt{2} \cdot V_{LL,PCC} = 7.35\,kV \quad (2)$$

Thus, for the considered three-level topologies the dc-link voltage will be imposed by the battery voltage and the modulation index has to adapt the output voltage in order to charge or discharge the batteries. For this purpose, the space vector pulse width modulation (SVPWM) is considered to have the best utilization of the DC-Link. A maximum theoretical modulation index close to 1.15 is imposed when the batteries are almost completely discharged.

Unlike the three-level topologies, the CHB topology divides the battery bank voltage in 4 to be used for each converter cell. This is a good advantage for this topology; lower voltage devices can be used and a redundant cell can improve the converter reliability. However, disadvantages arises when the batteries are connected to the H-Bridge cell, the 2nd harmonic ripple is seen at the batteries terminals through the cell capacitor [10].

3 Semiconductors Specifications

The amount of silicon in the converter design is a trade off which takes into consideration the total installed switch power, converter losses and desired converter lifetime. In Table 3 the semiconductors specifications are summarized. The selection was based on the available modules available on the market which comply with the converter requirements.

	3L-NPC	3L-ANPC	3L-FC	5L-CHB
$V_{DC,max}$	7350V	7350V	7350V	1837V
$V_{CE,n}$	6500V	6500V	6500V	3300V
$V_{com,max}$	3675V	3675V	3675V	1835V
$I_{C,n}$	750A	750A	750A	800A
$V_{CE(sat),typ}$	4.3V	4.3V	4.3V	3V
S_S [MVA]	73.125	87.75	58.5	63.36

Table 3: Semiconductors specifications ($T_{j,max} = 125°C$, $T_h = 80°C$, $S_C = 5MVA$, $I_{n,rms} = 694A$, $f_{sw,max} = 1050Hz$)

Thus, for the 3L-NPC, 3L-ANPC and 3L-FC converters the 6.5kV IGBT (FZ750R65KE3) from Infineon was considered with a nominal current of 750A and the 3.3kV IGBT (FZ800R33KL2C) for the 5L-CHB converter with a nominal current of 800A. In the ideal case the required devices current rating for the considered topologies will differ for the four quadrant converter operation, therefore the differences will show a different loss distribution and magnitudes for the restricted ratings.

The devices deadtime considered for the most critical fall times were chosen to be 8µs for the 6.5kV IGBTs and 5µs for the 3.3kV IGBT's.

Considering the present application the switches overrating is not desired. The system lifetime is limited by the battery technology which is expected to last for 1 to 4 years depending on the usage [12]. The total installed switch power (S_S) is given in equation (3), for *n* IGBT modules (transistors with recovery diodes) and *m* diodes which are considered with a typical half silicon area of the IGBTs:

$$S_S = V_{CE,n} \cdot I_{C,n} \cdot n + 0.5 \cdot V_{RRM} \cdot I_{F,n} \cdot m \quad (3)$$

4 Design of passive components

4.1. Output filter design

The L output filter will be considered in this study to determine the necessary current ripple reduction for the output current to comply with the maximum 8% THD imposed by the EN 61000-2-4 over the entire operation range. The ripple current is defined by [13]:

$$\Delta I = \frac{1}{n} \cdot \frac{V_{DC}}{L \cdot f_{sw}}, \quad (4)$$

where the factor n varies with the number of output voltages, 2 for two-level, 4 for three-level and 6 for five-levels.

The grid impedance has to be considered as well, and it can be estimated by the 20kV to 4.16kV short-circuit impedance calculated with:

$$z_k = \frac{v_k \cdot V_1}{\frac{S_n}{\sqrt{3} \cdot V_2} \cdot n^2}, \quad (5)$$

where V_1 is the primary winding voltage (4.16kV), V_2 secondary winding voltage (20kV), v_k the short circuit voltage, S_n the nominal power and n the transformation ratio.

Assuming a 5% short-circuit voltage, the short-circuit impedance is 12.76mΩ. Thus, considering also the HV to MV transformer impedance of around 1mΩ and a typical R/X ratio of 0.1 the grid inductance for 50Hz grid is found to be $L_g = 43.58\,\mu H$.

Taking the most critical operation point ($V_{DC,max}$), and choosing the converters switching frequency, the necessary filtering inductances are presented in Table 4. It can be noticed that the CHB has the smallest necessary filtering inductor while keeping the installed power smaller than NPC.

Topology	3L-NPC	3L-ANPC	3L-FC	5L-CHB
f_{sw}	1050 Hz	550 Hz	1050 Hz	550 Hz
L_f	1230 µH	3250 µH	1720 µH	980 µH

Table 4: Necessary filtering for $THD_{max} = 8\%$

4.2. Design of Flying-Capacitors

The flying capacitors size is inverse proportional with the commutation frequency, this being the main drawback of this topology. Even if the converter output frequency is doubled compared with the switching frequency like in ANPC converter [14], the switching frequency has to be kept high enough to minimize the capacitance. The capacitors size is approximated with the following equation:

$$C = \frac{I_{ph,rms}}{p \cdot \Delta V_C \cdot f_{sw}}, \qquad (6)$$

where p is the number of flying capacitor cells, and ΔV_C is the maximum voltage ripple. Thus, for a maximum ripple of 10% of the maximum capacitor voltage $V_{DC,max}/2$, the calculated capacitance is 900µF.

5 Simulation Results

The modulations strategies were implemented in Matlab/Simulink, and the power circuit including the thermal model were implemented using PLECS blockset under the same programming environment. The SVPWM technique was used, with level-shift for NPC and phase-shift for the other topologies.

In Fig.7. the output voltages for the 3L-NPC converter are presented for the considered switching frequency of 1050Hz, the same frequency as the output voltage. The advantage of the level-shift PWM over the phase-shift PWM can be noticed by comparing the output line voltage with 3L-ANPC and 3L-FC, Fig.8 and Fig.9, where the ripple is minimized to $V_{DC}/2$. This will lead to a smaller output filter as seen in Table 4. An increased common mode voltage is observed, going up to $V_{DC}/3$ compared to $V_{DC}/6$ in Fig.8.(e) and Fig.9.(e). This will result in higher common mode currents during switching dead times.

Using the phase-shift PWM for the ANPC converter it's possible to double the apparent switching frequency of the output voltage [14], thus a reduction of switching frequency is possible similar with the 3L-FC converter both of the converters having two bidirectional paths for 0V switching state. This improvement is achieved with the expense of having a line voltage ripple up to V_{DC}, and the necessary output filter increasing as well. This can be observed in Fig.7.(d), the phase voltage found at he load terminals which is the phase to neutral voltage without the common mode voltage ($V_{aN} - V_{nN}$).

For the 5L-CHB controlled at 550Hz, similar control strategy is applied phase-shifting the carrier with 180 degrees as well as the carriers. The result in terms of line voltage ripple is as well as the FC and the ANPC converters, but with a higher output redundancy which leads to the smallest output filter.

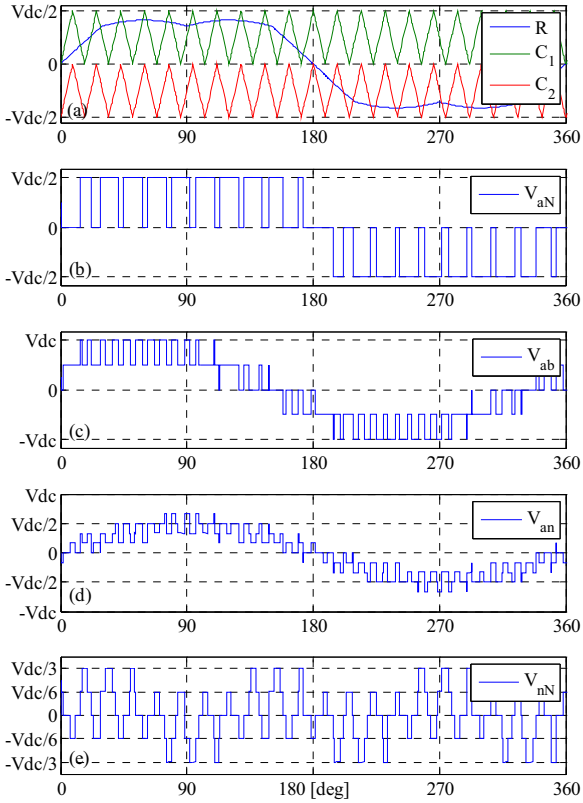

Fig.7. 3L-NPC output waveforms: (a) reference and carriers signals; (b) phase to neutral point voltage; (c) line to line voltage; (d) phase voltage; (e) common mode voltage

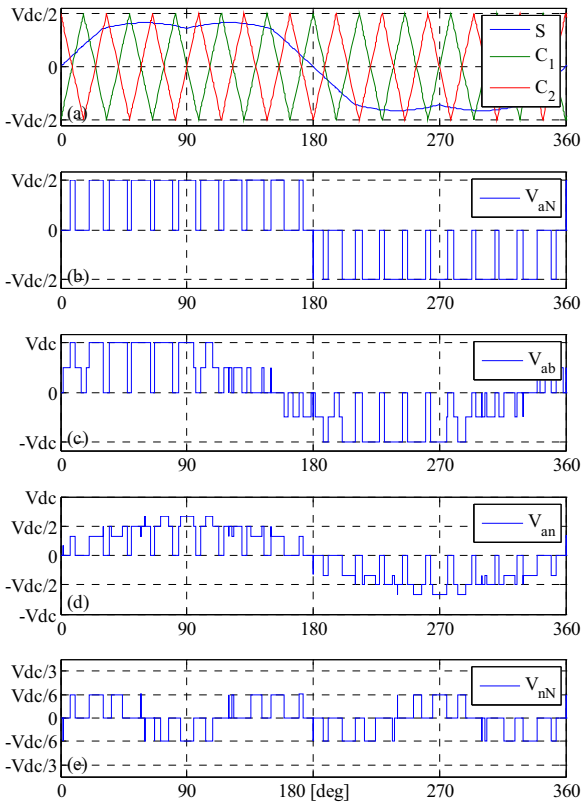

Fig.8. 3L-ANPC output waveforms: (a) reference and carriers signals; (b) phase to neutral point voltage; (c) line to line voltage; (d) phase voltage; (e) common mode voltage

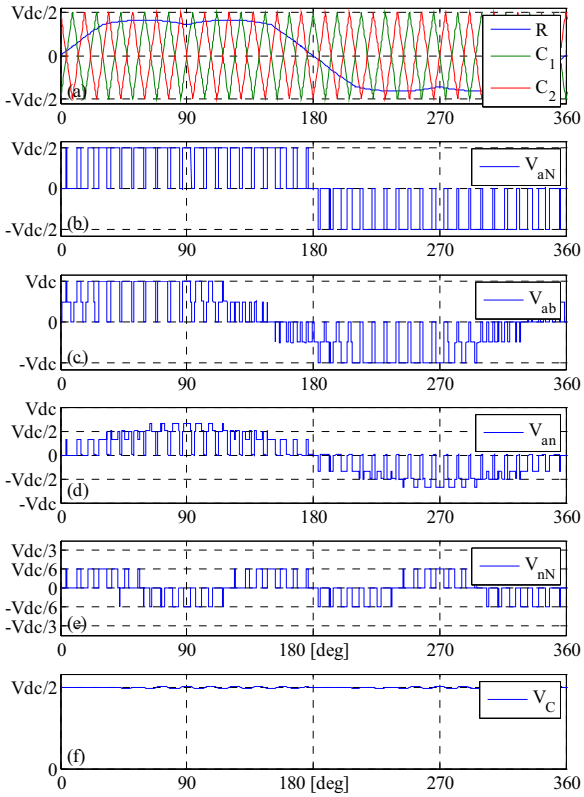

Fig.9. 3L-FC output waveforms: (a) reference and carriers signals; (b) phase to neutral point voltage; (c) line to line voltage; (d) phase voltage; (e) common mode voltage; (f) flying capacitor voltage

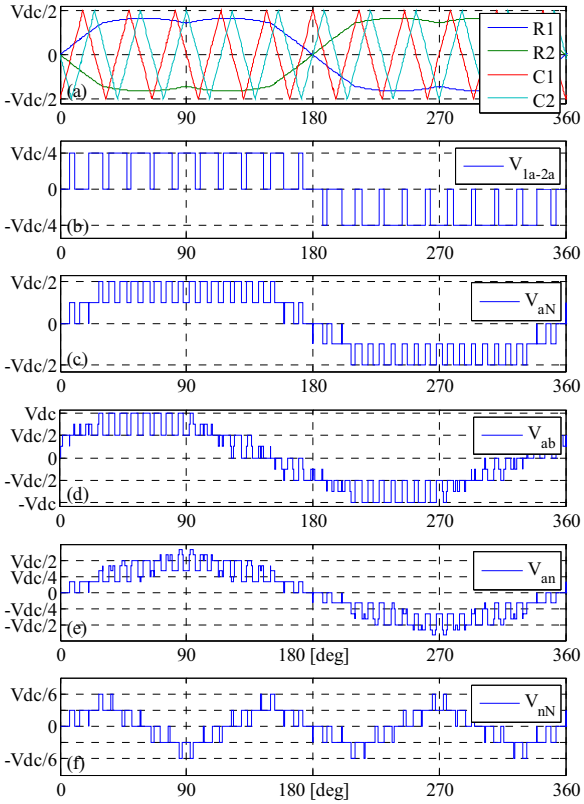

Fig.10. 5L-CHB output waveforms: (a) references and carriers signals; (b) cell output voltage; (c) phase to neutral voltage; (d) line to line voltage; (e) phase voltage; (f) common mode voltage

The converters losses were simulated for unity power factor, with the loss distribution presented in Fig.11-14, over the entire DC-Link voltage variation at nominal current.

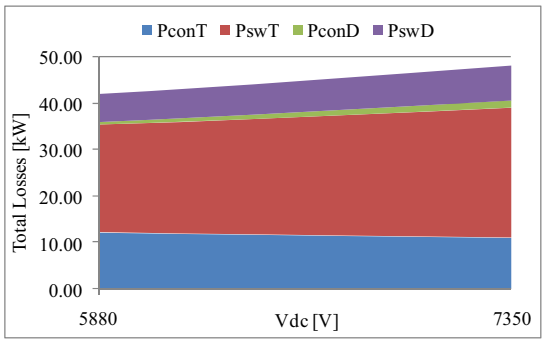

Fig.11. 3L-NPC losses @ f_{sw}=1050Hz, THD_{max}=8%

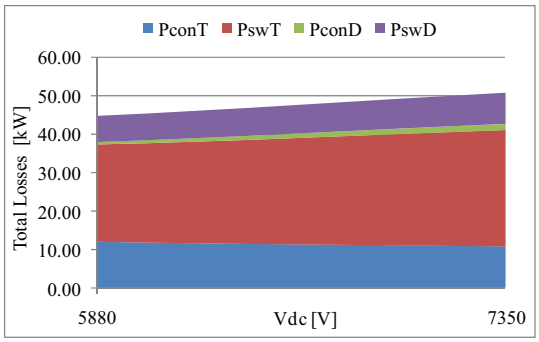

Fig.12. 3L-ANPC losses @ f_{sw}=550Hz, THD_{max}=8%

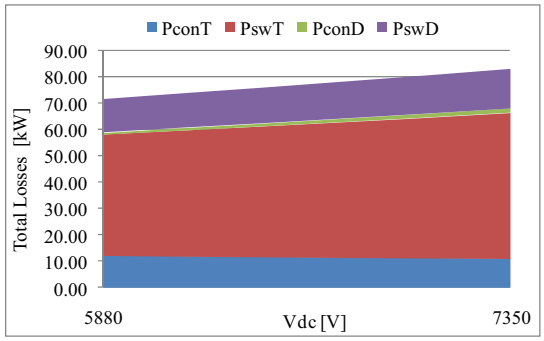

Fig.13. 3L-FC losses @ f_{sw}=1050Hz, THD_{max}=8%

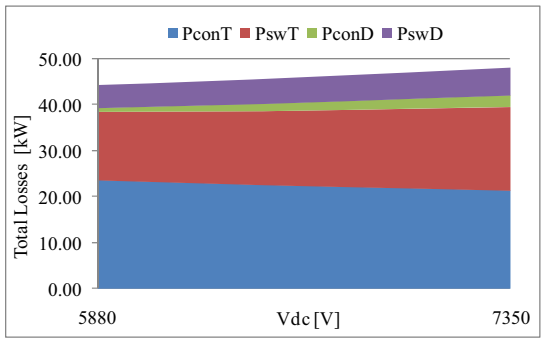

Fig.14. 5L-CHB losses @ f_{sw}=550Hz, THD_{max}=8%

Increased switching losses for the 3L-FC converter are noticed, the average switching frequency is higher to achieve the doubled output frequency, for the same silicon area as the other three-level converters. The loss distribution for an average DC-Link voltage is presented in Fig.15. NPC converter is shown as the most efficient topology with losses

in silicon of 0.91%. However, the loss distribution is unequal, the heat sink temperature being different among switches [6]. CHB converter with 0.93% silicon losses is interesting considering the small required output filter, but it requires a large number of gate drives and control signals.
The small installed switch power of the FC converter is paid in an increased switching loss, while in the case of ANPC converter the additional reactive power delivered to the filter inductor increases the switching losses, with a total of 0.96%.
The harmonic distortion variation is shown in Fig.16, for nominal output current. It must be noticed that for light load conditions, e.g. 10%, the distortion goes up to 38%.

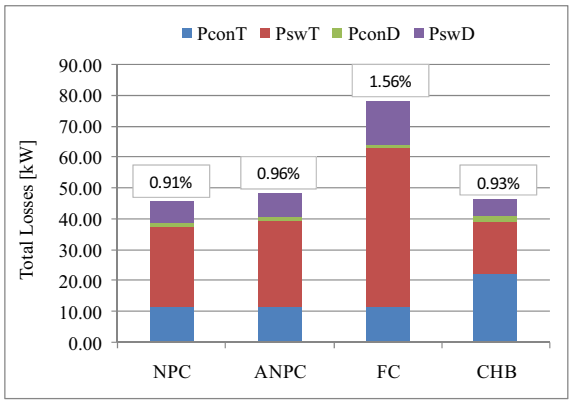

Fig.15. Converters loss distribution

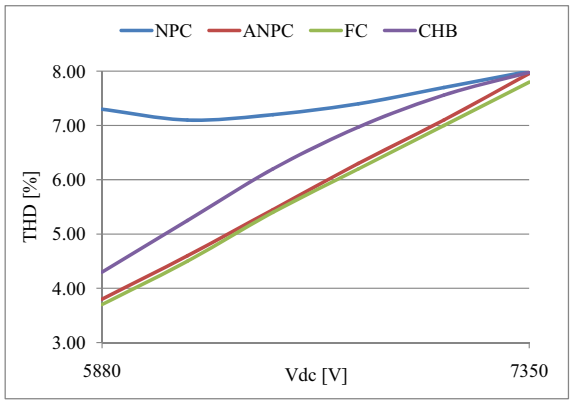

Fig.16. THD over the entire DC-Link voltage variation

6 Conclusion

Single stage converters for direct connection of medium voltage batteries to the grid were presented. The design of a 5MW converter module to achieve an AC output voltage of 4.16kV was presented using four different multilevel topologies based on 6.5- and 3.3-kV IGBT modules. The 3L-NPC, 3L-ANPC, 3L-FC and 5L-CHB converters were compared in terms of efficiency, common mode voltage and output redundancy at nominal output current over the entire voltage variation.

Acknowledgements

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