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Reinforcing Fault Ride Through Capability of Grid Forming Voltage Source Converters Using an Enhanced Voltage Control Scheme

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***Abstract*—Medium power distributed energy resources (DERs) are commonly connected to medium voltage distribution systems via voltage source converters (VSCs). Several guidelines and standards have been developed to establish the needed criteria and requirements for DERs interconnections. In this respect, it is preferred to reinforce the VSC fault ride through (FRT) capability, which considerably minimizes the DG outage period and reconnection time and results in a resilient system against short circuits. Considering the significant number of asymmetrical faults in distribution systems, the VSC response in such conditions must be investigated, and consequently, its FRT capability must be reinforced. In this paper firstly a comprehensive review on existing FRT methods has been presented and discussed. Accordingly, an adaptive virtual impedance-based voltage reference generation method is proposed, which enhances the VSC behavior under short circuits and increases the VSC FRT capability. Also, a fast sinusoidal current reference limiter is proposed to improve the performance. To evaluate the performance of the proposed scheme, state space analysis is presented, and a complete set of simulations is performed in PSCAD/EMTDC environment. Also, a comparison with the conventional method is presented.**

***Index Terms*—Asymmetrical short circuit fault, current reference limiter, distribution system, fault ride through, grid forming converters, voltage source converters, voltage controller.**

I. Introduction

VOLTAGE source converters (VSCs) are the most commonly used power electronic interfaces for the interconnection of distributed energy resources (DERs) to power grids, which provide fast dynamic, full controllability, and high efficiency [1]. Generally, two main operating modes of "grid feeding" and "grid forming" are categorized in the literature for electronically connected DERs (EC-DERs) [2]. In a grid forming option, the VSC is responsible for controlling its output voltages and frequency, which realizes the island operation of the system when the main grid is disconnected, namely islanded microgrid (MG) [3]. Conceptually, working in a voltage control mode makes the VSC vulnerable under overload conditions. For this reason, the output currents of the VSC are limited to typically 125% of its nominal value, which protects the power electronic switches under overload conditions [4]. However, VSCs generate distorted voltages under asymmetrical short circuit faults. This behavior along with related power quality standards such as IEEE std. 1547 require disconnection of the VSC when a short circuit occurs in the system. This is an undesirable characteristic in the distribution systems (DSs), which are exposed to many asymmetrical short circuit faults [5, 6]. In order to assure fault-resiliency for the system and to avoid any unnecessary disconnection of the electricity and the VSC outage, the VSC should effectively ride through these asymmetrical faults. In the following paragraphs, an overview on the subject of FRT for different applications is presented.

The term fault ride through (FRT) is firstly introduced for doubly fed induction generator (DFIG)-based wind turbine generators (WTGs) in which the grid faults threat their functionality and performance [7-10]. There is another kind of study related to FRT for photovoltaic (PV) systems. For these systems, avoiding overvoltage in the DC link and supporting the grid to recover the voltage by means of reactive power injection are the two concerns in short circuit conditions [11-13]. The researches in this topic also cover the single phase PV systems [14, 15]. Regarding the control of grid feeding converters (single-phase and three-phase), which covers both the photovoltaic and wind energy systems, extensive studies have been done in the literature under grid faults. The control of active and reactive powers in such conditions is the main purpose of these researches [16, 17]. In this respect, active power corresponds to DC link voltage control, while reactive power supports the grid voltages under short circuit condition [18]. The proposed methods in the aforementioned categories do not address the FRT issue for grid forming VSCs. In the following, related studies have been reviewed.

Regarding the grid forming VSCs operation under unbalanced condition, the existing methods can be categorized into two parts. i) Control methods such that grid forming VSCs can feed the necessary unbalanced currents of loads. This goal can be achieved by improving the voltage and current control loops of VSC [19]. ii) Sharing the unbalanced current of loads among the VSCs. Depending on the adopted criteria for current sharing, different methods have been proposed in the literature [20, 21]. The suggested methods in these topics cannot be effective for a severe unbalance condition such as asymmetrical short circuit faults.

Since the grid forming VSC controls the output voltages, it tends to increase the voltage by increasing the output current in case of short circuits. Considering the limited permissible current of switches, the current limiter is activated in this condition. In this respect, different approaches have been presented to improve the VSC behavior under a short circuit condition. For the sake of simplicity, hereafter "VSC" is referred to as "grid forming VSC".

Regarding the FRT of a VSC, the existing methods can be divided into two main categories: Strategy I) Using the conventional control scheme with instantaneous limiting

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strategy, Strategy II) switching to another control mode and control system. The first strategy keeps the main controller active during a fault, however the distorted waveforms cause power quality issues. In the second strategy, the poor power quality is avoided by using another control mode, however, it requires to change the control system and to switch the operation mode. Also, fault inception and clearance instances detection is needed. For the sake of conciseness, the description and review of these two strategies have been presented separately in section II.

Studying the literature shows that there is a lack of comprehensive and analytical studies on FRT of grid forming VSCs at the medium voltage level. In this paper, a comprehensive review on FRT of grid forming VSC and comparative explanation have been presented. Also, a fundamental and thorough analysis on this issue is provided. Accordingly, an adaptive virtual impedance-based voltage reference generation method is proposed, which reinforces the VSC behavior under short circuit conditions and enhances its FRT capability. The main idea behind the proposed method is that the voltage references in $\alpha\beta$ frame are adaptively reduced such that the current references and correspondingly the output currents are limited to safe values, besides that pure voltages and currents waveforms are generated and the power quality is improved. Further, a fast sinusoidal current reference limitation approach is proposed to improve the performance. To evaluate the stability of the proposed method and to calculate a proper value for the virtual impedance, state space modeling of the system with the proposed method is presented. Comparing to the existing methods in the literature, it should be noted that the proposed strategy adaptively controls the voltages without any need to detect fault occurrence and clearance instances, and there is no need to switch between different operating modes. Furthermore, the proposed control method is effective regardless of the type, severity, and location of the faults.

The rest of the paper is organized as follows. Section II presents an overview of the existing FRT methods of grid forming VSCs. In section III, the basics of the VSCs conventional control are presented. Also, the VSCs behavior under asymmetrical fault conditions are studied. In section IV, the proposed voltage control scheme is presented. Finally, simulation results and a conclusion of the work are presented in sections V and VI, respectively.

II. Existing FRT Methods of Grid Forming VSCs

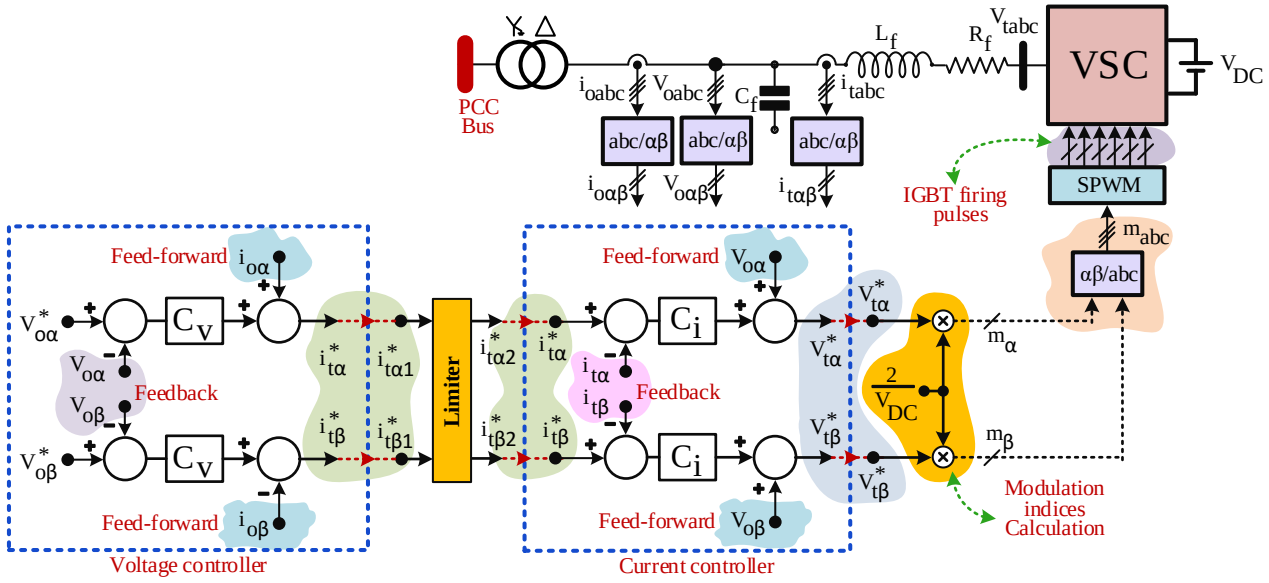
As mentioned in the previous section, there are two general strategies regarding the FRT of grid forming VSCs. In this section, both strategies have been reviewed. Also, a comparative explanation is given at the end of this section.

In the first category, the conventional voltage controller remains unchanged, and an instantaneous current limiting strategy is employed on the current references to protect the VSC switches. An instantaneous current limitation approach is implemented by a simple hard limiter in which the limiter output is held within a limit boundary when the input goes beyond the boundary [22]. The simple form of this method can be used for control structures in *abc* frame in which each phase can be limited independently. With some modifications, this strategy is extended for control structures in *dq*, and $\alpha\beta$ frames. Equation (2) shows the limitation approach for $\alpha\beta$ frame in which the current magnitude is limited and the phase difference between the two axes remain unchanged [4]. Using this method, [23] has controlled a four-leg VSC in *dq0* frame. A comparison between the behavior of three-leg and four-leg VSCs under different fault conditions has been presented by [24]. It is concluded that a four-leg VSC shows superior response. However it can only be used for low-voltage four-wire systems. This remedy instantaneously limits the output current and protect the VSC against short circuit faults. However, this remedy generates distorted voltage and current waveforms in the case of asymmetrical short circuit faults.

In the second category, the system control is replaced via mode switching by a trip signal in a short circuit condition. Also, it is necessary to return to the primary mode by a reset signal when the short circuit fault is removed by the system protection relays. Employing this strategy, [25] changes the current reference of the faulty phase from the value calculated by the conventional control mode to a predefined sinusoidal current reference with a predefined limited peak value. The method proposed in [26] is switched to another control mode in which a constant predefined current reference in *dq* frame is used upon detection of a fault. Since the current reference (higher than nominal value) is also injected to non-faulted phase(s) by *dq/abc* transformation, it causes an overvoltage in the healthy phase(s). To solve the problem, the study has decreased the current reference of the healthy phase(s) independently in the *abc* frame using output voltage measurement of each phase. The method is applicable to four-leg VSCs, also the reset signal is not elaborated. Reference [27] has compared different trip and reset signals to change the operating mode between normal and limit operation modes in short circuit condition. Comparing different strategies, this reference has concluded that using the current quantity for trip signal and voltage quantity for reset signal gives the desired response. In this study, a predefined limited current reference is used for short circuit condition, which protects the VSC against short circuit. The considered VSC is a four-leg one, and only symmetrical short circuit fault is considered. Assuming the similar strategy and considering asymmetrical faults, [28] has used a reset signal based on voltage quantity to change the operation mode in the case of single-line-to-ground (SLG) short circuit faults. Assuming this strategy, [29] has modeled the VSC in short circuit condition with a predefined current source. Using the schemes based on second category gives higher quality waveforms than the methods based on first category since the distorted current reference is replaced by another non-distorted reference. However, fault occurrence and clearance detection methods are required to issue trip and reset signals, respectively. In the case of delayed fault occurrence detection the VSC is unprotected. Also, in case of delayed fault clearance detection the previous short circuit current is injected to the grid, which causes overvoltage in the system. Then, a smooth transition between normal and limited modes is not guaranteed. Also, change in operation mode complicates the control system and may jeopardize the system reliability.

It is worth mentioning that both aforementioned strategies are employed in protection studies such as protection setting calculation for relays and fault detection strategies, which are based on assuming limited fault current of VSC [30-32]. Also, the distorted waveforms coming from the first control strategy are used in protection relays to detect and isolate the short circuit faults [33].

As a conclusion, some of the aforementioned control



R_f, L_f, C_f	VSC output filter parameters	$V_{oαβ}$	Output voltages in αβ frame	C_v	Voltage control loop compensator
V_{tabc}	VSC terminal voltages	$i_{tαβ}$	Terminal currents in αβ frame	C_i	Current control loop compensator
V_{oabc}	VSC output voltages	$i_{oαβ}$	Output currents in αβ frame	$ω_0$	System nominal frequency
i_{tabc}	VSC terminal currents	$i^*_{tαβ1}$	Unlimited current references	θ	Angular frequency
i_{oabc}	VSC output currents (grid side)	$i^*_{tαβ2}$	Limited current references	$m_{αβ}$	Modulation indices in αβ frame
$V^*_{oαβ}$	Voltage references in αβ frame	m_{abc}	Modulation indeces		

Fig. 1. Power circuit schematic and dynamic control model of a grid forming VSC operating in α–β frame.

methods and short circuit models have covered the FRT issue for VSCs in the low-voltage systems. In the LV system, a four-leg topology is a commonly used configuration for the VSCs providing a neutral connection for single phase loads. Assuming this topology, each phase of VSC can be controlled independently in the *abc* frame. This feature simplifies the control process but cannot be used for a VSC with a three-leg configuration. Also, in some works, instantaneous current limiting strategies are employed, which decreases the power quality by generating distorted output voltages in case of asymmetrical faults. Furthermore, some other methods have proposed control strategies, which requires mode switching for transition from normal mode to limit operation modes, and vice versa. Fault occurrence and clearance instances detection is also needed for such methods in order to issue trip and reset signals, respectively. Above all, dependency to short circuit fault type is another drawback of the suggested methods in some previous works.

III. Conventional Control of a VSC under Overload and Short Circuit Condition

To analyze the dynamics of a VSC, two stationary α–β and rotating d-q frames are introduced in [4]. Using the d-q frame gives the inherent benefit of independent control of active and reactive powers, while control of a VSC in the α–β frame is efficient in unbalanced conditions by using resonant controllers in the voltage and current control loops [4]. Also, working in the d-q frame requires more system bandwidth and consequently it results in higher switching frequencies than working in the α–β frame, when the system is unbalanced. For these reasons, the α–β frame is used in this paper. Fig. 1 shows the complete dynamic model of a grid forming VSC and power circuit schematic in the α–β frame [3]. As indicated in this figure, two cascaded control loops of voltage and current are the main components of the VSC control. In this structure, voltage references ($V^*_{oαβ}$) are specified by nominal voltage and frequency values which come from the outer controls such as droop control [2]. Considering the references, voltage controllers generate proper current references to supply the necessary output currents, and correspondingly maintain the output voltages. As shown in Fig. 1, measured output currents are used as feed forward signals to improve the voltage controller performance. The current controller (second controller) regulates the terminal or filter currents by producing proper terminal voltage references, and correspondingly modulation indices will be generated. Since all quantities are sinusoidal in the stationary α–β frame, proportional-resonant compensators are used for the voltage and current controllers with a typical form of (1) [34].

$$C(s) = k_p + \frac{k_i(s+z)}{s^2+\omega_0^2}. \quad (1)$$

Current reference limiter is another component of the system that limits the amplitude of the current references without any change on the phase angle. Equation (2) describes the functional logic of the conventional current limiter in which I_{max} is the amplitude of the maximum permissible output current [19]. Fig. 2 demonstrates the corresponding graphical representation of the current limiter.

$$\sqrt{i_{tα}^2 + i_{tβ}^2} \le I_{max} \quad (2)$$

In the following, analysis of the VSCs operation under asymmetrical short circuits will be presented. As mentioned in the previous section, distribution systems are exposed to temporary SLG faults, which are cleared by protection relays in

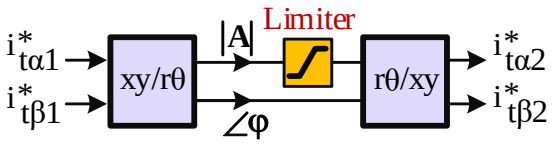


Fig. 2. Current references limiter in αβ frame.

few hundreds of milliseconds. Using conventional settings for protection relays, for faults further from the load, which are more severe, this may even increase to about one second [5, 6]. This clearing time is important from a power quality point of view for systems involving EC-DERs.

When an asymmetrical fault occurs, the VSC output voltages in the affected phases decrease, and consequently, the voltage error seen by the voltage controller becomes non-zero. Then, the voltage controller tries to increase the control effort and the current references. Increasing the control effort leads to the activation of the current limiter, which limits and cuts hardly the crest of the current references to avoid any damage to the VSC switches. To show the performance of the conventional controller, the test system of Fig. 3 is simulated. The VSC parameters are given in Table I. The voltage and current controller transfer functions are given in (3)-(4), respectively.

$$C_v(s) = \left(0.56 + \frac{250.33 \times s}{s^2 + (2\pi \times 50)^2}\right) \times \frac{s + 448.3}{s + 1000} \quad (3)$$

$$C_i(s) = 3.95 + 1763 \times \frac{s - 220.3}{s^2 + (2\pi \times 50)^2} \quad (4)$$

The VSC is, as a case, connected to a medium voltage distribution system via a 5 MVA, 5/20 kV step up DYg transformer. In the simulations, an SLG fault occurs in PCC with fault resistance of 10 Ω. Fig. 4 shows simple simulation results for the SLG fault. As a result of the limiter operation, the actual current references with the sinusoidal waveforms (output of the voltage controller as shown in Fig. 4-a) change to limited square-wave shape ones based on (2) as it is shown in Fig. 4-b. These limited currents are employed as the references of the current control block.

Since the current controller is designed for sinusoidal quantities, its response for such stepwise square wave inputs are accompanied by a non-zero steady state error and undesirable transient behavior in the terminal currents of the VSC. Fig. 4-b shows the current references with the corresponding terminal currents of the VSC in α–β frame.

From a power system analysis point of view, these output currents with the shape of square wave are injected to the parallel equivalent of the output filter capacitor and the equivalent impedance of the rest of the system including the power transformer. In the unaffected phase of the VSC, neglecting the output current, the square-wave shape terminal current is injected to the corresponding filter capacitor. Therefore, the voltage of this phase will be of a triangle shape. On the other side, in the affected phases, the output equivalent impedance seen by the VSC is low and inductive, which is in parallel with the filter capacitor in the corresponding phase. Hence, injecting a square wave current results in a triangle wave shape similar to that of the unaffected phase of the VSC along with the parallel LC resonant mode with low damping in the output voltages of the affected phases.

To clarify more the subject, a physical explanation would be useful. Generally the output filter of the VSC is an LCL filter considering the inductances in the output of the VSC. The filter capacitor of the VSC has an inherent resonance with the output Thevenin inductance of the VSC. At normal conditions, the feed-forward of the output currents employed in the voltage control block significantly compensates and dampens the resonant modes. In short circuit conditions and with the activation of the current limiter, the voltage control block is entirely isolated from the rest of the system, and the feed-forward term looses its effectiveness, and the resonant mode appears in the output voltages of the VSC. Since the fault resistance is the only damping component in the system, the resonant mode dampens slowly. Fig. 5 shows the output voltages of the VSC for an SLG fault in the ac grid of Fig. 3. Phases "a" and "b" are the affected phases, and phase "c" is the unaffected phase. As depicted in Fig. 5, the unaffected phase experiences a voltage with a triangular waveform with a peak value 25% more than that of the nominal value. Also, in the affected phase of "b" there are resonating components creating two peaks (over-voltages) in each cycle that is 50% higher than the nominal peak value. Also, there are the same resonating component in the affected phase of "a" with the opposite sign. The damping of the resonant components are directly determined by the fault resistance. Also, Fig. 6 demonstrates the PCC voltages during the short circuit, having the same undesired variations.

All the aforementioned propositions are based on simulation of basic control of Fig. 1, which gives the insight about the operation of VSC under short circuit condition. In practical applications, the dynamic states of the controls placed before a limiter are implemented with anti-windup mechanisms [35]. Using this mechanism for voltage controller avoids saturation of the controller and improves the VSC behavior under short circuit condition. However, the output waveforms distortion cannot be avoided. Discussion on the anti-windup mechanism performance is given in the simulation results section, which is another contribution of this paper.

The next section presents the proposed remedy to reinforce the VSC behavior under short circuit condition.

IV. Proposed Voltage Control Scheme for A VSC under Asymmetrical and Symmetrical Short Circuit Fault Conditions

The proposed control scheme includes three main parts. First, a fast sinusoidal current limiter is introduced. Next, an adaptive virtual impedance-based voltage reference is proposed as the second contribution of the paper. Finally, state space analysis of the system with the proposed scheme is presented.

A. Proposed Sinusoidal Current Limiter

Equation (2) described the operating principles of the conventional current limiter which cuts the crest of the sinusoidal references and generates the limited currents with square wave shape waveform. Consequently, it results in output voltage distortion and output LC resonant mode excitation. To avoid this, a sinusoidal current reference limiter is used in this paper, which appears as a gain in the control loop whose value is updated continuously based on the received inputs. The procedure proposed in this paper utilizes a quarter of a cycle of

Table I. Parameters of the simulated VSC

$r_f = 3.5\ m\Omega$	$L_f = 3.5\ mH$	$S_n = 5\ MVA$
$C_f = 30\ \mu F$	$x_t = 5\ \%$	$I_{max}^{peak} = 1021\ A$
$f_{sw} = 3\ kHz$	$V_{ll} = 5\ kV$	

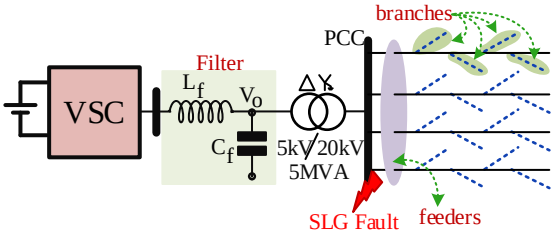
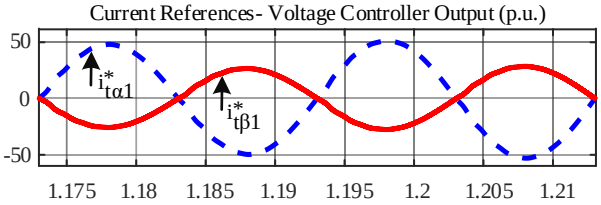
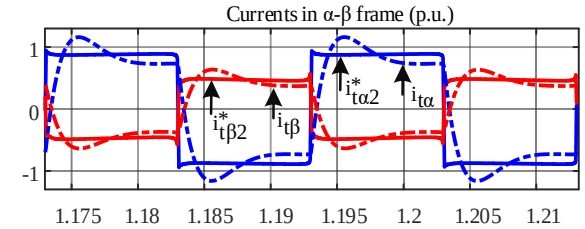


Fig. 3. Simulated VSC test system for an SLG fault.



(a)



(b)

Fig. 4. Current references generated by the voltage controller (a), and the limited current references and output currents of VSC (b) in α–β frame.

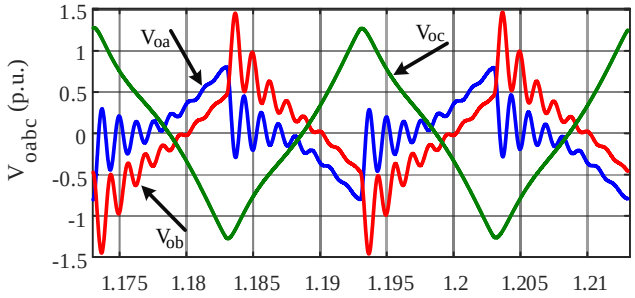


Fig. 5. VSC output voltage subjected to an SLG fault in the system.

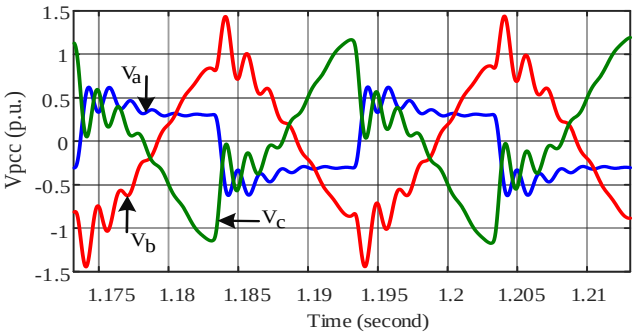


Fig. 6. PCC voltage subjected to an SLG fault in the system.

the delayed version of the input current references along with the actual current references to calculate the gain. Assume that the unlimited current references, which are the outputs of the voltage controller, are as those of (5) using sequence components, where I_1 and I_2 are the positive and negative sequence components amplitudes, respectively. Also, θ_1 and θ_2 are the corresponding phase angles.

$$\begin{aligned} i_{ta}^* &= I_1\cos(\omega t+\theta_1)+I_2\cos(\omega t+\theta_2)\\ i_{tb}^* &= I_1\cos\left(\omega t+\theta_1-\frac{2\pi}{3}\right)+I_2\cos\left(\omega t+\theta_2+\frac{2\pi}{3}\right)\\ i_{tc}^* &= I_1\cos\left(\omega t+\theta_1+\frac{2\pi}{3}\right)+I_2\cos\left(\omega t+\theta_2-\frac{2\pi}{3}\right) \end{aligned} \quad (5)$$

Sequence component modeling removes the dependency of the analysis to fault type and faulted phase. As an example, depending on the fault type and faulted phase in grid side, affected phase(s) changes which complicates the analysis. Using sequence component modeling, no matter which phase(s) is affected by fault, the sequence components parameters can be calculated. Accordingly, the limiter follows only one calculation procedure to update the gain.

Considering (5), the amplitude of the affected phase with maximum amplitude among the three phases is as shown in (6). This value is a continuous function of $\Delta\theta$, which is the phase angle difference between the positive and negative sequence components, $\Delta\theta = \theta_1 - \theta_2$.

$$I_p = \begin{cases} \sqrt{I_1^2+I_2^2+2I_1I_2\cos(\Delta\theta)}, & -\frac{\pi}{3}<\Delta\theta<\frac{\pi}{3}\\ \sqrt{I_1^2+I_2^2+2I_1I_2\cos\left(\Delta\theta-\frac{2\pi}{3}\right)}, & \frac{\pi}{3}<\Delta\theta<\pi\\ \sqrt{I_1^2+I_2^2+2I_1I_2\cos\left(\Delta\theta+\frac{2\pi}{3}\right)}, & \pi<\Delta\theta<\frac{5\pi}{3} \end{cases} \quad (6)$$

Then, the corresponding gain of the sinusoidal current reference limiter is calculated based on (7), where I_{max} is the maximum permissible current based on the VSC switches specifications.

$$k_1 = \begin{cases} \frac{I_{max}}{I_p} & I_p > I_{max}\\ 1 & I_p < I_{max} \end{cases} \quad (7)$$

Since the inputs are in α–β frame, then, it is necessary to calculate the values based on α–β frame quantities. For this purpose, (8) gives the α–β frame equivalence of (5).

$$\begin{cases} i_{t\alpha1}^* = I_1\cos(\omega t+\theta_1)+I_2\cos(\omega t+\theta_2)\\ i_{t\beta1}^* = I_1\sin(\omega t+\theta_1)-I_2\sin(\omega t+\theta_2) \end{cases} \quad (8)$$

Considering four unknown variables of $[I_1, I_2, \theta_1, \theta_2]$ and the two equations in (8), two other independent equations are needed to find the unknown variables. For this purpose, the quarter of cycle of the delayed version of (8) is used as:

$$\begin{cases} {i'_{t\alpha1}}^* = I_1\sin(\omega t+\theta_1)+I_2\sin(\omega t+\theta_2)\\ {i'_{t\beta1}}^* = -I_1\cos(\omega t+\theta_1)+I_2\cos(\omega t+\theta_2) \end{cases} \quad (9)$$

Solving (8) and (9) simultaneously results in (10) in which ωt is the angular frequency of the VSC, and consequently, the unknown variables of $[I_1, I_2, \theta_1, \theta_2]$ can be found.

$$\begin{aligned} I_1\cos(\theta_1) &= \cos(\omega t)\left(\frac{i_{t\alpha1}^*-{i'_{t\beta1}}^*}{2}\right)+\sin(\omega t)\left(\frac{{i'_{t\alpha1}}^*+i_{t\beta1}^*}{2}\right)\\ I_1\sin(\theta_1) &= \cos(\omega t)\left(\frac{{i'_{t\alpha1}}^*+i_{t\beta1}^*}{2}\right)-\sin(\omega t)\left(\frac{i_{t\alpha1}^*-{i'_{t\beta1}}^*}{2}\right)\\ I_2\cos(\theta_2) &= \cos(\omega t)\left(\frac{i_{t\alpha1}^*+{i'_{t\beta1}}^*}{2}\right)+\sin(\omega t)\left(\frac{{i'_{t\alpha1}}^*-i_{t\beta1}^*}{2}\right)\\ I_2\sin(\theta_2) &= \cos(\omega t)\left(\frac{{i'_{t\alpha1}}^*-i_{t\beta1}^*}{2}\right)-\sin(\omega t)\left(\frac{i_{t\alpha1}^*+{i'_{t\beta1}}^*}{2}\right) \end{aligned} \quad (10)$$

Now, I_p and consequently k_1 can simply be found based on equations, (6), (7), and (10). Finally, the new limited current references are as shown in (11) or equivalently in Fig. 7.

$$\begin{cases} i_{t\alpha2}^* = k_1\times(I_1\cos(\omega t+\theta_1)+I_2\cos(\omega t+\theta_2))\\ i_{t\beta2}^* = k_1\times(I_1\sin(\omega t+\theta_1)-I_2\sin(\omega t+\theta_2)) \end{cases} \quad (11)$$

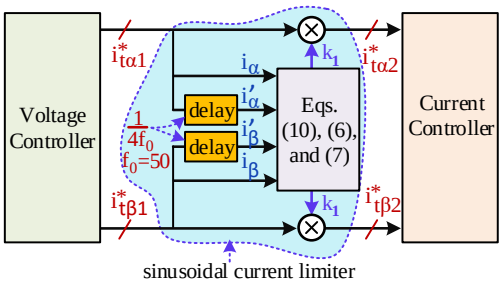


Fig. 7. Proposed current limiter providing sinusoidal reference currents.

In the next subsection, the proposed voltage control scheme is presented.

B. Proposed Adaptive Virtual Impedance-Based Voltage Reference Generation Scheme

In this part, an adaptive voltage control method based on virtual impedance concept is proposed. From the VSC side point of view, using virtual impedance in voltage control scheme in fact increases the seen impedance by VSC, which accordingly reduces the output currents of the VSC. On the other hand from the grid side point of view, using virtual impedance, the VSC decreases its output voltages in short circuit condition, which again means that the current references and the output currents are reduced. The detailed explanations are given in the following.

The proposed adaptive voltage reference generation scheme is as shown in Fig. 8 for the α-axis. The same control diagram is used for the β-axis, which is not shown due to space limitation. In Fig. 8, k_p and $k_i.\frac{s+k_z}{s^2+\omega_0^2}$ represent a proportional and resonant compensator, respectively. Also, the lead compensator of $\frac{s+z}{s+p}$ is employed to improve the control loop performance. Further, the output of the adaptive virtual impedance-based voltage reference generation block gives the desired voltage reference. This block consists of the following three parts.

1) Path Activation Block Based on Current Limiter:

In the fault conditions and when the current limiter is activated, k_1 decreases (from value 1), and the output of this block becomes a non-zero positive value. This means that the virtual impedance path is activated when a fault occurs. The gain k_1 is taken from the sinusoidal current limitation process, which inherently contains the level of the fault severity (low values correspond to severe faults). This gain is between 0 and 1. However, as it will be explained later, the virtual impedance prevents k_1 from becoming a very low value. Since, for more severe faults, k_1 has a smaller value, $1/k_1$ will be a larger value resulting in a higher gain which is reducing the voltage reference further. Also, to distinguish between a normal and a faulty condition, the gain of $k_1^{-1}-1$ is used, which deactivates the virtual impedance path at normal conditions with $k_1=1$. As a result, this block not only activates the voltage reference reduction process at fault conditions ($k_1<1$) but also adaptively changes the gain based on the severity of the fault. The equivalent model of the reference reduction method in Fig. 8 shows an adaptive change in the voltage reference characteristics.

2) Mid-pass Filtering:

This filter has mid-pass characteristic which removes all unwanted disturbances such as resonant mode frequency components at fault inception time. This compensator has a unity gain around the fundamental frequency (0 dB) and negative gains for all other frequency spectra. The filtering block ensures a pure sinusoidal output for the virtual impedance path.

3) Virtual Impedance:

The virtual impedance (k_2) is the most important element in the loop. This parameter directly determines how much the voltage reference must decrease at different fault conditions. To clarify the effect of virtual impedance of k_2 on VSC behavior, suppose that the rest of the system is modeled by a Thevenin equivalent model as shown in (12)-(13), where $V_{o\alpha\beta}$, $i_{o\alpha\beta}$, $z_{th\alpha\beta}$, and $V_{th\alpha\beta}$ are VSC output voltages and currents and the system Thevenin impedances and voltages in αβ frame, respectively. The superbars denote the phasor representation of quantities in the operating point of short circuit fault condition. In this condition, $V_{th\alpha\beta}$ decreases, and considering the low impedances under short circuits, applying nominal voltages by VSC ($V_{o\alpha\beta}=V^*_{o\alpha\beta}$) results in large currents according to (12)-(13) that should be avoided.

$$\overline{V_{o\alpha}} = z_{th\alpha}\overline{i_{o\alpha}} + \overline{V_{th\alpha}} \quad (12)$$

$$\overline{V_{o\beta}} = z_{th\beta}\overline{i_{o\beta}} + \overline{V_{th\beta}} \quad (13)$$

To limit the currents within the safe range, this paper has proposed a method based on virtual impedance. The method virtually simulates a relatively large impedance in series with the VSC (z_{VSC}) as shown in (14)-(15).

$$\overline{V_{o\alpha}} = \overline{V^*_{o\alpha}} - z_{VSC}\overline{i_{o\alpha}} \quad (14)$$

$$\overline{V_{o\beta}} = \overline{V^*_{o\beta}} - z_{VSC}\overline{i_{o\beta}} \quad (15)$$

Substituting (14)-(15) into (12)-(13) results in (16)-(17), in which the output impedance seen by the VSC is increased, which results in limited output currents.

$$\overline{V^*_{o\alpha}} = (z_{VSC}+z_{th\alpha})\overline{i_{o\alpha}} + \overline{V_{th\alpha}} \quad (16)$$

$$\overline{V^*_{o\beta}} = (z_{VSC}+z_{th\beta})\overline{i_{o\beta}} + \overline{V_{th\beta}} \quad (17)$$

To find the quantitative value of the mentioned impedance (z_{VSC}) considering the control block diagram of Fig. 8, the input error of voltage control loop compensator can be used as shown in (18)-(19).

$$E_{1\alpha} = V^*_{o\alpha} - \left(\frac{1}{k_1}-1\right)\left(\frac{2\xi\omega_0 s}{s^2+2\xi\omega_0 s+\omega_0^2}\right)k_2 i^*_{t\alpha 2} - V_{o\alpha} \quad (18)$$

$$E_{1\beta} = V^*_{o\beta} - \left(\frac{1}{k_1}-1\right)\left(\frac{2\xi\omega_0 s}{s^2+2\xi\omega_0 s+\omega_0^2}\right)k_2 i^*_{t\beta 2} - V_{o\beta} \quad (19)$$

Because of using PR compensator for voltage controller and considering the sinusoidal current and voltage waveforms, which are guaranteed by the sinusoidal current limiter, the steady state values of errors are zero as shown in (20)-(21) by substituting $s=j\omega_0$ into (18)-(19). It should be noted that $i^*_{t\alpha\beta 2}$ are replaced by $i_{o\alpha\beta}$ since the current controller has zero steady state error as well, and the capacitor currents are negligible comparing with the fault currents.

$$\overline{V^*_{o\alpha}} - (k_1^{-1}-1)k_2\overline{i_{o\alpha}} - \overline{V_{o\alpha}} = 0 \quad (20)$$

$$\overline{V^*_{o\beta}} - (k_1^{-1}-1)k_2\overline{i_{o\beta}} - \overline{V_{o\beta}} = 0 \quad (21)$$

Comparing Eqs. (20)-(21) with Eqs. (14)-(15) gives the effective virtual impedance of z_{VSC} as follows,

$$z_{VSC} = (k_1^{-1}-1)k_2. \quad (22)$$

Equation (22) implies that the current limiter and virtual

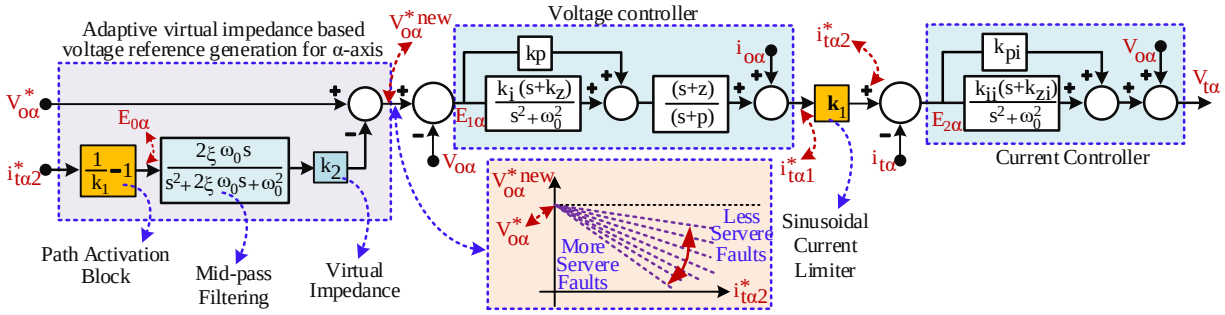


Fig. 8. Proposed voltage controller introducing virtual impedance.

impedance of k_2 both determines the VSC behavior under short circuit condition. Considering this fact, the system analysis is complicated since the virtual impedance (k_2) and gain k_1 are coupled together. In the following subsection, more detailed system modeling is presented to find the system stability margin versus k_2.

C. State Space Analysis of the Proposed Voltage Reference

As mentioned in the previous subsection, the virtual impedance of k_2 and the gain k_1 of the current limiter determine the system behavior under short circuit conditions. During a short circuit fault, the current limiter is activated, k_1 decreases and depending on the value of k_2, the voltage reference decreases by the gain of $(1/k_1 - 1) \times k_2$ (see Fig. 8). Consequently, because of the reduced voltage reference, k_1 increases until the current references reach their maximum values. In the meantime, an increase in k_1 decreases $(1/k_1 - 1)$ and consequently reduces the reduction of the voltage reference. As a result, k_1 decreases again and this process is repeated. This sequence of actions shows the complexity of the system analysis that needs further investigation. For this purpose, a complete state space analysis of the system with the proposed scheme is presented. It is worth noting that wherever there are the same state space equations for the α and β axis, only the equations for the α axis are presented for the sake of brevity.

State variables for the voltage controllers in both α and β frames are given in (23) based on Fig. 8.

$$\begin{cases} x_1 = \dfrac{1}{s^2+\omega_0^2}E_{1\alpha} \quad x_2 = x_1' \quad x_3 = \dfrac{z-p}{s+p}u_{1\alpha} \\ x_4 = \dfrac{1}{s^2+\omega_0^2}E_{1\beta} \quad x_5 = x_4' \quad x_6 = \dfrac{z-p}{s+p}u_{1\beta} \end{cases} \tag{23}$$

Accordingly, the corresponding state space equations are presented in (24) for α axis.

$$\begin{aligned} (\dot{x_1}) &= x_2 \\ (\dot{x_2}) &= V_{o\alpha}^* - \omega_0^2 x_1 - 2\xi k_2 \omega_0 x_{12} - V_{o\alpha} \\ (\dot{x_3}) &= k_p(z-p)V_{o\alpha}^* + k_i k_z (z-p)x_1 + k_i(z-p)x_2 \\ &\quad -px_3 - 2\xi k_p k_2 \omega_0 (z-p)x_{12} - k_p(z-p)V_{o\alpha} \end{aligned} \tag{24}$$

Fig. 8 also shows the current controller dynamic model for the α axis. The same model for the β axis can be considered. State variables for the current controllers in both α and β frames are given in (25).

$$\begin{aligned} x_7 &= \frac{1}{s^2+\omega_0^2}E_{2\alpha} \quad x_9 = \frac{1}{s^2+\omega_0^2}E_{2\beta} \\ x_8 &= x_7' \qquad\qquad x_{10} = x_9' \end{aligned} \tag{25}$$

The corresponding state space equations are presented in (26) for the α axis.

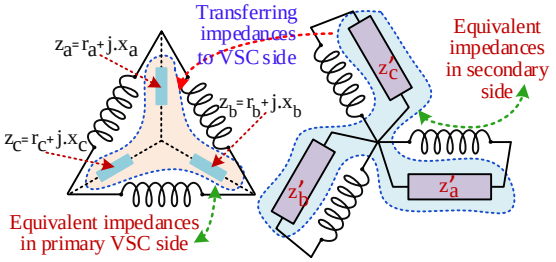


Fig. 9. Model of the transformer and the grid at fault for state space analysis.

$$\begin{aligned} (\dot{x_7}) &= x_8 \\ (\dot{x_8}) &= k_1 k_p V_{o\alpha}^* + k_1 k_i k_z x_1 + k_1 k_i x_2 + k_1 x_3 \\ &\quad -\omega_0^2 x_7 - 2\xi k_1 k_p k_2 \omega_0 x_{12} - i_{t\alpha} - k_1 k_p V_{o\alpha} + k_1\, i_{o\alpha} \end{aligned} \tag{26}$$

There are two state variables for both α and β frames, which corresponds to the virtual impedance filtering block as shown in (27).

$$\begin{aligned} x_{11} &= \frac{E_{0\alpha}}{s^2+2\xi\omega_0 s+\omega_0^2} \quad x_{13} = \frac{E_{0\beta}}{s^2+2\xi\omega_0 s+\omega_0^2} \\ x_{12} &= x_{11}' \qquad\qquad x_{14} = x_{13}' \end{aligned} \tag{27}$$

The corresponding state space equations are presented in (28) for the α axis.

$$\begin{aligned} (\dot{x_{11}}) &= x_{12} \\ (\dot{x_{12}}) &= k_1 k_p (k_1^{-1}-1)V_{o\alpha}^* + k_1(k_1^{-1}-1)k_i k_z x_1 \\ &+k_1(k_1^{-1}-1)k_i x_2 + k_1(k_1^{-1}-1)x_3 \; - \omega_0^2 x_{11} \\ &-2\xi\omega_0\big(1+k_1(k_1^{-1}-1)k_p k_2\big)x_{12} \\ &-k_1(k_1^{-1}-1)k_p V_{o\alpha} + k_1(k_1^{-1}-1)\, i_{o\alpha} \end{aligned} \tag{28}$$

The other state variables belong to the power system model, which include the terminal currents ($i_{t\alpha}, i_{t\beta}$), capacitor voltages ($V_{o\alpha}, V_{o\beta}$) and load currents ($i_{\alpha o}, i_{\beta o}$). The corresponding state space equations for the terminal current and the output voltage of the VSC are presented in (29), (30) for the α axis, respectively.

$$\begin{aligned} (\dot{\imath_{t\alpha}}) &= k_{pi}k_1 k_I k_z L_f^{-1} x_1 + k_{pi}k_1 k_I L_f^{-1} x_2 + k_{pi}k_1 L_f^{-1} x_3 \\ &+k_{ii}k_{zi}L_f^{-1}x_7 + k_{ii}L_f^{-1}x_8 - \big(r_f + k_{pi}\big)L_f^{-1} i_{t\alpha} \\ &-k_{pi}k_1 k_p L_f^{-1} V_{o\alpha} + k_{pi}k_1 L_f^{-1} i_{o\alpha} + k_{pi}k_1 k_p L_f^{-1} V_{o\alpha}^* \end{aligned} \tag{29}$$

$$(\dot{V_{o\alpha}}) = C_f^{-1} i_{t\alpha} - C_f^{-1} i_{o\alpha} \tag{30}$$

Also, to find the relevant equations for the state variables of the output currents of the VSC, all grid side impedances including the leakage reactance of the transformer are transferred to the delta side of the transformer (see Fig. 9). Using a delta to star transformation and employing abc to α-β transformation, (31) is derived. To consider the worst possible case, the fault impedance at the grid side is assumed zero (for example $z_a' = 0$).

$$
\begin{aligned}
6(\dot{\iota_{o\alpha}}) &= (4L_a^{-1} + L_b^{-1} + L_c^{-1})V_{o\alpha} + \sqrt{3}(L_c^{-1} - L_b^{-1})V_{o\beta} \\
&-(4r_aL_a^{-1} + r_bL_b^{-1} + r_cL_c^{-1})i_{o\alpha} - \sqrt{3}(r_cL_c^{-1} - r_bL_b^{-1})\, i_{o\beta} \\
6(\dot{\iota_{o\beta}}) &= +\sqrt{3}(L_c^{-1} - L_b^{-1})V_{o\alpha} + 3(L_b^{-1} + L_c^{-1})V_{o\beta} \\
&-\sqrt{3}(r_cL_c^{-1} - r_bL_b^{-1})i_{o\alpha} - 3(r_bL_b^{-1} + r_cL_c^{-1})\, i_{o\beta}
\end{aligned} \tag{31}
$$

All the variables in (23)-(31) are defined except the limiter gain k_1 and the virtual impedance k_2. As mentioned earlier, these variables depend on each other, and to find their relation, linearization of the system in the steady state operating point of the fault condition is used as follows. Assume that an SLG fault occurs in phase "a" of the system at the YG side of the transformer. This fault is seen as a line-line fault at the VSC side of the transformer with the affected phases of "a" and "b". Based on Fig. 9, (32) and (33) describe the relationship between the VSC side output voltages and currents in α–β and abc frames, respectively. Superbars refer to phasor representation in the operating point of a short circuit condition.

$$
\begin{bmatrix} \overline{I_{o\alpha}} \\ \overline{I_{o\beta}} \\ \overline{I_{o0}} \end{bmatrix} = \frac{\sqrt{3}}{2}\frac{1}{r_a + jx_a}\begin{bmatrix} \sqrt{3}\overline{V_{o\alpha}} - \overline{V_{o\beta}} \\ -\overline{V_{o\alpha}} + \overline{V_{o\beta}} \\ 0 \end{bmatrix} \tag{32}
$$

$$
\overline{I_{oa}} = -\overline{I_{ob}} = \left(\frac{\sqrt{3}}{2}\right)\left(\frac{\sqrt{3}\overline{V_{o\alpha}} - \overline{V_{o\beta}}}{r_a + jx_a}\right) \tag{33}
$$

Also, considering the proposed voltage reference at fault conditions, (34) describes the error of the voltage control loops at the steady state operating point of the fault condition, see Fig. 8.

$$
\begin{cases} \overline{E_{1\alpha}} = \overline{V_{o\alpha}^*} - k_2(k_1^{-1} - 1)\overline{\iota_{o\alpha}} - \overline{V_{o\alpha}} = 0 \\ \overline{E_{1\beta}} = \overline{V_{o\beta}^*} - k_2(k_1^{-1} - 1)\overline{\iota_{o\beta}} - \overline{V_{o\beta}} = 0 \end{cases} \tag{34}
$$

Solving (32) and (34) for $\overline{(V_{o\alpha})}$ and $\overline{(V_{o\beta})}$ yields (35) where $g = k_2k_1^{-1}(1 - k_1)(r_a + jx_a)$.

$$
\begin{bmatrix} \overline{V_{o\alpha}} \\ \overline{V_{o\beta}} \end{bmatrix} = \frac{1}{4g + 2}\begin{bmatrix} g + 2 & \sqrt{3}g \\ \sqrt{3}g & 3g + 2 \end{bmatrix}\begin{bmatrix} \overline{V_{o\alpha}^*} \\ \overline{V_{o\beta}^*} \end{bmatrix} \tag{35}
$$

Finally, substituting (35) into (33), considering the fact that $\overline{(I_a)}$ is limited to I_{max}, and solving the equations gives the relation between k_1 and k_2 as shown in (36). In this equation, $|V_m^*|$ is the peak value of nominal voltage. Following the same procedure, (37) and (38) give the relation for line-to-line (LL) and symmetrical (LLL) faults, respectively. To consider the worst possible case, the fault resistance r_a is neglected and the fault reactance is considered equal to the leakage reactance of the transformer, $x_a = x_l$, anywhere (36) - (38) are needed.

$$
k_1 = k_2 \times \left(k_2 + \sqrt{\left(\frac{0.87 \times |V_m^*|}{|I_{max}|}\right)^2 - \left(\frac{x_a}{2}\right)^2} - \frac{r_a}{2}\right)^{-1} \tag{36}
$$

$$
k_1 = k_2 \times \left(k_2 + \sqrt{\left(\frac{|V_m^*|}{|I_{max}|}\right)^2 - \left(\frac{x_a}{6}\right)^2} - \left(\frac{r_a}{12}\right)\right)^{-1} \tag{37}
$$

$$
k_1 = k_2 \times \left(k_2 + \sqrt{\left(\frac{|V_m^*|}{|I_{max}|}\right)^2 - \left(\frac{x_a}{3}\right)^2} - \left(\frac{r_a}{3}\right)\right)^{-1} \tag{38}
$$

Substituting (36) into entries of the state space matrix A and calculating the eigenvalues as a function of k_2 gives the stability margin. Fig. 10 represents the variations of the system eigenvalues versus k_2 ($k_2 > 0$) for an SLG short circuit fault. The considered short circuit fault is a solidly grounded fault ($r_f = 0$) and located at the PCC, which is the worst possible case. In this figure, the eigenvalues have been discriminated by their numbers, i.e. 1-20. Also, Table II demonstrates the absolute value of participation percent of the different state variables on different eigenvalues. As shown in this table, the state variables of $V_{o\alpha}, i_{o\alpha}, V_{o\beta}, i_{o\beta}$ have considerable participation on $\lambda_{2,3}$, which verifies the existence of the resonant modes in the system as described in section III. Looking at the eigenvalues of $\lambda_{2,3}$ in Fig. 10 demonstrates that the real part of the eigenvalues are high enough (with a negative sign), which can be considered as dominant poles. There is the same analysis for LL and LLL short circuit faults, which are not presented due to space limitation. Based on the results, for values of $k_2 > 0$, the system remains stable, which means that the proposed approach fully ensures the stability. Since all of the analysis are based on worst case assumptions, a fortiori, it guarantees the stability for other cases.

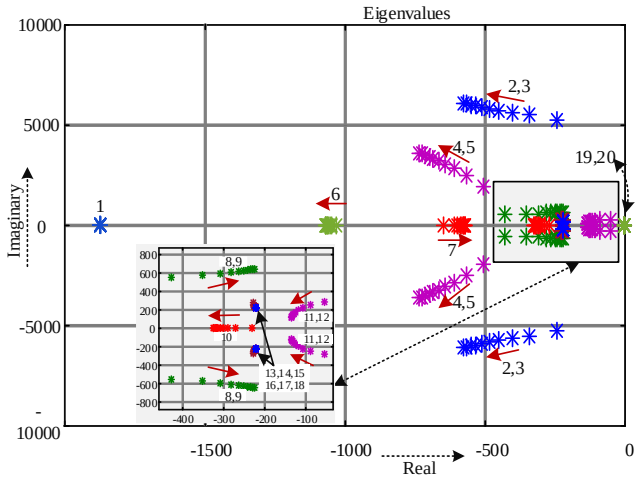


Fig. 10. The system eigenvalues variations versus increase in k_2 ($k_2 > 0$).

Table II. Percent of absolute value of state variables participations on eigenvalues.

	<10%	10-20%	20-30%	30-40%	40-50%	50%<
λ_1	-	-	$i_{o\alpha}$	-	-	$i_{o\beta}$
$\lambda_{2,3}$	$i_{t\alpha}$	$V_{o\beta}, i_{o\beta}$	-	$V_{o\alpha}, i_{o\alpha}$	-	-
$\lambda_{4,5}$	x_5, x_{10}	$x_6, i_{t\alpha}, V_{o\alpha}$	-	$V_{o\beta}$	$i_{t\beta}$	-
λ_6	$x_8, x_{12}, i_{t\alpha}$	-	x_6	-	-	x_3
λ_7	$x_5, i_{t\alpha}$	$x_3, x_8, i_{t\beta}, V_{o\beta}$	-	-	x_6, x_{10}	-
$\lambda_{8,9}$	x_7	$x_{10}, i_{t\beta}$	-	-	$x_8, i_{t\alpha}$	-
λ_{10}	$x_2, x_3, x_9, i_{t\beta}, V_{o\alpha}$	x_1, x_5, x_6, x_{10}	$V_{o\beta}$	x_4	-	-
$\lambda_{11,12}$	-	x_4, x_5, x_{11}, x_{12}	-	-	x_2	x_1
$\lambda_{13,14}$	$x_6, x_{10}, x_{13}, V_{o\beta}$	x_1, x_2, x_{14}	-	-	x_4	x_5
$\lambda_{15,16}$	-	x_1, x_2	x_{13}, x_{14}	-	-	x_{11}, x_{12}
$\lambda_{17,18}$	-	x_4, x_5	x_{11}, x_{12}	-	-	x_{13}, x_{14}
λ_{19}	-	$i_{t\alpha}$	x_9	-	-	x_7
λ_{20}	-	-	x_7	-	-	x_9

Regarding the selection of a proper value for k_2, $k_2 > 0$ ensures the system stability based on previous discussions. To discuss more the values, explanation on virtual series impedance of (22) would be useful. Suppose that a small positive value is taken for k_2. As a result, the limiter should decrease more the gain k_1 to achieve acceptable series impedance for current limitation. On the other side, using larger value for k_2 has opposite effect, which requires larger gain value for k_1. In this case, although the system is stable, k_1 still remains close to 1, and the calculation approach for finding k_1 continuously switches between the two presented criteria in (7). This characteristic affects the output voltages and currents quality, which should be avoided. As a rule of thumb, neglecting r_a and x_a in (36)- (38), and assuming $k_1 < 0.80$

gives an appropriate range for k_2.

V. Simulation Results

In the following case studies (A-D), the test system of Fig. 3 is simulated to verify the performance of the proposed voltage control approach. All the components of the VSC including the voltage and current control loops, current reference limiter are completely modeled. In all cases, short circuit faults are applied to PCC with negligible fault resistance ($r_f = 0$) to consider the worst possible case. Also, the virtual impedance of $k_2 = 4.5\ \Omega$ has been used in the simulations.

A. Performance Evaluation of Anti-windup Mechanism under SLG Short Circuits Using Conventional Method

In this part, an SLG fault is applied to PCC of Fig. 3. Since the faults close to the VSC are severe faults, the conventional control method leads to large distortions and overvoltage on the output voltages during and after clearing the fault when the anti-windup scheme is not modeled as described in section III. Employing anti-windup mechanism removes the overvoltage, however the waveforms remain distorted.

Fig. 11 and Fig. 12 show the response of the VSC with and without considering anti-windup mechanism, respectively. As inferred from voltage waveforms, anti-wind up mechanism effectively releases the voltage controller under short circuit condition and removes the overvoltage. On the other side, the VSC currents are still stepwise square wave waveforms, which is the reason for triangle shape distorted output voltages in affected phases from fault. Also, the resonant modes still exist, however their amplitudes are reduced. Considering the analysis presented in section III, it was expected to see larger resonant modes in the output voltages in the affected phases due to square wave shape currents. To figure out the reason, single-sided band amplitude spectrum of the VSC currents with and without employing anti-windup mechanism are depicted in Fig. 13. It is inferred that employing an anti-windup scheme approximately keeps the fundamental component unchanged, but considerably decreases higher frequencies, which avoids the excitation of resonant modes to some extent.

In the following, the performance of the proposed control scheme is analyzed under different short circuit fault scenarios. As mentioned in section II, there are two general strategies regarding the FRT of grid forming VSCs. The first strategy keeps the main voltage control loop and voltage controller active while limiting the output currents by means of the instantaneous current limiter. On the other side, in the second strategy, the control system is switched to another control mode which requires fault inception and clearance instances detection. The proposed method in this paper does not change the operational mode and keeps the main voltage controller active in short circuit condition. Accordingly, its performance is compared with the method based on strategy I, which is called conventional method hereafter.

B. Performance Evaluation of the Proposed Method under SLG Short Circuit Fault

To evaluate the performance of the proposed method, a solidly grounded SLG short circuit fault ($r_f = 0$) is applied to PCC of the test system of Fig. 3 at t = 1 *sec* which corresponds to worst possible case among SLG faults. This fault is seen as LL fault from VSC point of view because of transformer connection. This fault is cleared after 200 *msec* from inception. Fig. 14 shows the voltage and current waveforms. The currents are kept below the maximum value ($I_{tmax}^{peak} = 1.021\ kA$) by properly decreasing the VSC voltages by the proposed method. Also, the waveforms are sinusoidal without distortion, comparing with the waveforms of Fig. 11.

Also, the I_p and k_1 variations are depicted in Fig. 15 and Fig. 16, respectively. As shown in Fig. 15, I_p jumps to the final value in about a quarter of cycle, and correspondingly k_1 decreases to its final value at the same time. Upon fault inception, because of transients in the system, some variations appear around the final values of I_p and k_1, which lasts for half a cycle. Considering the short duration and fast changes, and knowing the BW of the current control loop, the variations cannot affect the current controller. The output current waveforms verify this claim.

C. Performance Evaluation of the Proposed Method under LL Short Circuit Fault

An LL short circuit fault is applied to the system in the condition same as the previous part. Fig. 18 and Fig. 19 show the voltage and current waveforms for conventional and proposed method, respectively. Comparing the figures shows the superiority of the proposed method. Also, Fig. 20 and Fig. 21 demonstrate the I_p and k_1 variations.

D. Performance Evaluation of the Proposed Method under LLL Short Circuit Fault

An LLL short circuit fault is applied to the system in the condition as the previous parts. Symmetrical short circuit rarely happens in the system. However, it may occur when the substation is grounded for maintenance works and accidentally connecting the VSC to a grounded substation which results in LLL fault. Fig. 22 and Fig. 23 show the voltage and current waveforms for conventional and proposed methods, respectively. It is inferred from Fig. 22 that the conventional control of VSC has acceptable response under symmetrical short circuit faults.

Based on Fig. 23, the proposed method shows also proper response against symmetrical short circuit faults. Further, Fig. 24 and Fig. 25 demonstrate the I_p and k_1 variations.

E. Performance Evaluation of the Proposed Method in a System with Two VSCs under SLG Short Circuit Fault.

To show the performance of the proposed method in a distribution system with more than one VSC, the test system of Fig. 17 is simulated in the PSCAD/EMTDC software environment. The VSCs are controlling the voltage and frequency of the distribution system via P/f and V/Q droop control strategy [36]. The droop coefficients are calculated based on the capacity of the VSCs, which are not elaborated due to space limitation. To show the effect of VSC capacity, the capacities of 3 MVA and 2 MVA are used in the system. Also, the same value for the virtual impedance of both VSCs ($k_2 = 4.5$) are selected to discuss the effect on the results.

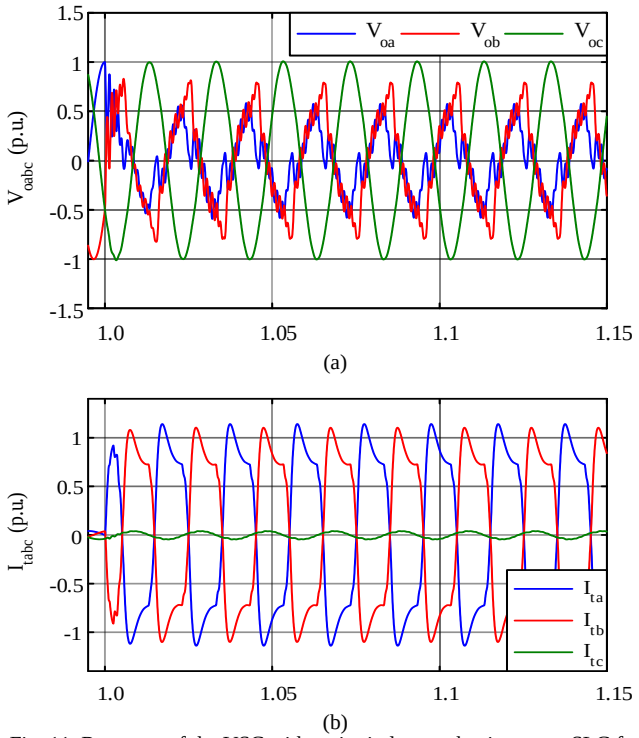


Fig. 11. Response of the VSC with anti-windup mechanism to an SLG fault, (a) output voltages, (b) terminal currents.

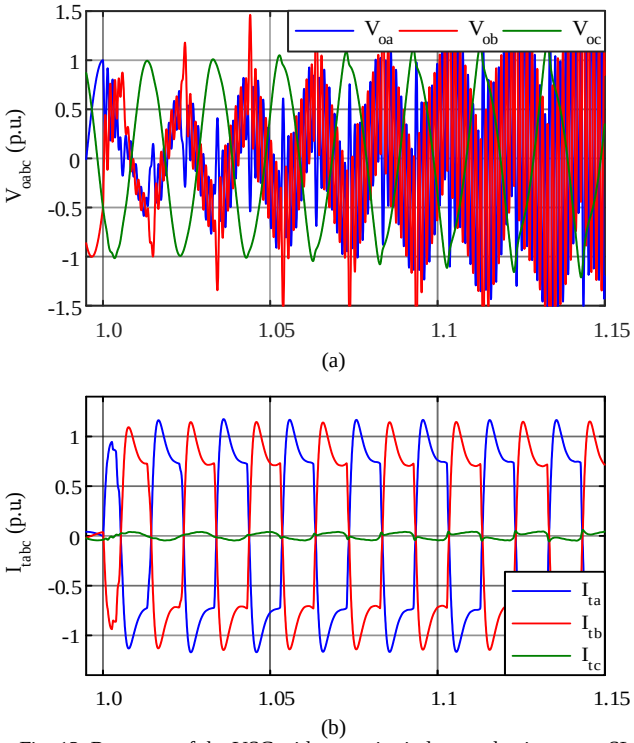


Fig. 12. Response of the VSC without anti-windup mechanism to an SLG fault, (a) output voltages, (b) terminal currents.

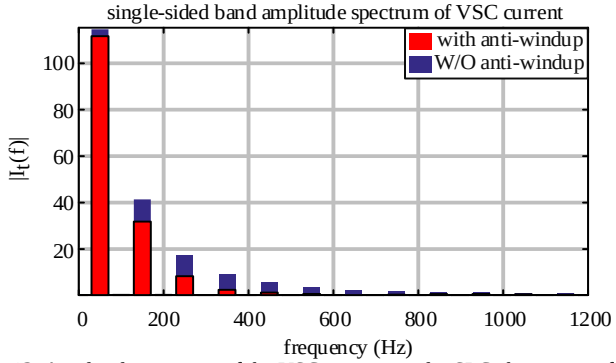


Fig. 13. Amplitude spectrum of the VSC currents under SLG short circuit fault with and without anti-windup mechanism.

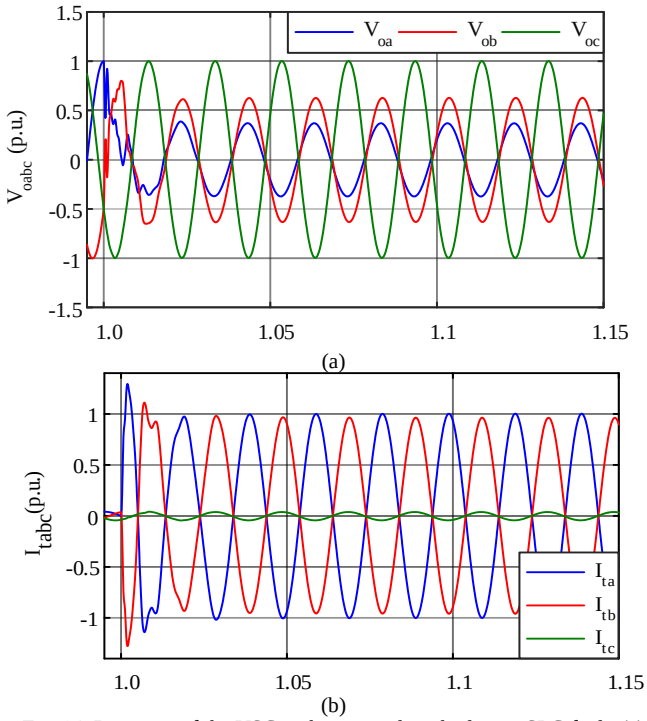


Fig. 14. Response of the VSC with proposed method to an SLG fault, (a) output voltages, (b) terminal currents.

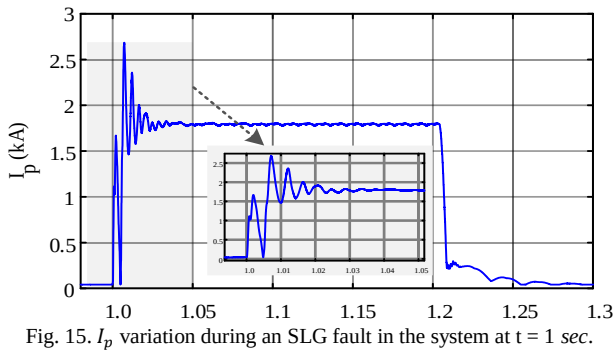


Fig. 15. I_p variation during an SLG fault in the system at t = 1 *sec*.

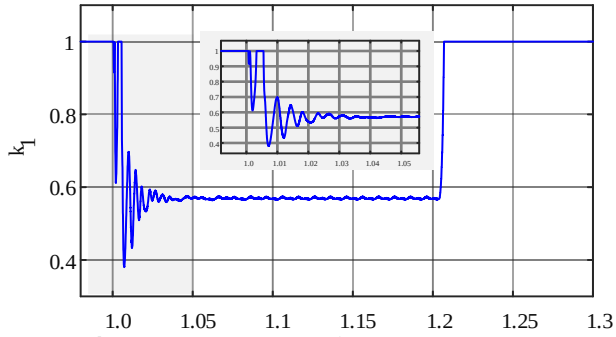
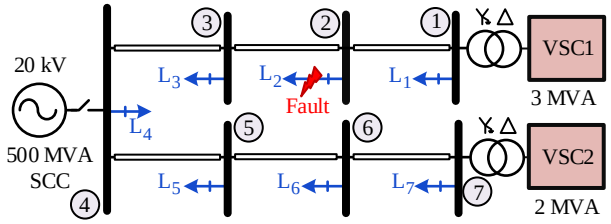


Fig. 16. k_1 variation during an SLG fault in the system at t = 1 sec.



Line impedances:
Positive seq.= 0.17+j0.36 Ω/km Zero seq.= 0.35+j1.5 Ω/km
Lines length:
ℓ12=3km; ℓ23=7km; ℓ34=12km; ℓ45=15km; ℓ56=10km; ℓ67=6km;

Fig. 17. The test distribution system with two VSCs.

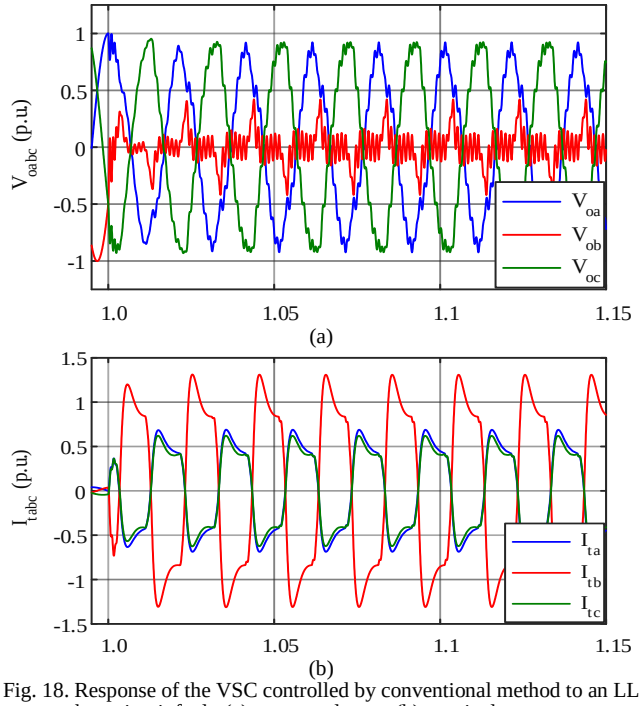


Fig. 18. Response of the VSC controlled by conventional method to an LL short circuit fault, (a) output voltages, (b) terminal currents.

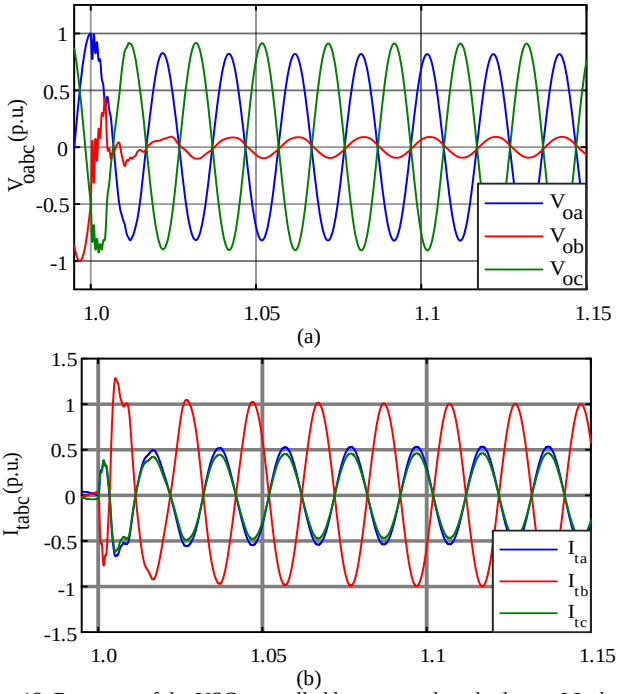


Fig. 19. Response of the VSC controlled by proposed method to an LL short circuit fault, (a) output voltages, (b) terminal currents.

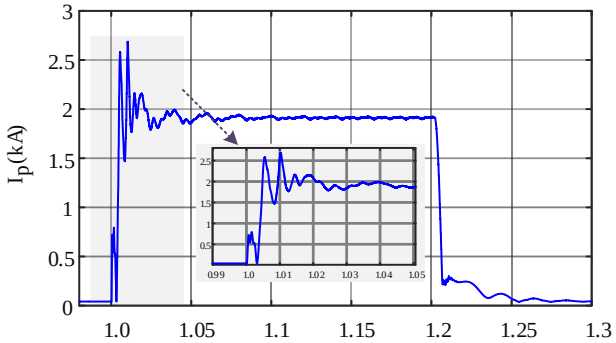


Fig. 20. I_p variation during an LL fault in the system at t = 1 sec.

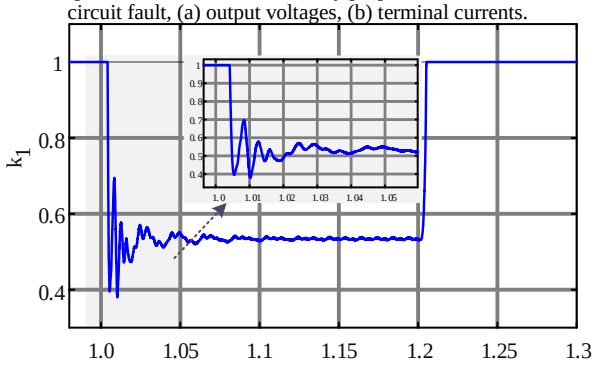


Fig. 21. k_1 variation during an LL fault in the system at t = 1 sec.

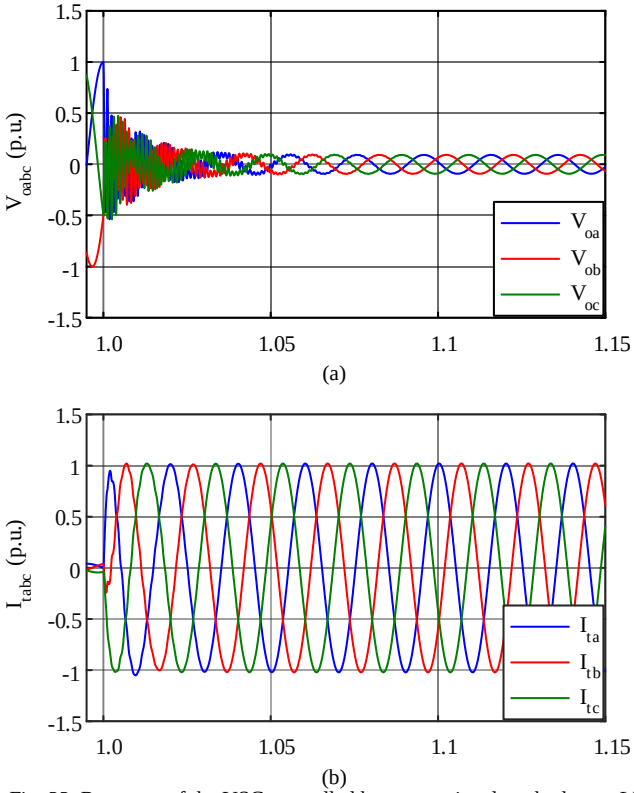


Fig. 22. Response of the VSC controlled by conventional method to an LLL short circuit fault, (a) output voltages, (b) terminal currents.

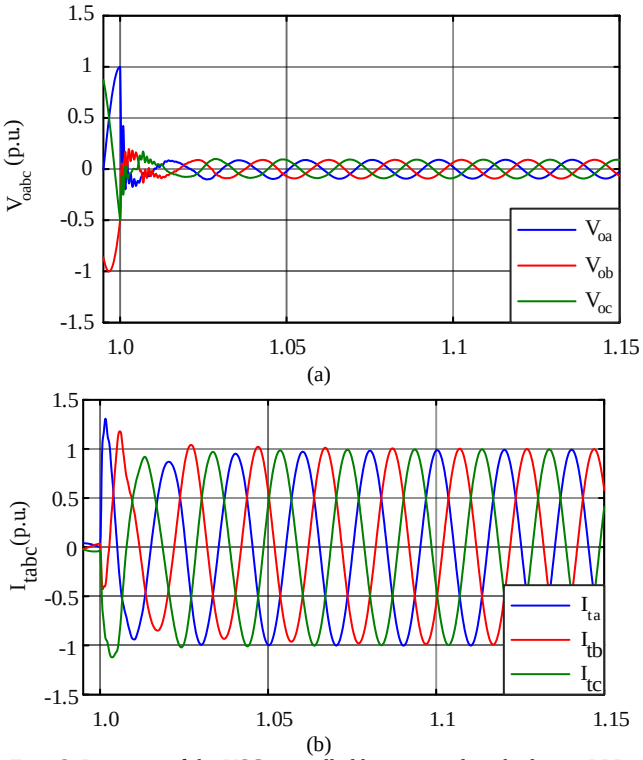


Fig. 23. Response of the VSC controlled by proposed method to an LLL short circuit fault, (a) output voltages, (b) terminal currents.

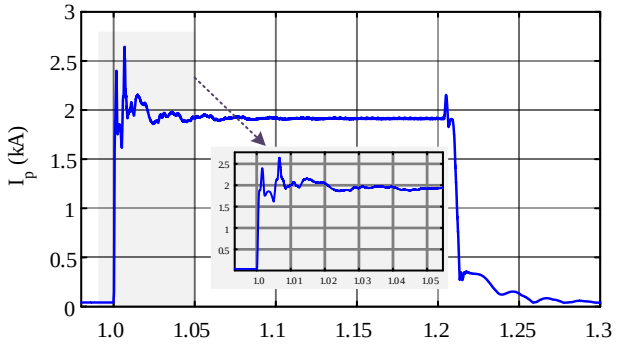


Fig. 24. I_p variation during an LLL fault in the system at t = 1 *sec*.

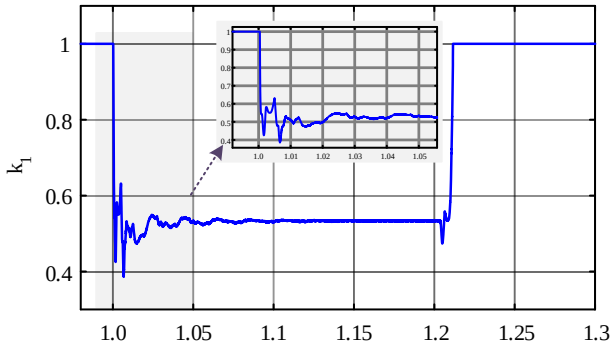


Fig. 25. k_1 variation during an LLL fault in the system at t = 1 *sec*.

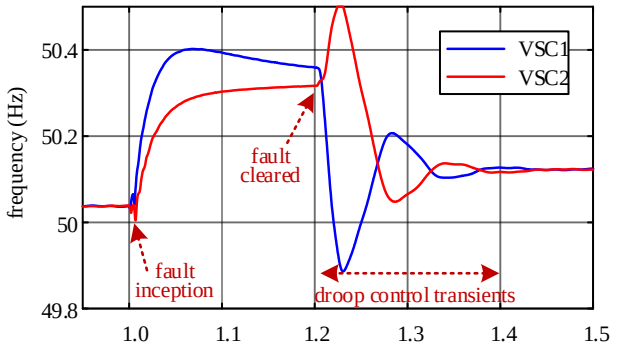


Fig. 26. The frequency of VSCs based on droop control.

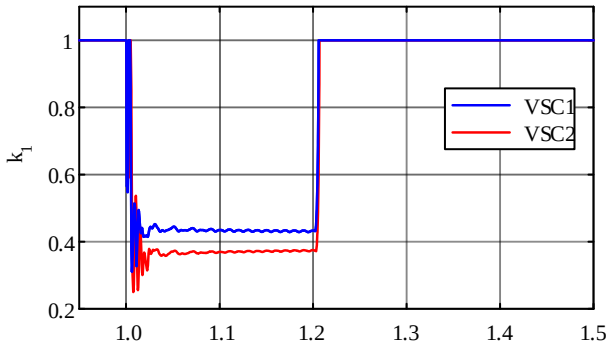


Fig. 27. k_1 for VSCs under SLG short circuit fault.

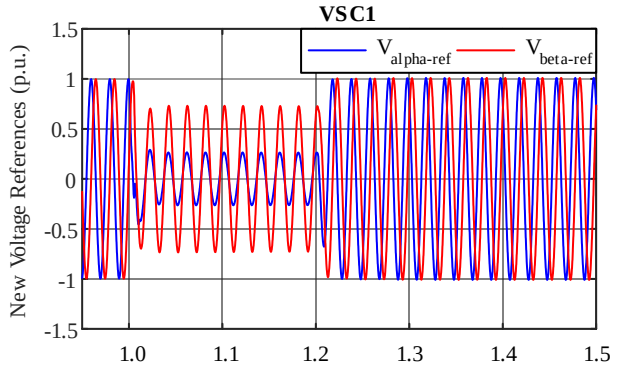


Fig. 28. New voltage references for VSC1 based on proposed method under SLG short circuit fault in αβ frame.

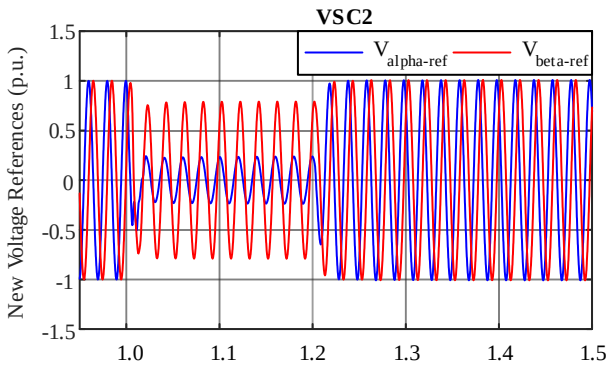


Fig. 29. New voltage references for VSC2 based on proposed method under SLG short circuit fault αβ frame.

The load values of the simulated distribution system are given in Table III. The VSCs parameters which are not shown in Fig. 17 are equal to corresponding values in Table I. It should be noted that the loads are modeled with delta connection because the loads of low voltage system are connected to medium voltage via DYg transformer. The total apparent power of the loads is 2.33 MVA.

Table III. Parameters of the simulated test system with two VSCs

	Active Power (kW)			Power Factor		
Load #	ab	bc	ca	ab	bc	ca
1	124.5	125.1	131.9	0.96	0.97	0.97
2	163.4	150	157.5	0.95	0.94	0.97
3	158.1	145.8	151.6	0.95	0.94	0.96
4	85	90.3	86.8	0.98	0.98	0.97
5	92.7	89.8	95.2	0.94	0.95	0.95
6	70.9	66.4	71.2	0.96	0.96	0.97
7	67.7	59	67.6	0.96	0.96	0.98

A solidly grounded SLG short circuit fault is applied to the distribution line connected to the Bus 2 of Fig. 17 at t = 1 *sec*. The line protection relay issues a trip, and the fault is cleared within 200 msec by the protection system installed at the beginning of that feeder, and the corresponding loads are disconnected.

Fig. 26 shows the frequency of the VSCs, which are generated by droop controller. During the short circuit, the frequencies deviate from the steady state value, however they are within the normal range. After fault clearance and droop control transients, the frequencies are settled in the new steady state value because of the disconnection of loads in Bus 2.

As shown in Fig. 27, upon fault inception, the current limiters reduce the gains k_1, which limits the output currents of the VSCs. Since the same virtual impedance of $k_2 = 4.5$ has been selected for both VSC, and considering different capacities used for VSCs, different values for k_1 are achieved as shown in the figure. As it was expected, the values of k_1 taken from Fig. 27 and those values calculated by (36) are the same.

Upon fault inception, the proposed voltage reference generation scheme reduces the references as shown in Fig. 28 and Fig. 29 in αβ frame for VSC1 and VSC2, respectively. Also, the three phase output currents and voltages of VSCs are demonstrated in Fig. 30-Fig. 31. As shown in these figures, the outputs are pure sinusoidal waveforms, and currents are limited to the corresponding maximum value. It should be noted that the base values for per-unit calculation have been selected based on nominal rating of each VSC.

All the above-mentioned propositions and explanations

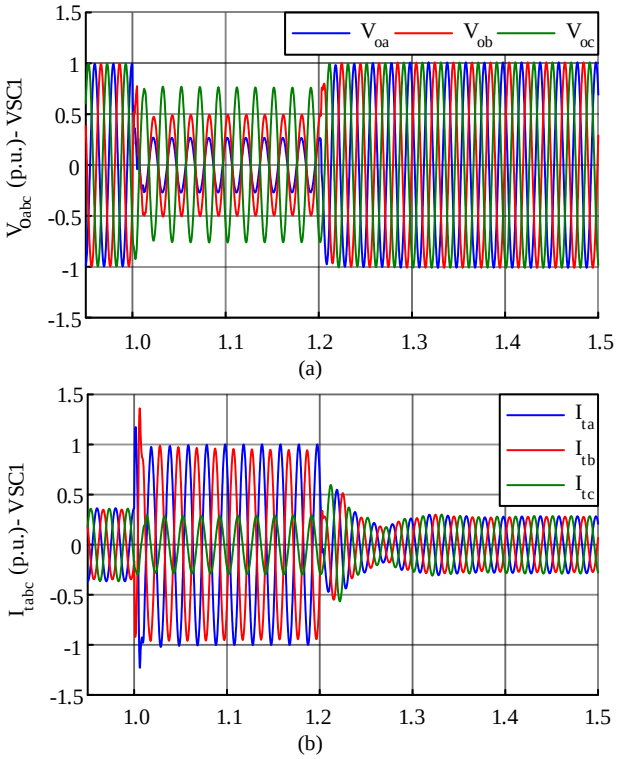


Fig. 30. Response of VSC1 to an SLG short circuit fault, (a) output voltages, (b) terminal currents.

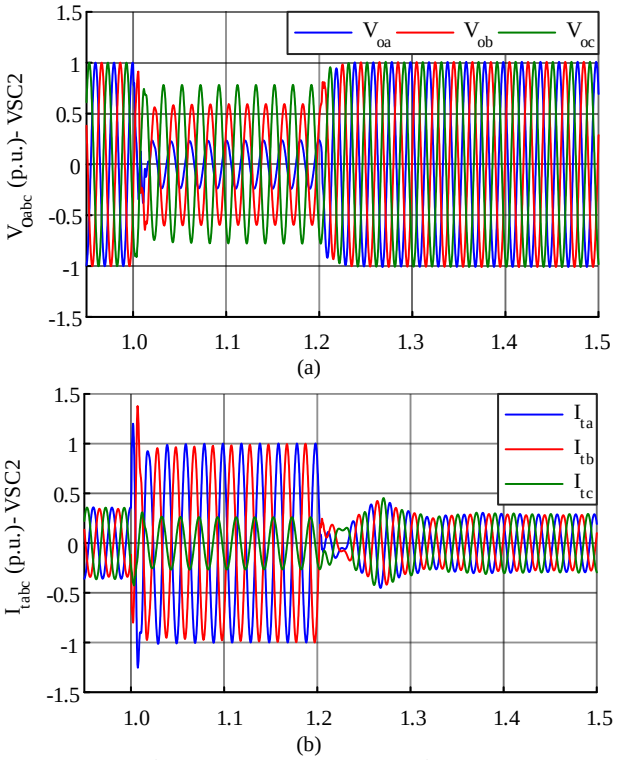


Fig. 31. Response of VSC2 to an SLG short circuit fault, (a) output voltages, (b) terminal currents.

demonstrate that using proposed method VSCs properly ride through the short circuit faults, and when the faults have been cleared by the corresponding protection system, the system comes back to normal operation, which ensures the continuity of the electricity supply.

VI. Conclusion

In this paper, the behavior of a grid forming voltage-source converter (VSC) based distributed energy resources (DERs) under both asymmetrical and symmetrical short circuit faults is analyzed. In this respect, the conventional control diagram of VSC without considering necessary FRT prerequisites has been analyzed to get detailed insight about VSC operation under short circuit condition. Also, a comprehensive review on existing methods on FRT of grid forming VSCs has been presented and discussed. It is shown that the existing methods either suffer from distorted waveforms or need to detect the fault inception and clearance instances to change the control mode in short circuit condition, which complicates the control system and may reduce the reliability. Accordingly, an adaptive voltage control scheme is proposed, which avoids any distortion in short circuit condition and keeps the main voltage controller active in this condition without any need to change the control mode and control system. In this respect a virtual impedance based voltage reference generation method is proposed. Also, a fast sinusoidal current limitation strategy is introduced. The proposed method does not affected by fault type, location and severity. To verify the proposed control strategy, the state space modeling of the system for worst possible cases has been performed. Accordingly, eigenvalue analysis with corresponding participation factors are presented to show the stability of the proposed method for the worst cases. Further, a complete set of simulation results for different fault types are presented and compared with another existing method. Simulation results for a test system with two VSCs are presented to demonstrate the proposed method performance in this circumstances.

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