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Intrinsic-Capacitance-based Differential Power Processing for Photovoltaic Modules

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***Abstract*— Partial shading reduces energy production and affects the lifetime of the overall PV system. To mitigate the mismatch effects caused by partial shading, several PV cell- or sub-panel-level techniques employing power electronics have been proposed in the literature, where discrete passive components, e.g., inductors and capacitors, are also used. In this paper, a differential power processing (DPP) technique, which utilizes only the intrinsic capacitance of solar cells, is introduced for small-scale PV applications. The developed DPP topology mitigates the mismatch effects by operating all PV cells at or near to their corresponding maximum power points (MPPs) even under mismatch conditions. The analysis of the topology and its comparison with the frequently used series- and series-parallel (SP)-connected techniques, are presented to validate its efficacy and operational capabilities, through simulation results. Moreover, a prototype is built to verify the topology. The experimental results confirm the elimination of multiple power peaks under mismatch along with maintaining the same voltages across the PV panels.**

***Keywords*—Partial shading, mismatch, Photovoltaic (PV), switched-capacitor (SC), differential power processing (DPP), solar cells, maximum power point (MPP).**

I. Introduction

Energy production from solar photovoltaic (PV) systems is contingent on the amount of sunlight appearing at the PV panel surface. In PV panels, the output current directly depends on the solar irradiance. If any part of a PV panel receives a different amount of irradiance in comparison to the other parts, a mismatch is created due to difference in the series current. This mismatch causes power reduction and induces stresses (e.g., hotspots) over the other PV panels in system. This stress not only affects the life of the PV panels itself but the overall system by reducing the overall power and life of a system. In general, on commercially available PV panels, there are usually three available sub-panels in series, as shown in Fig. 1. Each PV sub-panel has a parallel-connected bypass diode *D* to limit the mismatch caused by non-ideal conditions [1]–[3]. If there is no mismatch, the bypass diode *D* remains OFF, as shown in Fig. 1(b). However, under mismatch in Fig. 1(c), the bypass diode *D* associated with the shaded sub-panel is in ON-state and bypasses the PV sub-panel with lower current to keep the other non-shaded PV sub-panels unaffected. Hence, the bypass diodes help to maintain the current passing through the other sub-panels.

In the bypass diode technique, low power-producing PV sub-panels are bypassed by the diodes. Afterwards, multiple power peaks appear, as shown in Fig. 2. These multiple peaks increase the complexity of traditional tracking algorithms to track the global maximum power point (GMPP). Therefore, global maximum power point tracking (GMPPT) algorithms are required to track the maximum power point (MPP) [4], [5].

To mitigate the mismatch effects, PV panel- or sub-panel-level power electronics technologies are being employed in solar PV systems [6]–[12]. For instance, sub-panel-level differential power processing (DPP) topologies are the emerging mismatch mitigation techniques. These panel- or sub-panel-level DPP techniques only process the mismatched power instead of the full power. More importantly, DPP techniques also help to achieve the voltage equalization at the panel- or sub-panel-level [13]–[18]. However, the PV-PV DPP architectures are the most well-known due to their simplicity, cost-effectiveness, and scalability. Usually, PV-PV DPP converters are bi-directional, which allow the PV panels or sub-panels to operate near their MPPs.

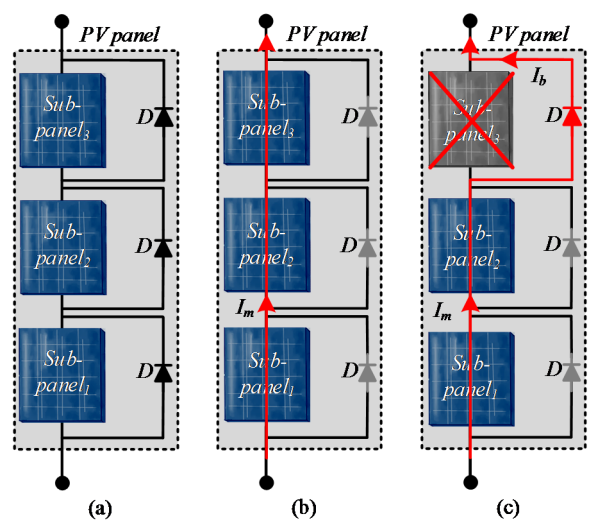


Fig. 1. A photovoltaic (PV) panel consists of three series-connected PV sub-panel (*sub-panel*$_1$, *sub-panel*$_2$, and *sub-panel*$_3$) with parallel-connected bypass diodes: (a) general schematic, (b) current flow no shading, and (c) current flow under shading on a PV *sub-panel*$_3$, which is bypassed by a diode *D*. Here, I_m is the module current and I_b is the current passing through the bypass diode [1].

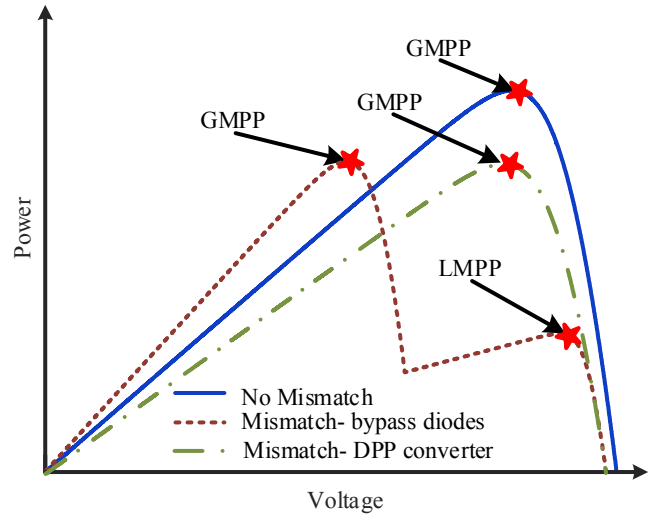


Fig. 2. Power-voltage (*P-V*) characteristics under shading and no shading with bypass diode and differential power processing (DPP) converter.

Many attractive PV-PV DPP topologies have been developed, i.e., energy recovery [19], buck-boost [20], and switched-capacitor (SC) [8], [9]. However, these DPP topologies use additional passive components and several switches for a fewer number of PV sub-panels. Hence, it increases the cost and complexity of the overall DPP topology. Another capacitor-less DPP topology using the diffusion charge redistribution (DCR) was proposed in [21]. This DCR topology utilizes diffusion capacitance C_d of PV cells, as shown in Fig. 3(a). A diffusion capacitance is a parasitic capacitance generated due to the *p-n* junction of PV cells and its values vary from microfarads to hundreds of microfarads [22]. This diffusion capacitance is used as a switching capacitor, which makes the PV-PV DPP family even simpler by eliminating discrete passive elements. However, DCR can only be applied to the cases with an odd number of PV cells. Hence, the practicality of the DCR-based DPP topology is limited.

In the light of the above, this work introduces a DPP converter utilizing the diffusion capacitance of PV cells, which can be applied to even number of PV cells. It can also be applied to standard small PV panels in various applications, e.g., drones [23], [24], wearable bags [25], moon rover [26], and other small portable devices. For other PV applications (e.g., electric cars), external capacitances are required to achieve the same goal as the value of diffusion capacitances becomes small due to the series connections of PV cells. The rest of the paper is organized as follows. The working principle of the improved DCR-based DPP is presented in Section II. Section III shows the simulation results and compares the developed architecture with other existing traditional solutions. Experimental results are presented in Section IV. Finally, Section V concludes the work.

II. Intrinsic Capacitance-based Topology

The introduced intrinsic diffusion capacitor-based DPP methodology is presented in this section. The topology has a ladder-based PV-PV architecture, where the mismatched power is processed by the diffusion capacitor C_d, as shown in Fig. 3(b).

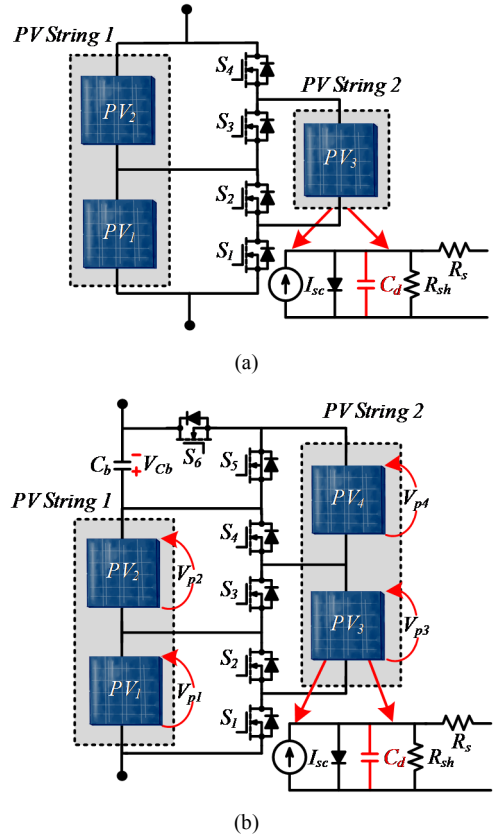


Fig. 3. Differential power processing (DPP) converters-based on: (a) diffusion charge redistribution (DCR) [21] and (b) modified topology. Here, C_d is the diffusion capacitance, I_{sc} is the light generated current, R_{sh} is the shunt resistance, and R_s is the series resistance of the solar PV cells.

The diffusion capacitor C_d of each solar PV cell serves as intermediate energy storage to eliminate the difference between the generated and extracted power from the solar cells during mismatch. The main advantage of the topology is that it has only two modes of operation. Assuming, that two PV cells are connected in series. One PV cell has a full irradiance and the other has a shading. The mismatch or difference of current will be diverted to the diffusion capacitor C_d during mode 1 from fully irradiated PV cell to store the energy temporary here. In mode 2, it releases that energy. By doing this, the series current is maintained at a level of a solar PV cell, which is shaded from one of the two series-connected PV cells. Hence, the low power-producing PV cell starts to contribute and there is no need to bypass it with a bypass diode as the current mismatch between the series-connected cells is eliminated. Moreover, the switches are operating at high frequency, which helps in achieving the voltage equalization across the PV cells. In continuation, the equivalent circuits of a DPP topology are shown in Fig. 4, which has two modes of operation. Six MOSFET devices ($S_{1\sim6}$) are used to redistribute the mismatch charges equally between two small PV strings (PV string 1 and PV string 2) by using their intrinsic capacitances, where each PV string containing two cells. Moreover, the MOSFET devices are switched at a duty cycle of 50%. During mode 1, the MOSFETs S_1, S_3, and S_5 are switched ON, as demonstrated

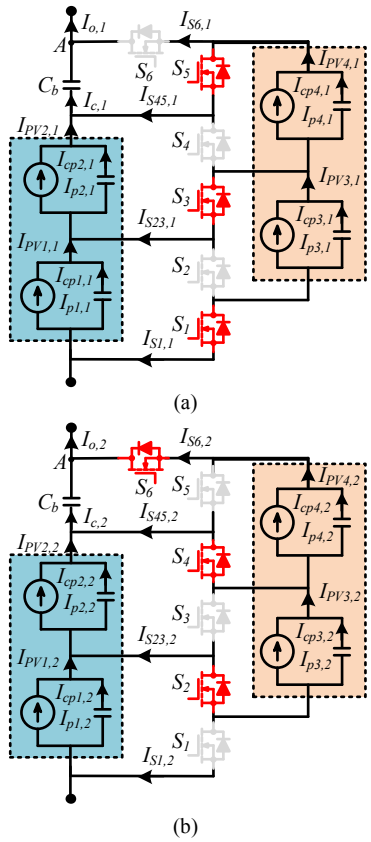


Fig. 4. Current flow in the introduced intrinsic diffusion capacitance-based DPP topology: (a) mode 1 and (b) mode 2.

in Fig. 4(a). In mode 2, the others are switched ON, while S_2, S_4, and S_6 become OFF, as shown in Fig. 4(b).

To further explain the operational principle, a current flow during both modes is shown in Fig. 4. In Fig. 4, the diffusion capacitance distributes the charges based on the mismatch between the PV cells. To simplify the analysis, a light generated current and diffusion capacitance is taken into account in the equivalent circuit model of PV cells (see the Fig. 3(b)). The other parameters are ignored, e.g., diode, series resistance (R_s), and shunt resistance (R_{sh}).

In Fig. 4, it is considered that all PV cells are generating the same amount of photocurrents $I_{pi,m}$ (number of cells: i=1…4 and number of operating modes: m=1 or 2) over the complete switching period. The photocurrent source for the cells in each mode is the same. Hence, by employing the charge balance principle on diffusion capacitors C_d, the amount of energy goes in and out of capacitors is the same. Therefore, the overall photocurrent and cell current generated by respective PV cell in both operating modes is the same, which can be written as

$$I_{PVi,1} = I_{PVi,2} = I_{PVi,m} \tag{1}$$

$$I_{PVi,m} = I_{pi,m} \tag{2}$$

where $I_{PVi,m}$ (number of cells: i=1…4 and number of operating modes: m=1 or 2) is the overall cell current. Furthermore, $I_{PVi,1}$ and $I_{PVi,2}$ are the cell currents for modes 1 and 2, respectively.

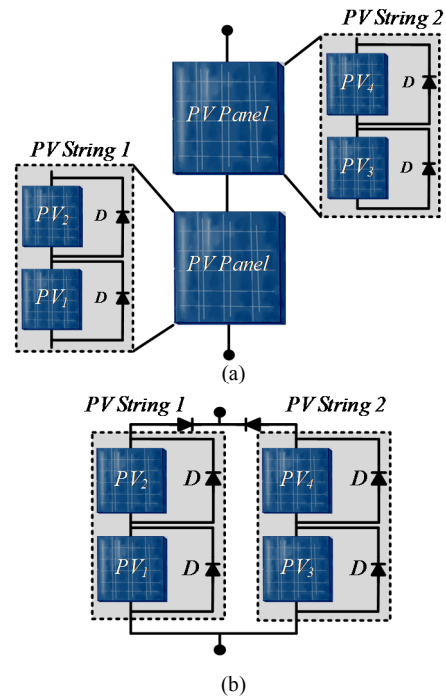


Fig. 5. PV connection techniques in a PV system: (a) PV cells in series connection in the form of two PV strings (string 1 and string 2) and (b) PV string 1 and string 2 connected in a series-parallel (SP) connection.

Moreover, the PV_1 is connected in parallel to PV_3 and PV_2 to PV_4 during mode 1. Similarly, during mode 2, PV_2 is connected in parallel to PV_3 and PV_4 to capacitor C_b. Hence, by using Kirchhoff's current law (KCL), we can further write (3) and (4) for these two modes as

$$I_{o,1} = I_{c,1} = I_{PV2,1} + I_{PV4,1} = I_{PV1,1} + I_{PV3,1} \tag{3}$$

$$I_{o,2} = I_{c,2} + I_{PV4,2} = I_{PV2,2} + I_{PV3,2} + I_{PV4,2} = I_{PV1,2} \tag{4}$$

where $I_{c,1}$ and $I_{c,2}$ are currents flowing through capacitor C_b during modes 1 and 2, respectively. Similarly, $I_{o,1}$ and $I_{o,2}$ are output currents during modes 1 and 2, respectively.

III. Simulated Results

In order to analyze and compare the improved intrinsic diffusion capacitor-based DPP topology in Fig. 3(b), the two most commonly used traditional PV connections are considered, i.e., the series connection in Fig. 5(a) and series-parallel (SP) connection in Fig. 5(b). For this purpose, two PV strings are used, where each string contains two PV cells, as shown in Fig. 5. Simulations are performed in PSIM under various partial shading scenarios, as depicted in Table I. In these cases, irradiance (E) is varied over PV cells shown in Figs. 3(b) and 5. The irradiance over PV_1, PV_2, PV_3, and PV_4 are represented as E_1, E_2, E_3, and E_4, respectively. Moreover, the rating of PV cells is given in Table II. The switching frequency of 50 kHz is used, where the switching devices are working at a duty cycle of 50%.

Furthermore, the inherent diffusion capacitor C_d is 40 uF and the capacitor C_b is 50 uF by considering the capacitor

TABLE I
MISMATCH CASES.

Irradiance (kW/m^2)	Case 1	Case 2	Case 3
E_1	0.30	0.50	1.00
E_2	1.00	1.00	0.75
E_3	0.30	0.50	0.60
E_4	0.70	0.20	0.70

TABLE II
RATINGS OF THE PV CELL UNDER STUDY.

Peak Power (P_{max})	5.01 W
Voltage at maximum power (V_{mp})	3.39 V
Current at maximum power (I_{mp})	1.48 A
Open-Circuit Voltage (V_{oc})	4.50 V
Short-Circuit Current (I_{sc})	1.55 A

voltage ripples ΔV_d and ΔV_b less than 5%. C_d depends on the biasing voltage, the lifetime of the charge carriers (τ), and the area of the cell. In [10], the value of C_d is larger than 6.0 mF for a PV cell size of 125 mm x 125 mm at 0.574 V_{MPP} (voltage at maximum power point). In other examples, C_d is 100 µF at 0.43 V for a PV cell size of 20 mm × 40 mm with the carrier lifetime of 4.12×10^{-5} s at 0.43 V and around 20 uF for a PV cell size of 152 mm x 152 mm with τ seeing 6.5×10^{-7} s [10]. Hence, the selected value of C_d is 40 uF for the PV cells in a string of series-connected PV cells. C_d can also be calculated as [22], [27]

$$C_d = \frac{1}{2\pi f R_{sh}} \tag{5}$$

where f is the switching frequency and R_{sh} is the parallel or shunt resistance of a solar cell.

In continuation, Fig. 6 presents the simulation results for the developed DPP topology and the other two traditional series and SP connections. In Fig. 6, the output power from the introduced DPP technique is higher than the other two traditional PV connections using bypass diodes under mismatch cases given in Table I. The output power yield for the introduced DPP architecture is 11.02 W, 10.77 W, and 14.98 W for case 1, case 2, and case 3, correspondingly. However, under mismatch case 1, case 2, and case 3, it is 7.26 W, 5.59 W, and 10.94 W for the series connection, respectively. Lastly, it is 6.38 W for case 1, 7.90 W for case 2, and 8.53 W for case 3 in the SP connection. Moreover, the results in Fig. 6 show that under a severe mismatch case, i.e., case 2, the DPP technique is extracting more than 90% of the available power while series connection is extracting only around 50% and the SP connection is around 70%.

The P-V characteristics are presented in Fig. 7 for the system shown in Fig. 3(b) under the mismatch cases given in Table I. These P-V curves show that the developed DPP topology has only one single peak, under all mismatch cases. Hence, the DPP topology has also simplified the problem of tracking the MPP. Therefore, a simple and cost-effective MPPT algorithm can be employed, which reduces the complexity of the overall system. Moreover, the photocurrent and PV cell

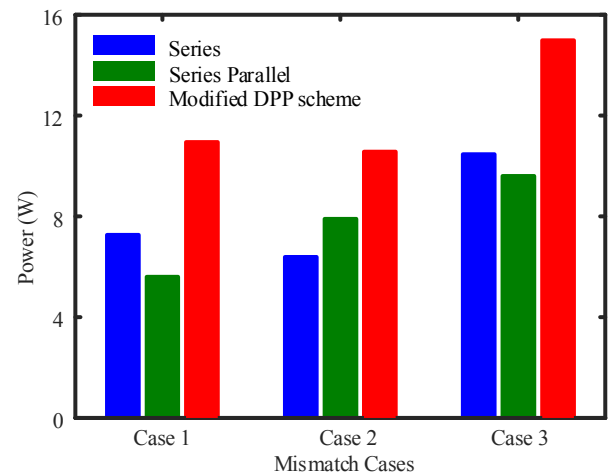


Fig. 6. Power extraction from the PV systems (i.e., the series connection in Fig. 5(a), series-parallel connection (SP) in Fig. 5(b), and intrinsic diffusion capacitance-based voltage equalizer in Fig. 4) under the mismatch cases in Table I.

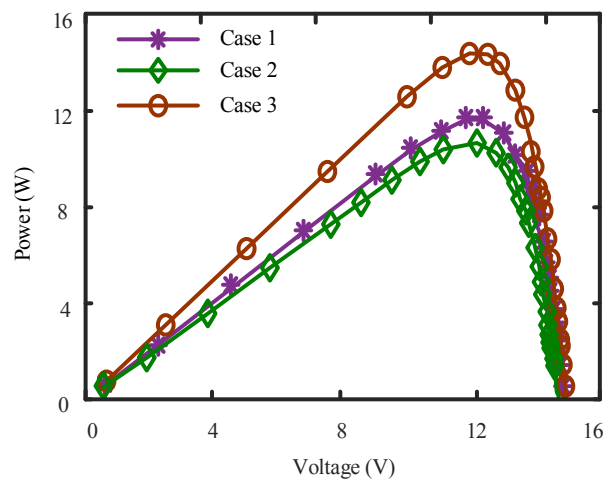
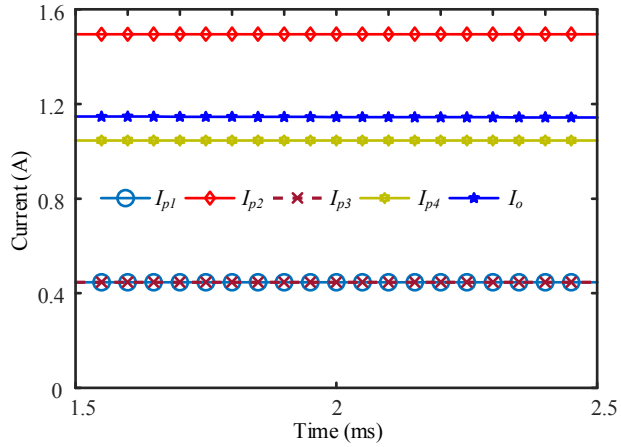


Fig. 7. Power-voltage (P-V) characteristics for the intrinsic diffusion capacitance-based voltage equalizer in Fig. 3(b) under the mismatch cases given in Table I.

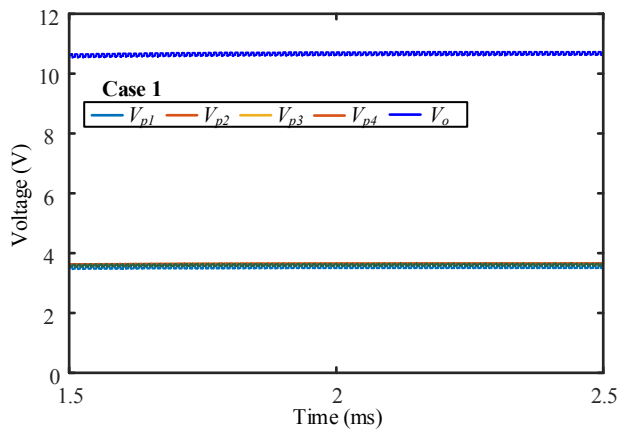
voltages under case 1 are presented in Fig. 8. In Fig. 8(a), the photocurrents I_{p1}, I_{p2}, I_{p3}, and I_{p4} are shown for the PV cells PV_1, PV_2, PV_3, and PV_4, respectively under mismatch case 1. Similarly, in Fig. 8(b), the voltages across the cells, i.e., PV_1, PV_2, PV_3, and PV_4 are around 3.5 V. Moreover, the voltage across the load (V_o) in Fig. 8 (b) is 10.48 V. Overall, the introduced intrinsic diffusion capacitor-based DPP topology can help to achieve almost identical voltages across the PV cells. Hence, the introduced topology can eliminate this multiple power peaks issues in the PV string.

IV. EXPERIMENTAL RESULTS

A prototype of the modified topology using four PV panels was built. Due to the unavailability of small PV cells, 45-W PV panels were used at lower power similar to small PV cells. Each PV panel consists of 36 cells in series. Therefore, the external capacitance of 40 uF is connected in parallel across both PV panels in a string 2, as shown in Fig. 3(b) to achieve the desired operation discussed above. Moreover, the capacitor C_b in



(a)



(b)

Fig. 8. Simulated results under mismatch case 1 given in Table I for the introduced intrinsic switched-capacitor-based DPP architecture: (a) photocurrents and overall string current (b) PV cell voltages under mismatch case 1 given in Table I for the introduced intrinsic switched-capacitor-based DPP architecture. Here, I_{p1}, I_{p2}, I_{p3}, and I_{p4} are the photocurrent from PV panel PV_1, PV_2, PV_3, and PV_4, respectively. I_o is the overall current towards the load. Similarly, V_{p1}, V_{p2}, V_{p3}, and V_{p4} are the voltages across the PV panel PV_1, PV_2, PV_3, and PV_4, respectively. Lastly, V_o is the output voltage across the load.

Fig. 3(b) is 50 uF by considering ΔV_b less than 5%. The prototype was operated at 100 kHz. The setup is shown in Fig. 9, which consists of four PV panels (PV_1, PV_2, PV_3, and PV_4) and a digital signal processing (DSP) from Texas Instruments (TI F28379D). The PV panels are connected in parallel with DC power supplies, which are operating in the constant-current (*CC*) mode to achieve the desire PV panel characteristics, as discussed in [28]. Moreover, different mismatch conditions can be generated by adjusting the value of the current in the *CC* mode, which is given in Table III.

The *P-V* characteristics are obtained by recording both the overall output voltage and current by sweeping the variable load. For testing, various mismatch scenarios are developed, which are given in Table III. The obtained experimental *P-V* characteristics are shown in Fig. 10 for the mismatch conditions mentioned in Table III. It can be seen from Fig. 10, there is only one power peak. Hence, the obtained *P-V* characteristics greatly reduce the complexity of the required MPPT algorithm.

Fig. 11(a) shows the currents supplied by the DC source in *CC* mode for creating a mismatch case 1 mentioned in

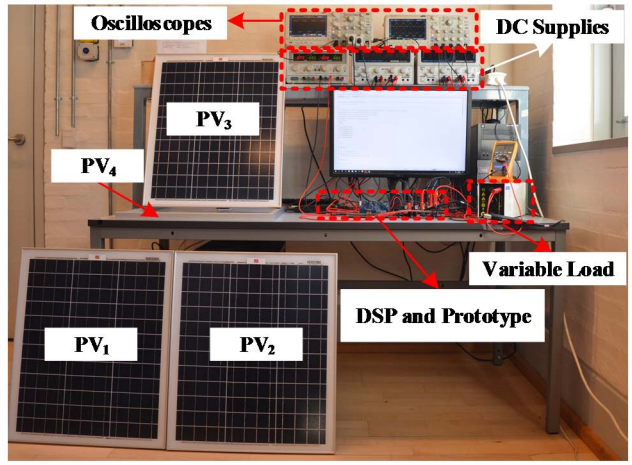


Fig. 9. Photograph showing indoor experimental setup.

TABLE III
MISMATCH CASES.

Photocurrents (A)	Case 1	Case 2	Case 3
I_{p1}	0.36	0.80	1.74
I_{p2}	1.38	1.62	1.30
I_{p3}	0.36	0.84	0.82
I_{p4}	1.03	0.30	1.24

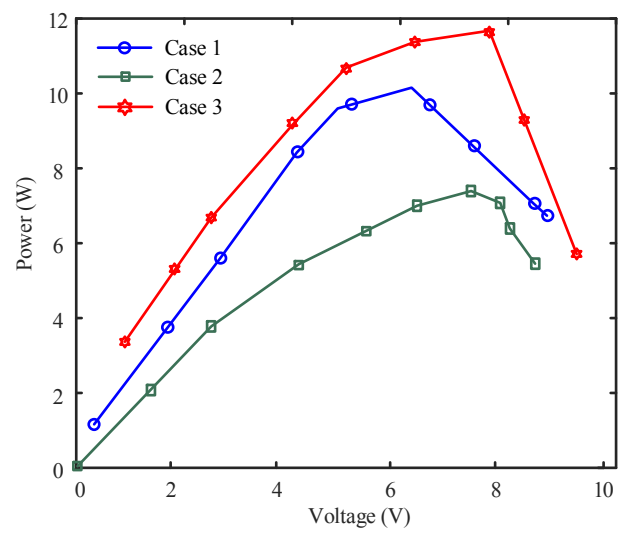
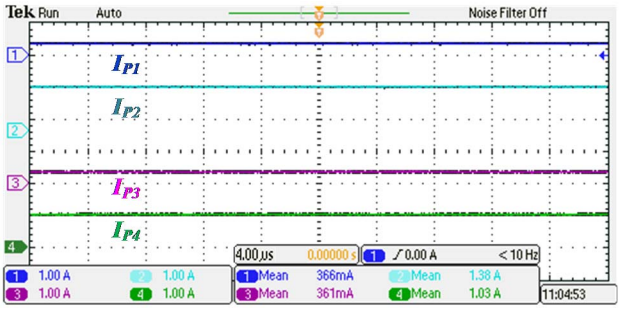


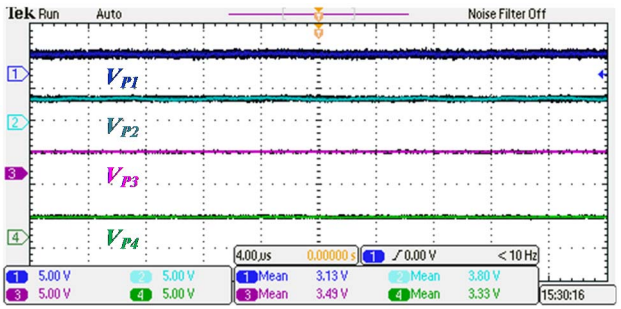
Fig. 10. *P-V* characteristic for the intrinsic diffusion capacitance-based proposed topology shown in Fig. 4 under the mismatch conditions.

Table III. Under the mismatch condition shown in Fig. 11(a), the PV panel voltages are 3.13 V, 3.80 V, 3.49 V, and 3.33 V for PV_1, PV_2, PV_3, and PV_4, respectively. It can be seen that the voltage equalization is achieved under mismatch by using the modified topology.

The developed topology can be applied to any number of PV cells, sub-panels, and panels, which can increase the applications for the switched capacitance-based DPP families. Moreover, this is a simple topology because it has only two modes of operation during mismatch, and the converter is operating at 50% duty. Furthermore, the modified topology is also cost-effective as it requires less number of components and can accommodate more PV panels as compared to other commonly existing DPP topologies. Additionally, the



(a)



(b)

Fig. 11. Experimental results under mismatch case 1 given in Table I for the introduced intrinsic switched-capacitor-based DPP architecture: (a) photocurrents from a DC source in *CC* mode (b) PV panel voltages under mismatch (case 1) for the introduced switched-capacitor-based voltage equalizer architecture. Here, I_{p1}, I_{p2}, I_{p3}, and I_{p4} are the current from the DC source, which is operating in *CC* mode connected in parallel to PV panel PV_1, PV_2, PV_3, and PV_4, respectively. Similarly, V_{p1}, V_{p2}, V_{p3}, and V_{p4} are the voltages across the PV panel PV_1, PV_2, PV_3, and PV_4, respectively.

developed DPP architecture extracts the maximum power from PV cells/panels by operating them at or near their respective MPPs, which increases the efficiency of the entire PV system.

V. Conclusion

In this paper, a switched-capacitor-based topology was introduced to mitigate the impact of mismatch on traditional PV panel's compromises of an even number of PV cells. The developed topology uses the internal diffusion capacitance of solar PV cells. However, external capacitors can also be used for PV panels, which consist of a series connection of PV cells. Moreover, the modified topology equalizes the voltage at the PV cell level, which also eliminates the multiple power peak issues in the PV system under mismatch conditions caused by partial shading. The simulation and experimental results confirm the validity of the presented converter.

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