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# Two-Stage Single-Source Full-Bridge Based Three-Phase Inverter for Medium Voltage Applications


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***Abstract*—Conventional half-bridge based three-phase inverter (HB-TPI) and neutral-point-clamped inverters (NPC) are popular in the industry. Nevertheless, they suffer from buck characteristics. To tackle the issue, this paper proposes a new full-bridge-based inverter topology that is able to develop a stepped ac voltage with low voltage stress across the components. Since the inverter side of the proposed inverter is based on a switched capacitor, it is integrated with a front-end dc-dc converter to further increase the voltage gain and avoid inrush current. Simulation results are provided to validate the feasibility and effectiveness of the proposed inverter.**



***Keywords— Inverters, voltage stress reduction, medium voltage application.***


## I. INTRODUCTION (*HEADING 1*)

Due to many increasing environmental problems, which mainly are stem from fossil fuel-based energy sources, renewable energy resources are at the center of attention in modern human societies [1], [2]. Generally, renewable energy generation systems are reliant on power electronic converters [2]-[5]. This has led to daily improvements in power electronic converter technologies [6].

Whereas many renewable energy generation systems produce dc voltages and the infrastructure of the existing power systems is based on ac voltage, inverters converting the dc voltage to ac voltage are most regarded converters in many applications [7], [8]. Among many inverters converter, the voltage source inverter stands out for their simplicity and versatility in different applications [9], [10]. The conventional three-phase inverter, which is a simple and low-cost inverter, is common in many low voltage industrial applications [9], [11]. However, due to high dv/dt, unipolar ac voltage, high Total Harmonic Distortion (THD), Electro-Magnetic Interference (EMI), high switching loss, and constraint in the voltage rating of commercially available semiconductor switches, multilevel inverters are preferred to the conventional inverter in medium and high voltage applications [12]-[14]. One of the usual multilevel inverter topologies that tackle some of the abovementioned problems is the T-type Neutral point clamped inverter [15]-[18]. This inverter, which has two unidirectional and one bidirectional switch in each phase, develops a three-level unipolar ac voltage. Therefore, the THD, dv/dt and EMI can be reduced by using this inverter. However, this inverter topology cannot reduce the voltage stress of the components and cannot be used in medium and high voltage applications. The most popular inverter in medium voltage applications is the neutral point clamped (NPC) multilevel inverter [19]. Each phase in NPC is synthesized with four semiconductors switches and two diodes. Additionally, two dividing capacitors are employed at the input side. The switches, diodes, and capacitors are exposed to half of the input dc voltage. The main deficiency of the conventional and NPC inverters is their buck characteristic as they develop peak voltage value equal to half the input dc voltage. The NPC can develop a zero voltage level along with the positive and negative voltage levels, whereas, the conventional inverter develops only positive and negative voltage levels. Thus, the NPC can decrease the THD, the EMI ,and dv/dt. On the contrary, the NPC needs six extra switches and diodes compared to the HB-TPI. It is worth mentioning that, whereas the above-mentioned inverter topologies are mid-pint clamped inverters they can limit the common-mode current (leakage current) in applications where the stray capacitors of the equipment cause difficulties [20].

In two-stage applications, in which the inverter is cascaded with a dc-dc converter (usually a boost converter), the buck characteristic limits the application of the mentioned inverters in medium-voltage applications [21]. In such applications, the components of the dc-dc converter are exposed to the full input dc voltage of the inverter. Since the NPC is required to be applicable in medium voltage applications, the mentioned problem limits the voltage rating of the two-stage NPC [22], [23]. To cover the challenge, a two-stage multilevel inverter is proposed in this paper, which is referred to as two-stage single-source full-bridge three-phase inverter (SSFB-THI). The proposed topology is comprised of three basic cells, and one dc-dc stage. All the components in the proposed topology tolerate the output voltage of the front-end boost converter (i.e. the dc- link). For a given input voltage and duty cycle, the SSFB-TPI offers a voltage gain that is two times the voltage gains of the two-stage HB-TPI and NPC.

The remainder of this work is organized as follows. In the next section, the configuration and operation concept of the proposed topology is defined. In section II the current and voltage stresses of the components are assessed. In section III the proposed inverter is compared with the HB-TPI and NPC. The performance of the proposed SSFB-TPI is scrutinized in section IV and the overall work is concluded in section V.

## II. THE PROPOSED SSFB-TPI CONFIGURATION AND OPERATION CONCEPT

The proposed inverter is shown in Fig. 1. As observed, each phase in the SSFB-TPI is composed of one full- bridge cell, one capacitor, one charging switch, and one diode. The three-phase inverter unit is cascaded with a front-end dc-dc converter. The front-end converter is synthesized with an inductor and switch. This converter can boost the input voltage and, smooth the input current. However, its main task is to avoid the inrush current of capacitors.

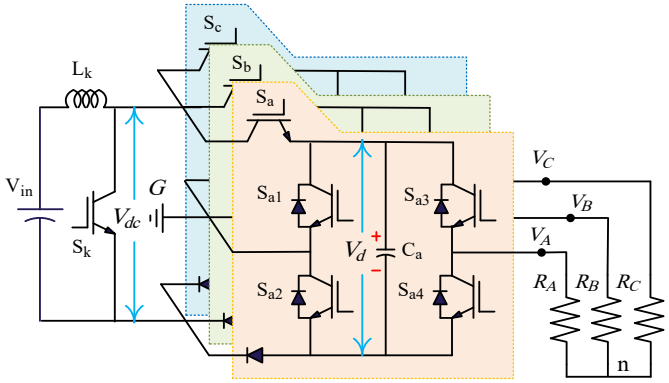



Fig. 1. Proposed two-stage single-source full-bridge based three-phase inverter.

### A. Operation Concept and Switching Strategy

The capacitors in the proposed SSFB-TIP are charged through the input dc-dc converter. By under the duty cycle of the $S_{ch}$, the voltage across the capacitors can be modulated. The capacitors voltage is given as

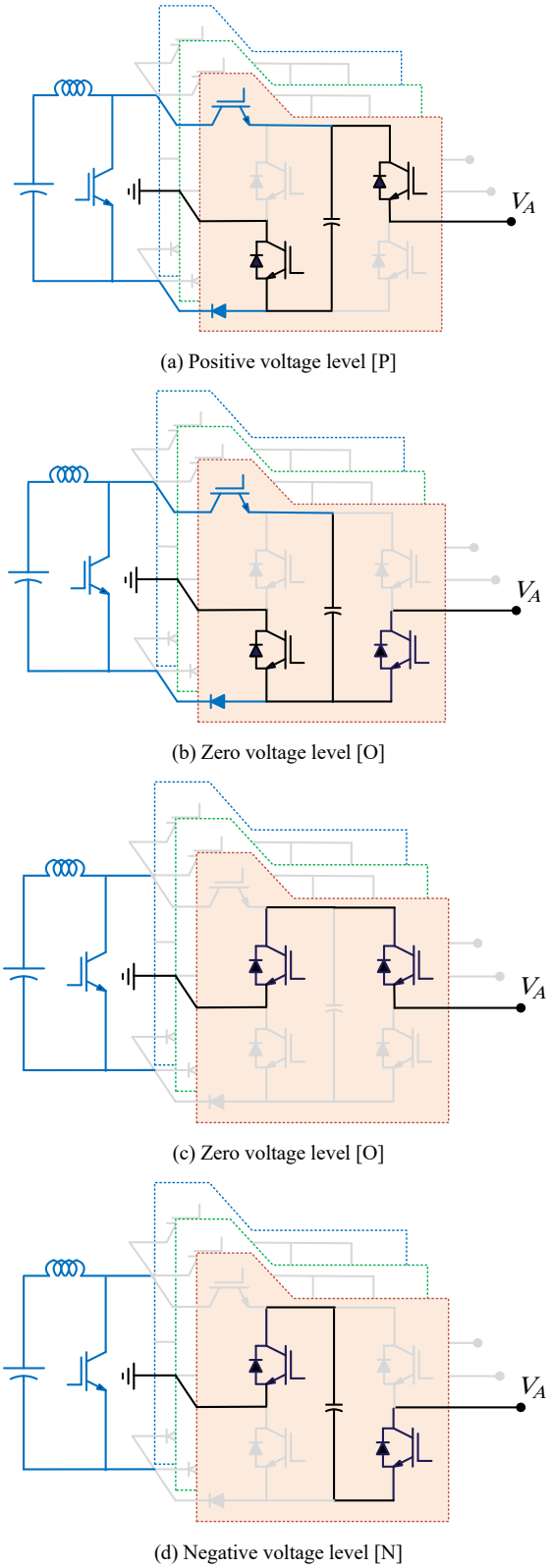
$$V_d = V_{dc} = \frac{V_{in}}{1-d} \quad (1)$$

where $V_d$, $V_{dc}$, $V_{in}$, and $d$ are the voltage across the capacitor, dc-link voltage, input voltage, and duty cycle, respectively. Each phase in the SSFB-TPI can develop positive, negative, and zero voltage levels.

In order to define the switching status, let's separate the dc and ac sides. The dc input, the dc-dc converter, and charging diodes and switches are considered as the dc side and the Full-bridges as the ac side. Since each phase in the ac side contains a full bridge, three voltage values ($\pm v_d$ and zero) are possible at each phase. For more clarity, the possible current paths in phase A are depicted in Fig. 2. In this figure, the symbols P, N, and O represent positive, negative, and zero voltage levels of the phases, respectively.

It is to be noted that, to prevent any undesired short circuit path at the dc side, the switches $S_{a1}$, $S_{b1}$ and $S_{c1}$ should have complementary states with switches $S_a$, $S_b$, and $S_c$.

Many switching strategies can be employed to compute the switching signals of the three-phase configuration of the proposed inverter. The possible switching actions and the related phase- and phase-to-phase voltages values are listed in Table I. Additionally, the switching vectors of the proposed inverter are depicted in Fig. 3.




(a) Positive voltage level [P]

(b) Zero voltage level [O]

(c) Zero voltage level [O]

(d) Negative voltage level [N]

Fig. 2. Current paths of the voltage levels of phase A in the SSFB-TPI.

For more clarity, the logic schematic of the switching signal computation process when using the level-shifted switching strategy is exhibited in Fig. 4.

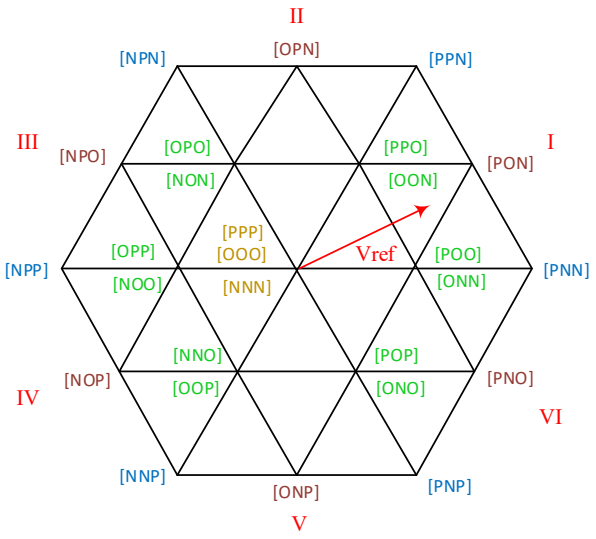



Fig. 3. Switching vectors of the proposed SSFB-TPI

TABLE. I VOLTAGE VECTORS AND POSSIBLE VOLTAGE LEVELS

| Pattern $[\phi_c,\phi_b,\phi_a]$ | $V_{an}$ | $V_{bn}$ | $V_{cn}$ | $V_{ng}$ |
|---|---|---|---|---|
| [OOP] | $2/3V_d$ | $-1/3V_d$ | $-1/3V_d$ | $1/3V_d$ |
| [OPO] | $-1/3V_d$ | $2/3V_d$ | $-1/3V_d$ | $1/3V_d$ |
| [POO] | $-1/3V_d$ | $-1/3V_d$ | $2/3V_d$ | $1/3V_d$ |
| [OON] | $-2/3V_d$ | $1/3V_d$ | $1/3V_d$ | $-1/3V_d$ |
| [ONO] | $1/3V_d$ | $-2/3V_d$ | $1/3V_d$ | $-1/3V_d$ |
| [NOO] | $1/3V_d$ | $1/3V_d$ | $-2/3V_d$ | $-1/3V_d$ |
| [NNP] | $4/3V_d$ | $-2/3V_d$ | $-2/3V_d$ | $-1/3V_d$ |
| [NPN] | $-2/3V_d$ | $4/3V_d$ | $-2/3V_d$ | $-1/3V_d$ |
| [PNN] | $-2/3V_d$ | $-2/3V_d$ | $4/3V_d$ | $-1/3V_d$ |
| [PPN] | $-4/3V_d$ | $2/3V_d$ | $2/3V_d$ | $1/3V_d$ |
| [PNP] | $2/3V_d$ | $-4/3V_d$ | $2/3V_d$ | $1/3V_d$ |
| [NPP] | $2/3V_d$ | $2/3V_d$ | $-4/3V_d$ | $1/3V_d$ |
| [PPO] | $-2/3V_d$ | $1/3V_d$ | $1/3V_d$ | $2/3V_d$ |
| [POP] | $1/3V_d$ | $-2/3V_d$ | $1/3V_d$ | $2/3V_d$ |
| [OPP] | $1/3V_d$ | $1/3V_d$ | $-2/3V_d$ | $2/3V_d$ |
| [NNO] | $2/3V_d$ | $-1/3V_d$ | $-1/3V_d$ | $-2/3V_d$ |
| [NON] | $-1/3V_d$ | $2/3V_d$ | $-1/3V_d$ | $-2/3V_d$ |
| [ONN] | $-1/3V_d$ | $-1/3V_d$ | $2/3V_d$ | $-2/3V_d$ |
| [PON] | $-V_d$ | 0 | $V_d$ | 0 |
| [PNO] | 0 | $-V_d$ | $V_d$ | 0 |
| [NPO] | 0 | $V_d$ | $-V_d$ | 0 |
| [OPN] | $-V_d$ | $V_d$ | 0 | 0 |
| [NOP] | $V_d$ | 0 | $-V_d$ | 0 |
| [ONP] | $V_d$ | $-V_d$ | 0 | 0 |
| [PPP] [OOO] [NNN] | 0 | 0 | 0 | 0 |

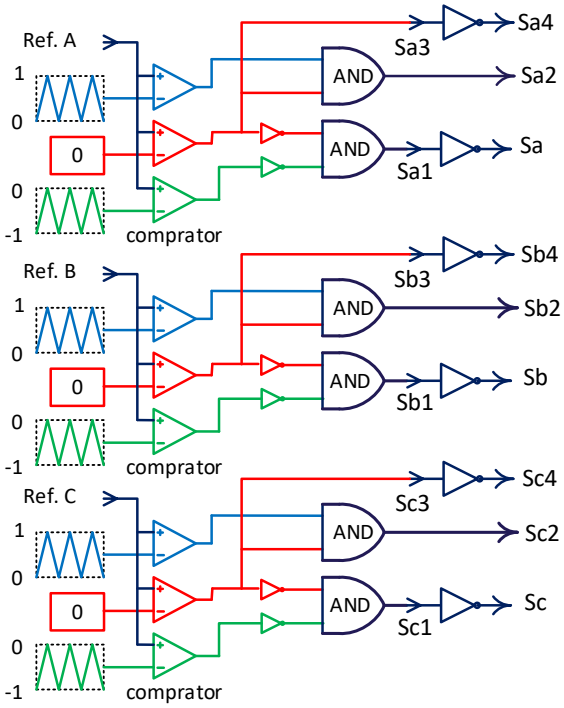



Fig. 4. logic schematic to compute the switching signals

## B. *Voltage and Current Stresses of the Components*

One of the technical competences of the proposed SSFB-TPI is using components with low voltage stress. For a given output voltage peak of $V_p$ , the voltage stress on the components is

$$V_{sc} = V_{sp} = V_{di} = V_c = V_p \tag{2}$$

where $V_{sc}$, $V_{sp}$, $V_{di}$, and $V_c$ are voltage stresses of switches in the dc side, the voltage of the switches in the ac side, the voltage of diodes, and voltage across the capacitors, respectively. Considering a given output load current of $I_l$ and ignoring the current ripple at the input side, the current stresses of the components are

$$I_k = I_{sc} = I_{di} = \sqrt{3}I_{sp} = \sqrt{3}I_l \tag{3}$$

where $I_k$, $I_{sc}$, $I_{di}$, and $I_{sp}$ are current of the switch in the dc-dc converter, current of charging switches, current of charging diode, and current of the switches in the ac side, respectively.

Assuming a given voltage ripple of $\Delta v$, the required capacitance of capacitors in the proposed inverter is calculated as

$$C = \frac{mI_l}{f_s \Delta v} \tag{4}$$

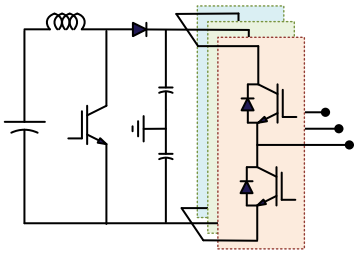
where $C$, $m$, $I_l$, and $f_s$, are the capacitances, modulation index, load current, and switching frequency of the switches in ac side, respectively. Furthermore, defining input current ripple as $\Delta I_{in}$, the input inductor $L_k$ is calculated as

$$L_k = \frac{V_{in} d}{f_{sk} \Delta I_{in}} \tag{5}$$

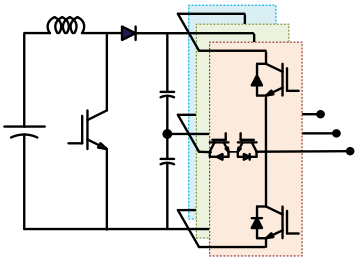
1r5where $V_{in}$, $d$ and $f_{sk}$, are the input voltage, duty cycle, and switching frequency of the dc-dc converter, respectively.

## III. BENCH MAKING WITH HB-TPI AND NPC

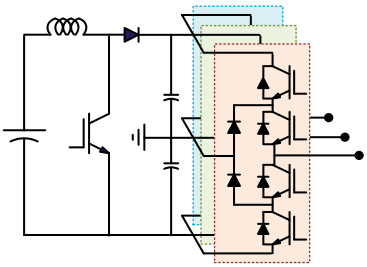
In order to assess the merits and deficiencies of the proposed inverter, it is compared with HB-TPI T-type NPC and NPC from a different points of view. For ease of reference, the two-stage HB-TPI, T-type NPC and NPC are shown in Fig. 5(a), (b) and (c), respectively. As observed in these figures, the HB-TPI requires fewer components. However, the components in this inverter are exposed to two times of the peak value of the output voltage. The T-type NPC needs two unidirectional and one bidirectional switches. The unidirectional switches are exposed to the full input voltage while the bidirectional switch is exposed to half of the input dc voltage. On the other side, the NPC requires four switches and two diodes at each phase. The components in the phase are exposed to the peak value of the output voltage (half of the input voltage). Moreover, the switch in the dc side is exposed to the voltage equal to two times the peak value of the output voltage. The proposed topology needs five switches and one diode in each phase. All the components, including the switch in the dc-dc converter, are exposed to the peak value of the output voltage. Therefore, compared to the three former two-stage inverters, the proposed two-stage inverter uses components with minimum voltage stress. Hence, the SSFB-TPI is applicable in higher voltage applications such as wind power generation [6]. Regarding the quality of ac voltage, the T-type NPC, the NPC, and proposed SSFB-TPI, which develop three voltage levels in each phase, offer lower THD, dv/dt, and EMI than the HB-TPI.



(a)two-stage HB-TPI



(b) two-stage T-type NPC



(c) two-stage NPC inverter

Fig. 3. Conventional two-stage three-phase inverter.

The main superiority of the proposed SSFB-TPI inverter is unity voltage gain. The voltage gains of the HB-TPI, the T-type NPC and NPC is 0.5. As mentioned earlier, this feature makes the proposed SSFB-TPI a suitable choice in medium voltage applications. For more clarity, let's exemplify the application with 11 kV Root Mean Square (RMS) phase-to-phase voltage range as shown in Fig. 4. The HB-TPI, T-type NPC and the NPC in such applications require at least a 13.43 kV input dc link, but the voltage range of the dc-link in the proposed SSFB-TPI is 6.72 kV (output of the front-end dc-dc converter is assumed as dc- link). Under the mentioned conditions, all components in the proposed SSFB-TPI are exposed to 6.72 kV, in this regards the unidirectional switches of the T-type NPC and all the switches of the HB-TPI are exposed to about 13.43 kV. In this case, the inverter side components of the NPC are exposed to 6.72 kV. However, the switch in the dc-dc converter of the latter inverter is exposed to 13.43 kV. Therefore, assuming that the highest voltage rating of available switches is around 7 kV, employing the two-stage NPC, T-type NPC and HB-TPI are impossible for the applications within the mentioned voltage range. However, since all the components in the proposed SSFB-TPI (including the switch in the dc-dc stage) are exposed to 6.72 kV, this inverter is applicable in the exemplified application.

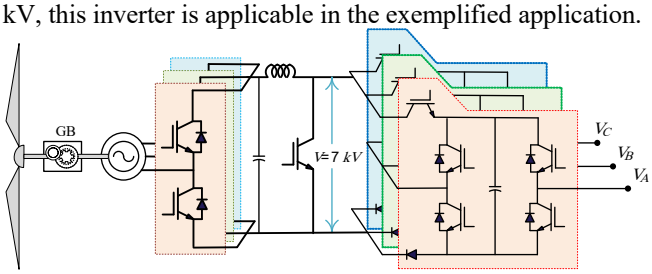



Fig. 4. Proposed SSFB-TPI in a medium voltage application.

## IV. SIMULATION RESULTS

To validated the feasibility and investigate the performance of the proposed SSFB-TPI topology, MATLAB/Simulink is employed for simulations. Specifications of the utilized prototype are provided in Table II. In this study, SPWM is used to generate the switching signals.

It is worth mentioning that the outer current and/or the voltage regulation loops for grid-integration of the proposed SSFB-TPI topology are not discussed in this study, because the main purpose of our paper is to propose a new inverter topology. However, different linear and nonlinear control techniques can be employed to regulate the dc voltage [24] and the output ac voltage [25], [26] using the proposed switching method.

TABLE II. SPECIFICATIONS OF THE SIMULATED MODEL.

| Parameter | Value |
|---|---|
| Input voltage | 3.25 kV |
| Duty cycle | 50% |
| Input inductor | 2 mH |
| Capacitors | 1200 µF |
| ac side $f_s$ | 12 kHz |
| dc side $f_s$ | 50 kHz |

To investigate the performance of the proposed SSFB-TPI, a resistive-inductive load of 180 kW +110 kVar is connected at the output terminal. The input current under the mentioned loading conditions is shown in Fig.5. As seen in this figure, the input current is a continuous current with %26 (15A)

ripple. The ripple could be further mitigated, as defined in Eq. (5).

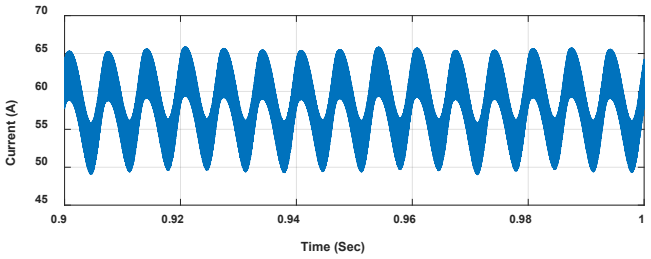
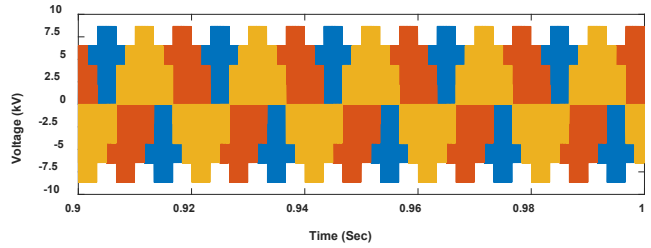
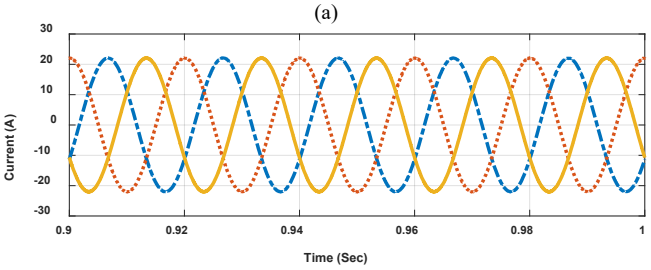



Fig.5. Simulation result of the input current

The output phase voltages and load current under the mentioned loading condition are exhibited in Figs. 6(a) and (b), respectively. As seen in this figure the output voltage of the proposed inverter is a staircase seven-level ac voltage. Since the load connected to the output terminal is has inductive feature the load current has a pure sinusoidal waveform.



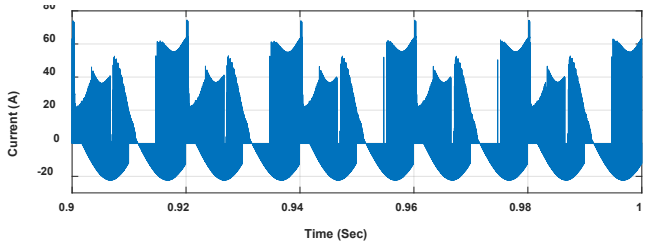

(a)



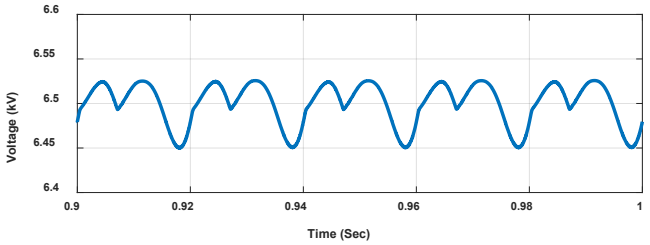

(b)

Fig.6. Simulation results of the ac output terminals (a) output voltage and, (b) load current.

Moreover, the capacitor current and voltage are shown in Figs. 7(a) and (b), respectively. Considering the current magnitude in Figs. 5 and 6(b), it is evident that the capacitor in the phases does not experience inrush current as the capacitor current magnitude is between the input and load currents. This is the case, because the capacitors are charged through the input inductor and this inductor limits the capacitor inrush current.




(a)




(b)

Fig.7. Simulation results of the capacitor parameters (a) capacitor current in one of the phases, and (b) capacitor voltage in one of the phases.

## V. CONCLUSION

In this paper, a two-stage single source full-bridge based three-phase inverter is proposed. The proposed inverter topology uses one full-bridge, one charging switch, and diode in each phase and a front-end dc-dc boost converter. All the components in the proposed inverter withstand unity per unit voltage stresses. The front-end dc-dc boost converter in this inverter smoothen the input current, boosts the voltage, and avoids inrush current of the capacitors. Since the proposed inverter uses a full-bridge cell in each phase, three voltage levels are developed. Thus, the THD, EMI, and dv/dt are reduced. Simulation results by using for a 211 kVA load were provided to validate the versatility of the proposed inverter.

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