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# Single-phase Bridgeless PFC Topology Derivation and Performance Benchmarking

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***Abstract*—This paper introduces two general ways to derive single-phase bridgeless power factor correction (PFC) topologies and then 15 accessible bridgeless topologies are derived based on the configuration of different basic types of DC-DC converter cells. Although the majority of the topologies have been previously proposed, other possible research points are reviewed. Besides, a consistent component sizing procedure with electric, thermal, and cost models is applied to conduct the performance benchmarking of these PFC topologies in terms of power loss, volume, and cost. Three boost-type PFC topologies are chosen as examples to demonstrate the procedure and the corresponding benchmarking results with both theoretical analyses and experimental verification. Finally, mission profiles of one specific application are introduced to show the material cost payback period of adopting one modified bridgeless boost topology instead of conventional one in different scenarios.**

***Index Terms*—Single-phase, PFC, Bridgeless, Topology, component sizing procedure, performance benchmarking.**

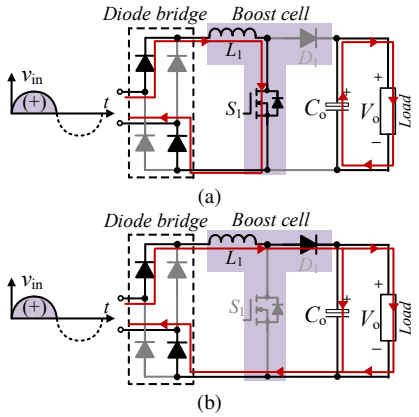


Fig. 1. The boost PFC converter topology with inductor operating in CCM both in the positive half line cycle: (a) $S_1$ in on-state, (b) $S_1$ in off-state.

## I. Introduction

In order to avoid the distorted AC input current in power electronic equipment, active power factor correction (PFC) converters are usually used as the front-end in the equipment [1]. Among them, the boost PFC converter is one of the most widely used topologies [2]. Fig. 1 shows its operation modes with the inductor operating in continuous conduction mode (CCM). Observations from Fig. 1 indicate that there are always three conducting power semiconductors (two in the diode bridge) in the current path, which causes considerable conduction losses [3]. Hence, on the demanding for minimizing conduction losses, high efficient AC-DC PFC converters without the diode bridges are gaining concentrations in recent decades [2]–[10].

Various bridgeless boost PFC converters with different features are proposed to replace the conventional boost or the interleaved boost PFC converters [2], [7]–[10], e.g., ZVS soft-switching resonant bridgeless boost topology with inherent PFC ability [9], bridgeless interleaved boost topology for applications with output power higher than 3 kW [10], etc. Moreover, bridgeless topologies are usually presumed to be employed in only relatively high power applications since they mainly reduce conduction losses, nonetheless, the surge of other type bridgeless topologies have changed the situation, e.g., bridgeless buck-boost PFC converters applied in LED, laptop power adapter, and adjustable speed motor drive (<250 W) [5], [6], [11], [12]. However, although there are numerous different bridgeless topologies, there are only several references to cover the topic that how to derive these bridgeless topologies [13]–[15]. It is self-evident that by understanding the topology derivation, more useful topologies can be identified and more improvements upon the defective topologies can be done. Thus, the introduction of the bridgeless topology derivation is meaningful and necessary. Compared to the existing literatures [14], [15], the bridgeless topology derivation method in this paper is not only applicable to the boost type but also others. Although one similar derivation method has been proposed in [13], a more systematic converter cell configurations and detailed discussions are given.

On the other hand, with so many bridgeless topologies derived, how to conduct a comparative study is also a problem. Most bridgeless topology comparisons between bridgeless topologies and their conventional topology counterparts adopt same devices or only based on the rated currents/voltages to select the components [9], [10], [12], [16]–[19], which are not a fair comparison in terms of converter multi-dimension performances, e.g., cost, volume, weight, reliability, and efficiency [20]. Because the 'same devices' based comparison ignores the fact that these bridgeless topologies usually have less thermal stresses upon components due to the employments of more components or less generated power losses. Then, the obtained topology comparison results in cost and volume

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perspectives are not convincing. Moreover, the quantitative question that how much pain these bridgeless topologies have to take in volume and cost aspects to gain efficiency improvement is still echoing in the air.

To shed light on this issue, a consistent component sizing procedure is introduced with consideration of electric, thermal, and cost models in this paper to offer an unbiased quantitative comparison results between topologies. Compared with the existing PFC topology comparative evaluation methods [16], [21], [22], this method selects the components based on their calculated junction temperatures, which are derived by an iteration loop between electric and thermal models. Although other inverter topology comparison methods also use the calculated junction temperatures to select components [23]–[25], cost models are not included. Another detailed inverter topology comparative study in [26] optimizes each compared topologies for a fair comparison, yet it is too complicated to follow and the running time (15-20 H) is too long. Meanwhile, using different devices from different manufacturers trigger the question that whether the converter performance differences are caused by the different manufacturing techniques or just the topologies. In contrast, the comparative method in this paper limits the component database to the same type components only from the same generate/series of the same manufacturers. In this way, the running time is reduced and the code is simplified.

The remainder of this paper is arranged as follows. In Section II, firstly, the principle of bridgeless PFC topology derivation is introduced. Afterward, the detailed graphics show how to use the two general configurations with different basic converter cells to derive the topologies. Later, 15 accessible topologies are derived and then brief reviews of these topologies along with a summary of the possible research points are presented. In Section III, for a fair comparison, an electrical, thermal, and cost models based component sizing procedure is introduced. And by using this procedure, three boost type topologies (two bridgeless named as M-IPOS and IPOP, one conventional) are compared to demonstrate their topology features in power loss, cost, and volume aspects, followed by detailed comparison results. Section IV shows three 850 W built prototypes and the test results. Moreover, typical power load mission profiles of the base stations are used to analyze the material cost payback period of using the M-IPOS boost topology instead of the conventional boost topology. The conclusion is drawn in Section V.

## II. The Topology Derivation

### A. The Principle to Derive Bridgeless

For ordinary converter cells (e.g. boost cell in Fig. 1), they can only handle either the positive or negative input voltage conversion, but AC input voltage requires converters to process both positive and negative input voltages. By using the diode bridge, the AC input voltage can be transferred to positive input voltage so that the diode bridge along with one converter cell is capable to function PFC. To gain the bridgeless topology, i.e., to eliminate the diode bridge, one straightforward way is to adopt two converter cells with each cell to deal with the positive or negative input voltage conversion, respectively. Then, most DC-DC converter cells should have the potentials to form their corresponding bridgeless topologies. Specifically, since each cell has to handle one polarity of the AC input, then for the input side, they can only be formed in the input parallel (IP) manner. As for the output side, the cells can be either in output parallel (OP) or output series (OS). Thus, there are IPOP and IPOS configurations of dual converter cells. Although these dual-cell based bridgeless solutions have doubled the components, however, since each converter cell only works in the half line cycle, the components in these bridgeless topologies have lower thermal stresses compared to their conventional topology counterparts.

On the other hand, another solution to achieve 'bridgeless' is using one single modified converter cell with the bidirectional switch, which can handle both polarities of the input power [18], [27], [28]. These type converters need a crucial and carefully designed resonant circuit in the bidirectional inductor current path, rather than just freewheeling diodes in the ordinary converter cells [18], [28]. Meanwhile, the leakage inductance in the transformer can be used to implement the resonant circuit, so this type of bridgeless topologies are more suitable in galvanic isolation applications [18], [28]. This paper only focuses on the first solution using two converter cells.

### B. How to Derive Bridgeless Topologies

Based on the positions of the eliminated diodes in the diode bridge, Fig. 2 shows three considered configurations with the corresponding imaging current flows. Fig. 3 shows these type I and II converter cells with the bidirectional current ability only in '*b*-*d*' and '*e*-*g*'. Because of the similarity of IPOP-I and IPOP-II topologies, this paper classifies them into IPOP.

Below discusses the requirements upon the converter cells when use IPOP and IPOS configurations to obtain their corresponding bridgeless topologies. Fig. 2(b), (c), and (d) show that the imaging current flow path in each cell is only one-directional. However, comparing the current flows of the type I converter cell in Figs. 2(b) and 2(d), it indicates that the type I converter cell should be able to cope with the bidirectional current flow only in '*b*-*d*' terminals, otherwise, the converter cells can not follow the method given in Fig. 2 to both form its IPOS and IPOP bridgeless topologies. Correspondingly, comparing the type II converter cell in Figs. 2(c) and 2(d), the bidirectional power flow are in '*f*-*h*' terminals.

Based on the aforementioned discussion, these categorized configurations are applicable for most converter cells and even for two different converter cells, as long as the converter cells meet the aforementioned requirement. Here, for simplicity, only the basic converter cells: boost, buck-boost, buck, sepic, and Cuk, are considered in this paper as examples to illustrate the effectiveness of these configurations. Note that even for these basic converter cells, here only list just type I and type II formats, not mention other modified converter cells. Hence, the topology derivation method presented here can be helpful to derive more bridgeless topologies. Anyway, based on the cells in Fig. 3, different IPOP and IPOS bridgeless PFC converters can be obtained in Fig. 4.

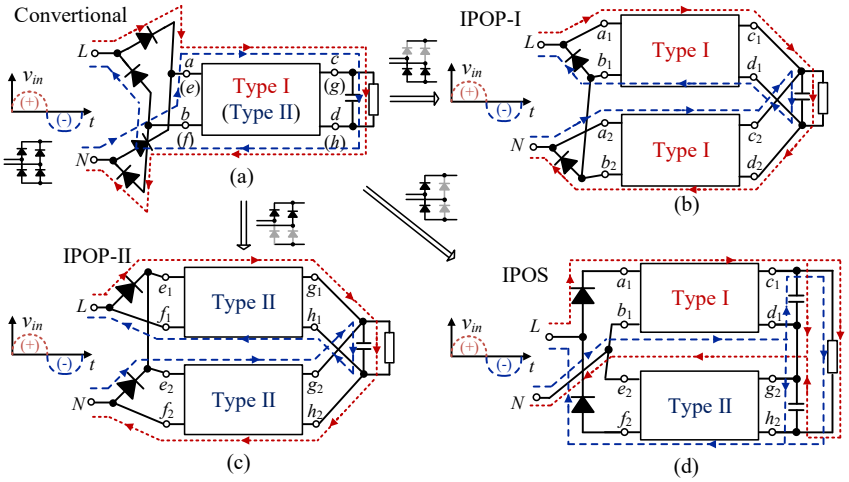


Fig. 2. Ways to derive bridgeless PFC topologies and their imaging current flows in positive and negative input voltage: (a) conventional PFC converter with a diode bridge, (b) converter cells in IPOP with the eliminated diodes in the high legs of the diode bridge, (c) converter cells in IPOP with the eliminated diodes in the low legs of the diode bridge, and (d) converter cells in IPOS with the eliminated diodes in one leg of the diode bridge.

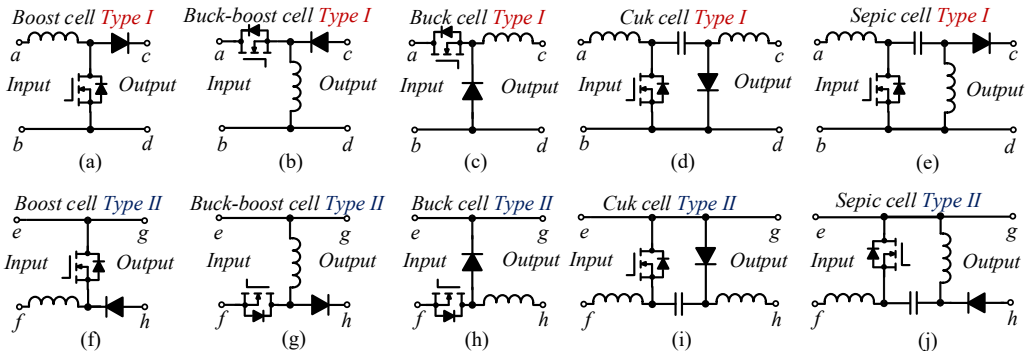


Fig. 3. The basic converter cells of boost, buck-boost, buck, Cuk and sepic, each with its type I and II versions. The type I converter cells have the bidirectional current path only in 'b-d' terminals and type II only in 'e-g' terminals. Note that for each basic cell, here only lists two corresponding versions for examples.

### *C. Reviews of Derived Topologies*

The IPOP-I/II buck, IPOS Cuk, and IPOS sepic topologies are not seen in the available references yet. Others have been proposed or have similar counterparts. The following reviews the derived bridgeless topologies given in Fig. 4.

**Boost:** the IPOP-I boost topology, proposed in [29], was an EMC modified version of an early dual boost topology without the extra diodes [32]. On the other hand, the IPOS boost topology has been proposed in 1995, named as DC split boost due to the output voltage of each boost cell is half of the total output voltage $V_o$ [14]. Unfortunately, this topology is unpopular because that if $V_o$ = 400 V, then the RMS input voltage $V_{in}$ is limited to 90∼135 Vac for the boost voltage ratio limitation $\sqrt{2}V_{in} < ½V_o$. However, it still has advantages, e.g., the two inductors can be integrated into a single one operating in both polarities of AC input and put in the input side. Actually, this modified IPOS (M-IPOS) boost topology can also be obtained from the modified type I and II boost cells with inductor located in the bidirectional path of each cell. In section III, this M-IPOS boost PFC converter is further studied. Besides, more modifications can be done upon the IPOS boost topology. For example, the well known totem-pole boost topology can be seen as one version of the modified IPOS boost topology [33]. Nonetheless, the simplified topology usually leads to more complexity in modulations, which also holds in the totem-pole boost topology. It has to use two different switch driving signals with dead zones, however, the original IPOS boost topology here can use one identical switch driving signal without dead zones.

**Buck-boost:** the IPOP-I buck-boost topology has been proposed for the LED applications and adjustable DC-link motor drive [5], [6] and it shows similar PF performance compared to its conventional buck-boost topology. However, one of the buck-boost converter cell's drawbacks is the high voltage stresses across semiconductors due to the inverse input and output voltages ($V_o$ + $\sqrt{2}V_{in}$). To avoid the high switching losses caused by the high voltage stresses, one solution is to use a double-switch based non-inverted buck-boost converter cell proposed in [34] and its modified IPOP-I bridgeless topology is proposed in [35]. However, this solution increases the conduction losses as more semiconductors included in the current path. Another solution is the IPOS buck-boost topology, in which the lower voltage stresses (½$V_o$ + $\sqrt{2}V_{in}$) across semiconductors allows the converter to have efficiency-enhanced performance in the light-load conditions, where switching losses are dominant in the total power losses [19]. Unfortunately, the IPOS buck-boost topology has higher conduction losses in the output diodes than its IPOP and

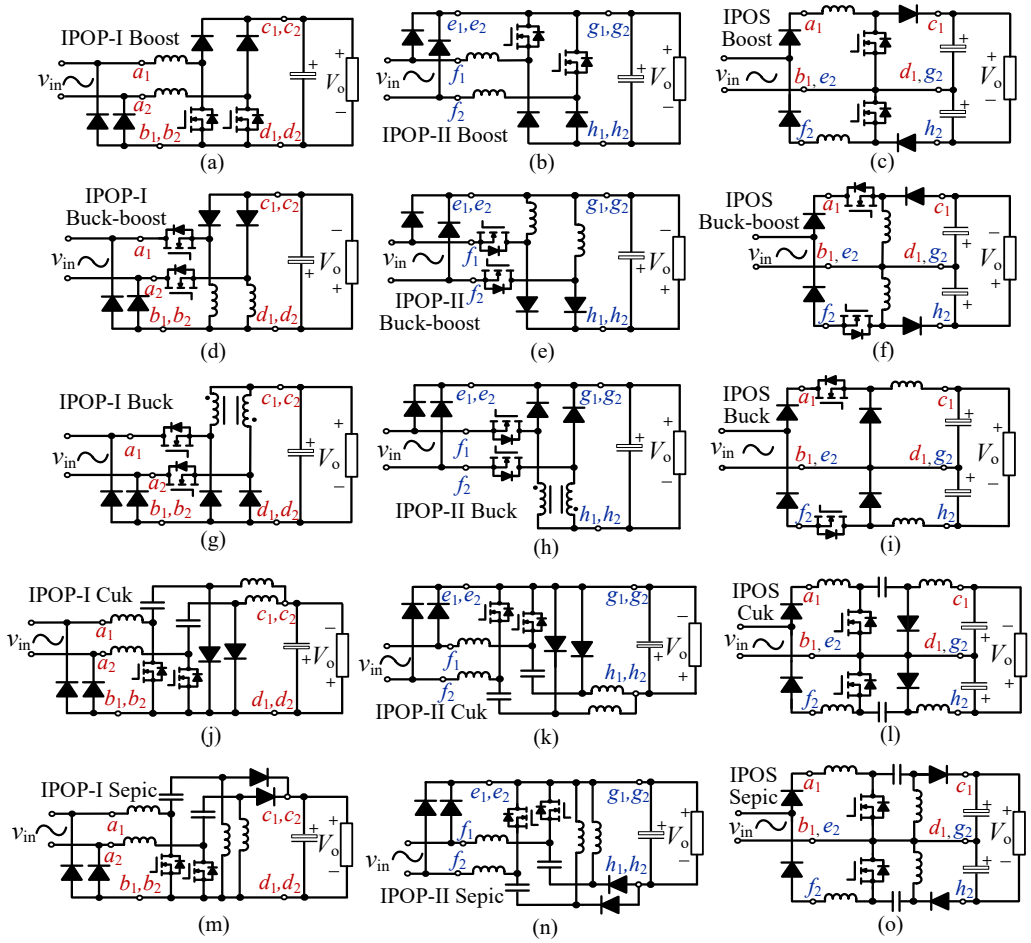


Fig. 4. IPOP-I/II and IPOS Bridgeless PFC topologies obtained by using basic converter cells. (a), (c), (d), (f), (i), (j) has been proposed in [29], [14], [6], [13], [4], and [30], respectively. (k) and (m) already have very similar counterparts proposed in [17] and [31]. In the other obtained topologies, (g), (l) and (o) still have some research values. For (g), it can eliminate the input current dead zones around the zero crossing of the AC input. For (l) and (O), they can be further simplified and have lower voltage stresses across switches than their IPOP topology counterparts.

conventional topology counterparts.

**Buck:** The IPOS buck topology was proposed and studied in [4] and it has relatively lower voltage stresses on the secondary converter since the lower voltage output compared to the conventional boost topology. On the other hand, directly using the buck cells in Fig. 3(c) and 3(h) to obtain the IPOP buck topology is not accessible. Because the input current can flow through the anti-parallel diodes of MOSFETs to charge both inductors even when the switch is off and then the unwanted inductor current leads to the high voltage spike due to the unavailable current path. Here, in Fig. 4(g) and 4(h), the integrated inductors based IPOP buck topologies are presented so that the unwanted inductor current can use the mutual inductor for the current path. Moreover, this modification can automatically eliminate the input current dead zones, since the integrated inductor turns this IPOP buck topology to flyback mode when the dead zones come. Apart from this solution, this input current dead zone issue can also be solved by using a relatively complicated control method, e.g., a modified IPOS buck topology with four active switches [36]. In contrast, another topological solution adopting only simple control is using a switch-integrated parallel buck and flyback converter cell to form the IPOP configuration, but it has poor efficiency for too many components employed [37].

**Cuk and sepic:** the IPOP-I Cuk topologies have been proposed in [35] with $\mathrm{THD}_i$ below 2% and efficiency above 93%. Moreover, this IPOP-I Cuk can be further simplified by integrating the dual output diodes and inductors into only one of each [31]. Furthermore, the two active switches can also be integrated into one so that drive circuit and control can be simplified [38], e.g., the IPOP-II Cuk topology with one active switch proposed in [17]. On the other hand, the IPOS Cuk and sepic topologies are not seen in the available references, which compared to their IPOP counterparts have lower switch stresses and lower switching losses.

### *D. Summary of Possible Research Points*

For these IPOP topologies, most researchers have proposed IPOP-I or the modified IPOP-I bridgeless PFC topologies [6], [14], [29]–[32], [39] and few attentions are upon the IPOP-II [17]. The major reason can be the similarity between these IPOP-I and IPOP-II topologies block the studying on the IPOP-II topologies unless IPOP-II offers apparent advantages over IPOP-I. For instance, a less-cost non-floating switch driving circuit is enough in the IPOP-II Cuk PFC converter, which is not applicable for the IPOP-I Cuk PFC converter [17].

On the other hand, only a few available references conduct the insight researches upon IPOS type bridgeless topologies [12], [13], [15], [19], [36], which means that these type bridgeless topologies still have considerable research values, e.g., the possibility of soft-switching [33], [40]. In summary, possible research points are listed as follows.

1) Two different or modified converter cells can be used when following the introduced configurations. For instance, Ref. [39] uses the type I buck and buck-boost converter cells to derive the hybrid IPOP topology so that the input current dead zones in the conventional buck PFC converter can be alleviated and PF is improved by using a simple voltage loop control. Similarly, in the IPOS type bridgeless topology, the bridgeless buck PFC converter mentioned in [36] can be derived by the IPOS manner based on the modified buck converter cell proposed in [41], which achieves high PF by using an additional active switch to eliminate the dead zones of the AC input current.
2) For certain types of IPOS topologies with MOSFETs in a bridge leg, they have the possibility to achieve a soft-switching transition [40], e.g., the ZVS switching in the totem-pole boost PFC converter [33] and the resonant boost bridgeless converter [9]. Moreover, even if these switches are unable to achieve soft-switching, the DC output split structure in the IPOS topologies still awards the lower switching losses compared to their conventional and IPOP topology counterparts, e.g., the derived IPOS buck-boost, Cuk, boost topologies.
3) The IPOS type bridgeless converters have the possibility of different output capacitor arrangements. For example, Ref. [12] has added a bidirectional capacitor in the IPOS buck-boost PFC converter, and then from output ripple side view, the added capacitor along with the two inductors serves as additional LC filter to minimize the switching frequency ripple. Consequently, smaller output current ripple is achieved, which is preferred by LED applications [42]. Meanwhile, the resultant expected lifetime of the electrolytic capacitor is also a valuable research point.

## III. The Performance Benchmarking

In this section, the component sizing procedure is introduced in the design for a fair performance comparison. Besides, as example, the M-IPOS boost topology is studied and compared with the conventional and IPOP-I (IPOP is used instead for short in the below) boost topologies in terms of power stage's power loss, cost, and volume. The design specifications are given in Table I and Fig. 5 shows the operation modes of the M-IPOS boost topology. Since the research on the M-IPOS boost topology is not available in references, so the analysis of this topology is given firstly.

### A. Analysis of The M-IPOS Boost

For the conventional and IPOP boost PFC converters, the operation modes and design guides are introduced in [43] and [3]. Here only briefly introduces the M-IPOS boost PFC converter. Assumptions are as follows. 1) All components are ideal. 2) Output capacitors are large enough to consider $V_{\rm o}$ as constant. 3) As the switching cycle $T_{\rm S}$ is much smaller than the line cycle $T_{\rm L}$, the instantaneous input voltage $v_{\rm in}(t)$ is considered as constant in each $T_{\rm S}$. Fig. 5 shows the operation modes of the M-IPOS boost converter and Fig. 6 shows the key waveforms. Due to the similarity in the positive and negative half line cycle, only the operation modes in the positive half line cycle is introduced.

TABLE I. Design Specifications of Converters

| Symbol | Parameters | Quantity |
|---|---|---|
| $f_{\rm S}$ | Switching frequency | 65 kHz |
| $f_{\rm L}$ | Line frequency cycle | 60 Hz |
| $V_{\rm in}$ | RMS input voltage | 90 to 135 Vac |
| $V_{\rm o}$ | Output voltage | 400 V |
| $P_{\rm o}$ | Output power | 850 W |
| $t_{\rm hold}$ | Hold-up time | 10 ms @ $V_{\rm o,min}$ = 320 V |
| $V_{\rm o,rip}$ | Output voltage ripple (P-P) | $\leq$ 10 V @ 850 W |
| $I_{\rm in}$ | RMS input current | $\leq$10 A @ 850 W with 90 Vac |
| $T_{\rm a}$ | Ambient temperature | -20 °C to 65 °C |

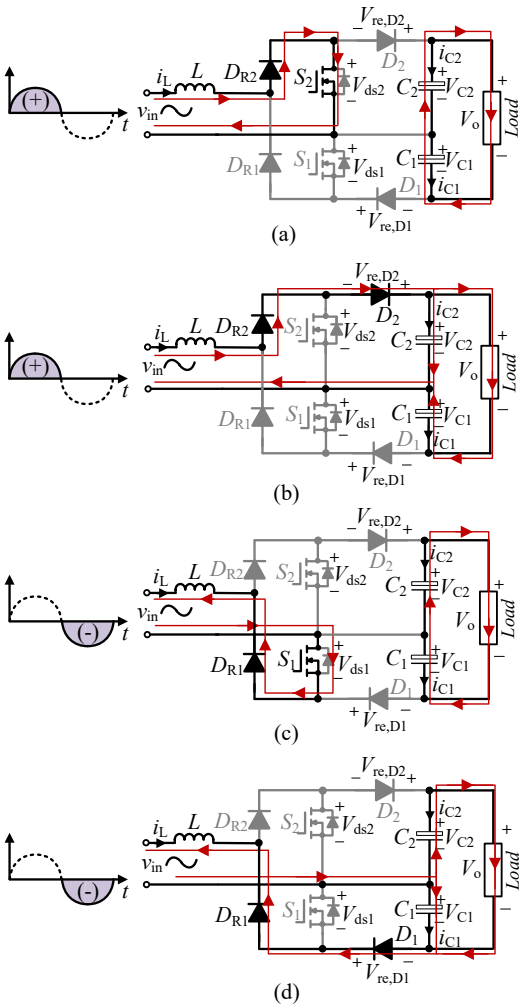


Fig. 5. Operation modes of the M-IPOS boost PFC converter: (a) and (b) in the positive half line cycle, (c) and (d) in the negative half line cycle, where $V_{\rm ds1}$, $V_{\rm ds2}$, $V_{\rm re,D1}$, and $V_{\rm re,D2}$ are the voltage stresses across the switches and output diodes, respectively.

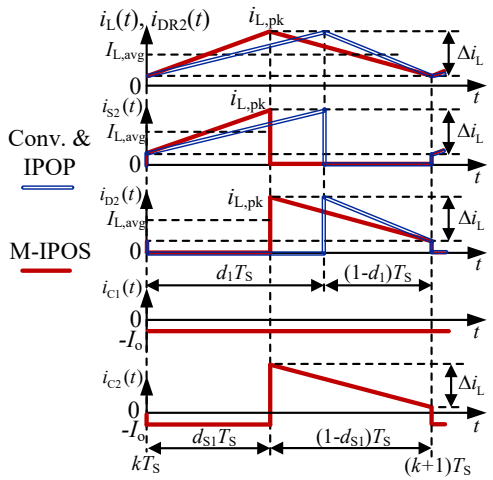


Fig. 6. Key waveforms of the conventional, IPOP, and M-IPOS boost PFC converters in one switching cycle during the positive half line period, where $I_{L,avg}$ is the average inductor current in the each switching cycle and considered as constant, $\Delta i_L$ being the switching-frequency inductor current ripple, and $I_o$ being the output current.

In Fig. 5(a), when the switch is in on-state, the input current flows through inductor $L$, rectifier diode $D_{R2}$, and switch $S_2$. The inductor current $i_L$ increase linearly. During this period, the voltage across inductor is equal to the input voltage $v_{in}$. The output capacitors $C_1$ and $C_2$ support the load.

In Fig. 5(b), when the switch is in off-state, the energy stored in the inductor transfers to load and charge $C_2$. Meanwhile, $C_1$ is discharging continuously and its voltage decreases. During this period, $i_L$ decreases linearly. The voltage across inductor is $v_{in}$ - ½$V_o$.

Note that in one switching cycle, the instantaneous voltages of capacitors $C_1$ and $C_2$ are different, however, in the line cycle, the average voltages of $C_1$ and $C_2$ are the same because the discharging and charging periods of these capacitors largely depend on their own voltages. For example, in the positive half line cycle, if $V_{C1}$ is low than $V_{C2}$, then the discharging time of $V_{C1}$ (equal to the charging period of $V_{C2}$) will be short. The principle of automatic voltage balance is the same as the IPOS buck topology in [4].

Assuming that $d_{S1}$ is the turning-on duty cycle and based on the operation modes, the voltage conversion ratio of the M-IPOS boost PFC converter can be derived as:

$$\frac{V_o}{v_{in}} = \frac{2}{1-d_{S1}}. \quad (1)$$

Here, assuming that $d_1$ is the turning-on duty cycle in the conventional and IPOP boost PFC converters, of which voltage conversion ratio are the same and equal to $1/(1-d_1)$. If all the three converters have the same input and output voltages, then the relationship between $d_1$ and $d_{S1}$ is:

$$d_{S1} = 2d_1 - 1 \quad (2)$$

which indicates that $d_{S1}$ is smaller than $d_1$, as $d_{S1}$ - $d_1$<0. Accordingly, referring to Fig. 6, compared to the conventional and IPOP boost PFC converters, the M-IPOS boost PFC converter has lower conduction losses in switches, as $d_{S1}$ is smaller than $d_1$, but higher conduction losses in the output

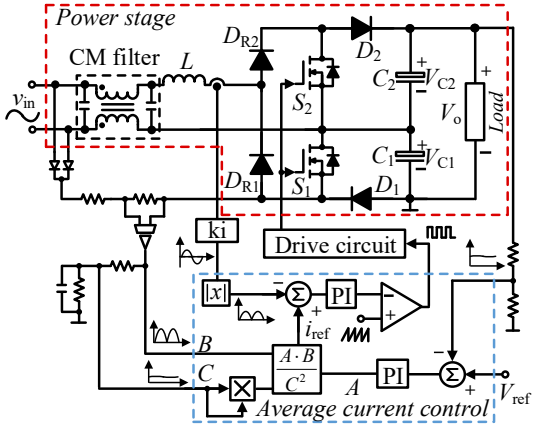


Fig. 7. Control schematic of the M-IPOS boost PFC converter.

diodes, as 1 - $d_{S1}$ is larger than 1 - $d_1$. Meanwhile, the M-IPOS boost PFC converter has lower switching losses in the switches and output diodes compared to the conventional and IPOP boost PFC converters, since its voltage stresses across switches and output diodes are only 50% of that in the conventional and IPOP boost PFC converters.

As the output capacitors $C_1$ and $C_2$ can achieve auto-balance, then the control implementation of the M-IPOS boost PFC converter can be as same as that of the conventional boost PFC converter. In this paper, average current control is adopted to achieve the close-loop control and Fig. 7 shows the corresponding control schematic.

### *B. Component Sizing Procedure*

Fig. 8 shows the component sizing procedure with considerations of electrical, thermal, and cost models. By following this procedure, the three compared converters are presumed to have similar stable junction temperatures (meaning values) in the same type components, e.g., the stable junction temperatures of MOSFETs in the three converters are evaluated to be within 100 ± 2 °C in the maximum input and output current condition (@ 850 W, 90 Vac). Usually, junction temperatures are considered as one of the important reliability criteria that affect the lifetime [44]. Besides, by choosing the junction temperatures of components as selection criteria, the obtained power loss, cost, and volume comparison results are more meaningful. The follows introduce the corresponding electric, thermal, and cost models with selected examples.

The electric models relate to components, topologies and design specifications. Based on the operation modes in Fig. 5, in one switching cycle, the RMS currents $i_{S2,RMS}$, $i_{C1,RMS}$, $i_{C2,RMS}$, and $i_{L,RMS}$ in $S_2$, $C_1$, $C_2$, and $L$, as well as the average currents $i_{D2,avg}$ and $i_{DR2,avg}$ of the output didoes $D_2$ and rectifier diodes $D_{R2}$ can be derived as:

$$i_{S2,RMS}^2 = d_{S1}\left(\frac{\Delta i_L{}^2}{12} + I_{L,avg}^2\right) \quad (3)$$

$$i_{C1,RMS}^2 = I_o^2 \quad (4)$$

$$i_{C2,RMS}^2 = (1-d_{S1})\left(\frac{\Delta i_L{}^2}{12} + I_{L,avg}^2 - 2I_oI_{L,avg}\right) + I_o^2 \quad (5)$$

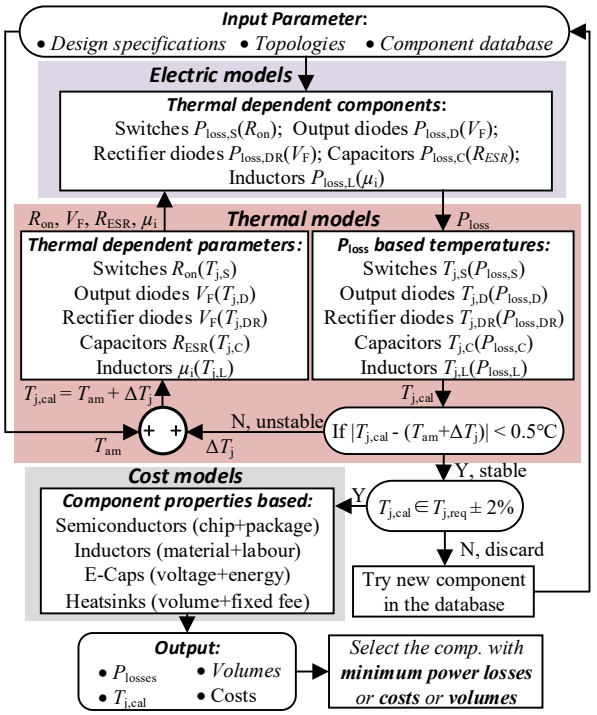


Fig. 8. The component sizing procedure. The electric models provide initial power losses $P_{\rm loss}$ to the thermal models under the maximum ambient temperature $T_{\rm am}$. Then, based on $P_{\rm loss}$, the thermal models compute the corresponding junction temperature $T_{\rm j,cal}$ of the considered component. Afterward, the sum of $T_{\rm am}$ and the assumed temperature difference $\Delta T_{\rm j}$ between junction and ambiance, is compared with $T_{\rm j,cal}$ to check whether the stable junction temperature is reached. If not, update the thermal dependent parameters (cf. Fig. 9) for the electric models to re-calculate $P_{\rm loss}$ . If yes, this loop aborts and the stable $T_{\rm j,cal}$ is compared with the required junction temperature $T_{\rm j,req}$ (with 2% tolerances). If the requirement is fulfilled, then the component is stored, otherwise, it is discarded. Moreover, the component properties based cost models are built to assess the component costs. The output information include $P_{\rm loss}$, $T_{\rm j,cal}$, cost, and volume for each component. Users select the stored (criteria-fulfilled) components based on their design priority. In this case, minimum power losses are the only considered priority.

$$i_{\rm L,RMS}^2 = \frac{\Delta {i_{\rm L}}^2}{12} + I_{\rm L,avg}^2 \tag{6}$$

$$i_{\rm D2,avg} = (1 - d_{\rm S1}) \cdot I_{\rm L,avg} \tag{7}$$

$$i_{\rm DR2,avg} = I_{\rm L,avg.} \tag{8}$$

Note that (3)-(8) are the derived results in one switching cycle, the corresponding RMS and average currents in a half line cycle can be further derived as:

$$i_{\rm X,RMS,L}^2 = \frac{1}{1/2 T_{\rm L}} \int_0^{1/2 T_{\rm L}} i_{\rm X,RMS}^2(t)dt, {\rm X} \in \{L, S, C\} \tag{9}$$

$$i_{\rm Y,avg,L} = \frac{1}{1/2 T_{\rm L}} \int_0^{1/2 T_{\rm L}} i_{\rm Y,avg}(t)dt, {\rm Y} \in \{D, D_{\rm R}\}. \tag{10}$$

The specific power loss calculation equations for switches, output capacitors, boost diodes, and the rectifier diodes in the entire line cycle can be found in [43]. And the RMS and average currents should be replaced by the results obtained from (9) and (10). Here, inductor power loss calculations are taken as examples to illustrate electric models.

As for the inductor power losses, there are two parts, copper losses $P_{\rm Cu,L}$ and core losses $P_{\rm core,L}$. Due to the good heat dissipation of the toroidal core, the inductor power losses are calculated only at the ambient temperature without considering the thermal impact. The selection criterion for the core is based on the winding factor (WF $\in 25\% \sim 40\%$) [45]. Moreover, for simplicity, the copper losses $P_{\rm Cu,L}$ is calculated without considering the skin and proximity effects caused by the eddy current, which is:

$$P_{\rm Cu,L} = R_{\rm Cu} \cdot i_{\rm L,RMS,L}^2 = \frac{\rho_{\rm Cu} \cdot l_{\rm Cu}}{A_{\rm Cu}} i_{\rm L,RMS,L}^2 \tag{11}$$

where $l_{\rm Cu}$, $A_{\rm Cu}$, and $\rho_{\rm Cu}$ are the winding length, cross section of core, and electrical resistivity of wire, respectively. Two paralleled AWG 17 wires are used in this design with current density 500 Amps/cm$^2$. The winding length $l_{\rm Cu}$ and turns can be calculated by the method in [45], which is helpful and practical for the inductor design. Regarding the core losses $P_{\rm core,L}$, it is calculated by improved generalized Steinmetz equation (iGSE) [46]. This iGSE can use the material parameters $\alpha$, $\beta$, and $k$ in the Steinmetz equation to calculate the time-average core losses per volume $P_{\rm core,vol,L}$ even under non-sinusoidal excitation. The $P_{\rm core,L}$ is calculated by:

$$\begin{cases} P_{\rm core,L} = P_{\rm core,vol,L} \cdot l_{\rm e} \cdot A_{\rm e} \cdot N_{\rm c} \\ P_{\rm core,vol,L} = \frac{k_{\rm i} \cdot (\Delta B/2)^{\beta-\alpha}}{T_{\rm L}/2} \cdot \sum_{j}^{T_{\rm L}/(2T_{\rm S})} \left(\frac{V_{\rm j}}{N A_{\rm e}}\right)^{\alpha} \Delta t_{\rm j} \\ k_{\rm i} = k \Big/ \left[2^{\beta+1} \pi^{\alpha-1} \left(0.2761 + \frac{1.706}{\alpha+1.354}\right)\right] \end{cases} \tag{12}$$

where $\Delta B$ is the peak-peak flux density, $j$ being the $j^{th}$ switching cycles in the half line cycle, $N$ being the number of turns, $A_{\rm e}$ being the effective cross section of the inductor core, $l_{\rm e}$ being the effective magnetic path length, $V_{\rm j}$ being the estimated voltages across the inductor during the time period $\Delta t_{\rm j}$, $N_{\rm c}$ being the inductor core number, and $k_{\rm i}$ being the coefficient relating to $\alpha$, $\beta$, and $k$.

The thermal models depend on the components themselves. The considered components in the database are MOSFETs from Infineon CoolMOS C7 with TO-247 package, output diodes from Infineon CoolSiC G5, diode bridges from Vishay New isoCink+, heatsinks from Aavid extruded channel fin types and Ohmite *P* series, toroidal cores from Magnetics Kool Mμ types, and output capacitors from Nichicon LGG series.

For example, Fig. 9 shows the junction temperature $T_{\rm j}$ and drain current $I_{\rm don}$ dependent on-state resistance $R_{\rm on}$ of MOSFETs, which can be expressed by a function with these two variables, $T_{\rm j}$ and $I_{\rm don}$. Moreover, the thermal model of the MOSFET has been given in Fig. 10. The thermal resistances $R_{\rm thjc}$ and $R_{\rm thhs}$ can be extracted from datasheets and $R_{\rm thch}$ is assumed to be 1 °C/W, which is caused by the thermal grease [43]. The thermal capacitance is not considered since here only concerns the stable junction temperature. Then, junction temperatures of MOSFETs are calculated by:

$$T_{\rm j,S} = T_{\rm am} + P_{\rm loss,S} \cdot R_{\rm th}. \tag{13}$$

where $R_{\rm th}$ is the sum of $R_{\rm thjc}$, $R_{\rm thch}$, and $R_{\rm thhs}$. The obtained $T_{\rm j,S}$ is further used in the procedure (cf. Fig. 8).

The cost models are built based on the component physical properties to avoid the price disruptions e.g., raw material price fluctuations, distributors' price strategies, etc. The specific

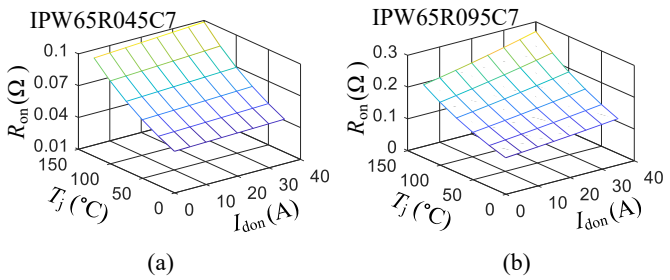


Fig. 9. The built thermal dependent on-state resistance $R_{on}$ with junction temperature $T_j$ and continuous on-state drain current $I_{don}$ as variables. These fitting curves are based on the data extracted from datasheets. Examples (a) IPW65R045C7 and (b) IPW65R095C7.

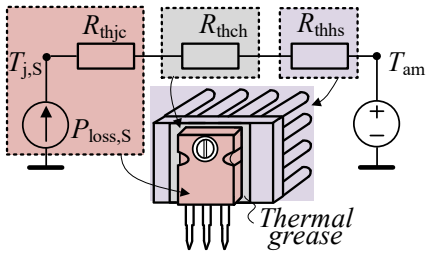


Fig. 10. The thermal model of the MOSFET with the thermal resistances from junction to case $R_{thjc}$, case to heatsink $R_{thch}$, and heatsink to ambiance $R_{thhs}$. This simplified thermal network does not consider the interactive thermal impacts between components and the thermal capacitors. The junction temperature can be evaluated from this model by using power losses.

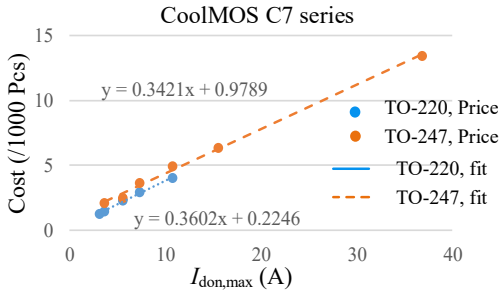


Fig. 11. The cost models of MOSFETs with packages TO-220 and TO-247. In this case, only TO-247 package with rated drain to source voltage being 650 V MOSFETs are used.

model equations can be referred from [47]. Fig. 11 shows the example cost models of the CoolMOS C7 MOSFETs with packages TO-220 and TO-247. The physical properties of these MOSFETs in considerations are chip area and package. Besides, because the chip area reflects the maximum rated continuous drain current $I_{don,max}$, Then, the specific cost model of MOSFET is:

$$C_{MOS} = a_{chip} \cdot I_{don,max} + b_{pack} \tag{14}$$

where $C_{MOS}$ is the price, $a_{chip}$ and $b_{pack}$ being the constants that represent the coefficients of chip area and package cost.

### C. Comparison Results

Before the component selection procedure, the inductance should be determined firstly, which relates to the inductor current ripple factor $k_{iL}$, usually set within [15%, 40%]. The inductance in the conventional and IPOP boost PFC converters can be determined by the design equations in [43] as:

$$L_{Conv,IPOP} \geq \left. \frac{d_1(1-d_1)V_{in,rms,min}}{\sqrt{2}k_{iL}P_{in}f_S} \right|_{d_1=0.5} \tag{15}$$

where duty cycle $d_1$ is equal to 0.5, and then (15) reaches its maximum value. Here, $k_{iL}$ = 22% because too large $k_{iL}$ will lead the converter into DCM/CCM operation mode even in heavy load conditions and cause the poor PF performance.

On the other hand, for the M-IPOS boost PFC converter, the inductor current ripple is assumed as $i_{L,rip}$ and it can be expressed by:

$$i_{L,rip} = \frac{\sqrt{2}k_{iL}P_{in}}{V_{in,rms}} \tag{16}$$

$$i_{L,rip} = \frac{V_o(1-d_{S1})d_{S1}T_S}{2L}. \tag{17}$$

Combining (1), (16), and (17), the inductance design equation in the M-IPOS boost PFC converter can be derived as:

$$L_{M-IPOS} \geq \left. \frac{d_{S1}(1-d_{S1})V_{in,rms,min}}{2\sqrt{2}k_{iL}P_{in}f_S} \right|_{d_{S1}=0.5} \tag{18}$$

Comparing (15) and (18), if all three converters have the same inductor current ripple requirement, the M-IPOS boost PFC converter only need half inductance of that in the conventional and IPOP boost PFC converters, which is an advantage in terms of volume and cost. Based on (15) and (18), each inductance in the three compared converters can be determined and the components are selected as listed in Table II. Fig. 12 shows the corresponding comparison results in terms of cost, power loss, and volume. Note that the comparison results presented here only considers the components in the power stage since this paper mainly discusses the topologies. The required capacitance calculation can refer to [43].

In Table II, since that Infineon CoolMOS C7 have only 600 V and 650 V rated voltage series [48] and for CoolSiC G5 , they only have 650 V and 1200 V rated voltage series [49]. Thus, even though the M-IPOS boost PFC converter has lower voltage stresses across switches and diodes compared to the conventional and IPOP boost PFC converters, the same voltage rated components are selected in this case. Meanwhile, the considered design priority here is minimal power losses, thus MOSFETs IPW65R045C7 with different heatsinks are selected in the all three compared converters to ensure the minimal power losses target in each topology. Note that if the considered design priority is minimal cost, then in the M-IPOS boost PFC converter, IPW65R065C7 with heatsink SW50_2G ($R_{thhs}$=8.8 °C/W) should be selected, as this combination has lower total cost (10.8 €) than the combination IPW65R045C7 with heatsink SW25_2G (total cost 12.3 €), even although this combination has higher power losses than the combination IPW65R045C7 with heatsink SW25_2G.

For this design results at hand (cf. Fig. 12), the conventional boost PFC converter still has lower cost and volume advantages over the bridgeless type boost PFC converters even though relatively large heatsinks have been used for the diode bridge and MOSFET. Nevertheless, both bridgeless type converters have comparable higher efficiency than the

TABLE II. Component selection results of converters

| Converters | $L$ (WF$\in$ 25% $\sim$ 40%) | $S+Hs$ ($T_{\mathrm{j,cal}} \in 100 \pm 2$ °C) | $Caps$ ($T_{\mathrm{j,cal}} \in 95 \pm 5$ °C) | $D+Hs$ ($T_{\mathrm{j,cal}} \in 100 \pm 2$ °C) | $D_{\mathrm{R}}$+$Hs$ ($T_{\mathrm{j,cal}} \in 135 \pm 2$ °C) |
|---|---|---|---|---|---|
| M-IPOS boost | 0077094A7 ×1<br>(254 µH) | IPW65R045C7 (650 V) ×2<br>SW25-2G ($R_{\mathrm{thhs}}$ = 11.4 °C/W) ×2 | LGG2E152MELB50 ×2<br>(250 V / 1500 µF) | IDH06G65C5 (650 V) ×2<br>SW38-2G ($R_{\mathrm{thhs}}$ = 10.2 °C/W) ×2 | BU2506 (600 V) ×1<br>YB32-4G ($R_{\mathrm{thhs}}$ = 6.8 °C/W) ×1 |
| IPOP boost | 0077730A7 ×2<br>(508 µH each) | IPW65R045C7 (650 V) ×2<br>PA-T2X-38E ($R_{\mathrm{thhs}}$ = 7.5 °C/W) ×2 | LGG2W391MELB40 ×2<br>(450 V / 390 µF) | IDH06G65C5 (650 V)×2<br>507302B00000G ($R_{\mathrm{thhs}}$ = 24.5 °C/W) ×2 | BU2506 (600 V) ×1<br>YB32-4G ($R_{\mathrm{thhs}}$ = 6.8 °C/W) ×1 |
| Conv. boost | 0077730A7 ×1<br>(508 µH) | IPW65R045C7 (650 V) ×1<br>PA-T21-38E ($R_{\mathrm{thhs}}$ = 3.1 °C/W) ×1 | LGG2W391MELB40 ×2<br>(450 V / 390 µF) | IDH06G65C5 (650 V) ×1<br>SW38-2G ($R_{\mathrm{thhs}}$ = 10.2 °C/W) ×1 | PB4006 (600 V) ×1<br>PA-T21-38E ($R_{\mathrm{thhs}}$ = 3.1 °C/W) ×1 |

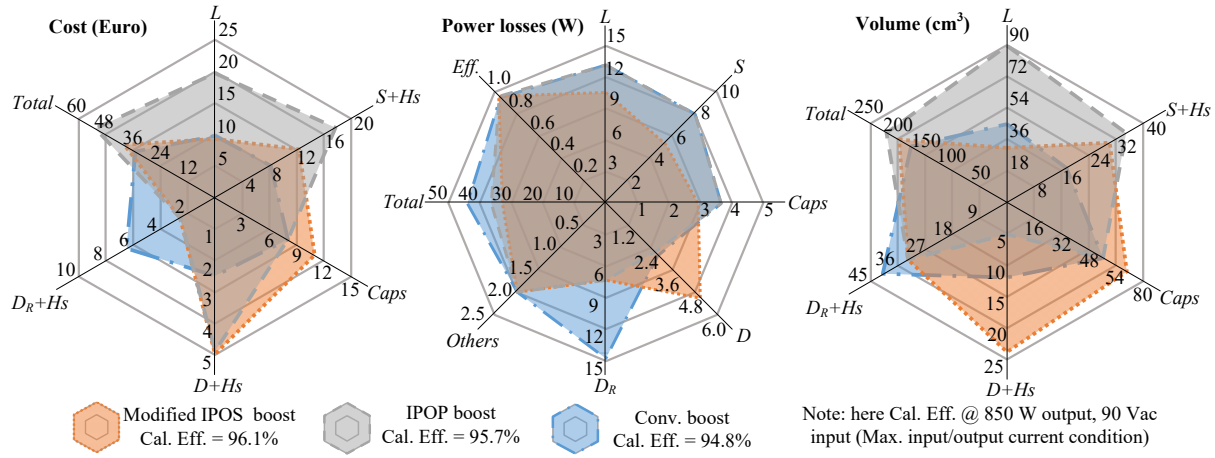


Fig. 12. Comparison results between the M-IPOS, IPOP, and Conventional boost PFC converters in terms of power stage's cost, power loss, and volume.

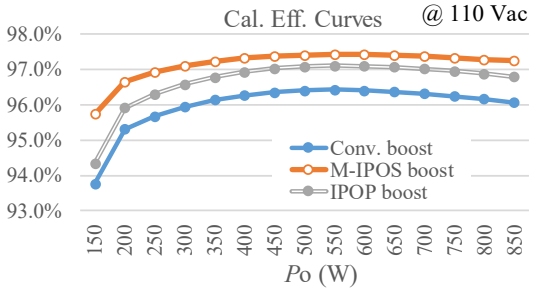


Fig. 13. The calculated efficiency of the M-IPOS boost, IPOP boost, and conventional boost PFC converters over different load conditions. Here for simplicity, CM chock is considered as a pure resistant in each topology.

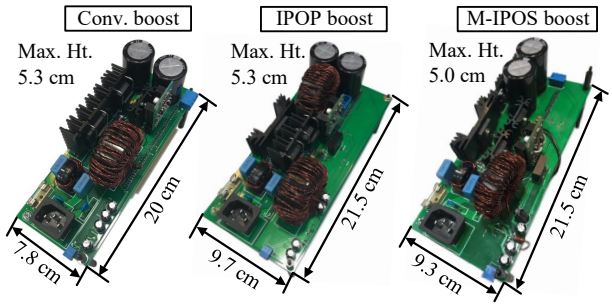


Fig. 14. Experimental prototypes of three compared converters.

conventional boost PFC converter. Besides, compared to the IPOP boost PFC converter, the M-IPOS boost PFC converter has lower cost and volume due to the requirement of only one single smaller inductor and the switches with cheaper heatsinks (cf. '$L$' and '$S+Hs$' dimensions in Fig. 12).

However, in order to have the same output power, the output diode currents in the M-IPOS boost PFC converter have to be twice large as that in the IPOS and conventional boost PFC converters, because of the split DC output voltage (½$V_{\mathrm{o}}$) in each converter cell. Therefore, the output diodes consume more power losses in the M-IPOS boost PFC converter and larger heatsinks have to be used with the output diodes, which increase the volume and cost in the M-IPOS boost PFC converter. That is a disadvantage of this topology.

Fig. 13 shows the calculated efficiency curves of the three compared converters. It indicates that among the three converters, the M-IPOS boost PFC converter has higher efficiency over different load conditions, especially, in light-load conditions. This is because the lower switching losses in the M-IPOS boost PFC converter do not decrease too much its efficiency curve as what happened in the IPOP and conventional boost PFC converters.

## IV. Experimental Validations and Analysis

### A. Prototypes

Based on Table I and Table II, the conventional, IPOP, and M-IPOS boost PFC converters have been built and Fig. 14 shows these prototypes. The control board, implemented by TMS320F28335, is inserted on the bottom of each main board. The efficiency, PF, and THD$_i$ are measured by the N4L. Fig. 14 shows that among the three compared converters, the conventional boost PFC converter has the smallest volume and the IPOP boost PFC converter has the largest one.

### B. Experimental Results

Fig. 15 shows the input and output waveforms of the three compared converters in 850 W load condition and Fig. 16

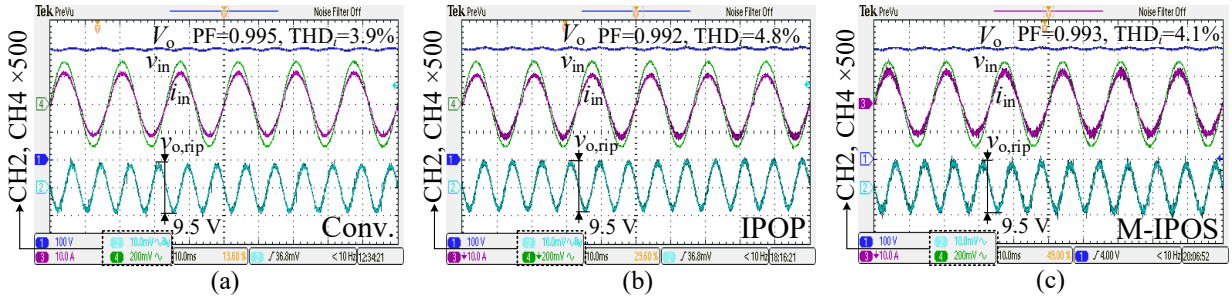


Fig. 15. The input and output waveforms of the three compared converters in 850 W load condition: output voltage $V_{\rm o}$ [100 V/div], input voltage $v_{\rm in}$ [100 V/div], input current $i_{\rm in}$ [10 A/div], and output voltage ripple $v_{\rm o,rip}$ [5 V/div] of (a) the conventional boost, (b) the IPOP boost, and (c) the M-IPOS boost.

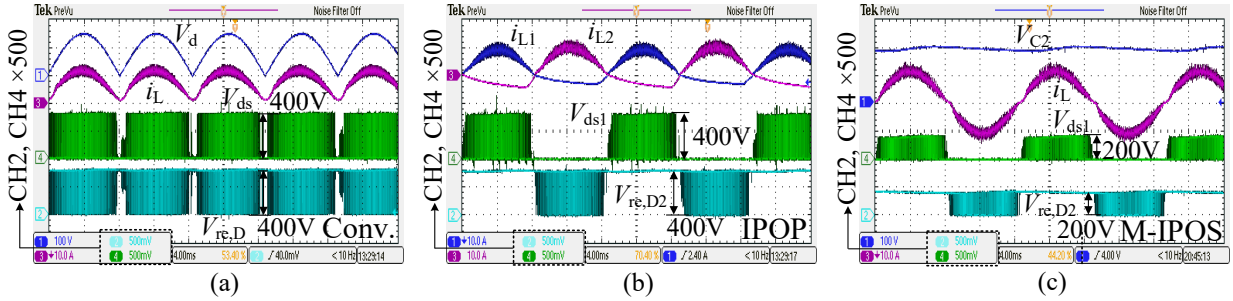


Fig. 16. The waveforms inside the compared converters in 850 W load condition: (a) conventional boost with the voltage after diode bridge $V_{\rm d}$ [100 V/div], inductor current $i_{\rm L}$ [10 A/div], drain-source voltage of switch $V_{\rm ds}$ [250 V/div], and reverse voltage across output diode $V_{\rm re,D}$ [250 V/div]; (b) IPOP boost with inductor current $i_{\rm L1}$ and $i_{\rm L2}$ [10 A/div], drain-source voltage of switch $V_{\rm ds1}$ [250 V/div], and reverse voltage across output diode $V_{\rm re,D2}$ [250 V/div]; (c) IPOS boost with output capacitor voltage $V_{\rm C2}$ [100 V/div], inductor current $i_{\rm L}$ [10 A/div], drain-source voltage of switch $V_{\rm ds1}$ [250 V/div], and reverse voltage across output diode $V_{\rm re,D2}$ [250 V/div].

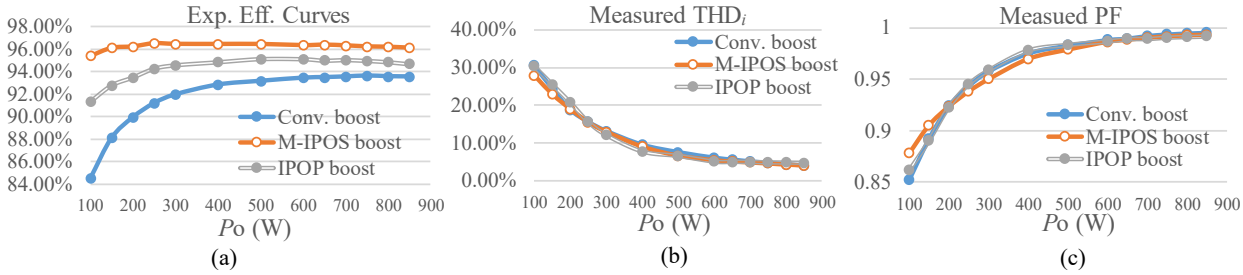


Fig. 17. The measured efficiency, THD$_i$, and PF of the conventional, M-IPOS, and IPOP boost PFC converters in different load conditions at 110 Vac input voltage: (a) efficiency, (b) THD$_i$, and (c) PF.

shows the corresponding waveforms inside the converters. Comparing Figs. 15(a), (b), and (c), it indicates that all three converters have similar performances in 850 W load condition in terms of output voltage ripple, PF, and THD$_i$. Seen from Figs. 16(a), (b), and (c), the IPOP and M-IPOS boost PFC converters have achieved bridgeless operations since there is no voltage stresses across semiconductors in the corresponding half line cycle. Meanwhile, due to the presences of the anti-parallel diodes across MOSFETs, the inductor currents in the IPOP boost PFC converter has negative returning current flow, which leads to slightly poor PF and THD$_i$ performances [3]. Moreover, the maximum voltage stresses across semiconductors in the M-IPOS boost PFC converter are 200 V, only half of that in the conventional and IPOP boost PFC converters (400 V), which results in lower switching losses in the M-IPOS boost PFC converter.

The measured efficiency, THD$_i$, and PF of the three converters in different load conditions is shown in Fig. 17. Obviously, THD$_i$ and PF performances of these three converters in different load conditions are nearly the same. However, regarding efficiency, both bridgeless topologies have higher efficiency than the conventional boost PFC converter and the M-IPOS boost PFC converter has the highest efficiency among these three converters in the measured load ranges 100∼850 W. Also note that the M-IPOS boost PFC converter, different from its IPOP and conventional topology counterparts, has relatively flat efficiency curve over different load conditions, which means high efficiency is achieved in the light load conditions. Here, mainly due to the presences of the RCD snubber circuits across MOSFETs in the experiment, the measured efficiency curve is different from the calculated one in Fig. 13.

Fig. 18 shows the load transition waveforms of the M-IOPS boost PFC converter. In Fig. 18, the capacitor voltages $V_{\rm C1}$ and $V_{\rm C2}$ are stable and equal to 200 V before and after the load transition, which means that the automatic balance of the capacitor voltages is achieved. Meanwhile, the output voltage

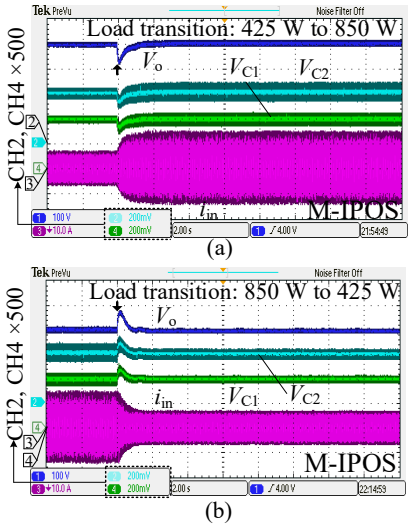


Fig. 18. Load transitions of the M-IPOS boost PFC converter at 110 Vac input voltage with output voltage $V_o$ [100 V/div], capacitor voltages $V_{C1}$ and $V_{C2}$ [100 V/div], and input current $i_{in}$ [10 A/div]: (a) 425 W to 850 W, (b) 850 W to 425 W.

$V_o$ and the input current $i_{in}$ are stable after the load transition so the average current control is effective enough to control this M-IPOS boost topology.

### C. Mission Profiles Based Energy Losses Comparison

In order to make the comparison between bridgeless topologies more meaningful, this part introduces two power load mission profiles of the typical telecom base stations in the urban area and countryside, extracted from [8]. A base station is an important facility to receive, process, and send the telecom signals. Fig. 19 shows the specific mission profiles and the typical configuration of a base station. Due to the tolerant operation requirement in the base station, there are at least two power supply units (PSUs) in the power chassis to support these different units. Among these units, the remote radio units (RRUs) and feeder are the most power consumption sections, which receive and send the information between devices, e.g., cell phones and the base stations. That is the reason that the extracted mission profiles have such a power load curve in a typical day, i.e., heavy loads in working hours and light loads in the late night.

Based on Fig. 19, assuming the three compared topologies are used in the PSU AC-DC conversion part and fan is not required to conduct the heat dissipation here. Then, based on the power load mission profiles, the long-term energy losses and the corresponding operation costs in one year of these topologies can be calculated according to the experimental efficiency curves in Fig. 17(a) and the industrial electricity prices (0.06 €/kWh) in USA [50]. Meanwhile, besides the component costs in the power stage (cf. Fig. 12), other key devices' prices are also estimated by referring the average prices (only consider devices in stock) given in Mouser [51] and Table **??** shows the key devices in each topology. Afterward, by summing up all the evaluated components' prices, the final material costs of the three compared converters are obtained.

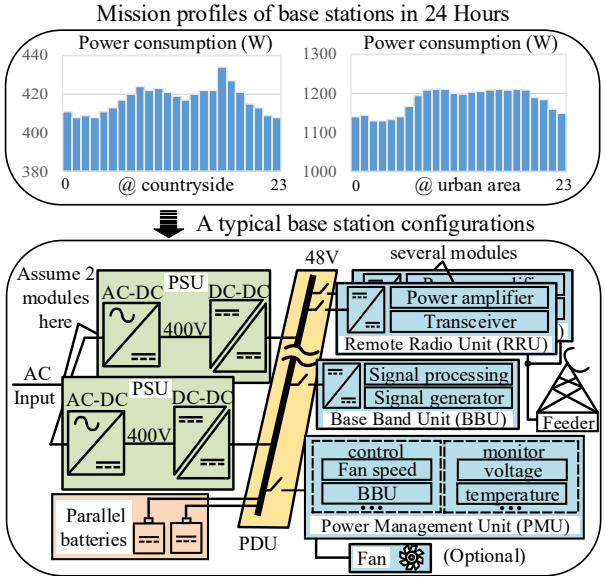


Fig. 19. Two power load mission profiles of the base stations within 24 hours in the countryside and urban, along with a typical base station configuration. Two 850 W PSUs are assumed in the base station to support the different load conditions.

TABLE III. Component Count Comparison of Bridgeless Topologies

| Part number | Conv. | IPOS | IPOP |
|---|---|---|---|
| ACPL-C790-000E (Sampling) | $2.79\times1$ | $2.79\times3$ | $2.79\times2$ |
| TMA 1205S (Iso. DC-DC) | $3.18\times1$ | $3.18\times3$ | $3.18\times2$ |
| TMA 1212S (Iso. DC-DC) | $3.18\times1$ | $3.18\times2$ | $3.18\times2$ |
| LM1117MP-3.3 (5 V to 3.3 V) | 0.45 | 0.45 | 0.45 |
| LM2596S-5.0 (12 V to 5 V) | 2.25 | 2.25 | 2.25 |
| ADUM3223ARZ (drive) | 2.18 | 2.18 | 2.18 |
| CM chock (7448042001) | 8.10 | 8.10 | 8.10 |
| TMS320F28335PGFA | 16.73 | 16.73 | 16.73 |

Fig. 20 shows the operation costs in one year and the estimated material costs of these three compared converters. According to Fig. 20, if the M-IPOS boost topology is used to replace the conventional boost topology, it takes 3.9 years to get payback in the countryside and 0.36 years in the urban area. The results presented here have neglected the power losses in fan for heat dissipation, which will reduce the payback period if they are taken into account since the lower power losses generated by the M-IPOS boost topology can result in lower power consumed by fan.

## V. Conclusion

This paper consists of two major parts. In the first part, this paper introduces bridgeless topology derivation method by arranging two different or same converter cells in IPOP and IPOS manners, which can serve as a tool to derive more other bridgeless topologies. Specifically, 'why these configurations work' and 'how they can be obtained' have been elaborated with detailed graphics, which include using the basic converter cells as examples to derive their corresponding bridgeless topologies (cf. Figs. 2, 3, and 4). Furthermore, possible research points are summarized after the topology reviews.

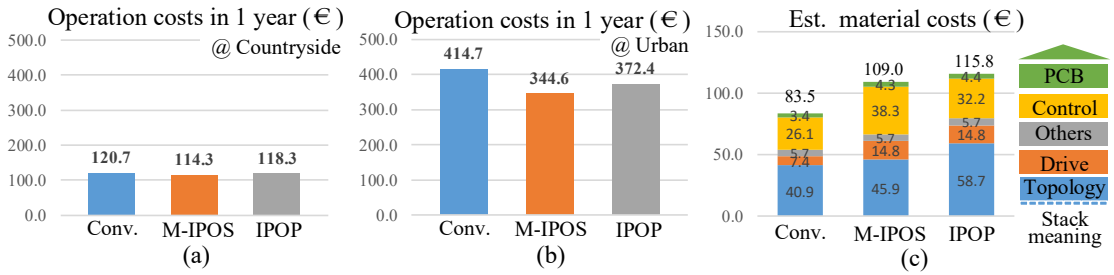


Fig. 20. The cost comparison between the conventional, M-IPOS, and IPOP boost PFC converters: (a) operation costs at the countryside, (b) operation costs at the urban area, (c) estimated material costs in experiment prototypes.

In the second part, a consistent component sizing procedure with the electrical, thermal, and cost models is applied to the conventional, IPOP, and M-IPOS boost PFC converters. The comparison results in considerations of power stage's cost, power loss, and volume indicate that compared to the IPOP and M-IPOS boost PFC converters, the conventional boost PFC converter still has lower cost and volume, although larger heatsinks are employed in semiconductors; Nonetheless, regarding efficiency, it has apparently poor performance than the two compared bridgeless converters. On the other hand, the M-IPOS boost PFC converter has higher efficiency with lower cost and volume compared to its IPOP boost topology counterpart. Moreover, experimental results of three built 850 W prototypes show similar performances between converters regarding PF and $\text{THD}_i$, and confirm the theoretical efficiency results obtained from the component sizing procedure. Finally, combining the power load mission profiles of base stations and the measured efficiency curves, the material cost payback periods of using the M-IPOS boost topology instead of the conventional boost topology are calculated as 0.36 years in the urban and 3.9 years in the countryside.

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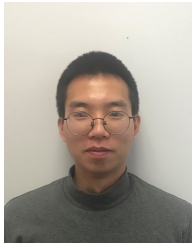

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