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Evaluation of Three-Phase Transformerless DC-Bypass PV Inverters for Leakage Current Reduction

Xiaoqiang Guo, Senior Member, IEEE, Na Wang, Baocheng Wang, Zhigang Lu, and Frede Blaabjerg, Fellow, IEEE

Abstract—In transformerless PV systems, the leakage current reduction is one of the most important issues. Many interesting single-phase dc-bypass transformerless PV inverters have been proposed for the leakage current reduction. And there is a well-known conclusion that the clamping topology is better than the unclamping one in terms of leakage current reduction. However, is this conclusion correct for three-phase dc-bypass ones? The main objective of this paper is to investigate the impact of clamping and unclamping dc-bypass switches on the leakage current reduction capability of three-phase transformerless inverters. The findings reveal that the conclusion is different from the single-phase dc-bypass ones. The theoretical analysis and experimental results are provided to verify the new insights.

Index Terms—Three-phase PV system, transformerless dc-bypass inverter, common mode voltage, leakage current

I. INTRODUCTION

PV systems are becoming more prevalent due to their advantages over conventional power generations [1], [2]. By harvesting energy from PV panels, they can provide a sustainable solution for the power generation. Typically, solar energy can be harvested by a grid-connected PV inverter with or without the transformer. Basically, the transformer is heavy, bulky, costly, and suffers from the power loss. Also, the control performance would be affected by the transformer depending on the winding configurations [3], which is often overlooked in literature. Therefore, the transformerless PV inverters have received more and more attention in both academic and industrial fields [4-6]. However, there are technical challenges to deal with before connecting them into grid. One of the technical issues is to reduce the leakage current, which is mainly due to the lack of galvanic isolation [7]. The leakage current has the adverse impact on the grid current, potential human safety and the EMI problems. Therefore, the VDE 0126-1-1 specifies that the PV systems must be disconnected from the grid on the condition that the leakage current is beyond 300 mA.

In order to cope with this problem, many insightful single-phase topologies have been proposed such as H5, H6, Heric and so on [8-15]. The basic goal is to achieve constant common-mode voltage for eliminating the leakage current, and meanwhile output the three-level PWM waveform, instead of two-level one, in order to reduce the power loss and alleviate the filter size towards the high power density and low cost. Theoretically, the constant common-mode voltage can be achieved with the abovementioned topologies. In practice, however, the common mode voltage is time-varying depending on the junction capacitor of the power switches. Yang and Li, et al [16] presented, for the first time, a systematic analysis of this technical point, and the findings revealed that the common-mode voltage varied depending on the junction capacitances of the power switches in the dc-decoupling states. One possible solution is installing the additional capacitors paralleled to the respective power switches to match the value principle of the junction capacitors. The idea is interesting and insightful, but the junction capacitances of practical switches are generally nonlinear and hard to be matched accurately. Also, the switching losses would be increased by the additionally paralleled capacitors. Another solution is integrating the clamping branch in the previous topology. Xiao and Xie, et al, proposed an optimized transformerless photovoltaic grid-connected inverter, named oH5 [17]. Two additional switches are installed in the single-phase full-bridge inverter, which aims that the freewheeling path is clamped to half input voltage. Therefore, it is able to achieve the constant common mode voltage during the entire operation cycle to eliminate the leakage current. In similar manner, Kerekés, et al [18] proposed a HB-ZVR topology with a switch clamping to the dc midpoint. A modified HB-ZVR topology proposed by Freddy, et al uses an additional fast-recovery diode to optimize the common-mode behavior [19]. Li, et al presented a comprehensive review of the state-of-art of transformerless PV inverters, and then proposed an interesting family of clamping solutions to the Heric topology for the constant common-mode voltage. One active switch or two passive diodes can be used to clamp the common-mode voltage to half of the dc bus voltage during the freewheeling mode [20]. Roberto, et al integrated two passive diodes in dc-bypass H6 for clamping the common-mode voltage to half of the input voltage [21]. In this way, the common-mode voltage would be constant all the time, in order to eliminate the leakage current.

From the abovementioned single-phase topologies, there is a well-known conclusion that the clamping topology is better than the unclamping one in terms of leakage current reduction [20]. However, is this conclusion correct for three-phase dc-bypass ones? So far this has not yet been explored, and is the motivation to cover this gap.

The objective of this paper is to investigate the impact of clamping and unclamping dc-bypass switches on the leakage current reduction capability of three-phase transformerless inverters. The rest of the paper is organized as follows. Section II provides the theoretical analysis of the common-mode behavior for both clamping and unclamping dc-bypass topologies of three-phase transformerless PV inverters. Section III presents the experimental results. Finally, new insights are concluded in Section IV.
II. ADDITIONAL REQUIREMENTS

This section presents the theoretical analysis of the common-mode behavior of three-phase dc-bypass topologies, in order to figure out the impact of clamping and unclamping dc-bypass switches on the leakage current reduction capability of three-phase transformerless inverters. Inspired by the recent single-phase dc-bypass inverters, the three-phase dc-bypass ones can be derived [22-23], as shown in Fig. 1. There is a question, which is the best choice for the leakage current reduction among different three-phase dc-bypass topologies.

A. Common-mode Behavior of H7 Topology

Similar to single-phase H5, an additional switch can be integrated in the dc side of three-phase H-bridge inverter, name H7, as shown in Fig. 1(a). The additional switch is used to isolate the PV panel from the grid during the freewheeling operation mode. An interesting modulation method is proposed in [22]. The switching gating signal can be obtained by simple carrier-based modulation and logic functions as shown in Fig. 2, where $m_a, m_b, m_c$ are the sinusoidal modulating signals, and $V_0$ is the zero-sequence signal. The logic functions are defined in (1).

\[
\begin{align*}
S_a &= A + (A + B + C) \quad S_2 = \overline{S_1} \\
S_b &= B + (A + B + C) \quad S_3 = \overline{S_2} \\
S_c &= C + (A + B + C) \quad S_4 = \overline{S_3} \\
S_7 &= \overline{ABC}
\end{align*}
\]
The relationship between switching states of H7 topology and common-mode voltage is listed in Table I.

**SWITCHING STATES AND COMMON-MODE VOLTAGE OF H7 TOPOLOGY**

<table>
<thead>
<tr>
<th>Mode</th>
<th>(U_{AN})</th>
<th>(U_{BN})</th>
<th>(U_{CN})</th>
<th>(U_{CM})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1(1001))</td>
<td>(U_D)</td>
<td>0</td>
<td>0</td>
<td>(U_D/3)</td>
</tr>
<tr>
<td>(M_2(0101))</td>
<td>0</td>
<td>(U_D)</td>
<td>0</td>
<td>(U_D/3)</td>
</tr>
<tr>
<td>(M_3(0011))</td>
<td>0</td>
<td>0</td>
<td>(U_D)</td>
<td>(2U_D/3)</td>
</tr>
<tr>
<td>(M_4(1101))</td>
<td>(U_D)</td>
<td>(U_D)</td>
<td>0</td>
<td>(2U_D/3)</td>
</tr>
<tr>
<td>(M_5(0111))</td>
<td>0</td>
<td>0</td>
<td>(U_D)</td>
<td>(2U_D/3)</td>
</tr>
<tr>
<td>(M_6(1011))</td>
<td>(U_D)</td>
<td>0</td>
<td>(U_D)</td>
<td>(2U_D/3)</td>
</tr>
<tr>
<td>(M_7(1111))</td>
<td>(U_D)</td>
<td>(U_D)</td>
<td>(U_D)</td>
<td>(2U_D/3)</td>
</tr>
<tr>
<td>(M_9(1100))</td>
<td>3(U_D/4)</td>
<td>3(U_D/4)</td>
<td>3(U_D/4)</td>
<td>3(U_D/4)</td>
</tr>
</tbody>
</table>

During the freewheeling period, switches \(S_1\), \(S_3\) and \(S_5\) turn on and switches \(S_2\), \(S_4\), \(S_6\) and \(S_7\) turn off. Theoretically, there is no path for the leakage current to flow. The values of \(U_{AN}\) and \(U_{CN}\) decrease, and \(U_{BN}\) increase until their values are equivalent. However, it is not the case in practice. Considering the junction capacitances of power switches, as shown in Fig. 3(b). \(C_1\) and \(C_7\) represent the junction capacitors of the switches \(S_1\) and \(S_7\). Fig. 4 shows the equivalent circuit, where \(R\) is the ground resistance [22], and the initial voltages are indicated in the brackets. It can be observed that the junction capacitor \(C_4\) is charged by \(C_2\), \(C_6\) and \(C_7\) in parallel. From Fig. 4, the common-mode voltage \(U_{CM}\), \(U_{AN}\), \(U_{BN}\) and \(U_{CN}\) can be obtained as follows.

\[
U_{CM} = U_{AN} = U_{BN} = U_{CN} = \frac{C_2 + C_6 + C_7}{C_2 + C_6 + C_7} U_D \tag{3}
\]

From (3), it can be seen that the common-mode voltage is \(3U_D/4\) on the condition that the junction capacitances of the power switches are equal. However, in practice, \(U_{AN}\), \(U_{BN}\) and \(U_{CN}\) are dependent on both system parasitic parameters and junction capacitances of the switches. Consequently, the common-mode voltage would oscillate during the freewheeling state, which will be verified in experimental section. Fig. 5 shows the corresponding common-mode model. The transfer function between \(U_{BN}\) and \(U_{CM}\) can be calculated, which is useful in order to evaluate the leakage current reduction capability. Assuming that the junction capacitances of the switches are same, and its value is \(C_s\).

\[
G_s(s) = \frac{U_{BN}}{U_{CM}} = \frac{1 + sC_{PV}R}{1 + C_s + sC_{PV}R + 2s^2LC_{PV}/3} \tag{4}
\]

As discussed above, the common-mode voltage oscillates during the freewheeling period. The oscillation can be avoided by adding the clamping branch, as shown in Fig. 1(b). The function of the clamping circuit is to clamp the voltage of point A, B and C to \(U_D/2\) during the freewheeling switching period. The clamping switch \(S_8\) operates complementally with
S7. During the freewheeling period, the current flow through the dc side capacitor and the clamping switch, and the corresponding common-mode model of oH7 topology is shown in Fig. 6, where \( C_{d1} \) and \( C_{d2} \) are the dc-link capacitors.

\[
G_2(s) = \frac{U_{ON}}{U_{CM}} = \frac{1 + sC_{PV}R}{1 + C_{PV}/(2C_{d1} + C_{d2}) + sC_{PV}R + 2s^2LC_{PV}/3} 
\]  

(5)

It should be noted that the operation states of H7 and oH7 are the same during the active states. The only difference is during the freewheeling period, where the common-mode model is different, as shown in Fig. 5 and Fig. 6. In order to compare the leakage current reduction capability of H7 and oH7, the Bode diagram of the transfer function in (4) and (5) is provided in Fig. 7. Each of the parameters in (4) and (5) is given in Table III, where both the capacitors of dc link (\( C_{d1}, C_{d2} \)) are 940 μF and the junction capacitance of the switch is specified to be 39 pF.

![Fig.6 Common-mode model of oH7 topology during freewheeling period.](image)

Similarly, the transfer function between \( U_{ON} \) and \( U_{CM} \) can be calculated from Fig. 6, as shown in (5). Assuming that the dc-link capacitors \( C_{d1} \) and \( C_{d2} \) are equal, and both of their values are \( C_D \).

\[
G_2(s) = \frac{U_{ON}}{U_{CM}} = \frac{1 + sC_{PV}R}{1 + C_{PV}/(2C_{d1} + C_{d2}) + sC_{PV}R + 2s^2LC_{PV}/3} 
\]  

(5)

From Fig.7, it can be observed that the operation states of H7 and oH7 are the same during the active states. The only difference is during the freewheeling period, where the common-mode model is different, as shown in Fig. 5 and Fig. 6. In order to compare the leakage current reduction capability of H7 and oH7, the Bode diagram of the transfer function in (4) and (5) is provided in Fig. 7. Each of the parameters in (4) and (5) is given in Table III, where both the capacitors of dc link (\( C_{d1}, C_{d2} \)) are 940 μF and the junction capacitance of the switch is specified to be 39 pF.

![Fig.7 Bode diagram of (4) and (5) for H7 and oH7.](image)

B. Common-mode Behavior of H8 Topology

Inspired by single-phase H6 topology, an H8 topology can be derived, as shown in Fig. 1(c). The gating signal can be obtained with modulation structure shown in Fig. 2. The only difference is the logic function, which is defined as follows.

\[
S_1 = A + \overline{B}C \quad S_2 = \overline{A} + BC
\]

\[
S_3 = B + \overline{A}C \quad S_4 = \overline{B} + AC
\]

\[
S_5 = C + \overline{A}B \quad S_6 = \overline{C} + AB
\]

\[
S_7 = S_5 = \overline{A}C + \overline{A}B + B\overline{C}
\]

(6)

The switching patterns and corresponding common-mode voltage of H8 are shown in Table II. Different from H7, in Mode 7 of M8(***0), S7 and S8 are turned off, and other six switches are turned on. Compared with the change range of the common-mode voltage (\( U_{MAX-MIN} \)) of 2\( U_D/3 \) in Table I for H7, it can be observed that \( U_{MAX-MIN} \) is reduced by 50% to \( U_D/3 \), as shown in Table II. Therefore, the leakage current reduction capability of the H8 is better than of the H7.

<table>
<thead>
<tr>
<th>Mode</th>
<th>( U_{AN} )</th>
<th>( U_{BN} )</th>
<th>( U_{CN} )</th>
<th>( U_{CM} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1(1001)</td>
<td>( U_D )</td>
<td>0</td>
<td>0</td>
<td>( U_D/3 )</td>
</tr>
<tr>
<td>M2(1010)</td>
<td>0</td>
<td>( U_D )</td>
<td>0</td>
<td>( U_D/3 )</td>
</tr>
<tr>
<td>M3(0011)</td>
<td>0</td>
<td>0</td>
<td>( U_D )</td>
<td>( U_D/3 )</td>
</tr>
<tr>
<td>M4(1011)</td>
<td>( U_D )</td>
<td>( U_D )</td>
<td>0</td>
<td>2( U_D/3 )</td>
</tr>
<tr>
<td>M5(1011)</td>
<td>0</td>
<td>( U_D )</td>
<td>( U_D )</td>
<td>2( U_D/3 )</td>
</tr>
<tr>
<td>M6(***0)</td>
<td>( U_D/2 )</td>
<td>( U_D/2 )</td>
<td>( U_D/2 )</td>
<td>( U_D/2 )</td>
</tr>
</tbody>
</table>

When the switching state is M6(1011), the switches S1, S4, S5, and S6 turn on, and the switches S2, S3, and S7 turn off, as shown in Fig. 8(a). In this mode, it is obvious that the common mode voltage is 2\( U_D/3 \). During the freewheeling period, S7 and S8 turn off, and other six switches turn on. The equivalent circuit of the freewheeling switching state is illustrated in Fig. 8(b). Taking into account the junction capacitance of the power switches, the corresponding common-mode voltage can be calculated from Fig. 9.

\[
U_{CM} = U_{AN} = U_{BN} = U_{CN} = \frac{C_7}{C_7 + C_D} U_D 
\]  

(7)

![Fig.9 Equivalent circuit of H8 topology during the freewheeling period.](image)
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From (7), it can be observed that the common-mode voltage is $U_D/2$ if the junction capacitances of power switches are identical. Similarly, the common-mode voltage would oscillate during the freewheeling state, which will be verified in experimental section in this paper. Fig. 10 shows the corresponding common-mode model. The larger the leakage current flows in the common-mode loop, the greater the influence of the grid current is [2]. Therefore, the small leakage current leads to better grid current. The transfer function between $U_{ON}$ and $U_{CM}$ of H8 topology is calculated as:

$$G_a(s) = \frac{U_{ON}}{U_{CM}} = \frac{1 + sC_{PV}R}{1 + C_{PV} / (C_1 + sC_{PV}R + 2s^2LC_{PV}/3)} \quad (8)$$

Fig. 10: Common-mode model of H8 topology during the freewheeling period.

As discussed above, the common-mode voltage oscillates during the freewheeling period. The oscillation can be avoided by adding the clamping branch, as shown in Fig. 1(d). The function of the clamping circuit is to clamp $U_{ON}$, $U_{DN}$ and $U_{CN}$ to $U_D/2$ during the freewheeling period. The upper diode ($D_1$) turns on when the unclamped voltage is less than $U_D/2$, while the lower diode ($D_2$) turns on when the unclamped voltage is beyond $U_D/2$. Take the former case for example, the common-mode model is shown in Fig. 11.

Similarly, the transfer function between $U_{ON}$ and $U_{CM}$ can be calculated from Fig. 11, as shown in (9).

$$G_a(s) = \frac{U_{ON}}{U_{CM}} = \frac{1 + sC_{PV}R}{1 + C_{PV} / (C_1 + sC_{PV}R + 2s^2LC_{PV}/3)} \quad (9)$$

Note that the operation states of H8 and oH8 are identical during the active states. The only difference is during the freewheeling period, where the common-mode model is different, as shown in Fig. 10 and Fig. 11. In order to compare the leakage current reduction capability of H8 and oH8, the Bode diagram of the transfer function in (8) and (9) is as illustrated in Fig. 12.

From Fig. 12, it can be seen that the amplitude of oH8 is higher than of H8. That is to say, for a given common-mode voltage, the parasitic capacitor voltage of the oH8 is higher than of the H8. Consequently, the leakage current of the oH8 would be higher than of the H8 topology. Similarly, the leakage current reduces when the parasitic capacitor increases as shown in Fig. 8.

In summary, different from the well-known conclusion for single-phase dc-bypass transformerless PV inverters [20], the unclamping three-phase dc-bypass topology is better than the clamping one in terms of the leakage current reduction. In addition, H8 is better than H7, due to the reduced amplitude of common-mode voltage by 50%, which is beneficial to the leakage current attenuation. The new insights will be experimentally verified in the following section.

### III. EXPERIMENTAL RESULTS

In order to verify the impact of dc-bypass switches on the leakage current reduction capability of three-phase topologies, a prototype is built in the lab. The control is implemented with TMS320F28335 DSP, while the logic function of (1) and (6) is implemented in Xilinx XC6SLX9 FPGA. The system parameters are listed in Table III.

The control structures of the four topologies in Fig. 1 are similar, except the logic functions for doing the modulation. For simplicity, only one control structure is presented in Fig. 13. The grid voltage is collected into the phase-locked loop (PLL), and the output of the PLL is the phase angle $\theta$ of the grid. The current reference is generated according to the phase angle of the grid, and then the current control loop is entered. Where, the PR regulator is adopted in the current close loop. The outputs of the current closed loop are the three-phase modulated signals, which are compared with the triangular carrier to obtain the input signals of the logic function. The logic operation is performed in the FPGA, and the gating signals of the H8 topology can be obtained according to (6).
Table III

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>1 kW</td>
</tr>
<tr>
<td>Input voltage</td>
<td>250 V</td>
</tr>
<tr>
<td>Grid voltage (peak value of grid voltage/50 Hz)</td>
<td>100 V</td>
</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>10kHz</td>
</tr>
<tr>
<td>Filter inductors (L)</td>
<td>5 mH</td>
</tr>
<tr>
<td>Stray capacitor ($C_{PV}$)</td>
<td>300 nF</td>
</tr>
<tr>
<td>DC-link capacitors ($C_{d1}$, $C_{d2}$)</td>
<td>940 μF</td>
</tr>
<tr>
<td>IGBT</td>
<td>IKW40T120</td>
</tr>
<tr>
<td>Diode</td>
<td>DSEJ30-10A</td>
</tr>
</tbody>
</table>

Fig. 13 General system control block diagram used for control of the inverter.

Fig. 14 shows the experimental results of the output line-line voltage, grid voltage and grid current of four topologies. It can be observed that all line-line voltages are unipolar three-level. The grid current THDs of H7, oH7, H8, and oH8 are 4.97%, 6.09%, 4.33%, 5.07%, respectively.
Fig. 14 Experimental results of line-line voltage, grid voltage and grid current. (a) H7 topology; (b) H8 topology; (c) oH7 topology; (d) oH8 topology.

Fig. 15 shows the experimental results of $U_{AN}$, $U_{BN}$ and $U_{CN}$. The detailed waveforms during the switching cycle are shown in Fig. 16. It can be observed that the experimental results are in agreement with theoretical analysis given in Table I and Table II. On the other hand, the voltage oscillates for unclamped H7 and H8 during the freewheeling period, mainly due to the junction capacitance of the switches and system parasitic parameters. While for oH7 and oH8, $U_{AN}$, $U_{BN}$ and $U_{CN}$ are clamped in $U_D/2$ during freewheeling period.

Fig. 15  Experimental results of $U_{AN}$ (top), $U_{BN}$ (middle) and $U_{CN}$ (bottom). (a) H7 topology; (b) H8 topology; (c) oH7 topology; (d) oH8 topology.
Fig. 16 Experimental results of $U_{AN}$ (top), $U_{BN}$ (middle) and $U_{CN}$ (bottom). (a) H7 topology; (b) H8 topology; (c) oH7 topology; (d) oH8 topology.

Fig. 17 shows the experimental results of parasitic capacitor voltage and leakage current of the four topologies. In agreement with the theoretical analysis in Section II, the unclamping three-phase dc-bypass topology is better than the clamping one in terms of the leakage current reduction. And the H8 is better than H7, due to the reduced amplitude of the common-mode voltage. The maximum of leakage currents for H7, oH7, H8, and oH8 are 528 mA, 544 mA, 192 mA, 272 mA, respectively. Only H8 and oH8 can reduce the leakage current below 300 mA, which well meet the VDE 0126-1-1 standard. With the clamping branch, the leakage currents for oH7 or oH8 are higher than H7 or H8, which is in agreement with theoretical analysis in Fig. 7 and Fig. 12. A performance comparison is listed in Table IV.

Fig. 17 Experimental results of parasitic capacitor voltage and leakage current. (a) H7 topology; (b) H8 topology; (c) oH7 topology; (d) oH8 topology.
As can be seen from Table IV, the three-phase dc-bypass inverters without clamping switches have smaller leakage current than the three-phase dc-bypass inverters with clamping switches. And the above experimental waveforms are obtained when the parasitic capacitance is 300 nF. In order to verify the influence of the parasitic capacitance on the leakage current, experiments are carried out with different parasitic capacitances using H8 topology and oH8 topology as examples. The experimental results are shown in Fig.18 and the experimental results are summarized in Table V. It can be seen from the results that the leakage current decreases as the parasitic capacitance increases, which verify the theoretical analysis mentioned in section II.

### TABLE IV

<table>
<thead>
<tr>
<th>Topologies</th>
<th>Switches</th>
<th>Diodes</th>
<th>Leakage current</th>
<th>Current THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>H7</td>
<td>7</td>
<td>0</td>
<td>528 mA</td>
<td>4.97%</td>
</tr>
<tr>
<td>oH7</td>
<td>8</td>
<td>0</td>
<td>544 mA</td>
<td>6.09%</td>
</tr>
<tr>
<td>H8</td>
<td>8</td>
<td>0</td>
<td>192 mA</td>
<td>4.33%</td>
</tr>
<tr>
<td>oH8</td>
<td>8</td>
<td>2</td>
<td>272 mA</td>
<td>5.07%</td>
</tr>
</tbody>
</table>

### TABLE V

<table>
<thead>
<tr>
<th>Leakage current</th>
<th>300nF</th>
<th>150nF</th>
<th>75nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>H8</td>
<td>192 mA</td>
<td>232 mA</td>
<td>248 mA</td>
</tr>
<tr>
<td>oH8</td>
<td>272 mA</td>
<td>352 mA</td>
<td>464 mA</td>
</tr>
</tbody>
</table>

Further tests are carried out under different power ratings. As shown in Fig. 19, it can be observed that the unclamped dc-bypass topology is superior to the clamp one for the leakage current reduction, which again verifies the new insight.

### IV. CONCLUSION

This paper has presented the theoretical analysis and experimental evaluation about the impact of clamping and unclamping dc-bypass switches on the leakage current reduction capability for three-phase transformerless PV inverters. The new insights have revealed that, different from the well-known conclusion for single-phase dc-bypass transformerless PV inverters, the unclamping three-phase dc-bypass topology is better than the clamping one in terms of leakage current reduction. In addition, H8 is better than H7, due to the reduced common-mode voltage amplitude, which is beneficial to leakage current attenuation. In summary, the unclamped H8 is the best choice among four dc-bypass topologies for the leakage current reduction. Future research is towards soft-switching three-phase Hx (x=6,7,8,...) topologies, inspired by the soft-switching single-phase H6 topology [24].

### REFERENCES

