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Voltage Grid Supporting by Using Variable Structure Adaptive Virtual Impedance for LCL-VSC DG Converters

Thales Queiroz Fonsêca, *Student Member, IEEE*, Ricardo L. A. Ribeiro, *Senior Member, IEEE*, Thiago de Oliveira Alves Rocha, *Member, IEEE*, Flavio Bezerra Costa, *Member, IEEE*, and Josep M. Guerrero, *Fellow, IEEE*

Abstract—This paper proposes a voltage grid supporting applied for DGs based on LCL-VSC converters to control the delivered power flow and improve the PCC voltage regulation. A variable structure adaptive virtual impedance (VS-AVI) imposes the required DG impedance for achieving the system voltage requirements, considering the power rating of the DG converter. Differently of the solutions presented in the literature, the proposed VS-AVI employs adaptive piecewise linear droop function and dead zone for emulating the virtual capacitance for shaping the equivalent grid impedance and achieves the required PCC voltage regulation. Simulation and experimental results validate the proposed VS-AVI and demonstrate its effectiveness.

Index Terms—Adaptive virtual impedance, distributed generation (DG), droop control, LCL-VSC convertion.

I. Introduction

THE growing demands for clean energy sources have driven the insertion of renewable energy sources (RESs) as distributed generators (DG), generally interconnected to the grid through power converters. This new electrical system concept tends to be more distributed, intelligent, and flexible to fulfill the actual system reliability and power quality requirements. Moreover, these DGs are highly variable and stochastic, which causes voltage fluctuations or frequency deviations, depending on the penetration level [1]. Centralized voltage/Var control (VVC) based on traditional devices such as capacitor banks (CBs) or on-load tap changers (OLTCs) are slow and ineffective to cope with fast voltage deviation [2]. Conversely, voltage source converters (VSC) employed to interconnect DGs to the point of common coupling (PCC) have a fast response and flexibility for reactive power injection range [3] and can act for regulating the PCC local voltage.

Grid-connected VSCs interconnect the PCC via LC (LC-VSC) or LCL (LCL-VSC) filters [4]. The LC-VSC operates like a controlled voltage source with low-output impedance and can regulate the PCC voltage and frequency [5]. On the other hand, LCL-VSC works as a controlled current source with high impedance, suitable to deliver power to an energized grid [6]. Most of the control schemes work based on a tradeoff of energy balance [7]. Both LC-VSC and LCL-VSC can provide reactive power compensation and VVC support.

Droop-based control method applied for LC-VSC has been identified as a viable approach for regulating microgrid power flow and local voltage amplitude [8], [9]. The reason is that the droop control only uses local measurements and does not need communication links between DG units [10]. However, considering that most of the DG units are connected in a low-voltage (LV) microgrid, the droop-method is subjected to a few problems [11], such as

1) active and reactive power coupling;
2) reactive power-sharing inaccuracy.

Most of the microgrid output voltage regulation presented in the literature employ droop control strategies for regulating the power flow delivered by DGs based on RES, and they are implemented by LC-VSC grid-connected converters in which the virtual impedance concept (VIC) has been used to shape the interconnection impedance. They can overcome the droop control drawbacks being effective on active and reactive power decoupling, and power flow control [7], [10], [12]–[22]. The VIC approaches can be implemented by using fixed parameters or adaptive schemes.

Both fixed parameters techniques and adaptive schemes can provide effectiveness voltage supporting in the power grid [12]–[14]. Usually, the implementation of the virtual inductance employs a time derivative approach, making the system sensitive to current noise measurements. The use of a second-order general-integrator (SOGI) overcome these drawbacks, as presented in [23]. Both [10] and [23] consider the line impedance with the inductive profile, not verified in LV networks. In these cases, it is possible to employ a virtual complex impedance approach to achieve the

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T. Q. Fonsêca, R. L. A. Ribeiro, T. O. A. Rocha, and F. B. Costa are with Federal University of Rio Grande do Norte (UFRN), Natal 59072-970, Brazil (e-mail: thalesqf2012@gmail.com, rlucio@ct.ufrn.br, thiago.rocha@ct.ufrn.br, and flaviocosta@ect.ufrn.br).

J. M. Guerrero is with the Department of Energy Technology, Aalborg University, 9220 Aalborg East, Denmark (Tel: +45 2037 8262; Fax: +45 9815 1411; e-mail: joz@et.aau.dk). J. M. Guerrero was funded by a Villum Investigator grant (no. 25920) from The Villum Fonden.

proper power-sharing and overcome the power coupling [17]. Small-signal microgrid models considering the power control decoupling can match the suitable interconnection impedance for providing the required power flow control [15]. However, it must be inside the system power range for achieving the optimal system performance, which can be determined by using particle swarm optimization as proposed in [7]. This approach identifies the optimal virtual impedance, considering the microgrid constraints to achieve the required performance criteria. VIC can also be implemented following hierarchical control approach to supplement conventional control strategies and improve the compensation capabilities [12]. Recently, the development of a modified double-loop control demonstrated to be effective for affording the PCC voltage regulation and power-sharing in which the power flow inner loop employs a VIC approach [18]. More recently, a coupled virtual impedance based on coordinated control strategy provided the power-sharing, and voltage regulation issues applied for an ac/dc hybrid microgrid [19].

As aforementioned, generally DG units are connected in LV microgrids with low X/R ratios feeders that can vary randomly due to intermitency of DG sources and nonlinear loads, and standard power flow control strategies could be ineffective [12], [13]. Adaptive approaches associated with VIC can overcome these drawbacks. The use of an adaptive virtual inductance for achieving the proper reactive power-sharing under unbalanced conditions has been proposed in [10]. Adaptive VIC also can improve the microgrid power-sharing via communication systems, mitigating the mismatches in voltage droop across feeders [14]. The same approach could be employed without communication for power-sharing and voltage regulation [20]. Similar adaptive VIC methods associated with distributed consensus technique have been proposed to compensate the mismathes in line impedances for required reactive power-sharing [21] or mitigating the power-sharing errors verified in meshed microgrids [22].

All mentioned VIC concepts applied for power flow control and voltage regulation are based on LC-VSC DGs. However, most of the DG systems based on RES, such as photovoltaic (PV) or wind power, still employ LCL-VSC operating as a controlled current source [24]. Even though these systems are the most used choice, they have some limitations in microgrid applications because they only operate in grid-connected mode [25]. LCL-VSC can also participate in the grid voltage amplitude and frequency supporting by imposing the suitable level of the delivered active and reactive power [6]. In these DG systems, the maximum power point tracking (MPPT) defines the delivered active power [25], while the PCC voltage regulation determines reactive power compensation [12].

Regarding VVC supporting issues provided by DG based on LCL-VSC converters, piecewise linear droop control approaches [26], [27], or multimode control techniques [28] could be employed for providing the required reactive power and reaching the proper voltage regulation. The piecewise proposed in [12] presents an adaptive mechanism for adjusting the droop functions slopes without considering the converter stress. The introduction of a dead-zone into the piecewise droop function can overcome this drawback [2].

In the same direction, this paper proposes a variable structure adaptive virtual impedance (VS-AVI) control strategy applied for DGs based on LCL-VSC converters for providing reactive power compensation and regulation of the PCC voltage. Differently from the piecewise linear droop functions presented in [26], [27], the proposed droop function comprises two adaptive sectors for determining the required virtual capacitance for suitable reactive power compensation and reaching the required voltage regulation. The first refers to an adaptive dead-zone, used when PCC voltage is within allowed limits, in which an optimized virtual capacitance is implemented, based on the analysis of PCC voltage error and its derivative, mitigates possible voltage deviations. The second corresponds to two independent droop functions for positive and negative voltage errors in which their slopes varies as a function of voltage error, dead-zone width, and converter power rating. Comparison with existing solutions evaluates the effectiveness of the proposed solution. Simulation and experimental results obtained from a DG laboratory setup validate the proposed VS-AVI and demonstrate its effectiveness.

The organization of the paper comprises the following sections. Section II presents the description and modeling of the microgrid employed in this study, while section III discusses the standard control strategy applied for DGs based on LCL-VSC. The proposed VS-AVI is introduced in section IV, including the discussion of compensation limits. Simulation studies are presented in section V, and section VI depicts the experimental results of the proposed VS-AVI. The last section summarizes the present investigation.

II. Grid-Connected LCL Voltage Source Converter Description and Modeling

Figure 1 shows the block diagram of the microgrid employed in this study. It comprises a DG implemented by a PV system (VSC 1) interconnected in parallel with an indoor DG emulator (VSC 2). A PCC interconnects both DGs, the power grid, and a configurated three-phase load. The PV system employs a standard dual-stage power conversion system, and a controlled voltage source implements the primary source of the DG emulator. Both DGs employ LCL-VSC topology and operate as controlled current source. The LCL filters comprise the inverter and grid side inductors $l_f(l_t)$ and $l_g(l_r)$, the filter capacitors $c_f(c_g)$ and damping resistors $r_d(r_l)$. Block (SB) and controlled switches (K1 and K2) emulate different operational conditions.

The dynamic model of the LCL-filter comes from the design methodology proposed in [29], [30], which transfer function can be given by

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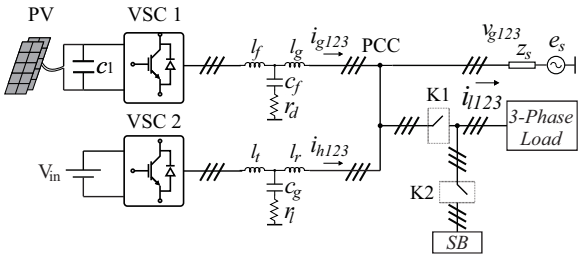

Fig. 1. Block diagram of the laboratory setup.

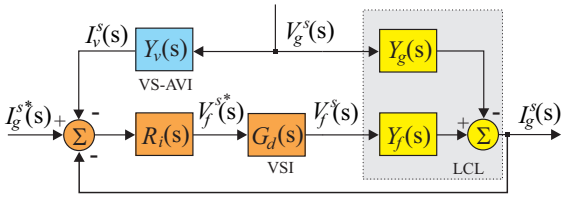

Fig. 2. Block diagram of the DG output current control loop.

$$Y_f(s) = \frac{c_f r_d s + 1}{l_f l_g c_f s^3 + (l_f + l_g) r_d c_f s^2 + (l_f + l_g) s}, \quad (1)$$

The transfer function in (1) has one zero and three poles, with one pole situated at the origin and two complex poles determined by the resonance frequency and damping set-points. Considering the effects of the parasitic resistors r_f and r_g, related to the LCL-filter inductors l_f and l_g, the transfer function in (1) becomes

$$I_g^s(s) = Y_f(s) V_f^s(s) - Y_g(s) V_g^s(s), \quad (2)$$

where

$$Y_f(s) = \frac{z_1 s + z_0}{p_3 s^3 + p_2 s^2 + p_1 s + p_0}, \quad (3)$$

and

$$Y_g(s) = \frac{w_2 s^2 + w_1 s + w_0}{p_3 s^3 + p_2 s^2 + p_1 s + p_0}, \quad (4)$$

where I_g^s is the DG output current, V_f^s is the VSI output voltage, V_g^s is the PCC voltage in which the superscript s denotes the stationary reference frame. The transfer function parameters are $z_1 = r_d c_f$, $z_0 = w_0 = 1$, $w_2 = l_f c_f$, $w_1 = (r_f + r_d) c_f$, $p_3 = l_f l_g c_f$, $p_2 = (l_f + l_g) r_d c_f + (r_f l_g + r_g l_f) c_f$, $p_1 = (r_f r_d + r_f r_g + r_g r_d) c_f + l_f + l_g$ and $p_0 = r_f + r_f$. In this dynamic model, the three poles in (1) are moved by $|\sigma_f|$ to the left side of the s-plane. The localization of the whole transfer function (2) demonstrates that there is a real dominant pole, closed to the origin, and two nondominant complex poles in the left side of s-plane far from it. Therefore, applying a reduction order process in the transfer function in (3) results in

$$Y_f'(s) \cong \frac{\kappa_f}{s + \sigma_f}, \quad (5)$$

where $\kappa_f \cong 1/r_d C \omega_r^2$ and $\sigma_f \cong (r_f + r_g)/l_t$ is the pole introduced in (1) by considering the inclusion of the parasitic elements.

III. Grid-Connected LCL Control System

The DG systems employ the most common multiloop control strategy for a grid-connected LCL converter in which the inner control loop regulates output phase currents, and the outer control loop sets the dc-link voltage. Figure 2 presents the block diagram of the DG inner control loop. Blocks $Y_f(s)$ and $Y_g(s)$ are the open-loop transfer functions of the grid-connected converter output currents and the open-loop output admittance, represented by the first and second terms in (2). The block $G_d(s)$ models the VSI by a time delay required to synthesize the output voltage $V_f^s(s)$, the block $R_i(s)$ is the current regulator and the block $Y_v(s)$ refers to the VS-AVI detailed in the following section.

A. DG Current Control Strategy

The system closed-loop transfer function of the DG without virtual impedance approach is given by

$$I_g(s) = Y_{fc}(s) I_g^{s*}(s) - Y_{gc}(s) V_g^s(s), \quad (6)$$

where

$$Y_{fc}(s) = \frac{R_i(s) G_d(s) Y_f(s)}{1 + R_i(s) G_d(s) Y_f(s)}, \quad (7)$$

and

$$Y_{gc}(s) = \frac{Y_g(s)}{1 + R_i(s) G_d(s) Y_f(s)}, \quad (8)$$

where $I_g^{s*}(s)$, $I_g^s(s)$ and $V_g^s(s)$ are the DG output reference current, DG controlled current and PCC voltage; $Y_{fc}(s)$ and $Y_{gc}(s)$ are closed-loop transfer functions of the output current $I_g^s(s)$ and the system admittance, respectively. In terms of control purposes, $Y_{gc}(s)$ is a disturbance to be compensated by the current regulator that also represents the DG admittance which modifies dynamically the interconnection impedance between DG and PCC. The Padé approximation models the time delay $G_d(s)$ of the PWM and VSI, given as

$$G_d(s) = \frac{2 - \tau_a s}{2 + \tau_a s}, \quad (9)$$

in which $\tau_a = 1.5 T_s$, and T_s is the sampling time of the PWM scheme [16].

B. Design Criterion for the DG output current controller

The implementation and the design of the DG current control strategy follow the pole placements and tracking objectives defined by the following control laws

$$Q_m(s) L(s) V_f^{s*}(s) = -P(s) \left(I_g^s(s) - I_g^{s*}(s) \right), \quad (10)$$

where $Q_m(s)$ is the internal model of reference currents $I_g^{s*}(s)$, $P(s)$ and $L(s)$ are polynomials (with $L(s)$ monic). For zero tracking error, the choice of $Q_m(s)$ satisfies $Q_m(s) I_g^{s*}(s) = 0$, which results in the following controller transfer function

$$R_i(s) = \frac{P(s)}{Q_m(s) L(s)}. \quad (11)$$

Considering that the LCL-filter transfer function described in (5) and, the implementation of the control algorithm on the stationary reference frame, the choice of the controller polynomials are $Q_m(s) = s^2 + \omega_g^2$, $L(s) = 1$ and $P(s) = a_2 s^2 + a_1 s + a_0$. Therefore, the following transfer function can be written

$$R_i(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + \omega_g^2}, \tag{12}$$

where a_2, a_1 and a_0 are the controller gains. With the proposed current regulator, the characteristic polynomial of the closed-loop transfer function of the DG output current can be given by

$$s^3 + (\sigma_f + \kappa_f a_2)s^2 + (\kappa_f a_1 + \omega_g^2)s + \kappa_f a_1 + \sigma_f \omega_g^2. \tag{13}$$

Based on this approach, the suitable closed-loop poles of the DG current control loop are assigned to those of an Hurwitz polynomial $A_s^*(s)$ given by

$$A_s^*(s) = \left(s^2 + 2\zeta_n \omega_n s + \omega_n^2\right)(s + \eta\zeta_n\omega_n), \tag{14}$$

where ζ_n and ω_n are the design damping ratio and natural frequency, and $-\eta\zeta_n\omega_n$ is the position of the nondominant pole. By solving the Diophantine equation for the Hurwitz polynomial $A_s^*(s)$, the gains of the controller are

$$a_2 = \frac{\delta_2^* - \sigma_f}{\kappa_f}, \tag{15}$$

$$a_1 = \frac{\delta_1^* - \omega_g^2}{\kappa_f}, \tag{16}$$

$$a_0 = \frac{\delta_0^* - \omega_g^2 \sigma_f}{\kappa_f}, \tag{17}$$

IV. The Proposed Virtual Impedance Control Approach for Grid Voltage Regulation

The closed-loop transfer function of the DG current control loop with the virtual impedance insertion is given by

$$I_g^s(s) = Y_{fc}(s) I_g^{s*}(s) - Y_{gcv}(s) V_g^s(s), \tag{18}$$

where

$$Y_{vc}(s) = \frac{Y_g(s) + R_i(s) G_d(s) Y_f(s)}{1 + R_i(s) G_d(s) Y_f(s)}. \tag{19}$$

In comparison with (2), the first term remained the same while the second term was modified with the insertion of the virtual admittance $Y_v(s)$ that results in the transfer function $Y_{vc}(s)$, and still refers to a disturbance to be compensated by the current regulator. However, it modifies the DG-PCC interconnection impedance that follows the control purpose imposing the required power flow control. The effect of the virtual impedance insertion can be verified in the equivalent circuit shown in Fig. 3. According to this equivalent circuit, the synthesized admittance $Y_{vc}(s) = Y_{fc}(s)Y_v(s)$ is parallel associated with the standard closed-loop admittance $Y_{gc}(s)$. Based on this observation, it is possible to propose a design methodology for both accomplishing the performance constraints of the DG current control loop and achieving the suitable DG-PCC interconnection impedance.

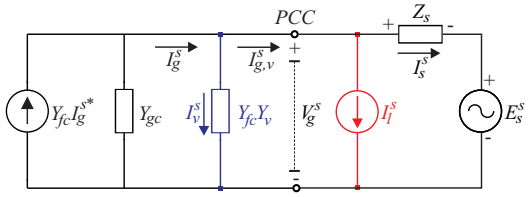

Fig. 3. Virtual impedance-based equivalent circuit for ac current control loop.

A. Mitigation of Voltage Deviation by using Virtual Impedance Approach

The LCL-VSC topologies behave like a controlled current source in which the primary objective is to inject active power in the microgrid. However, the introduction of the virtual impedance can contribute for regulating the voltage of the microgrid by modifying the DG reference current for injecting reactive power into the grid and providing the voltage system requirements. To understand how the use of virtual impedance can help to improve the PCC voltage regulation, considers the unifilar electric circuit of Fig. 3 operating under following scenarios: (a) the DG produces enough energy to feed the load and injects the surplus into the grid and, (b) the load consumption becomes higher than the DG rated power and, the microgrid provides the rest of the energy required by the load.

Figure 4 presents the phasor diagram of the steady-state operation of the DG under the scenarios described before without and with the introduction of the virtual impedance-based control scheme. Figure 4 (a) shows the first scenario in which the DG produces enough energy to feed the load and injects the surplus into the microgrid ($I_{g,l} > I_l$). In this case, the higher R/X ratio of microgrid produces PCC voltage $V_{g,l}$ higher than the maximum voltage ($V_{g(\max)}$) allowed by the standards. The insertion of the virtual impedance generates the current jI_v that modifies the DG output current $I_{g,v}$, compensating the load reactive and reducing the voltage amplitude of the PCC to $V_{g,v}$, inside the range delimited by the standards [31]. $\delta_{g,l}$ and $\delta_{g,v}$ are the phase displacements between the internal voltage (E_s) and the PCC voltage (V_g) without and with the introduction of the virtual impedance, respectively, and ϕ_l is the phase displacement between E_s and the load current I_l. Figure 4(b) presents the second scenario when the load consumption overcomes the DG power rating ($I_l > I_{g(\max)}$), and the microgrid feeds the rest of the required energy. In this case, the R/X ratio results in a PCC voltage with an amplitude $V_{g,l}$ smaller than the lower limit imposed by standards ($V_{g(\min)}$). The insertion of the virtual impedance approach injects a current $-jI_v$ that modifies the DG output current to $I_{g,v}$ and increases the PCC voltage amplitude to $V_{g,v}$, inside the allowed range imposed by the standards.

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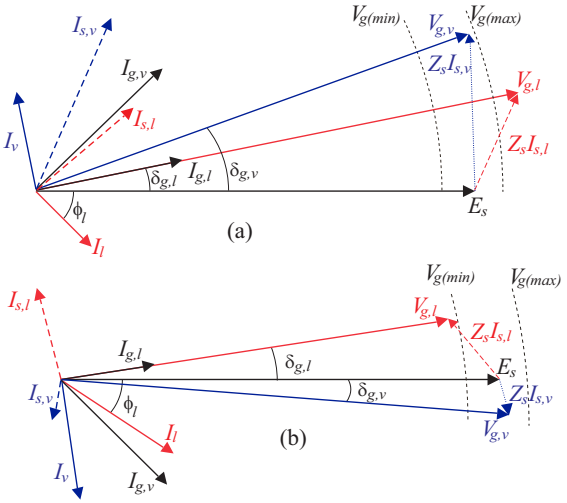

Fig. 4. Vector diagram of DG system operating on the following scenarios: (a) DG feeds the load and injects the surplus on the grid and, (b) the load consumption is higher than the DG rated power and the microgrid provides the rest of the energy to the load.

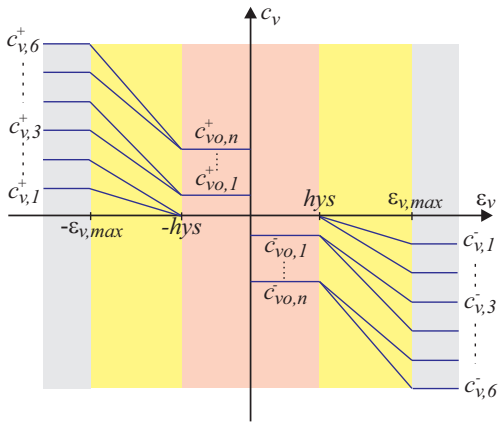

Fig. 5. Graph of adaptive piecewise droop functions used to implement the virtual impedance.

B. Variable Structure Adaptive Virtual Impedance Approach

As aforementioned, DG grid-connected based on LCL-VSC can also implement VVC functionalities. Their implementation requires the definition of the type and value of the virtual capacitance for matching the PCC voltage amplitude within the allowed limits imposed by the standards or grid-codes [31]. However, the exact dimensioning of the required capacitance depends on the knowledge of the grid impedance that can range stochastically due to the microgrid operation. To overcome grid impedance uncertainty, the proposed VS-AVI employs an adaptive linear piecewise droop function for determining the required virtual capacitance to be emulated. Figure 5 presents the adaptive piecewise droop function employed in the proposed VS-AVI. The piecewise droop function comprises two adaptive droop capacitive functions C_v^+ and C_v^- for injecting or absorbing reactive power into PCC, and an adaptive dead-zone hys delimited by the allowed voltage limits.

Figure 6 presents the block diagram of the VS-AVI. In this diagram, the block DLB refers to a decision logic-based that determines the impedance structure to be used based on the normalized voltage error (ε_v), the length of the dead-zone (hys) and, the amplitude of maximum voltage regulation allowable by the standards ($\varepsilon_{v,\max}$). The normalized voltage error is defined as

$$\varepsilon_v = \frac{(v_g - V_{gn})}{V_{gn}} \times 100\%, \tag{20}$$

where v_g is the rms value of the PCC voltage and V_{gn} is the nominal voltage of the microgrid.

The DLB defines four zones used for implementing the virtual capacitances denoted here as: (a) adaptive dead-zone ($-hys < \varepsilon_v < hys$); (b) adaptive droop functions C_v^+ ($-\varepsilon_{v,\max} < \varepsilon_v < -hys$) and C_v^- ($hys > \varepsilon_v > \varepsilon_{v,\max}$) and, saturation zone ($|\varepsilon_v| > \varepsilon_{v,\max}$) as presented in Fig. 5. The virtual capacitances implemented in the proposed VS-AVI are calculated based on the available reactive power of the DG, length of the dead-zone and, maximum voltage regulation. The maximum available reactive power can be determined as

$$q_{\max} = \sqrt{S_r^2 - p_g^2}, \tag{21}$$

where S_r is the power rating of the LCL-VSC and p_g is the active power delivered by the DG.

Based on the $q_{\max}$, the value of the maximum capacitance that could be implemented is given by

$$c_{v,\max} = \frac{q_{\max}}{3V_{gn}^2\omega_g}. \tag{22}$$

The insertion of an adaptive dead-zone into the piecewise droop function optimizes the power balance and reduces the LCL-VSC energy loss when the voltage error is within the allowed voltage limits. The dead-zone length employed in this work takes into account the allowed PCC voltage limits recommended in [31].

When the voltage error is inside the dead-zone, the VS-AVI can implement two different control actions based on the signals observation of the voltage error and its derivative. If both signals are equal, the VS-AVI implements a virtual capacitance optimizing the reactive power compensation and reducing PCC voltage deviation. Otherwise, if both signals are different, zero virtual capacitance is implemented. Table I summarizes the control actions related the dead-zone. The value of $c_{vo} = \pm\kappa c_{v,\max}$ in which the constant κ can be determined based on power flow studies.

TABLE I
Dead-zone control actions

$sign(\varepsilon_v)$	$sign\left(\frac{d\varepsilon_v}{dt}\right)$	c_{vo}
+	+	$+\kappa c_{v,\max}$
+	−	0
−	+	0
−	−	$-\kappa c_{v,\max}$

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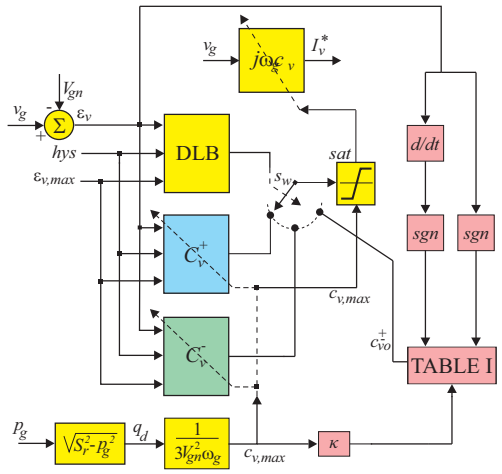

Fig. 6. Block diagram of the proposed variable structure adaptive virtual impedance VS-AVI.

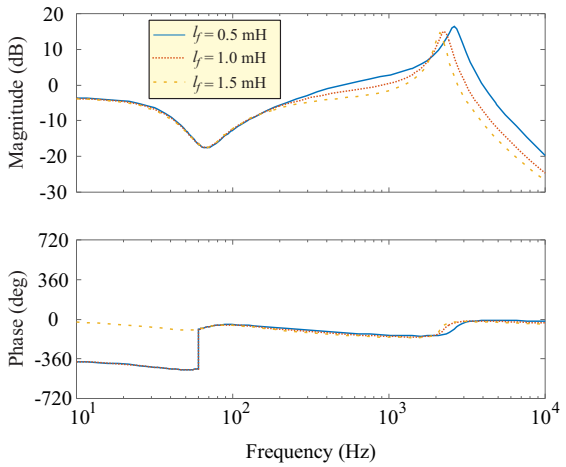

Fig. 7. Bode diagram of the LCL-VSC output admittance with a variation of the inverter-side inductance

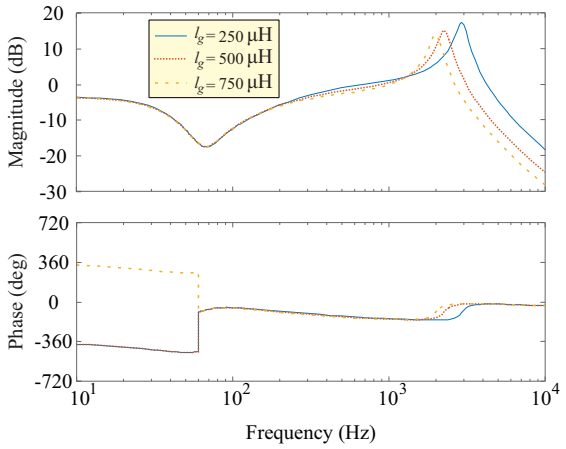

Fig. 8. Bode diagram of the LCL-VSC output admittance with a variation of the grid-side inductance

When the voltage error is inside the zones $-\varepsilon_{v,\max} < \varepsilon_v < -hys$ or $hys > \varepsilon_v > \varepsilon_{v,\max}$, the droop functions employed for implementing the required virtual capacitances are defined as follows: if the voltage error ε_v is inside the zone delimited by $-\varepsilon_{v,\max} < \varepsilon_v < -hys$, the virtual capacitance tracks the function droop, implemented by block C_v^+, given by

$$c_v^+(\varepsilon_v) = \frac{c_{v,\max} - c_{vo}}{-\varepsilon_{v,\max} + hys}\varepsilon_v + \frac{c_{v,\max} hys - c_{vo}\varepsilon_{v,\max}}{-\varepsilon_{v,\max} + hys}, \quad (23)$$

else, if the voltage error ε_v is inside the zone delimited by $hys > \varepsilon_v > \varepsilon_{v,\max}$, the virtual capacitance follows the droop function, implemented by block C_v^-, expressed by

$$c_v^-(\varepsilon_v) = \frac{-c_{v,\max} + c_{vo}}{\varepsilon_{v,\max} - hys}\varepsilon_v + \frac{c_{v,\max} hys - c_{vo}\varepsilon_{v,\max}}{\varepsilon_{v,\max} - hys}. \quad (24)$$

Finally, when the voltage error extrapolates the limits imposed by the standards (i.e. $|\varepsilon_v| > \varepsilon_{v,\max}$), the value of the virtual capacitance is limited in $c_{v,\max}$.

C. Analysis of the DG output admittance

According to (18) the total output admittance of the LCL-VSC DG consists of the closed-loop admittance $Y_{gc}(s)$ in parallel with the virtual admittance $Y_{vc}(s)$ synthesized by the VS-AVI. According to (13) the closed-loop admittance $Y_{gc}(s)$ depends on LCL parameters and controller gains. For evaluating the dynamic behavior of $Y_{gcv}(s)$ under system parameter variation, three simulation tests were realized in which the inverter-side and grid-side inductances as well as filter capacitor range. In each test, these parameters ranged by 50 % of the nominal values presented in Table II. In all simulations, the VS-AVI emulates a virtual capacitance of $c_v^- = -400$ μF. Moreover, the delay imposed by the VSI for synthesizing the output voltage modeled by the block $G_d(s)$ is neglected.

Figure 7 presents the bode diagram of $Y_{gcv}(s)$ for inverter-side inductance with step-variation of 50 % from LCL-VSC nominal value. Figure 8 shows the bode diagram of $Y_{gcv}(s)$ for grid-side inductance with also step-variation of 50 % from the rated value. Finally, the same procedure is applied for filter capacitance variation, as presented in Fig. 9. In all simulations, the bode diagrams present, at the fundamental frequency, a magnitude of approximately -16.4 dB and a phase degree of -90 degrees, which correspond to the emulation of virtual capacitance $c_v^- = -400$ μF. These simulation results demonstrate the effectiveness of the proposed VS-AVI.

V. Simulation Results

This section evaluates the reactive power-sharing capabilities of the proposed VS-AVI method in a scenario with multiple DGs interconnected in parallel regulating the same PCC voltage cooperatively. Referring to Fig. 1, the system topology used in the simulation study uses a PV panel linked to a dc-link capacitor instead of the voltage source V_{in} for VSC 2. Moreover, the switch K1 is open. Both DG systems use the same LCL-filter in Table II with the power rating of VSC 1 and VSC 2 being 10 kVA and 5 kVA, respectively. The simulation studies employ the PSIM for accomplishing the power-sharing analysis.

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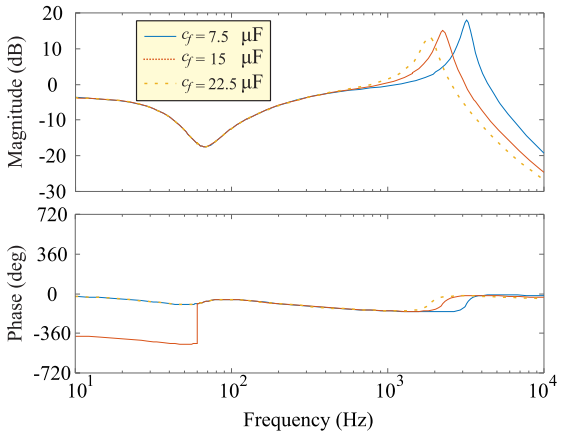

Fig. 9. Bode diagram of the LCL-VSC output admittance with a variation of the filter capacitance

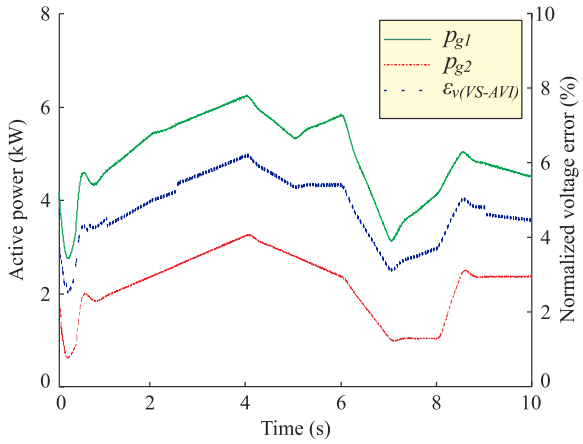

Fig. 10. Simulation results of the voltage regulation for the DGs operating under different penetration levels.

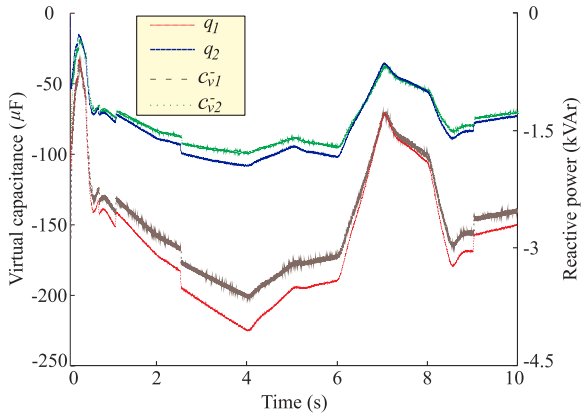

Fig. 11. Simulation results of the virtual capacitance implemented and reactive power absorbed by the DGs.

The VS-AVI setpoints are $hys = 2\%$ and $\varepsilon_{v,max} = 10\%$ according to [31].

Figures 10 and 11 present the simulation results of the reactive power-sharing evaluation. Figure 10 shows the active power delivered by both DG1 (p_{g1}) and DG2 (p_{g2}) systems as well as the voltage error ($\varepsilon_{v(VS-AVI)}$) at the PCC. The voltage error is under the allowed limits imposed by standards [31]. Figure 11 depicts (c_{v1}^- and c_{v2}^-) as well as the reactive power absorbed by both LCL-VSC converters (q_1 and q_2), respectively. According to Figs. 10 and 11 the proposed VS-AVI operates cooperatively for regulating the PCC voltage by emulating the required virtual capacitance and absorbing the required reactive power according to their power rating.

VI. Experimental Results

The experimental results were obtained from a laboratory setup described in Fig. 1, in which VSC 1 and VSC 2 have the power rating 8 kWp and 5 kWp, respectively, and the proposed VS-AVI control strategy is implemented in the PV system. A fast prototyping system dSPACE 1103 executes the algorithms of the control strategy and proposed VS-AVI at a sampling rate of $T_s = 100$ μs. The dSPACE A/D converters realize measurements of system voltages and currents obtained via Hall-effect sensors, with the use of anti-aliasing filters with a cutoff frequency of 2.5 kHz for reduce the noise introduced by the LCL-VSC PWM. The experimental setup has the same parameters of those presented in Table II. Figure 12 shows the experimental platform employed for realizing the validation essays.

TABLE II
DG System Parameters

Parameter	Value
Rated line-to-line voltage	220 V rms
Grid frequency	$2\pi 60$ rad/s
Grid impedance	$r_s = 0.43\ \Omega$, $l_s = 375\ \mu$H
Filter inductance l_f	1 mH
Intrinsic resistance r_f	0.13 Ω
Filter inductance l_g	500 μH
Intrinsic resistance r_g	0.065 Ω
Filter capacitance c_f	15 μF
Damping resistor r_d	4.7 Ω
Controller gain a_2	3.4048
Controller gain a_1	1106.8
Controller gain a_0	212280

The essays employed to validate the proposed VS-AVI control strategy are as follows: (A) Comparison with existing solutions; (B) proposed method effectiveness: parametric variation; (C) proposed method effectiveness: undervoltage condition and (D) effectiveness of the adaptive dead-zone.

A. Comparison with existing solutions

In this experiment, only the PV system in Fig. 1 was operating connected to the grid, and the proposed VS-AVI was evaluated when the PV operates under overvoltage caused by weak-grid conditions. In this essay, the SB circuit in Fig. 1 modifies the internal grid impedance by interconnecting an RL three-phase branch $z_{wg} = (0.5 + j0.188)\ \Omega$ in series via controlled switches for emulating

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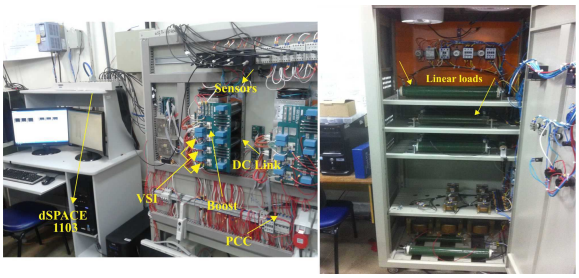

Fig. 12. Laboratory setup of LCL-VSC-based grid-connected PV system.

a weak-grid condition. The proposed VS-AVI was tested in comparison with the piecewise droop reactive control (PDRC) approach [26] and conventional droop control strategy (DCS) [25] for evaluating its effectiveness.

Figure 13 depicts the PV delivered power (p_g), and voltage errors of VS-AVI($\varepsilon_{v(VS-AVI)}$), PDRC (ε_{v1}) and DCS (ε_{v2}). In this experiment, the active power delivered by the PV was $p_g = 6.2$ kW. Before the grid impedance modification, the voltage errors are approximately $\varepsilon_{v1} \cong 4.5\%$, $\varepsilon_{v2} \cong 4.1\%$ and $\varepsilon_{v(VS-AVI)} \cong 4.6\%$, respectively. The conventional solution depicts the smallest error (ε_{v2}) due to the absence of a dead-zone. However, it produces more power losses. At $t = 7.51$ s, the SB circuit modifies the grid impedance emulating the weak-grid condition. The average value of the voltage errors are approximately $\varepsilon_{v1} \cong 5.7$ %, $\varepsilon_{v2} \cong 5$ % and $\varepsilon_{v(VS-AVI)} \cong 5.2$ %. However, voltage errors related to the PRDC (ε_{v1}) and DCS (ε_{v2}) present undesired oscillations with maximum values arriving at 6.3 % and 5.7 %, respectively. Instead, the results obtained from the proposed VS-AVI presented a steady average error, which is more appropriate for PCC voltage regulation purposes.

B. Proposed method effectiveness: parametric variation

The robustness of the proposed VS-AVI, under grid impedance variations, was evaluated in this test. The impedance variation employs the same procedure as the essay realized in Section VI-A. Also, both DGs implemented by power converters VSC 1 and VSC 2 operate in parallel, delivering power to the grid. Figure 14 presents the experimental results of the proposed VS-AVI with the grid impedance modification. Before the grid impedance modification, the voltage error $\varepsilon_{v(VS-AVI)}$ is approximately 4.7 %, and the grid impedance Z_s and virtual reactance X_v are 0.46 Ω and -8.3 Ω (presented in the graph as $X_v/10$), respectively. At $t = 8.84$ s, the SB circuit changes the grid impedance, making the voltage error $\varepsilon_{v(VS-AVI)}$ being approximately 8.8 %, the new grid impedance reaches 0.8 Ω, resulting in the virtual reactance of -5.6 Ω.

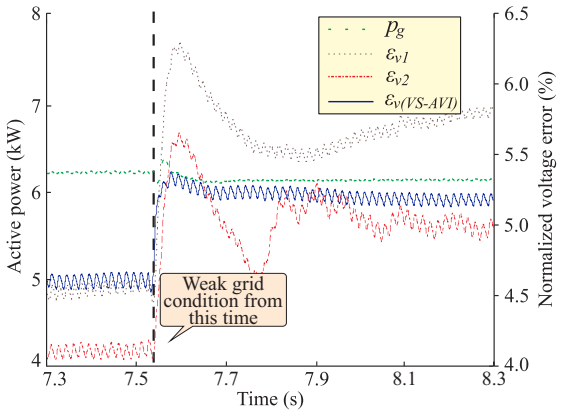

Fig. 13. Experimental results of the voltage regulation for the DG operating in weak-grid conditions.

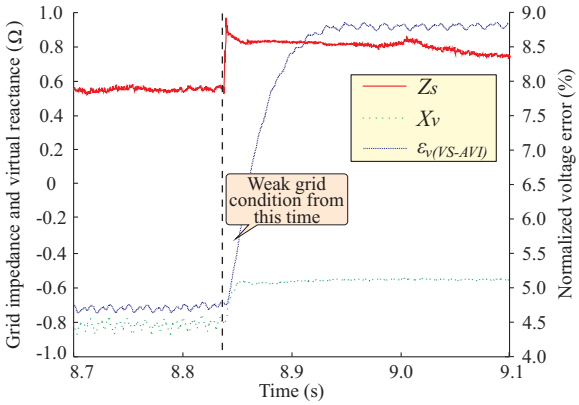

Fig. 14. Experimental results of the virtual reactance implemented, internal grid impedance and normalized voltage error in weak-grid conditions.

Figure 15 illustrates the reactive power (q) absorbed by the VSC 1 and the droop function slope (α) of the VS-AVI, normalized with respect of the base capacitance of the system, under grid impedance variation. The droop function slope represents the tangent of the angle between the droop curve and the horizontal axis. Before the grid impedance modification, the absorbed reactive power is approximately -4.8 kVAr and the droop function slope is -0.86. At $t = 8.84$ s the grid impedance changes and the reactive power becomes -9.5 kVAr with droop function slope of approximately -2.3. These experimental results demonstrate the adaptive capability of proposed solution under grid impedance variation by changing piecewise droop function parameters for achieving the required PCC voltage regulation.

C. Proposed method effectiveness: undervoltage condition

In this test, the SB circuit (see figure 1) interconnects a three-phase resistive load ($r_{wl} = 5$ Ω) in parallel to the RL load ($z_l = 20 + j22.61$ Ω) for provoking an undervoltage at the PCC. Figure 16 presents experimental results of the proposed VS-AVI operating under undervoltage condition. At the startup condition, the internal grid impedance is 0.46 Ω with a voltage error of approximately 2.32 %, resulting in a virtual reactance of -53.1 Ω (presented in the graph as $X_v/100$). At $t = 4.36$ s, the SB circuit modifies the three-phase load increasing the phase currents i_{g123} from 4 A to approximately 30 A, and provoking an

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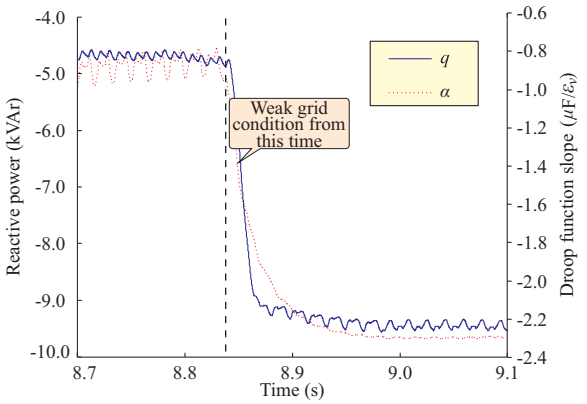

Fig. 15. Experimental results of the reactive power and the droop function slope for the DG operating in weak-grid conditions.

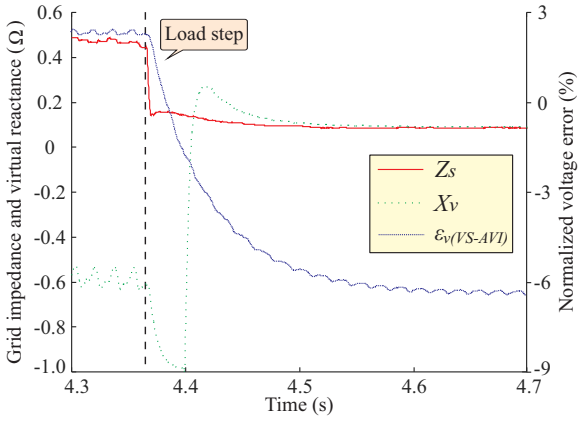

Fig. 16. Experimental results of the virtual reactance implemented, internal grid impedance and normalized voltage error with undervoltage conditions.

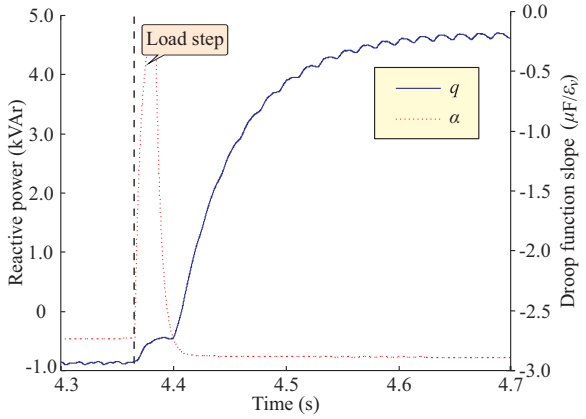

Fig. 17. Experimental results of the reactive power and the droop function slope for the DG operating in undervoltage conditions.

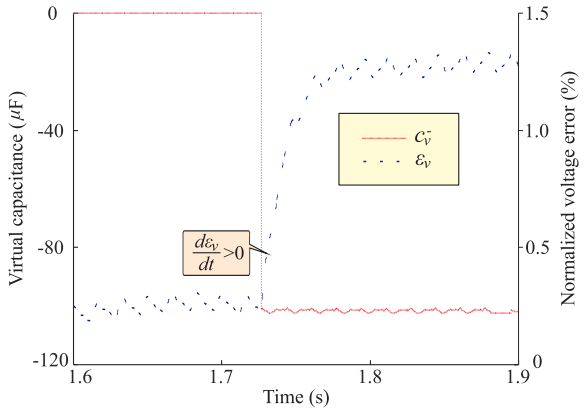

Fig. 18. Experimental results of the virtual capacitance and error $\varepsilon_{v(VS-AVI)}$ inside the dead-zone.

undervoltage that generates a voltage error of $\varepsilon_v \cong -6.3\%$. In this condition, the equivalent grid impedance and the virtual reactance become 0.12 Ω and 9.01 Ω, respectively.

Figure 17 depicts the graphs of reactive power injected by the VSC 1 and droop function slope of the proposed VS-AVI under load step variation. Before the three-phase load connection, the VSC 1 absorbs a reactive power of approximately 0.8 kVAr, and the droop function slope is -2.6. After $t = 4.36$ s the proposed method synthesizes a virtual reactance that results in a reactive power of 4.7 kVAr injected by VSC 1 with the droop function slope of approximately -2.95.

The experimental results of the VS-AVI operating under undervoltage conditions demonstrate that the system regulates the PCC voltage within the allowed limits. Moreover, it demonstrated the adaptive action for compensating PCC voltage in an undervoltage occurrence.

D. Effectiveness of the adaptive dead-zone

This test evaluates the efficiency of the proposed adaptive dead-zone for preventing PCC voltage deviation when $-hys < \varepsilon_v < hys$. For accomplishing this operation condition, the DG operated in low-penetration level, which addresses to voltage error inside the dead-zone. Figure 18 shows the emulated virtual capacitance (c_v^-) and the PCC voltage error (ε_v). At the beginning, the DG operates in steady-state condition ($d\varepsilon_v/dt$=0), and the proposed VS-AVI synthesizes zero virtual capacitance. At $t = 1.73$ s, the SB circuit modifies the grid impedance similarly to the weak-grid experiment. The derivative $d\varepsilon_v/dt$ becomes positive like the voltage error ε_v. Thus, the adaptive dead-zone approach synthesizes a virtual capacitance of $c_{vo} = -\kappa c_{v,max}$ according to Table I. In this test, the optimized constant is $\kappa = 0.1$, which results in the virtual capacitance of $c_{vo} \cong -100.9\mu$F.

VII. Conclusion

Differently from most of the virtual impedance solutions presented in the literature, an adaptive piecewise linear droop function determines the virtual capacitance for providing the PCC voltage regulation by injecting or absorbing suitable reactive power according to grid constraints and DG power rating. The piecewise droop function, composed of two adaptive sectors, determines the required virtual capacitance. In the first, an adaptive dead-zone defines an optimized virtual capacitance, based on signal analysis of PCC voltage error and its derivative, for mitigating voltage deviations when PCC voltage is within

allowed limits. In the second, two independent adaptive droop functions, for positive and negative voltage errors, adjusts their slopes based on the voltage error, dead-zone width, and converter power rating. Besides the voltage regulation, it provides power balancing and optimized reactive power compensation. The design concepts employed for determining the VS-AVI parameters was also detailed. Experimental results demonstrated the effectiveness of the proposed method for performing VVC issues in DGs based on LCL-VSC systems.

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Thales Queiroz Fonsêca was born in Natal, Brazil, in 1992.

He received the B.Sc., and M.Sc. degrees in electrical engineering from the Federal University of Rio Grande do Norte, Natal, Brazil, in 2016 and 2018, respectively, where he is currently working toward the Ph.D degree in the Department of Electrical Engineering. His research interests include renewable energy systems, microgrids and power system stability.

Mr. Fonsêca is President of the IEEE - IAS/PELS Student Branch Chapter of the Federal University of Rio Grande do Norte, and Member of the IEEE Power Electronics and Power Energy Societies.

Ricardo Lucio de Araujo Ribeiro (M'04-SM'19) was born in Campina Grande, Brazil, in 1961.

He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 1990, 1992, and 2003, respectively. From 2001 to 2002, he was with Department of Electrical Engineering, Politecnico di Torino, Turin, Italy, as a Visiting Scholar. Since March 2004, he has been with the Department of Electrical Engineering, the Federal University of Rio Grande do Norte, Natal, Brazil, as an Associate Professor and the Director of the Research Laboratory of Power Electronics and Renewable Energy-LEPER. His research interests include power electronics, renewable energy systems, power quality control, energy efficiency, ac/dc microgrids, storage systems, and power system stability.

Dr. Ribeiro is Secretary of Joint Chapter - PES/IAS/PELS - IEEE Bahia Section R9, Tutor of the IEEE - IAS/PELS Student Branch of the Federal University of Rio Grande do Norte, Member of the IEEE Industrial Electronics and Power Electronics Society and SOBRAEP-Brazilian Association of Power Electronics.

Thiago de Oliveira Alves Rocha Thiago de Oliveira Alves Rocha was born in Natal, Brazil, in 1986.

He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Rio Grande do Norte, Natal, Brazil, in 2011, 2013, and 2015, respectively. From October 2014 to June 2016, he was a Faculty Member with the Federal Institute of Rio Grande do Norte, João Câmara, Brazil. From June 2016 to July 2017, he has been with the Department of Electrical Engineering, Federal University of Pernambuco, Recife, Brazil, as an Adjunct Professor. Since July 2017, he has been with the Department of Electrical Engineering, Federal University of Rio Grande do Norte, Natal, Brazil, as an Adjunct Professor. Since June 2010, he has been a Researcher in the Laboratory of Industrial Electronics and Renewable Energy (LEIER/UFRN) and since July 2017 he has been the Adjunct Director of LEIER/UFRN. His research interests include renewable energy systems, power electronics, active power filters, and electrical drives.

Dr. Rocha is a Member of the IEEE and SOBRAEP-Brazilian Association of Power Electronics.

Flavio Bezerra Costa (M'10) was born in Brazil, 1978.

He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2005, 2006, and 2010, respectively. He is currently a Professor with the Federal University of Rio Grande do Norte, Natal, Brazil. His research interests include power system protection, electric power quality, renewable energy systems, and smart-grid solutions.

Josep M. Guerrero (S'01-M'04-SM'08-FM'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program (www.microgrids.et.aau.dk). From 2014 he is chair Professor in Shandong University; from 2015 he is a distinguished guest Professor in Hunan University; and from 2016 he is a visiting professor fellow at Aston University, UK, and a guest Professor at the Nanjing University of Posts and Telecommunications. From 2019, he became a Villum Investigator by The Villum Fonden, which supports the Center for Research on Microgrids (CROM) at Aalborg University, being Prof. Guerrero the founder and Director of the same centre. His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering and the internet of things for AC/DC microgrid clusters and islanded minigrids. Specially focused on maritime microgrids for electrical ships, vessels, ferries and seaports.

Prof. Guerrero is an Associate Editor for a number of IEEE TRANSACTIONS. He has published more than 500 journal papers in the fields of microgrids and renewable energy systems, which are cited more than 40,000 times. He received the best paper award of the IEEE Transactions on Energy Conversion for the period 2014-2015, and the best paper prize of IEEE-PES in 2015. As well, he received the best paper award of the Journal of Power Electronics in 2016. During six consecutive years, from 2014 to 2019, he was awarded by Clarivate Analytics (former Thomson Reuters) as Highly Cited Researcher. In 2015 he was elevated as IEEE Fellow for his contributions on âdistributed power systems and microgrids.â