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# Non-Isolated High-Gain Triple Port DC–DC Buck-Boost Converter With Positive Output Voltage for Photovoltaic Applications

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**ABSTRACT** The solar PV based power generation systems are growing faster due to the depletion of fossil fuels and environmental concerns. Combining PV panels and energy buffers such as battery through multi-port converter is one of the viable solutions to deal with the intermittency of PV power. The goal of this paper is to design and analyze the proposed triple port DC-DC buck-boost converter for high step-up/step-down applications. It has two unidirectional ports (port-1 and port-3) and one bi-directional port (port-2) for harnessing photovoltaic energy and charging the battery. At port-1, the combined structure of buck and buck-boost converter is used with a particular arrangement of switches and inductors. The step-up/step-down voltage conversion ratio is higher than the conventional buck-boost converter, and the polarity of the output voltage is maintained positive. The battery is added at the bi-directional port, for the storage of energy through the bi-directional boost converter. The switches operate synchronously for most of the modes making the control strategy simple. The characteristics and modes of operation along with a switching strategy, are elaborated. Experimental results are presented which validate the agreement with the developed theoretical expectation.

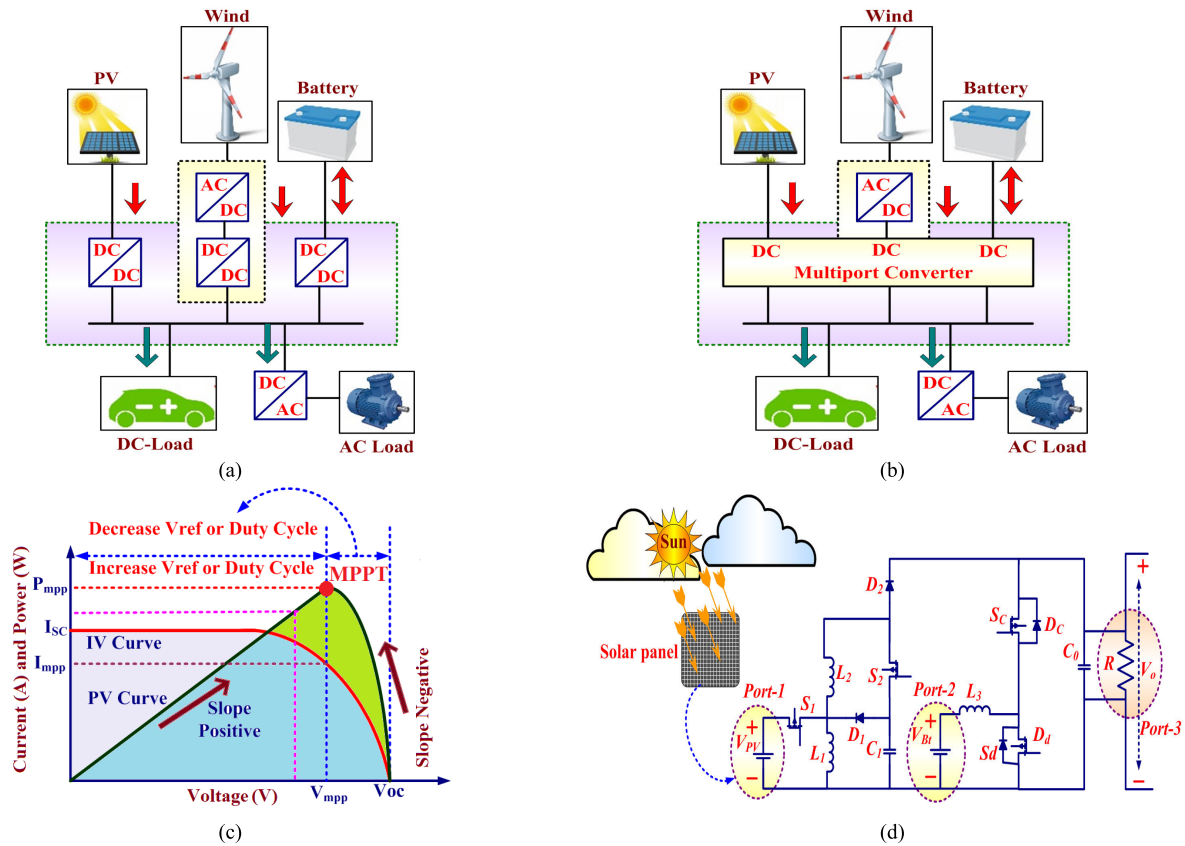
**INDEX TERMS** Buck-Boost converter, DC-DC, non-isolated, bi-directional, triple port, photovoltaic.

## NOMENCLATURE

$S_1, S_2, S_c, S_d$	Switches
$D_1, D_2, D_c, D_d$	Diodes
$L_1, L_2, L_3$	Inductors
$C_0, C_1$	Capacitors
$V_{PV}, V_{Bt}, V_o$	Photovoltaic voltage, Battery voltage, Load voltage (Average values)
$k_1, k_2, k_3$	The duty cycle of state 1, 2, 3
$V_{S1}, V_{S2}, V_{Si}, V_{Sc}, V_{Sd}$	Voltage across switches

$\Delta i_{L1}, \Delta i_{L2}, \Delta i_{L3}$	Ripples in the current of inductor $L_1, L_2$ , and $L_3$ .
$i_{L1}, i_{L2}, i_{L3}$	inductor $L_1, L_2$ , and $L_3$ currents
$I_{L1}, I_{L2}, I_{L3}$	Average inductor $L_1, L_2$ , and $L_3$ currents
$V_{C1}, V_{C0}$	The average voltage across capacitor $C_1$ and $C_0$
$v_{C1}, v_{C0}$	The voltage across capacitor $C_1$ and $C_0$
$\Delta V_{C1}, \Delta V_{C0}$	Ripples voltage across capacitor $C_1$ and $C_0$ .
$R, T, f_s$	Load, total time-period, switching frequency
$i_{C1}, i_{C2}, i_{C0}$	currents through capacitor $C_1, C_2, C_0$

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**FIGURE 1.** Block Diagram, PV characteristics and Power Circuit (a) Structure of conventional converter based PV-Wind-Battery system, (b) Structure of multi-port converter based PV-Wind-Battery system, (c) Concept to track Maximum Power Point (MPP) using P-V and I-V characteristics, (d) Proposed triple port DC-DC buck-boost converter.

$I_{C1}, I_{C2}, I_{C0}$	Average currents through capacitor $C_1, C_2, C_0$
$k_{Sx}$	The duty cycle of switch $S_x$
$\Delta i_{L(peak-peak)}$	Peak-to-peak inductor current variation
$x(t), u(t)$	State vector and input vector
$V_o(ref)$	Reference of the load voltage
$SOC$	State of charge of the battery
$I_{Bt(ref)}$	The maximum discharge current of the battery
$I_{Bt(avg)}$	Regulated average battery current

## I. INTRODUCTION

Presently the fossil fuels like coal, oil and natural gas are being depleted at a steady rate and soon cease to exist. Effects are immense pollution and detrimental to the environment. Consequently, extensive research is being carried out in the field of renewable energy resources and systems to find an environmentally free, cheap, efficient, and reliable solution [1]. Nevertheless, renewable energy resources are intermittent. As a result, multiple energy resources usage and their storage become necessary at the point of a power crisis scenario. However, the challenging task is the integration of multiple energy sources with different magnitude scales. Step-up and step-down voltage conversions are also mandatory with

high efficiency for real-time applications due to the variation of voltage range in demand. The series/parallel combination of the photovoltaic (PV) panels is not a viable solution to increase the voltage/current due to the requirement of large space and cost [2]–[4]. Thus, the DC-DC converter with a high gain voltage conversion ratio is required to achieve high voltage outputs [5]. Several DC-DC converters are addressed and achieved high voltage by using several inductors and capacitors combinations with increased parasitic losses and bulky in size [6], [7]. Multi-port converters technologies are proven to utilize renewable energy resources efficiently. Also, it plays an essential role in charging/discharging of battery for real-time application. Fig. 1(a)–(b) elaborates the PV-Wind-Battery system using a conventional and multi-port converter, respectively. Recently, various multi-port converter topologies are addressed in the literature with postulated various rules for the effective designing of converters. In [8], sextuple output triad converter is proposed by utilizing switched inductor, boost, CUK and SEPIC configurations. Three unidirectional ports are powered from the single input port and using this sextupling converter loading is possible. In [9], four basic rules, assumptions, restrictions and conditions have been stated, to realize a multiple-input converter from its single input version with a minimum number of components and high feasibility. Using CUK and SEPIC, six new

multi-port converter topologies are addressed. However, reliability is negatively affected as standard components and also acts as single points of failure for the entire converter. There is no bi-directional port (hence, charging and discharging operation is not possible). This converter also required a large number of semiconductor devices with a high voltage rating. In [10], the general approach was proposed to develop multi-input converters. Which supplies power from all the input sources to the load either individually or simultaneously without using coupled transformers. Extra Pulsating Voltage Sources (PVS) and Pulsating Current Source (PCS) are added in the PWM converter with suitable connection to derive new multiple-input converters (MIC). Quasi-MIC and Duplicated MIC structures are proposed by utilizing (PVS and PCS) in six PWM converter. Nonetheless, due to the absence of the bi-directional port, these topologies are not suitable for the battery-powered system. A new family of multi-input converters based on three switches leg introduced in [11]. Depending on the switching states, the converters have three modes of operations; buck, boost and inverter mode. However, the duty ratio is limited due to buck, and boost the operation of DC-DC conversion ports. Further, the complexity of the control circuit, the number of inductors and switches are increased as the number the ports increases.

A triple port high gain non-isolated DC-DC converter for PV application addressed by [12], which uses a coupled inductor technique to obtain high voltage gain. The solution to feeding PV energy to high voltage DC bus is achieved and suitable for multiple renewable energy sources due to its multiple input capability. However, this converter required a large number of semiconductor devices with the coupled inductor; which makes the circuit bulky and costly bulky circuit. In [13], a systematic method to derive a multi-port converter family (multi-input as well as multi-output) is proposed based on DC-Link Inductor (DLI) concept and buck-boost converter. These configurations are the prominent solution for renewable energy systems compared to conventional standard DC-bus based solution. Since the bulky DC-link, a capacitor is avoided. However, the number of switches increases and challenges are with the digital controller implementation. In [14], the design of a single switch non-isolated triple port converter for a stand-alone photovoltaic power system with energy storage is proposed. A synchronous switch with two diodes is used to replace two individual switches. Here, the challenging task is that the converters in both stages must work synchronously to have a single switching and only suitable for floating type loads. In [15], new single switch non-isolated transformer-less buck-boost DC-DC converter is proposed with low-voltage stress on the switch. The voltage gain is higher than the conventional boost, buck-boost, Cuk, SEPIC, and Zeta converters for a given duty cycle.

Nonetheless, no provision is present for the storage of excess energy and required a large number of diode, inductor, and capacitor. In [16], a set of basic rules for generating multi-input converters topologies are proposed. In particular, systematic synthesis of two multi-input converter families are

derived by hybridizing two conventional converters. However, the filter capacitor is linked with two different converters and becomes the challenging task to maintain a constant voltage across the filter capacitor. Moreover, some configurations also required a large number of reactive, and semiconductor components along with the transformer, i.e. decrease the efficiency and make circuit again bulky. In [17], multi-port converter configurations are proposed by the hybridization of the full-bridge and bi-directional DC-DC converter. The complex power circuitry and control are the main drawback of these converters. In addition, a large number of reactive components and semiconductor devices, along with an isolated transformer, are required. Hence, the circuitry is bulky with increased losses.

In [18], dual output single input three-level DC-DC converter proposed. It is a hybrid combination of three-level buck and boost converters. The voltage stress of switches is reduced, but the sophisticated control and voltage balancing of the output side capacitor is the challenging task for this converter. Moreover, the converter failed to function if anyone device fails. In [19], the decoupled tri-port converter is proposed by using two buck-boost converters and an isolated full-bridge converter. The number of power switches is reduced, and soft switching is achieved. However, the selection of isolated transformer, power-sharing between two converters, and sophisticated control are difficult tasks.

In [20], the isolated converter is proposed with high efficiency using a boost-flyback configuration. However, the configuration required an isolated transformer, which undoubtedly increases the size and cost of the converter and makes the system bulky. Moreover, the saturation of transformer and leakage reactance will limit the performance of the converter. Therefore, the selection of isolated transformer and sophisticated control is a difficult task. Recently, various DC-DC converters also proposed in [21]–[25] with a high voltage conversion ratio. On applications, with variation in the irradiances, it becomes necessary to extract maximum power from the PV panel by tracking Maximum Power Point (MPP) using tracking algorithms. Incremental-conductance, hill climbing, and Perturb & Observe (P&O) algorithms are well-liked Maximum Power Point Tracking (MPPT) algorithms by their simplicity and easy implementation. Based on the power increase/decrease perturbation condition, the MPPT controller generates pulses for the DC-DC converter to locate MPP. Accordingly, the power and voltage slope used to decide the next perturbation should be and to locate MPP. Fig. 1(c) depicts the concept to track MPP by using P-V and I-V characteristics of the PV panel.

In light of the advantages of the tri-port DC-DC converter, this paper presents a new triple-port converter. The proposed configuration is derived by integrating buck-boost converter with a bi-directional boost converter for harnessing and storage of PV energy. It also aims at storing the energy and further used during energy deficiency. The advantage of the proposed converter holds the higher conversion gain, simple working, and mode of control are adjusted by switching for the power

**TABLE 1.** Summary of modes of operation of proposed triple port converter.

Modes	Input Port	Output Port	Power flow direction	Type of Mode
Mode-1	Port -1	Port-3	PV panel to Load	Single Input Single Output (SISO-1)
Mode-2	Port -2	Port-3	Battery to Load	Single Input Single Output (SISO-2)
Mode-3	Port -1	Port -2 and Port -3	PV panel to Load and Battery	Single Input Dual Output (SIDO)
Mode-4	Port -1 and Port -2	Port-3	PV panel and Battery to Load	Dual Input Single Output (DISO)

flow direction. Furthermore, the proposed triple port converter is designed by using conventional power converters, i.e. simple circuitry arrangement, and the principles used in [9], [16] and [26] are integrated to form the basis collectively. The buck-boost structure is chosen because of the suitability for the applications with overlapping source and load voltages.

## II. PROPOSED TRIPLE PORT DC-DC BUCK-BOOST CONVERTER

Fig. 1(d) shows the power circuit of the proposed triple port DC-DC converter. It consists of four power-controlled switches ( $S_1$ ,  $S_2$ ,  $S_c$ , and  $S_d$ ), three inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ), two capacitors ( $C_1$  and  $C_0$ ), four uncontrolled switches ( $D_1$ ,  $D_2$ ,  $D_c$  and  $D_d$ , including antiparallel diode of MOSFET's) and a resistive load  $R$ . The power switches  $S_1$  and  $S_2$  are controlled synchronously to transfer the power from Port-1 to other ports. The proposed converter has two unidirectional (Port-1 and 3) and one bi-directional port (Port-2); where Port-1 is, input Port and Port-3 is output port. Thus, photovoltaic panel and load are connected at the Port-1 and Port-3, respectively, and the battery is connected at Port-2. Thus, when the energy in the battery is less, the PV panel provides energy to load. It is assumed that the converter is operating in steady-state, all the capacitors are large enough to keep the voltage across them with fewer ripples, and all the components are ideal. In the power circuit, the connection of  $S_1$ ,  $L_1$ ,  $D_1$  and  $C_1$  forms the conventional unidirectional buck-boost converter and the connection of  $L_3$ ,  $S_d$  and  $S_c$  form the bi-directional boost converter. Additionally,  $L_2$ ,  $S_2$ , and  $D_2$  are connected to enhance the power flow and voltage conversion capability of the buck-boost converter. Consider the case, when the PV power is just sufficient only to supply the load demand, and the battery has less charge. During this situation, all PV power must be directed to load, and the battery should be completely isolated; otherwise, reverse current flow through the body diode of switch  $S_c$ . Notably, battery isolation and battery charging/discharging operation can be possible in a simple mode: turn off both  $S_d$ , and  $S_c$  switches. In this case, no energy transfer will be made either from or to the battery. The only condition for battery isolation with  $S_c$  and  $S_d$  off is that battery voltage to be lower than the voltage on  $C_0$ . As per Table 1, this condition is always met as  $V_{Bt}$  is lesser than  $V_{C0}$ . Also, turning off the switches  $S_c$  and  $S_d$  prevent the battery from overcharging and deep discharging.

## III. ANALYSIS OF PROPOSED TRIPLE PORT DC-DC CONVERTER

The different modes of operation with their switching states and equivalent circuit diagrams are explained in this section. In Table 1, modes of operation of the proposed DC-DC converter are provided with information of ports and power flow direction in the converter.

### A. MODE-1 (PV TO LOAD)

In mode-1, the PV panel (Port-1) delivers power to the load (Port-3). The power flow from the PV panel to load is maintained by controlling switches  $S_1$ , and  $S_2$  are simultaneously turned ON and OFF. Thus, this mode is divided into two states; one when both switches are turned ON (duty cycle for state-1 is  $k_1$ ) and another when they are turned OFF (duty cycle for state-2 is  $k_2$ ), hence,  $k_1 + k_2 = 1$ . The battery disconnected in this mode and switches  $S_c$  and  $S_d$  are in OFF state. The equivalent circuit when switches  $S_1$ ,  $S_2$  simultaneously are turned ON and OFF is shown in Fig. 2(a) and 2(b) respectively. The characteristics waveforms of mode-1 are shown in Fig. 2(c). When switches  $S_1$  and  $S_2$  are turned ON, inductor  $L_1$  is magnetized by input supply ( $V_{PV}$ ) and inductor  $L_2$  is magnetized by input supply ( $V_{PV}$ ) and capacitor  $C_1$  voltage. Diode  $D_1$ ,  $D_2$ ,  $D_c$ , and  $D_d$  are in reverse biased. The inductor ( $L_1$  and  $L_2$ ) current slope and capacitor ( $C_0$  and  $C_1$ ) voltage slope in ON state obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_{PV}}{L_1}, \quad \frac{dv_{C0}}{dt} = \frac{-V_o}{RC_0} \\ \frac{di_{L2}}{dt} &= \frac{V_{PV} + V_{C1}}{L_2}, \quad \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1} \end{aligned} \right\} \quad (1)$$

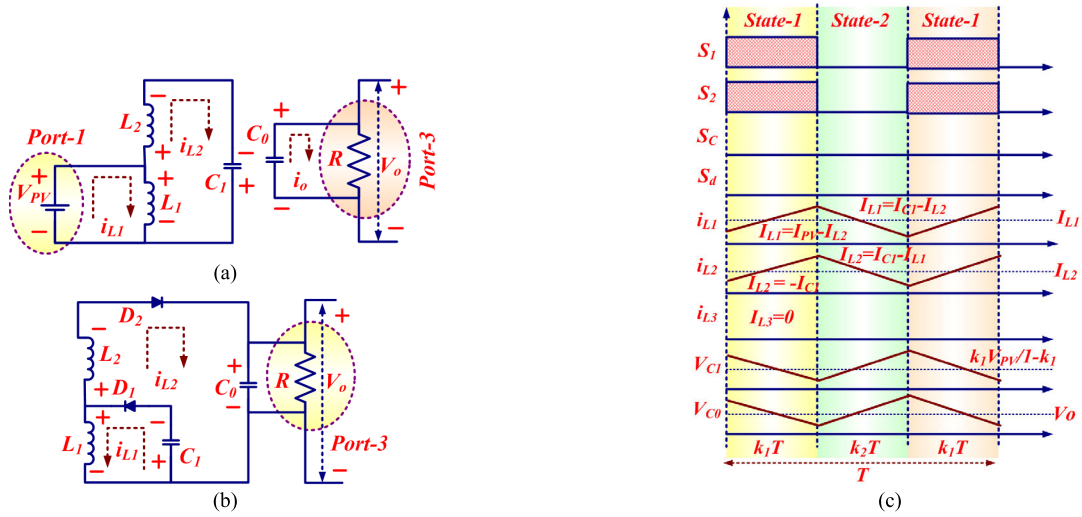
When switches  $S_1$  and  $S_2$  are turned OFF, inductor  $L_1$  is demagnetized to charge capacitor  $C_1$ . Inductor  $L_2$  is demagnetized through the load and also charging the capacitor  $C_0$ . Diodes  $D_1$ ,  $D_2$  are forward biased, and diodes  $D_c$ , and  $D_d$  are reversed biased. The inductors ( $L_1$  and  $L_2$ ) current slope and capacitors ( $C_0$  and  $C_1$ ) voltage slope in OFF state are obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{-V_{C1}}{L_1}, \quad \frac{dv_{C0}}{dt} = \frac{i_{L2} - V_0 R^{-1}}{C_0} \\ \frac{di_{L2}}{dt} &= \frac{-V_0 - V_{C1}}{L_2}, \quad \frac{dv_{C1}}{dt} = \frac{i_{L1} + i_{L2}}{C_1} \end{aligned} \right\} \quad (2)$$

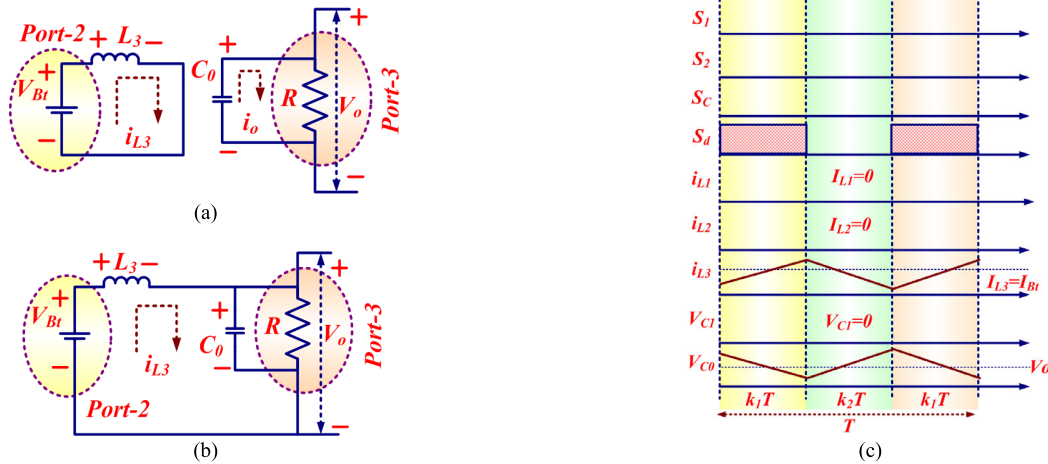
The voltage across the capacitors ( $C_0$  and  $C_1$ ) is obtained as,

$$V_{C1} = \frac{k_1}{1 - k_1} V_{PV}, \quad V_{C0} = \left( \frac{k_1}{1 - k_1} \right)^2 V_{PV} \quad (3)$$





**FIGURE 2.** Mode-1 equivalent circuit of the proposed converter (a) When Switches  $S_1$  and  $S_2$  are ON (State-1), (b) When switches  $S_1$  and  $S_2$  are in OFF (State-2), (c) Characteristic waveforms for mode-1.



**FIGURE 3.** Mode-2 equivalent circuit of the proposed converter (a) When switch  $S_d$  is ON (State-1), (b) When switch  $S_d$  is OFF (State-2), (c) Characteristic waveform for mode-2.

The drain to source voltage across switches and Peak Inverse Voltage (PIV) of diodes is obtained as,

$$\left. \begin{aligned} V_{S1} &= V_{C1} + V_{PV}, V_{S2} = V_{C1} + V_0, \\ -V_{Si} &= V_{Sc} = V_{Sd} = V_0/3 \\ V_{D1} &= -(V_{C1} + V_{PV}), V_{D2} = -(V_{C1} + V_0) \end{aligned} \right\} \quad (4)$$

### B. MODE-2 (BATTERY TO LOAD)

In mode-2, the battery (Port-2) delivers power to the load (Port-3). This happens during the absence of sufficient PV power. The power flow of battery to load is maintained by controlling switch  $S_d$ . This mode is divided into two states; one when switch  $S_d$  is turned ON (duty cycle for state-1 is  $k_1$ ) and another when switch  $S_d$  is OFF (duty cycle for state-2 is  $k_2$ ), hence,  $k_1 + k_2 = 1$ . Switch  $S_d$  is turned ON; diode  $D_c$  plays a critical role to connect inductor  $L_3$  to load.

The equivalent circuit when switch  $S_d$  is turned ON is shown in Fig. 3(a). In this case, inductor  $L_3$  is magnetized by battery supply ( $V_{Bt}$ ), and capacitor  $C_0$  is discharged through

the load. Diodes  $D_1, D_2, D_c$ , and  $D_d$  are reversed biased. The inductor ( $L_3$ ) current slope and capacitor ( $C_0$ ) voltage slope is obtained as,

$$\frac{di_{L3}}{dt} = \frac{V_{Bt}}{L_3}, \quad \frac{dv_{C0}}{dt} = \frac{-V_o}{RC_0} \quad (5)$$

The equivalent circuit when switch  $S_d$  turned OFF is shown in Fig. 3(b). In this case, inductor  $L_3$  is demagnetized in series with battery ( $V_{Bt}$ ) and transfers its energy to charge capacitor  $C_0$  through diode  $D_c$ . Diode  $D_1, D_2$ , and  $D_d$  are reverse biased. The inductor ( $L_3$ ) current slope and capacitor ( $C_0$ ) voltage slope are obtained as,

$$\frac{di_{L3}}{dt} = \frac{-V_o + V_{Bt}}{L_3}, \quad \frac{dv_{C0}}{dt} = \frac{i_{L3} - V_o R^{-1}}{C_0} \quad (6)$$

The voltage across the capacitor ( $C_0$ ) is obtained as,

$$V_{C0} = \frac{1}{1 - k_1} V_{Bt} \quad (7)$$

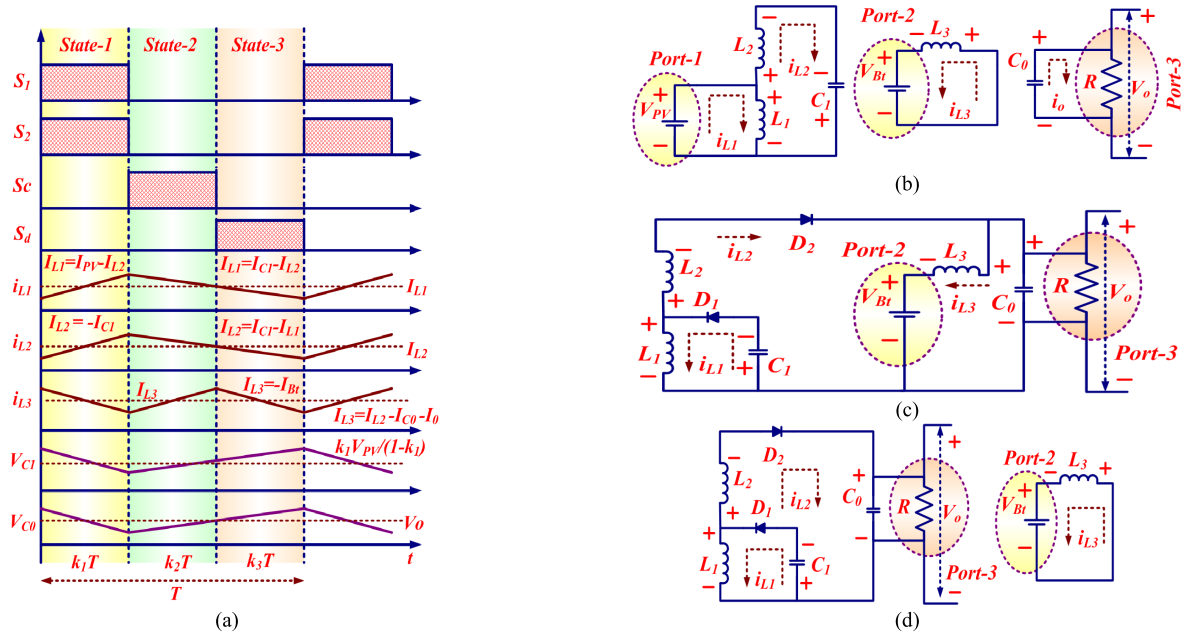


FIGURE 4. Mode-3 equivalent circuit of proposed converter (a) Characteristic waveform for mode-3 (b) State-1 (c) State-2 (d) State-3.

The drain to source voltage across switches and PIV of diodes are obtained as,

$$V_{Sd} = V_0, \quad V_{Si} = V_{Sc} = V_0/2 \quad (8)$$

The characteristics waveforms of mode-2 are shown in Fig. 3(c).

### C. MODE-3 (PV TO BATTERY AND LOAD)

Depending on the switching states, this mode consists of three sub-states (duty cycles for state-1, state-2, and state-3 are  $k_1, k_2$ , and  $k_3$  respectively; hence,  $k_1 + k_2 + k_3 = 1$ ) and characteristics waveforms for mode-3 are shown in Fig. 4(a). At the Port-1 and Port-3 photovoltaic panel and load are connected, respectively, and the battery is connected at Port-2.

#### 1) STATE-1

In this state, switches  $S_1$  and  $S_2$  are synchronously turned ON. Diodes  $D_1, D_2$  and  $D_c$  are reversed biased, and diode  $D_d$  is in forward biased condition. Inductor  $L_1$  is magnetized by input supply ( $V_{PV}$ ) through switch  $S_1$ . Inductor  $L_2$  is magnetized by input supply ( $V_{PV}$ ) and capacitor  $C_1$  through switch  $S_2$ . Thus, the slope of the inductor  $L_1$  and  $L_2$  current is positive. Capacitor  $C_0$  is discharged to make the load voltage constant. The power switches  $S_c$ , and  $S_d$  are turned OFF.

The inductor  $L_3$  is demagnetized through diode  $D_d$  and supply power to charge the battery (Port-2). Thus, the slope of the inductor  $L_3$  current is negative, and diode  $D_d$  is forward biased. The equivalent circuit diagram for this state is shown in Fig. 4(b). The inductor ( $L_1, L_2$ , and  $L_3$ ) current slopes and capacitor ( $C_0$  and  $C_1$ ) voltage slopes for this state are obtained

as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_{PV}}{L_1}, \quad \frac{di_{L2}}{dt} = \frac{V_{PV} + V_{C1}}{L_2}, \quad \frac{di_{L3}}{dt} = \frac{-V_{Bt}}{L_3} \\ \frac{dv_{C0}}{dt} &= \frac{-V_0}{RC_0}, \quad \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1} \end{aligned} \right\} \quad (9)$$

#### 2) STATE-2

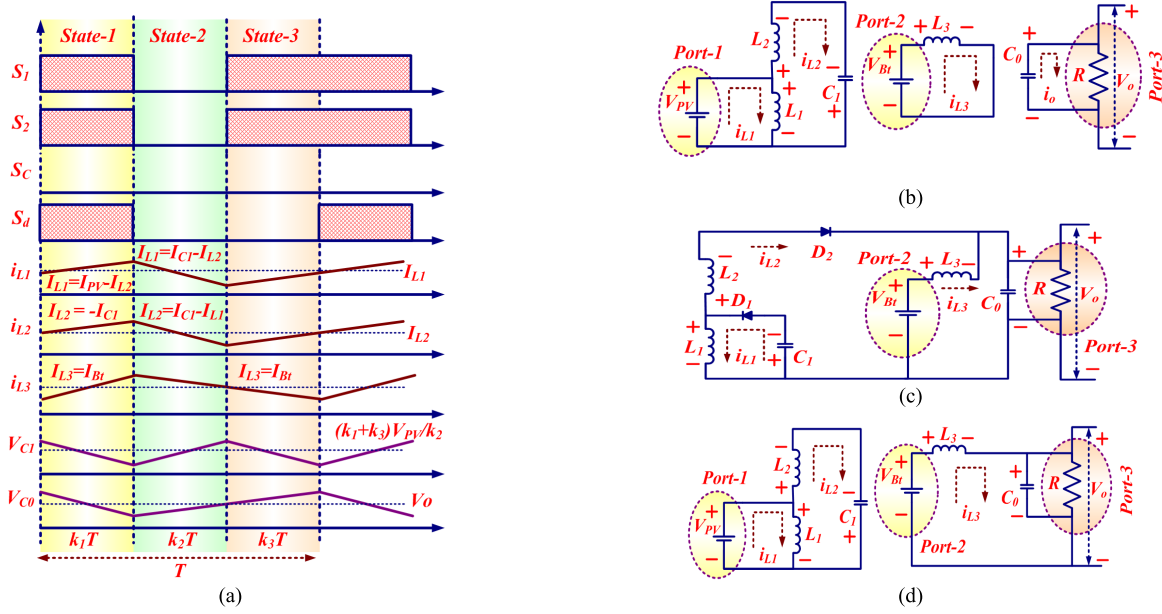
The power switches  $S_1$  and  $S_2$  are synchronously turned OFF. Diodes  $D_1$  and  $D_2$  are forward biased and diodes  $D_c, D_d$  is reversed biased. Inductor  $L_1$  is demagnetized to charge the capacitor  $C_1$  through diode  $D_1$ . Inductor  $L_2$  is demagnetized to charge the capacitors  $C_0$  through diode  $D_2$ . Switch  $S_c$  is turned ON and switch  $S_d$  is turned OFF. Inductor  $L_3$  is magnetized, and the battery is charged by inductor  $L_2$  through switch  $S_c$ . As a result, the slope of inductor ( $L_1$  and  $L_2$ ) current is negative, and the slope of inductor  $L_3$  is positive. The equivalent circuit diagram for this state is shown in Fig. 4(c). The inductor ( $L_1, L_2$ , and  $L_3$ ) current slope and capacitor ( $C_0$  and  $C_1$ ) voltage slope for this state is obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{-V_{C1}}{L_1}, \quad \frac{di_{L2}}{dt} = \frac{-V_0 - V_{C1}}{L_2}, \quad \frac{di_{L3}}{dt} = \frac{V_0 - V_{Bt}}{L_3} \\ \frac{dv_{C0}}{dt} &= \frac{i_{L2} - i_{L3} - V_0 R^{-1}}{C_0}, \quad \frac{dv_{C1}}{dt} = \frac{i_{L1} + i_{L2}}{C_1} \end{aligned} \right\} \quad (10)$$

#### 3) STATE-3

In this state, switches  $S_1, S_2, S_d$ , and  $S_c$  are turned OFF. In this state, inductors  $L_1$  and  $L_2$  are demagnetized to charge capacitors  $C_1$  and  $C_0$  respectively. The inductor  $L_3$  is demagnetized, and energy is transferred to charge the battery through diode  $D_d$ . Thus, the slopes of the inductors  $L_1, L_2$  and  $L_3$  currents are negative. Diodes  $D_1, D_2$ , and  $D_d$  are forward biased, and diodes  $D_c$  are reversed biased. The equivalent circuit diagram





**FIGURE 5.** Mode-4 equivalent circuit of proposed converter (a) Characteristic waveform for mode-4 (b) State-1 (c) State-2 (d) State-3.

for this state is shown in Fig. 4(d). The inductor ( $L_1$ ,  $L_2$ , and  $L_3$ ) current slope and capacitor ( $C_0$  and  $C_1$ ) voltage slope for this state is obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{-V_{C1}}{L_1}, \frac{di_{L2}}{dt} = \frac{-V_0 - V_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{-V_{Bt}}{L_3} \\ \frac{dv_{C0}}{dt} &= \frac{i_{L2} - V_0 R^{-1}}{C_0}, \frac{dv_{C1}}{dt} = \frac{i_{L1} + i_{L2}}{C_1} \end{aligned} \right\} \quad (11)$$

The voltage across capacitors ( $C_0$  and  $C_1$ ) and battery voltage ( $V_{Bt}$ ) are obtained as,

$$\left. \begin{aligned} V_{C1} &= \frac{k_1}{1 - k_1} V_{PV}, V_{C0} = \left( \frac{k_1}{1 - k_1} \right)^2 V_{PV} \\ V_{Bt} &= (k_2) \left( \frac{k_1}{1 - k_1} \right)^2 V_{PV} \end{aligned} \right\} \quad (12)$$

The drain to source voltage magnitude across switches and PIV of diodes are obtained as

$$\left. \begin{aligned} V_{S1} &= V_{C1} + V_{PV}, V_{S2} = V_{C1} + V_0, -V_{Si} = V_{Sc} = V_0/2, \\ V_{Sd} &= V_0, V_{D1} = -(V_{C1} + V_{PV}), V_{D2} = -(V_{C2} + V_0) \end{aligned} \right\} \quad (13)$$

#### D. MODE-4 (PV AND BATTERY TO LOAD)

This mode is employed when the PV energy is not sufficient to drive the load. Also, Port-1 and Port-2 are the input ports, and Port-3 is the output port. Depending on the switching states, this mode is divided into three sub-states (duty cycles for state-1, state-2, and state-3 are  $k_1$ ,  $k_2$ , and  $k_3$  respectively; hence,  $k_1 + k_2 + k_3 = 1$ ) and characteristics waveforms of the converter are shown in Fig. 5(a).

##### 1) STATE-1

In this state, switches  $S_1$ ,  $S_2$ , and  $S_d$  are turned ON. Inductor  $L_1$  is magnetized by input supply ( $V_{PV}$ ) through switch  $S_1$ .

At the same time, inductor  $L_2$  is magnetized by input supply ( $V_{PV}$ ) and capacitors  $C_1$  through switch  $S_2$ . Capacitor  $C_0$  is discharged through load  $R$ . The inductor  $L_3$  is magnetized by battery voltage ( $V_{Bt}$ ) through switch  $S_d$ . Therefore, in this state slope of the inductors  $L_1$ ,  $L_2$  and  $L_3$  current is positive. In this state, switch  $S_c$  is turned OFF, and diodes  $D_1$ ,  $D_2$ ,  $D_c$ , and  $D_d$  are reverse biased. The equivalent circuit diagram for this state is shown in Fig. 5(b). The inductor ( $L_1$ ,  $L_2$ , and  $L_3$ ) current slope and capacitor ( $C_0$  and  $C_1$ ) voltage slope for this state is obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_{PV}}{L_1}, \frac{di_{L2}}{dt} = \frac{V_{PV} + V_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{V_{Bt}}{L_3} \\ \frac{dv_{C0}}{dt} &= \frac{-V_0}{RC_0}, \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1} \end{aligned} \right\} \quad (14)$$

##### 2) STATE-2

In this state, switches  $S_1$  and  $S_2$  are synchronously turned OFF. Inductors  $L_1$  and  $L_2$  are demagnetized to charge the capacitors  $C_1$  and  $C_0$ , respectively. Switches  $S_c$  and  $S_d$  are turned OFF. Inductor  $L_3$  is also demagnetized to supply load. Therefore, in this state slope of the inductor  $L_1$ ,  $L_2$  and  $L_3$  currents are negative. In this state, the circuit from the battery (Port-2) to load (Port-3) is acting as a conventional boost converter; diodes  $D_1$ ,  $D_2$ ,  $D_c$  are forward biased, and diode  $D_d$  is reverse biased. As a result, the load is supplied throughout the state by battery and inductor  $L_2$ . The equivalent circuit diagram for this state is shown in Fig. 5(c). The inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ) current slope and capacitors ( $C_0$  and  $C_1$ ) voltage slope for this state is obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{-V_{C1}}{L_1}, \frac{di_{L2}}{dt} = \frac{-V_0 - V_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{V_{Bt} - V_0}{L_3} \\ \frac{dv_{C0}}{dt} &= \frac{i_{L2} + i_{L3} - V_0 R^{-1}}{C_0}, \frac{dv_{C1}}{dt} = \frac{i_{L1} + i_{L2}}{C_1} \end{aligned} \right\} \quad (15)$$

### 3) STATE-3

In this state, switches  $S_1$  and  $S_2$  are synchronously turned ON. Inductor  $L_1$  is magnetized by input supply ( $V_{PV}$ ) through switch  $S_1$ . Inductor  $L_2$  is magnetized by input supply ( $V_{PV}$ ) and capacitors  $C_1$  through switch  $S_2$ . Switches  $S_C$  and  $S_d$  are turned OFF. Inductor  $L_3$  is demagnetized to supply load. Therefore, the slope of the inductor  $L_1$ ,  $L_2$  current is positive, and inductor  $L_3$  current is negative. The circuit from the battery (Port-2) to load (Port-3) is acting as a conventional boost converter. In this state, diode  $D_c$  is forward biased, and diodes  $D_1$ ,  $D_2$ , and  $D_d$  are reversed biased. Thus, the load is supplied by battery throughout the state. The equivalent circuit diagram for this state is shown in Fig. 5(d). The inductors ( $L_1$ ,  $L_2$ , and  $L_3$ ) current slope and capacitors ( $C_0$  and  $C_1$ ) voltage slope for this state is obtained as,

$$\left. \begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_{PV}}{L_1}, \frac{di_{L2}}{dt} = \frac{V_{PV} + V_{C1}}{L_2}, \frac{di_{L3}}{dt} = \frac{V_{Bt} - V_o}{L_3} \\ \frac{dV_{C0}}{dt} &= \frac{i_{L3} - V_o R^{-1}}{C_0}, \frac{dV_{C1}}{dt} = \frac{-i_{L2}}{C_1} \end{aligned} \right\} \quad (16)$$

The voltage across the capacitors ( $C_1$  and  $C_0$ ) is obtained as,

$$\left. \begin{aligned} V_{C1} &= \frac{k_1 + k_3}{1 - (k_1 + k_3)} V_{PV} \\ V_{C0} &= \left( \frac{k_1 + k_3}{1 - (k_1 + k_3)} \right)^2 V_{PV} = \frac{1}{1 - k_1} V_{Bt} \end{aligned} \right\} \quad (17)$$

The drain to source voltage magnitude across switches and PIV of diodes are obtained as,

$$\left. \begin{aligned} V_{S1} &= V_{C1} + V_{PV} \\ V_{S2} &= V_{C1} + V_o, -V_{Si} = V_{Sc} = V_o/2, V_{Sd} = V_o \\ V_{D1} &= -(V_{C1} + V_{PV}), V_{D2} = -(V_{C1} + V_o) \end{aligned} \right\} \quad (18)$$

### E. DESIGN OF INDUCTORS

In general,  $k_{Sx}$  is the duty cycle of switch  $S_x$  and thus  $k_{Sx} + k'_{Sx} = 1$ . The inductors are designed to ensure the condition that the peak-to-peak inductor current variation,  $\Delta i_{L(peak-peak)}$  is within 20% of the average inductor current. The critical point between positive current and negative current in the inductor is assumed at  $\Delta i_L = 10\%$  of the rated dc current. In addition, the maximum possible input voltage has been used for calculations. The desired current ripple of inductor and inductor volt-sec balance principle is used to design inductor  $L_1$  as:

$$\Delta i_{L1} = \frac{V_{PV}}{L_1} k_{S1} T = \frac{V_{PV}}{L_1 f_s} k_{S1} \Rightarrow L_1 = \frac{V_{PV}}{\Delta i_{L1} \times f_s} k_{S1} \quad (19)$$

where  $\Delta i_{L1}$  is a ripple of inductor  $L_1$  current. Similarly, the current ripple inductor  $L_2$  and its slope are used to design inductor  $L_2$  as

$$\left. \begin{aligned} \Delta i_{L2} &= \frac{V_{PV} + V_{C1}}{L_2} k_{S2} T = \frac{\left(1 + \frac{k_{S1}}{1 - k_{S1}}\right) V_{PV}}{L_2 f_s} k_{S2} \\ L_2 &= \frac{V_{PV} + V_{C1}}{\Delta i_{L2} \times f_s} k_{S2}, V_{C1} = \frac{k_{S1}}{1 - k_{S1}} V_{PV} \end{aligned} \right\} \quad (20)$$

where  $\Delta i_{L2}$  is a ripple of inductor  $L_2$  current. Similarly, Volt-sec balance and desired current ripple on inductor  $L_3$  are used to design  $L_3$  as

$$\Delta i_{L3} = \frac{V_{Bt}}{L_3} k_{Sd} T = \frac{V_{Bt}}{L_3 \times f_s} k_{Sd} \Rightarrow L_3 = \frac{V_{Bt}}{\Delta i_{L3} \times f_s} k_{Sd} \quad (21)$$

where  $\Delta i_{L3}$  is a ripple of inductor  $L_3$  current.

### F. DESIGN OF CAPACITORS

The capacitor charge-sec balance and the voltage ripples of capacitor  $C_1$  are used to design capacitor  $C_1$  as,

$$\left. \begin{aligned} \Delta V_{C1} &= \frac{i_{L2}}{C_1} k_{S1} T = \frac{V_o}{RC_{1f_s}(1 - k_{S1})} k_{S1} \\ C_1 &= \frac{V_o}{R \Delta V_{C1} f_s (1 - k_{S1})} k_{S1} \end{aligned} \right\} \quad (22)$$

The voltage ripples of capacitor  $C_0$  and its slope are used to design capacitor  $C_0$  as,

$$\Delta V_{C0} = \frac{V_o}{RC_0} k_{S2} T = \frac{V_o}{RC_0 f_s} k_{S2}, \quad C_0 = \frac{V_o}{R \Delta V_{C0} f_s} k_{S2} \quad (23)$$

The voltage and current stress across switches are diodes is calculated as follows,

$$V_{S1} = V_{D1} = \frac{1}{1 - d_1} V_{PV}, \quad V_{S2} = V_{D2} = \frac{1}{d_1} V_o \quad (24)$$

$$\left. \begin{aligned} I_{S1} &= \frac{d_1^4}{(1 - d_1)^4} \frac{V_{PV}}{R}, I_{S2} = I_{D1} = \frac{d_1^3}{(1 - d_1)^3} \frac{V_{PV}}{R}, \\ I_{D2} &= \frac{d_1^2}{(1 - d_1)^2} \frac{V_{PV}}{R} \end{aligned} \right\} \quad (25)$$

## IV. STATE SPACE ANALYSIS OF PROPOSED THREE PORT DC-DC CONVERTER

In [27], by using the state-space averaging method, a hybrid PV/wind battery charger is presented with a mathematical background. In this section, the state space analysis of the proposed triple port converter is discussed for each mode. Let us consider  $x(t)$  is state vector and  $u(t)$  is input vector. The state variables are inductor currents and capacitor voltages. In general, when the switch is ON and OFF, the circuit is illustrated by the state space equation as follows,

$$\left. \begin{aligned} \text{ON state} &\left\{ \begin{aligned} K \dot{x}(t) &= A'x(t) + B'u(t) \\ y(t) &= C'x(t) + D'u(t) \end{aligned} \right. \\ \text{OFF state} &\left\{ \begin{aligned} K \dot{x}(t) &= A''x(t) + B''u(t) \\ y(t) &= C''x(t) + D''u(t) \end{aligned} \right. \end{aligned} \right\} \quad (26)$$

### A. MODE-1 (PV TO LOAD)

In this mode, the converter is operated as SISO converter; where PV is, the input port and load is the output port. When switches  $S_1$  and  $S_2$  are simultaneously turned ON, the state-space matrices are obtained as (27), shown at the bottom of the next page. When switches  $S_1$  and  $S_2$  are simultaneously turned OFF, the state-space matrices are obtained as (28), shown at the bottom of the next page. By (27)-(28), the voltage and current conversion ratio are obtained as (29).

$$\frac{V_{C1}}{V_{PV}} = \frac{k_1}{1 - k_1}, \quad \frac{V_{C0}}{V_{PV}} = \left( \frac{k_1}{1 - k_1} \right)^2, \quad \frac{I_o}{I_{PV}} = \left( \frac{1 - k_1}{k_1} \right)^2 \quad (29)$$

**B. MODE-2 (BATTERY TO LOAD)**

In this mode, the converter is operated as SISO converter; where the battery is an input port and load is output port. When switch  $S_d$  is turned ON, the state-space matrices are obtained as follow,

$$\begin{bmatrix} \dot{i}_{L3}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC_0} \end{bmatrix}}_{A'} \begin{bmatrix} i_{L3}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_3} \\ 0 \end{bmatrix}}_{B'} [V_{Bt}] \quad (30)$$

$$\begin{bmatrix} i_{Bt} \\ V_o \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}_{C'} \begin{bmatrix} i_{L3}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{D'} [V_{Bt}] \quad (31)$$

When switch  $S_d$  is turned OFF, the state-space matrices are obtained as follows,

$$\begin{bmatrix} \dot{i}_{L3}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \frac{-1}{L_3} \\ \frac{1}{C_0} & \frac{-1}{RC_0} \end{bmatrix}}_{A''} \begin{bmatrix} i_{L3}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_3} \\ 0 \end{bmatrix}}_{B''} [V_{Bt}] \quad (32)$$

$$\begin{bmatrix} i_{Bt} \\ V_o \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}_{C''} \begin{bmatrix} i_{L3}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{D''} [V_{Bt}] \quad (33)$$

By (30)-(33), the voltage and current conversion ratio are obtained as,

$$\frac{V_{C0}}{V_{Bt}} = \frac{1}{1 - k_1}, \quad \frac{I_0}{I_{Bt}} = 1 - k_1 \quad (34)$$

**C. MODE-3 (PV TO BATTERY AND LOAD)**

In this mode, the converter is operated as SIDO converter; where PV is input port, battery and load are output ports. When switches  $S_1$ ,  $S_2$ , and  $S_d$  are simultaneously turned ON, the state-space matrices are obtained as (35), shown at the bottom of the next page. When switches  $S_1$ ,  $S_2$ , and  $S_d$  are simultaneously turned OFF, the state-space matrices are obtained as (36), shown at the bottom of the next page. When switches  $S_1$ ,  $S_2$  are turned OFF, and  $S_d$  is ON the state-space matrices are obtained as (37), shown at the bottom of the page 113659.

Using (35)-(37), the voltage and current conversion ratio are obtained as,

$$\frac{V_{Bt}}{V_{PV}} = \left( \frac{\sqrt{k_2 k_1}}{1 - k_1} \right)^2, \quad \frac{V_{C0}}{V_{PV}} = \frac{I_{PV}}{I_0} = \left( \frac{k_1}{1 - k_1} \right)^2 \quad (38)$$

**D. MODE-4 (PV AND BATTERY TO LOAD)**

In this mode, the converter is operated as DISO converter; where PV and battery are input ports and load is an

$$\begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{R_L C_0} \end{bmatrix}}_{A'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B'} [V_{PV}],$$

$$\begin{bmatrix} i_{PV} \\ V_o \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{D'} [V_{PV}] \quad (27)$$

$$\begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & 0 & \frac{-1}{R_L C_0} \end{bmatrix}}_{A''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B''} [V_{PV}],$$

$$\begin{bmatrix} i_{PV} \\ V_o \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{D''} [V_{PV}] \quad (28)$$

output port. Both input ports share the output current. When switches  $S_1$ ,  $S_2$ , and  $S_d$  are simultaneously turned ON, the state-space matrices are obtained as (39), shown at the bottom of the page 113659. When switches  $S_1$ ,  $S_2$ , and  $S_d$  are simultaneously turned OFF, the state-space matrices are obtained as (40), shown at the bottom of the page 113659. When Switches  $S_1$ ,  $S_2$  are turned ON, and  $S_d$  is OFF the state-space matrices are obtained as (41), shown at the bottom of the page 113660. The voltage conversion ratio is obtained as,

$$\frac{V_{C0}}{V_{Bt}} = \frac{1}{1-k_1}, \quad \frac{V_{C0}}{V_{PV}} = \frac{I_{PV}}{I_0} = \left( \frac{(k_1 + k_3)}{1 - (k_1 + k_3)} \right)^2 \quad (42)$$

## V. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

The system-level control block diagram for the proposed TPC and control logic algorithm for mode selection is given in Fig. 6(a)-(b) respectively. The multi-objective control algorithm was designed to achieve the battery management, the direction of power flow, mode of operation and duty cycle selection. The selection of the mode of operation and the corresponding switching signals are made based on the present PV power, SOC or maximum current pre-set of battery and the load demand. A simple voltage control method is used to maintain output voltage, in which an error signal is generated by the comparing output voltage against a reference voltage.

$$\begin{aligned} \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \\ \dot{v}_{CBt}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{RC_0} & 0 \\ 0 & 0 & \frac{-1}{C_{Bt}} & 0 & 0 & \frac{1}{R_{Bt}C_{Bt}} \end{bmatrix}}_{A'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B'} [V_{PV}], \\ \begin{bmatrix} i_{PV} \\ V_o \\ V_{Bt} \end{bmatrix} &= \underbrace{\begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{D'} [V_{PV}] \quad (35) \\ \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \\ \dot{v}_{CBt}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_3} & \frac{-1}{L_3} \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_0} & \frac{-1}{C_0} & 0 & \frac{-1}{RC_0} & 0 \\ 0 & 0 & \frac{-1}{C_{Bt}} & 0 & 0 & \frac{1}{R_{Bt}C_{Bt}} \end{bmatrix}}_{A''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B''} [V_{PV}], \\ \begin{bmatrix} i_{PV} \\ V_o \\ V_{Bt} \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{D''} [V_{PV}] \quad (36) \end{aligned}$$

$$\begin{aligned}
 \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \\ \dot{v}_{CBt}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & 0 & \frac{-1}{RC_0} & 0 \\ 0 & 0 & \frac{1}{C_{Bt}} & 0 & 0 & \frac{-1}{R_{Bt}C_{Bt}} \end{bmatrix}}_{A'''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B'''} [V_{PV}], \\
 \begin{bmatrix} i_{PV} \\ V_o \\ V_{Bt} \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C'''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \\ v_{CBt}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{D'''} [V_{PV}] \quad (37)
 \end{aligned}$$

$$\begin{aligned}
 \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{RC_0} \end{bmatrix}}_{A'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & \frac{1}{L_3} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B'} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix}, \\
 \begin{bmatrix} i_{PV} \\ i_{Bt} \\ V_o \end{bmatrix} &= \underbrace{\begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C'} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{D'} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix} \quad (39)
 \end{aligned}$$

$$\begin{aligned}
 \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_0} & \frac{1}{C_0} & 0 & \frac{-1}{RC_0} \end{bmatrix}}_{A''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_3} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B''} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix}, \\
 \begin{bmatrix} i_{PV} \\ i_{Bt} \\ V_o \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{D''} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix} \quad (40)
 \end{aligned}$$

**TABLE 2.** Parameters of proposed system.

Input voltage $V_{in}$	12V (boost mode) and 30V (buck mode) for mode 1 (PV) 12V (Battery) mode 2, 18V (PV) for mode 3 18 V (PV) and 12 V (Battery) for mode 4
Output voltage $V_o$	24V (boost mode) and 18V (buck mode) for mode 1 24V for mode 2, 24V for mode 3, 24V for mode 4
Inductors $L_1, L_2, L_3$	1.4mH, 3.3mH, 0.75mH
Capacitors $C_1, C_0$	7.5μF, 18.75μF
Battery Voltage $V_{Bt}$	12V, 12 Ah
Switching frequency $f_s$	20kHz

This error is compared with the fixed frequency sawtooth signal to determine the duty ratio. A 200W prototype is developed to demonstrate the feasibility of the proposed converter. The proposed prototype and experimental setup are shown in Fig. 6(c)-(d), respectively.

The control signals generated from Xilinx FPGA Spartan 6 are applied as gate pulses to power switches. The switching frequency of the gate pulses is 20 kHz. The components were chosen to allow a robust converter in the 25W to 200W output power range and guarantee operation in continuous conduction mode. The inductors  $L_1$ ,  $L_2$ , and  $L_3$  are designed to support the inductor currents in the selected power range. The designed components values of the proposed system are listed in Table 2. Various currents and voltages are sensed using the current sensor LA25-P and IC 7840 voltage sensors, respectively. A PV array with three series-connected 75W, 12V panels, 12V, 12 Ah sealed lead-acid batteries, and a resistive load are employed in the prototype.

### A. MODE-1 (PV TO LOAD)

In this mode, the reference of the load voltage is defined as 24 V and load resistance  $R = 40\Omega$ . Fig. 7(a) shows the gate signal and the inductor currents. Identical gate signals are applied to  $S_1$  and  $S_2$  since both switches conduct synchronously. The average value of inductor currents  $I_{L1}$  and  $I_{L2}$  are 6.24A and 7.99A, respectively. With 12.5V input voltage, the buck-boost converter (Port-1 to Port-3) operates in boost mode with a duty cycle of 0.6 and gives the output voltage of 24V, as shown in Fig. 7(b).

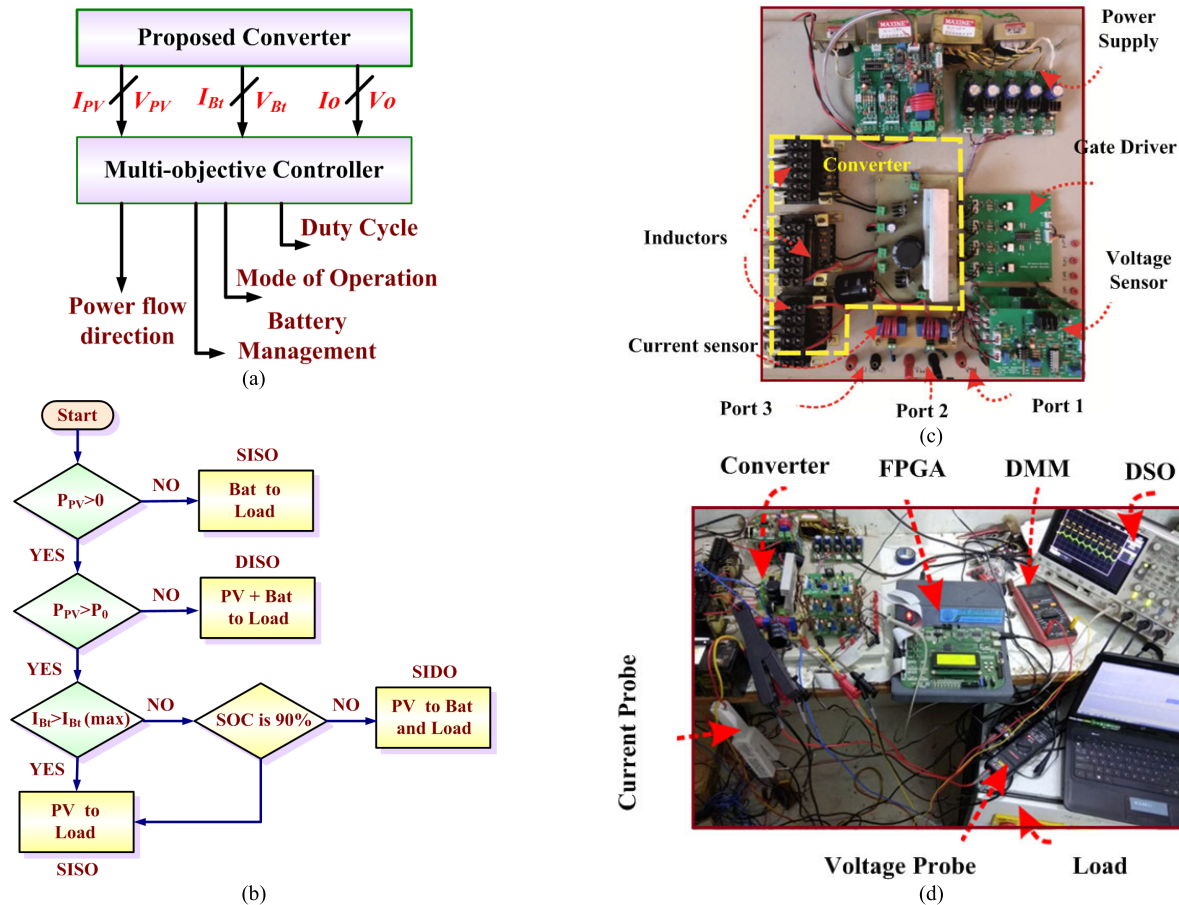
The input and output current ripple is found to be 14% and 11%, respectively, which are slightly more than the assumed value of 10% in design calculation. Fig. 7(c) shows the gate signal and the inductor current when the input voltage is 30V, and a duty cycle is 0.4. The buck-boost converter operates in buck mode and gives 18V output to load. The obtained average value of inductor currents  $I_{L1}$  and  $I_{L2}$  are 750mA and 800mA, respectively. The PV voltage, current, load voltage and current are shown in Fig. 7(d). Input and output current ripple is found to be 12% and 10.2%, respectively. The observed efficiency of proposed converter through simulation and experiment is shown in Fig. 8(a). The maximum efficiency from the experimental results is about 93.6% and 82.7% during boost and buck mode, respectively. The dynamic response with the input voltage variation and load variation is shown in Fig. 8(b). As shown, the load voltage (Port-3) is maintained at 23.6V in spite of continuous fluctuations in PV voltage. In addition, the response of the converter when the load is varied from 25Ω to 50Ω and back from 50 Ω to 25 Ω is shown.

### B. MODE-2 (BATTERY TO LOAD)

The battery provides energy to the load in the absence of PV power and regulates the load voltage. The maximum discharge current limit of the battery and the output voltage is defined as  $I_{Bt(ref)} = 15A$  and 24V, respectively. Fig. 9(a)-(b) shows the measured waveforms with  $V_{Bt} = 12.6V$ , and the

$$\begin{aligned}
 \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{i}_{L3}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C0}(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_0} & 0 & \frac{-1}{RC_0} \end{bmatrix}}_{A'''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ \frac{1}{L_3} & 0 \\ 0 & \frac{1}{L_3} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B'''} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix}, \\
 \begin{bmatrix} i_{PV} \\ V_{Bt} \\ V_o \end{bmatrix} &= \underbrace{\begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{C'''} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ i_{L3}(t) \\ v_{C1}(t) \\ v_{C0}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{D'''} \begin{bmatrix} V_{PV} \\ V_{Bt} \end{bmatrix} \quad (41)
 \end{aligned}$$





**FIGURE 6.** Control logic and hardware setup (a) System level control block diagram, (b) Flowchart for control logic of mode selection, (c) Prototype of the proposed multi-port converter, (d) Experimental prototype setup.

power of the battery is 96.4W. The gate signal to switch  $S_d$  and inductor current  $i_{L3}$  are shown in Fig. 9(a). The output voltage is controlled with  $S_d$ . Fig. 9(b) shows the regulated average battery current,  $I_{Bt(avg)} = 7.65A$ . It can be seen that the battery current in this mode has a positive value, which implies that the battery is discharging. The input and output current ripples are found as 11.7% and 11.1% respectively. The output voltage is regulated well. The dynamic response of the converter with the load variation is shown in Fig. 9(c). As shown, the load voltage (Port-3) is maintained at 24V.

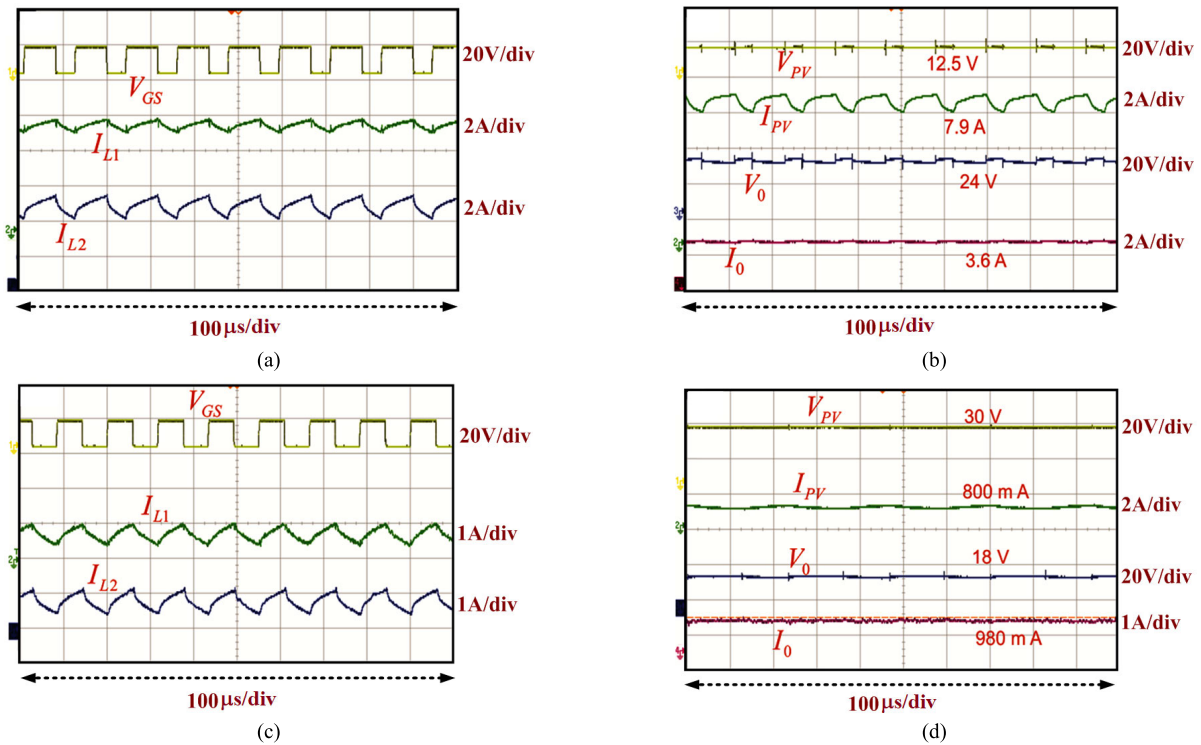
### C. MODE-3 (BATTERY CHARGING) AND MODE-4 (BATTERY DISCHARGING)

In this mode-3, PV provides energy to both load and battery. The battery charging current is limited to 1.5A, and the load (Port-3) voltage is defined as 24V. The Port-3 voltage is controlled by  $S_1$  and  $S_2$ . The converter works in buck mode, and the battery voltage is regulated with  $S_C$ . The battery charging has been achieved with current mode control followed by voltage control.

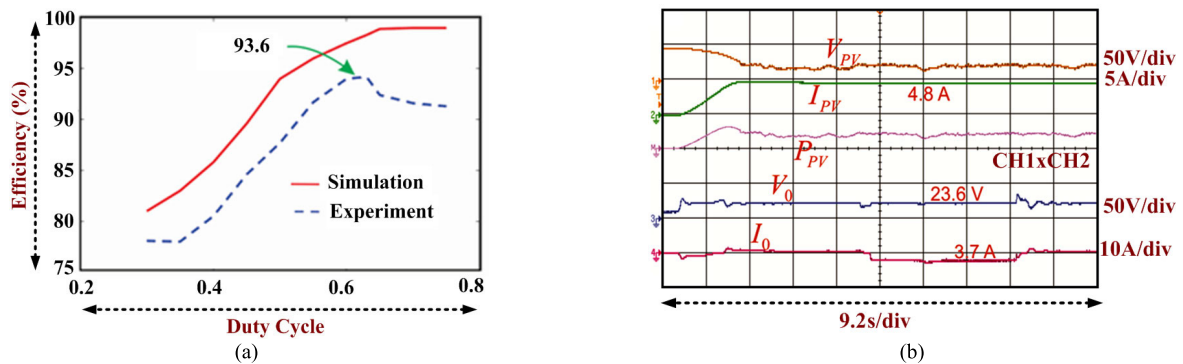
Fig. 10(a) and Fig. 10(b) show the dynamic performance of the proposed converter in various modes of operation. After the converter is switched ON, the battery caters the load (Mode-2) until the MPPT tracks the maximum power

as illustrated in Fig. 10(a). As the PV power increases, the current taken from the battery gradually reduces (Mode-4), i.e., both PV and battery ports share the output current. When it reaches maximum power, and PV power is more than the load consumption, the surplus PV power is fed to the battery for charging (Mode-3). When the load increases the charging current of the battery reduces to maintain the power balance. The positive average battery current  $I_{Bt(avg)} = 1.2A$  shows the charging characteristics. Also, the response of the converter when the input currents from port-1 and port-2 are continuously changing during mode-2 and mode-4 operations are shown in Fig. 10(a). The output voltage is regulated irrespective of the changes in input currents.

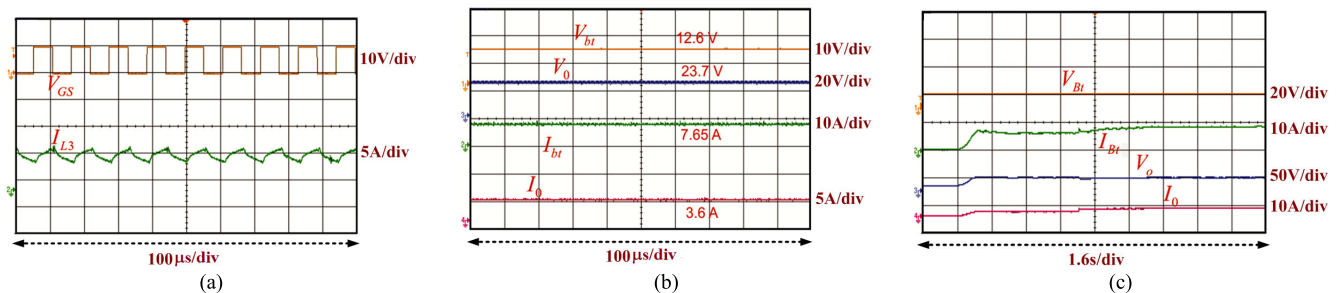
In Mode-4, both the PV and battery are supplying the load. The experimental results with  $V_{PV} = 18V$ ,  $V_{Bt} = 12.4V$  and PV input power of 108W are illustrated in Fig. 10(b). The experiment has been carried out to show the response of the proposed converter for the sudden changes in parameters. When PV power is more, battery and load are catered by the PV source (Mode-3). When PV power suddenly reduces to zero, the battery is discharged and the current direction changes (Mode-2). In this condition, the battery provides energy to load. When PV power resumes, the current taken from the battery reduces (Mode-4). When the load reduces



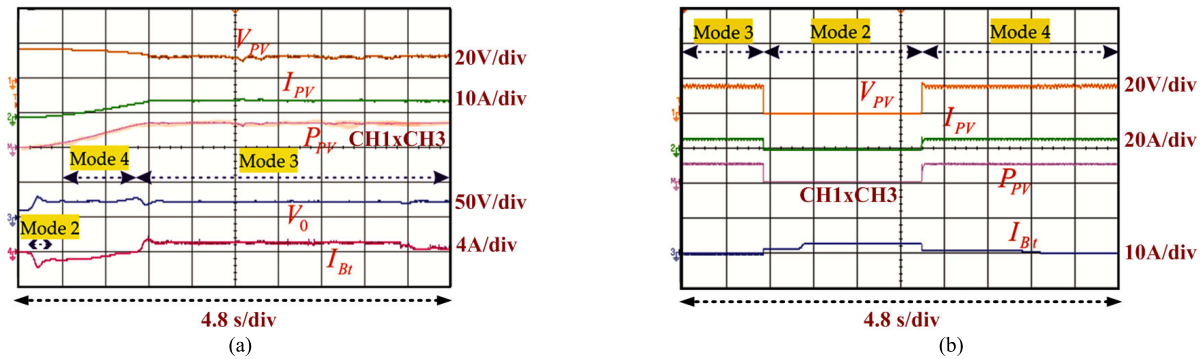
**FIGURE 7.** Hardware Result of mode-1 (a) Gate pulse, Inductor currents  $I_{L1}$  and  $I_{L2}$  (top to bottom) with duty cycle 60%, (b) PV voltage, PV current, Load voltage and Load current (top to bottom) with duty cycle 60%, (c) Gate pulse, Inductor currents  $I_{L1}$  and  $I_{L2}$  (top to bottom) with duty cycle 40%, (d) PV Voltage, PV current, Load voltage and Load current (top to bottom) with duty cycle 40%.



**FIGURE 8.** Efficiency and Dynamic Behavior (a) Efficiency versus duty cycle buck and boost operation. (plot through experimental data) (b) Dynamic response PV Voltage, current, load voltage and current (top to bottom).



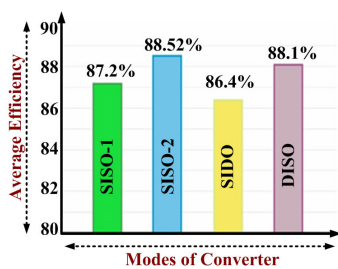
**FIGURE 9.** Hardware Result of mode-2 (a) Gate pulse, inductor current  $I_{L3}$  (top and bottom), (b) Battery voltage, load voltage, battery current and load current (top to bottom), (c) Dynamic response -Battery voltage, current, load voltage and current (top and bottom).



**FIGURE 10.** Hardware result of Mode 3 and Mode 4. (a) Dynamic behavior for  $P_{max}$  - PV Voltage, PV current, power, load voltage and battery current (top to bottom) (b) Dynamic behavior for 108W -PV voltage, PV current, power and battery current (top to bottom).

**TABLE 3.** Comparison of the proposed triple port converter with recently reported converters.

Converter	Number of Active switches	Number of diodes	Number of inductors	Number of capacitors	Switching frequency	Voltage Gain	Efficiency (%)	Reported power rating
[28]	4	2	1	1	10 kHz	High	91	-
[29]	3	4	2	3	40 kHz	High	92.7	200W
[30]	4	2	2	1	20 kHz	Medium	93.97	1kW
[31]	3	1	3	4	100 kHz	Medium	93.5	1.2kW
[32]	4	3	2	3	100 kHz	Low	96	400W
[33]	8	8	2, 2 coupled inductor	3	50 kHz	Medium	92 (expected)	-
[34]	3	3	1	2	20 kHz	High	93.5	120W
[35]	2	1	3	3	20 kHz	Low	92.74	100W
[36]	3	1	1	3	50 kHz	Medium	93.75	80W
Proposed converter	4	4	3	2	20 kHz	High	93.6	200W



**FIGURE 11.** Experimentally observed average efficiencies for each mode.

the discharging current of the battery reduces to maintain the power balance. These responses indicate that the converter is controlled and offers stable operation. Several tests are conducted, and the graph of average efficiency for each mode is shown in Fig. 11 and the observed average efficiency for Mode 1 to Mode 4 is 87.2%, 88.52%, 86.4%, and 88.1%, respectively.

Table 3 shows a comparison of the NI-TP-BBB converter and other state-of-the-art TPCs in terms of components, voltage gain and efficiency. The converters [47], [53] and [82] have less efficiency and gain relatively. Thanks to the additional semiconductors which gives high step-up/step-down feature. Though the proposed triple port buck-boost converter has relatively more components, it provides high gain and relatively good efficiency when comparing with the TPC

proposed in [83]. The power density (P.d) of the proposed converter is,

$$P.d = \frac{\text{Power}}{\text{Volume}} = \frac{200}{15 \times 21 \times 6} = 0.105 \text{ W/cm}^3 \quad (43)$$

## VI. CONCLUSIONS

A new triple port converter with two unidirectional and one bi-directional port which integrate a photovoltaic module, battery and DC load is proposed. The proposed converter system provides a robust option for interfacing multiple renewable energy sources. The modes of operations with the characteristics waveform are discussed in detail. When PV is sufficient only to feed load, isolation of the battery from the main supply is achieved by using the switch control method. Also, the switch control method prevents the battery from overcharging and discharging. The proposed converter has positive high step-up/step-down output voltage (squared times of the voltage conversion ratio of classical buck-boost converter), and has a provision for step-up as well as step-down conversion with the simple control strategy. The higher voltage conversion ratio of the buck-boost converter is achieved by attaching an extra inductor at the drain of the switch of the buck-boost converter (the obtained structure is the hybrid version of buck and buck-boost converter). A constant DC bus voltage is maintained, and the PV array power characteristics follow the irradiance curve. Thus, the maximum power flow confirms from the PV array. The presented



converter overcomes the drawback of the traditional buck-boost converter and verified by the obtained results. Experiment results are provided with dynamic performance, and it is verified that the proposed converter is an excellent choice for applications in both industrial and domestic applications.

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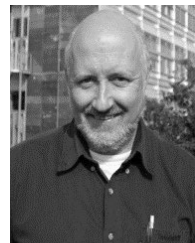


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