A Novel Power Sharing Scheme of Controlling Parallel-Operated Inverters in Islanded Microgrids

Cao, Wenyuan; Han, Minxiao; Zhang, Xiahui ; Xie, Wenqiang; Tinajero, Gibran David Agundis; Guerrero, Josep M.

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3048522

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

A Novel Power Sharing Scheme of Controlling Parallel-Operated Inverters in Islanded Microgrids

Wenyuan Cao, *Student Member, IEEE*, Minxiao Han, *Senior Member, IEEE*, Xiahui Zhang, Wenqiang Xie, *Student Member, IEEE*, Gibran Agundis-Tinajero, *Member, IEEE*, and Josep M. Guerrero, *Fellow, IEEE*

***Abstract*—Virtual impedances are often used in droop-controlled paralleled-voltage-sourced inverters (VSIs) to achieve proper power sharing. However, different and unknown output impedances of VSIs will affect the power decoupling and power sharing performances. To solve this problem, this paper proposes a novel controller for VSIs by using a disturbance observer (DOB). The DOB is adopted to observe the output currents of VSIs without any extra current sensors. On the one hand, the observed currents are fed forward to the output of voltage compensators, thereby the output impedances of VSIs are eliminated. On the other hand, the observed currents are introduced into the virtual complex impedance loops, which not only reconstructs the impedances of VSIs but also realizes the proper power sharing. Besides, to improve the reactive power sharing accuracy, a synchronization control is proposed to strictly synchronize the VSIs only by using local measurements. Each VSI operates at a constant frequency, so the inherent frequency deviation of the traditional droop control is eliminated. A universal parameter design method is also presented based on the detailed discussion of system stability and voltage quality. Finally, simulation and experimental results clearly validate the proposed control scheme and the parameter design method.**

***Index Terms*—Voltage-sourced inverters, disturbance observer, feed-forward control, virtual complex impedance, synchronization control.**

I. Introduction

Droop control has become the focus of research in recent years due to its advantages of communication-free and high reliability. It has been widely used in UPS and islanded microgrid fields to realize the independent operation of islanding systems and the accurate power distribution between VSIs [1]-[3]. However, the traditional frequency-and voltage-droop control method has the following problems: 1) the mismatch of output impedances and line impedances leads to the power coupling and low power sharing accuracy, it even causes instability due to the decoupling and nonlinearity of the power loop [4]; 2) the low-pass filter (LPF) in power calculation loop results in poor dynamic performance [5]; 3) the droop characteristics cause the inherent frequency and voltage deviations [6]. To overcome the above problems, several improved droop control methods have been proposed, including 1) variants of droop control methods; 2) virtual structure-based methods; 3) construct- and compensate-based methods; 4) hybrid droop/signal-injection-based methods [7].

Among many improved droop control methods, virtual impedance is a typical method that can realize power decoupling and improve power sharing accuracy [8], [9]. The virtual impedances simulate the actual impedances by subtracting the voltage drop of the virtual impedances from the voltage reference. Therefore, the virtual impedances can be changed accordingly to be pure inductive, pure resistive, or inductive-resistive [10], [11]. However, only when the combined impedances, that is, the sum of the output impedances, virtual impedances, and line impedances match, can the virtual impedances guarantee the accurate reactive power sharing of each VSI [12]. In other words, when designing virtual impedances, the value of output impedances and line impedances should be known in advance. Although the line impedances can be obtained through measurements or the grid parameter estimator proposed in [13], it is difficult to accurately acquire the output impedances, due to the harmonic injection and signal acquisition error. Consequently, how to avoid the influence of the output impedances on power decoupling and power sharing has become a critical issue. The output impedances can be easily reduced by increasing the proportional term and the integral term of the voltage compensator [10]. Nevertheless, a trade-off is required between the compensator parameters and system stability. PR controller in $\alpha\beta$ coordinates is also put forward to weaken the output impedances [14], [15]. Whereas, the inherent frequency deviation characteristic of droop control makes the system unable to work at the resonant point precisely and the tracking accuracy of voltages deteriorates. Compared with the above two methods, the feed-forward compensation of output currents

This work was supported by National Key R&D Program of China (2018YFB0904700).

W. Cao and M. Han, X. Zhang and W. Xie are with the School of Electric and Electronic Engineering, North China Electric Power University, Beijing 102206, China (e-mail: bjcaowenyuan@163.com; hanminxiao@263.net; zhangxiahui97@163.com; bjxiewenqiang@163.com;).

Gibran Agundis-Tinajero and J. M. Guerrero are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: gibran.zigma@gmail.com; joz@et.aau.dk).

becomes a more practical and effective way. The output impedance is modified by feeding forward the output current that is usually measured through current sensors [16]. But this method not only increases the cost of current sensors and signal processing circuits (especially in high-power situations), but also takes up the A/D converters of DSP. To tackle the aforementioned, the DOB [17], [18], which has a simple structure and requires no current sensors, is proposed to collect the output currents [19], [20]. Since the virtual impedance method also requires the output currents, the authors wonder whether DOB-based feed-forward compensation could be incorporated with the virtual impedance loop to form a unified sensorless controller. There are no relevant researches have been carried out yet, so this paper focuses on the principle of this novel controller and puts forward a detailed scheme.

Poor dynamic performance is another problem that needs to be solved. Recently, the *V-I* droop characteristic-based strategy is becoming a promising alternative, designed to achieve proper power sharing between VSIs through voltage control, rather than power control [14], [21]-[25]. Due to the absence of LPF in the power loop, the *V-I* droop control possesses faster dynamics. Besides, compared with the conventional droop control, it enhances stability since adding a *V-I* droop is equivalent to providing an increased damping [22], [24]. While the advantages of this approach are tempting, the disadvantage is also obvious. With the power loop removed, the synchronization mechanism of VSIs is also eliminated. To handle this, [14] and [21] adopt a PLL or an improved PLL to synchronize VSIs with the common AC bus, which will inevitably introduce a master VSI to offer a fixed reference phase angle. Such operation reduces the reliability of the system and increases the complexity of the control. In [22]-[24], a global positioning system (GPS) is utilized as a time reference. In this case, the accurate power sharing is affected by the GPS delay, and the failure of the GPS leads to the collapse of the entire system. Accordingly, [25] proposes a self-synchronous method based on local information. However, the circulating current between VSIs during the transient process is not considered.

The third drawback with the traditional droop control is that the frequency and voltage offset with the change of power. The virtual negative resistances or negative reactances can alleviate the voltage magnitude deviation [15], whereas they can not improve the frequency quality of the output voltage. Therefore, some secondary control schemes are proposed to compensate for the voltage magnitude and frequency deviations, which utilize a central controller [26] or a distributed controller [27], [28] to obtain global information. While these control methods effectively eliminate the voltage magnitude and frequency deviations, such communications increase the complexity and reduce reliability.

In summary, although many approaches have been proposed to address the obstacles faced by the traditional power droop control, few have figured out them all at once in a simple way. Therefore, a novel controller without the power loop is proposed in this paper, which comprises a DOB, a current feed-forward loop, a virtual complex impedance loop, and a synchronizer. The main contributions of this paper can be summarized as follows.

1) Proposing a unified impedance controller based on DOB, which not only eliminates the inherent output impedance by the current feed-forward loop, but also incorporates a virtual impedance loop to reconstructs the impedance in a sensorless way.
2) Developing a synchronization method to strictly synchronize the paralleled-VSIs only by using local measurements. In this method, each VSI operates at a constant frequency of 50 Hz, and the exit of any VSI will not affect the normal operation of other VSIs.

The rest of this paper is organized as follows: In Section II, the power flow of the parallel system is analyzed when the virtual complex impedances are applied. Section III proposes a novel DOB based controller with a universal parameter design method and system stability analysis. A synchronization method for VSIs operated in constant frequency is developed in Section IV. Simulations and experiments are conducted respectively in Section V and Section VI, to validate the effectiveness of the proposed control strategy. Finally, the conclusions are depicted in Section VII.

II. Power Flow Analysis of the Parallel System

The equivalent circuit diagram of paralleled-VSIs and single VSI are shown in Fig. 1 and Fig. 2, respectively. Where, $U_0\angle 0$ is the AC bus voltage, $Z_L\angle\theta_L$ is the load impedance, $U_i\angle\varphi_i$ and $U_j\angle\varphi_j$ are the no-load output voltages, $U_{oi}\angle\varphi_{oi}$ and $U_{oj}\angle\varphi_{oj}$ are the output voltages, $I_i\angle\varphi_{Ii}$ and $I_j\angle\varphi_{Ij}$ are the output currents, $Z_{oi}\angle\theta_{oi}$ and $Z_{oj}\angle\theta_{oj}$ are the inherent output impedances, $Z_{viri}\angle\theta_{viri} = R_{viri} + jX_{viri}$ and $Z_{virj}\angle\theta_{virj} = R_{virj} + jX_{virj}$ are the virtual impedances, $Z_{linei}\angle\theta_{linei} = R_{linei} + jX_{linei}$ and $Z_{linej}\angle\theta_{linej} = R_{linej} + jX_{linej}$ are the line impedances of VSI#*i* and VSI#*j*, respectively. The combined impedance $Z_i\angle\theta_i = R_i + jX_i$ is the sum of $Z_{oi}\angle\theta_{oi}$, $Z_{viri}\angle\theta_{viri}$, and $Z_{linei}\angle\theta_{linei}$.

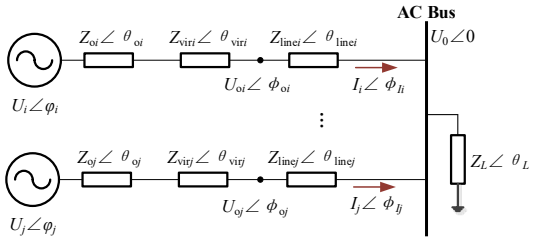


Fig.1. Equivalent circuit of paralleled VSIs.

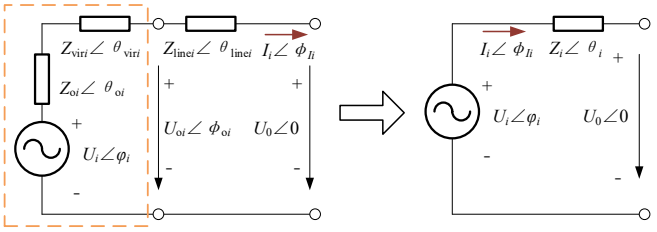


Fig.2. Equivalent circuit of single VSI.

According to Fig. 2, the active power P_i and reactive power Q_i provided by VSI$_i$ to the load can be obtained as

$$\begin{cases} P_i = \dfrac{U_i U_0}{Z_i}\cos(\theta_i - \varphi_i) - \dfrac{U_0^2}{Z_i}\cos\theta_i \\ Q_i = \dfrac{U_i U_0}{Z_i}\sin(\theta_i - \varphi_i) - \dfrac{U_0^2}{Z_i}\sin\theta_i \end{cases} . \quad (1)$$

Since $Z_i\angle\theta_i$ is very small relative to $Z_L\angle\theta_L$, we have $\sin\varphi_i \approx \varphi_i$, $\cos\varphi_i \approx 1$. Substitute them into (1), and we can get

$$\begin{cases} P_i = \dfrac{U_0}{Z_i}[(U_i - U_0)\cos\theta_i + U_i\varphi_i\sin\theta_i] \\ Q_i = \dfrac{U_0}{Z_i}[(U_i - U_0)\sin\theta_i - U_i\varphi_i\cos\theta_i] \end{cases} . \quad (2)$$

For the combined impedance $Z_i\angle\theta_i$, on the one hand, the inherent output impedance $Z_{oi}\angle\theta_{oi}$ is usually unknown and different that affected by plant and control parameters. Due to the harmonic injection and signal acquisition error, it is also difficult to accurately acquire the inherent output impedance. Therefore, the best way to eliminate the inherent output impedance deviations is to remove the inherent output impedance, which is realized through a DOB-based feed-forward control loop in this paper (discussed later in Section III). On the other hand, since the line impedance Z_{linei} is practically very small in low-scale systems, a larger R_{viri} becomes the predominant component of $Z_i\angle\theta_i$ [14]. However, a virtual complex impedance Z_{vir} composed of a virtual resistance R_{vir} and a virtual inductance L_{vir} is preferred when the line impedances can be accurately obtained. In this case, L_{vir} is designed to counteract the line inductance L_{line}, whereas R_{vir} is constructed to realize the power sharing between VSIs. Therefore, $Z_i\angle\theta_i$ will be determined only by the combined resistance R_i. Substitute $Z_i\angle\theta_i = R_i$ into equation (2), then we can present

$$\begin{cases} P_i = \dfrac{U_0}{R_i}(U_i - U_0) \\ Q_i = -\dfrac{U_i U_0}{R_i}\varphi_i \end{cases} . \quad (3)$$

For each VSI, U_0 is identical, and U_i can also be controlled to be equal. Therefore, according to (3), the output active power P_i of each VSI is inversely proportional to its combined resistance R_i. If the voltage phase φ_i of each VSI can be unified (discussed later in Section IV), then the output reactive power Q_i is also inversely proportional to the combined resistance R_i. Essentially, the proposed controller is based on *V-I* droop characteristic, designed to achieve proper power sharing between VSIs through voltage control, rather than power control [14], [21]-[25]. The droop characteristic is presented as $U_0 = U_i - I_i R_i$, since U_0 is identical and U_i can be controlled to be identical for each VSI, the output current I_i is inversely proportional to its combined resistance R_i. It also can be seen that the AC bus voltage U_0 varies with the load, due to inherent *V-I* droop characteristic. However, U_0 can be guaranteed by the proper design of R_i. Therefore, although the AC bus voltage U_0 varies with the load, it is within an acceptable range. Besides, the AC bus voltage fluctuation can be compensated through a secondary control, which ensures that the voltage deviation is regulated toward zero after every change of load or generation inside the microgrids [23]. This paper focuses on the primary controller designing, and the secondary layer control will be carried out in subsequent studies.

Fig.3 takes two VSIs as an example to further illustrate the principle that R_i affects the power distribution between VSIs. In Fig.3, curve 1 and curve 2 are the relationship curves between the output power and the voltage magnitudes of VSI#1 and VSI#2, respectively. The slopes of the curves represent the combined resistances. Since $U_1 = U_2$ can be easily realized by the voltage controller, if R_1:R_2=2:1, then we can get P_1:P_2=1:2. Similarly, if φ_1=φ_2 is achieved, then we have Q_1:Q_2=1:2. It is apparent that R_i determines the power sharing ratio of VSIs, which plays the role of the droop coefficient in traditional droop control.

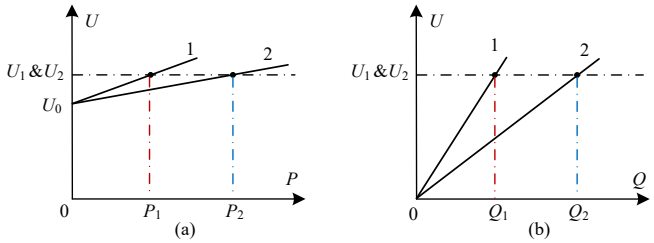


Fig.3. The effect of combined resistances on power sharing. (a) *P-U* curves. (b) *Q-U* curves.

In conclusion, the virtual complex impedance loop can not only reconstruct the impedances of VSIs, but also realizes the proper power sharing among VSIs under the 2 premises of 1) the output impedances of VSIs are suppressed and 2) the voltage phases of VSIs are synchronized. In the following Section III and Section IV, the DOB-based impedance controller and the synchronization method are proposed respectively to address the above two issues.

III. Proposed DOB-based Impedance Controller

A. Principles of the Proposed Impedance Controller

The detailed structure of a VSI connected to the AC bus is shown in Fig. 4. Where, L_f is the filter inductance, R_f is the resistance of the filter inductor, C_f is the filter capacitance, Z_{line} is the line impedance, u_{dc} denotes the DC voltage, u_{oabc} represents the output three-phase voltage, i_{labc} and i_{abc} are the inductor three-phase current and output three-phase current, respectively.

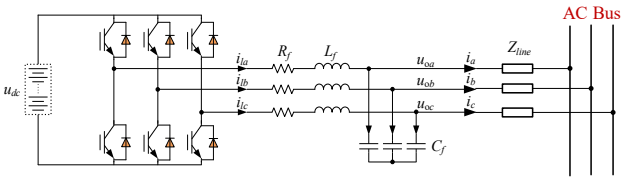


Fig. 4. Circuit diagram of VSI connected to the AC bus.

The frequency-domain simplified dual closed-loop controller presented in Fig. 5 is often used to control the VSI depicted in Fig.4. Where superscript * denotes the corresponding reference value, $K_I(s) = k_{pI} + k_{iI}/s$ and $K_U(s) = k_{pU} + k_{iU}/s$ are the

compensators of current loop and voltage loop respectively. The current loop is included in the generalized plant to facilitate the implementation of the subsequent disturbance observer.

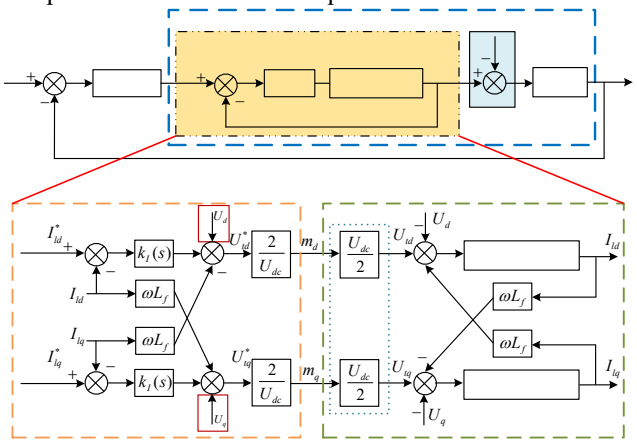


Fig. 5. Simplified traditional dual closed-loop controller.

According to Fig. 5, the transfer function of the inner current loop is obtained as

$$G_{cI}(s)=\frac{I_l}{I_l^*}=\frac{k_{pI}s+k_{iI}}{L_f s^2+(R_f+r_{on}+k_{pI})s+k_{iI}}. \tag{4}$$

Then the actual model and nominal model of the generalized plant are respectively presented as

$$\begin{cases} P(s)=G_{cI}(s)/(C_f s) \\ P_n(s)=G_{ncI}(s)/(C_{nf}s) \end{cases}. \tag{5}$$

Based on (4) and (5), the output voltage of VSI is given by

$$U_o=G(s)U^*-Z_o(s)I. \tag{6}$$

Being

$$\begin{cases} G(s)=\dfrac{K_U(s)P(s)}{1+K_U(s)P(s)} \\ Z_o(s)=\dfrac{1/(C_f s)}{1+K_U(s)P(s)} \end{cases}.$$

In this case, the output voltage U_o is not only determined by the reference voltage U^*, but also disturbed by the output current I. Namely, the VSI has an inherent output impedance $Z_o(s)$.

To suppress $Z_o(s)$ and achieve proper power sharing between VSIs, a unified controller is proposed in this section. This novel controller superimposes a DOB, a current feed-forward loop, and a virtual complex impedance loop on the traditional dual closed-loop, as shown in Fig.6. Where $\xi(s)$ denotes the external noise, $W(s)$ is an LPF, $G_{ncI}(s)$ and C_{nf} are the nominal models of the current loop and the filter capacitor respectively, I_f is the output current of DOB. According to Fig. 6, the observed current I_f and the output current $\tilde{I}$ has an intuitive relationship of $I_f=W(s)\tilde{I}$ (neglecting the external noise). In this way, the output current is estimated from the local variables, rather than measured by the current sensor. On the one hand, I_f is fed forward to the output of voltage compensator. On the other hand, I_f is introduced into the virtual complex impedance loop. The virtual impedance Z_{vir} is actually a larger resistance R_{vir}. However, Z_{vir} can also be composed of a virtual resistance R_{vir} and a virtual inductance L_{vir} when the line impedances can be accurately obtained. In this case, L_{vir} is designed to counteract the line inductance L_{line}, whereas R_{vir} is constructed to realize the power sharing between VSIs. Since $G_{cI}(s)\approx 1$, the equivalent disturbance current $\tilde{I}=G_{cI}^{-1}(s)I$ is used to replace the output current I to make the DOB available [18]. According to (4) and (5), the generalized plant is a second-order system, so $W(s)$ can be selected as [19]

$$W(s)=\frac{1}{(\tau_f s+1)^2}=\frac{1}{(\tau_f s)^2+2\tau_f s+1}. \tag{7}$$

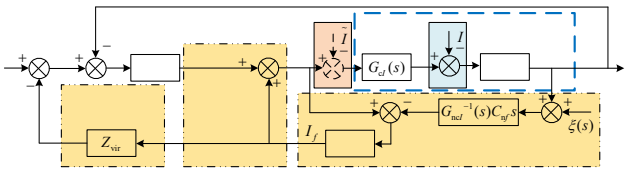


Fig. 6. Block diagram of the proposed impedance controller.

From Fig.6, the output voltage U_o in the proposed controller can be obtained as

$$U_o=G'(s)U^*-Z_o'(s)\tilde{I}-G'(s)Z_{vir}\tilde{I}+O(s)\xi(s). \tag{8}$$

Being

$$\begin{cases} G'(s)=\dfrac{K_U(s)P(s)P_n(s)}{W(s)[P(s)-P_n(s)]+P_n(s)[1+K_U(s)P(s)]+W(s)K_U(s)Z_{vir}[P(s)-P_n(s)]} \\ Z_o'(s)=\dfrac{P(s)P_n(s)[1-W(s)]}{W(s)[P(s)-P_n(s)]+P_n(s)[1+K_U(s)P(s)]+W(s)K_U(s)Z_{vir}[P(s)-P_n(s)]} \\ O(s)=\dfrac{P(s)W(s)[K_U(s)Z_{vir}-1]}{W(s)[P(s)-P_n(s)]+P_n(s)[1+K_U(s)P(s)]+W(s)K_U(s)Z_{vir}[P(s)-P_n(s)]} \end{cases}.$$

If the model is completely accurate, i.e., $P_n(s)=P(s)$, then (8) is simplified as

$$U_o=G'(s)U^*-Z_o'(s)\tilde{I}-G'(s)Z_{vir}\tilde{I}+O(s)\xi(s). \tag{9}$$

Being

$$\begin{cases} G'(s)=\dfrac{K_U(s)P(s)}{1+K_U(s)P(s)} \\ Z_o'(s)=\dfrac{P(s)[1-W(s)]}{1+K_U(s)P(s)} \\ O(s)=\dfrac{W(s)[K_U(s)Z_{vir}-1]}{[1+K_U(s)P(s)]} \end{cases}.$$

Observing (6) and (9) the following conclusions can be drawn.

1) The proposed controller has the same voltage transfer function as the traditional dual-loop controller, that is, $G'(s)=G(s)$.
2) Since $W(s)$ is designed as an LPF, we have $W(s)=1$ in the low-frequency region. In this case, the output impedance with low-frequency is eliminated, i.e., $Z_o'(s)=0$. Whereas, in the high-frequency region, we have $W(s)=0$. The high-frequency noise is also suppressed, i.e., $O(s)=0$.
3) The value of virtual impedance is $G'(s)Z_{vir}$ in the proposed controller, which is consistent with the principle of the traditional virtual impedance method.
4) $Z_o'(s)$ and $G'(s)Z_{vir}$ are independent of each other, which satisfies the two-degree-of-freedom (2-DOF) algorithm. Therefore, the feed-forward loop and the virtual

complex impedance loop can be designed separately.

B. Design of Parameters

1) Design of Current and Voltage Compensators

According to [29], the formulas to calculate the compensator parameters in the current loop are given as

$$k_{pI} = L_f / \tau_i \,, \tag{10}$$

$$k_{iI} = R_f / \tau_i \,. \tag{11}$$

Where τ_i is the time constant of the current loop, which should be small enough to improve the fast response-ability of the current loop, while large enough to ensure that the bandwidth $1/\tau_i$ is less than the switching angular frequency of the inverter.

In addition, the compensator parameters and the gain cutoff frequency of the voltage loop are obtained by the following formulas [30] as

$$k_{pU} = \frac{C_f}{\tau_i}\left(\frac{1-\sin\gamma}{1+\sin\gamma}\right)^{\frac{1}{2}}, \tag{12}$$

$$k_{iU} = \frac{C_f}{\tau_i^2}\left(\frac{1-\sin\gamma}{1+\sin\gamma}\right)^{\frac{3}{2}}, \tag{13}$$

$$\omega_c = \sqrt{(k_{iU}/k_{pU})\tau_i^{-1}} \,. \tag{14}$$

Where the phase margin γ is typically chosen as 40 ~ 50 degrees, and ω_c is the gain cutoff frequency of the open-loop voltage transfer function.

2) Design of the LPF

To ensure the effective and stable operation of the proposed controller, the design of the LPF should at least satisfy the following two requirements.

1) The bandwidth of LPF should be large enough to allow the output current to pass through, i.e., $\omega_b > \omega_d$. Where ω_b is the bandwidth of LPF, ω_d is the angular frequency of the output current disturbance. In the steady-state case, we have $\omega_d = 0$ in the *dq* rotation coordinates.
2) Besides, ω_b should be small enough to reject the high-frequency noise, while ensuring that the introduction of DOB does not decrease the stability margin of the voltage loop. Namely, $\omega_b < \min\{\omega_n, \omega_c\}$ should be satisfied, where ω_n is the angular frequency of noise disturbance.

In order to let through the observed current, while ensuring good noise filtering ability and stability, it is advisable to

$$10\omega_d < \omega_b < \frac{1}{10}\min\{\omega_n, \omega_c\} \,. \tag{15}$$

According to (7), the bandwidth of the LPF is

$$\omega_b = (\sqrt{2}-1)^{1/2}\frac{1}{\tau_f} \,. \tag{16}$$

Substitute it into (15), and the selection range of time constant τ_f can be presented as

$$(\sqrt{2}-1)^{1/2}\max\left\{\frac{10}{\omega_n}, \frac{10}{\omega_c}\right\} < \tau_f < (\sqrt{2}-1)^{1/2}\frac{1}{10\omega_d} \,. \tag{17}$$

The value of τ_f should be kept as small as possible under the premise of satisfying (17), to achieve fast-tracking of output current during load mutation and improve the dynamic performance of the system. It is noted that the noise disturbance varies with different conditions, so it should be suppressed by tuning τ_f according to experimental results.

3) Design of the Combined Resistance

A larger R_i will improve the power sharing accuracy, whereas it will cause a larger magnitude deviation of the AC bus voltage. Therefore, the value of R_i should be restricted by the voltage quality requirement of the AC bus. According to Fig. 2, when $Z_i\angle\theta_i = R_i$, only if $\varphi_i = \varphi_{li}$, the AC bus voltage has a minimum magnitude of U^*-I_iR_i. In this case, R_i can be selected as:

$$R_i \le \frac{U^* - U_{0\min}}{I_{i\max}} \tag{18}$$

Where $U_{0\min}$ is the minimum magnitude permitted by AC bus voltage, $I_{i\max}$ is the maximum output current of VSI#*i*. $U^* = 1.03U_N$ and $U_{0\min} = 0.97U_N$ are adopted in this paper, which conforms to IEEE std. 1547−2003 [31].

C. Sensitivity and Stability Analysis

The related circuit parameters and the calculated control parameters are shown in Table I.

1) Sensitivity Analysis of Output Impedance to Plant Parameters

According to (5), model parameters, especially the filter capacitance C_f, will be offset due to heating or aging. Therefore, the sensitivity of inherent output impedance to filter capacitance C_f is investigated. When the traditional dual closed-loop controller is adopted, according to (6), the log sensitivity of inherent output impedance $Z_o(s)$ to filter capacitance C_f is presented as

$$\left.\frac{\partial \ln Z_o(s)}{\partial \ln C_f}\right|_{C_f = C_{nf}} = \frac{-1}{1 + H(s)P_n(s)} \,. \tag{19}$$

When the proposed controller is applied, according to (9), the log sensitivity of inherent output impedance $Z_o'(s)$ to filter capacitance C_f is presented as

$$\left.\frac{\partial \ln Z_o'(s)}{\partial \ln C_f}\right|_{C_f = C_{nf}} = \frac{[W(s)-1]}{[1 + H(s)P_n(s)]s} \,. \tag{20}$$

Based on (19) and (20), the sensitivities of output impedance to filter capacitance without DOB and with DOB are depicted in Fig. 7(a). It can be seen from Fig. 7(a) that in the low-frequency domain, the output impedance is insensitive to filter capacitance C_f with or without DOB, and the sensitivity is even less with DOB than without DOB. Actually, this result is obvious from the parameter sensitivity perspective, which claims that if the gain of the open-loop transfer function is large enough, the control system will be insensitive to the parameters in the feed-forward path of the loop. Similarly, the precision of another variable $G_{cI}(s)$ in (5) will not affect the output impedance, since $G_{cI}(s)$ is also in the feed-forward path of the loop.

2) The Impact of DOB on System Stability

Based on the controller presented in Fig. 6 and the parameters given in Table I, the characteristics of the open-loop voltage transfer functions with or without DOB are depicted in Fig. 7(b). Compared with the case without DOB, the low-frequency gain of the open-loop voltage transfer function becomes larger when DOB is augmented, indicating that the proposed control strategy has stronger voltage tracking capability. Meanwhile, it is also confirmed that the system stability would not deteriorate

when τ_f =5 ms, since the phase margin maintains at 45°. Whereas, the phase margin diminishes to 18° when τ_f=5 ms. In fact, as long as $\tau_f > (\sqrt{2}-1)^{1/2} \cdot 10/\omega_c = 3.11$ ms, according to (17), the introduction of DOB will not reduce the phase margin of the original dual-loop controller. Besides, when τ_f=5 ms, it can be calculated by (16) that the bandwidth of the LPF in DOB is 128.72 rad /s, which is much higher than the typical bandwidth of the LPF in the traditional power droop control loop of 30 rad/s [32]. That is to say, although the proposed controller introduces an LPF, it still has a better dynamic performance than the traditional droop control.

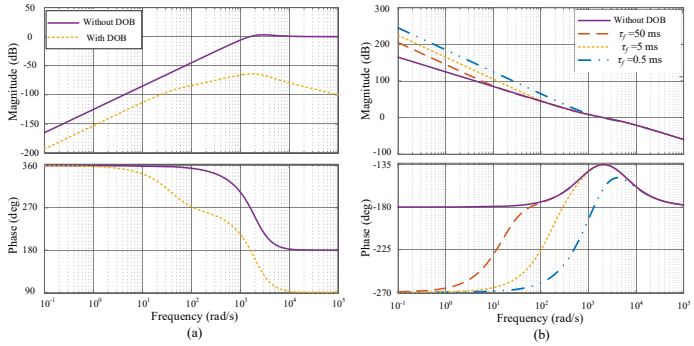


Fig. 7. The bode plots. (a) The sensitivity of inherent output impedance to filter capacitance. (b) The open-loop voltage transfer function.

3) The Impact of Virtual Impedance Loop on System Stability

The stability of the proposed controller with the variations of the parameters is further analyzed. Fig. 8(a) and Fig. 8(b) respectively present the root locus plots considering a variation of the virtual resistance R_{vir}∈[-10 Ω, 10 Ω] and the virtual inductance L_{vir}∈[-10 mH, 10 mH]. Notice that this system has six roots: two conjugated poles and four real poles. Since in both cases the poles remain in the left half *s*-plane, the system endows superior stability in the range of concern.

The robustness of the system under the perturbation of the plant parameter is also investigated. According to (5), the capacitance C_f is the dominant component of the generalized plant $P(s)$. Therefore, the root locus of the system is depicted in Fig. 8(c) considering C_f perturbs from $0.1C_{nf}$ to $2C_{nf}$, namely C_f∈[0.9 uF, 18 uF]. It can be noted that the poles also remain in the left half *s*-plane during the perturbation of C_f, the proposed controller possesses excellent robustness.

IV. Proposed Synchronization Method

A. Principle of the Proposed Synchronization Method

According to the analysis conducted in Section II, the accurate reactive power sharing also requires that the voltage phase of each VSI is the same. The traditional PLL adopts a master VSI to offer a fixed reference phase angle. However,

TABLE I. System parameters

Circuit parameters	Value	Control parameters	Value
Rated capacity S	10 kVA	Time constant of current loop τ_i	0.2 ms
DC voltage U_{dc}	800 V	Current proportional term k_{pI}	2.7
Rated AC voltage U_N	380 V	Current integral term k_{iI}	391.25
Voltage reference U^*	391 V	Voltage proportional term k_{pU}	0.0186
Rated frequency f^*	50 Hz	Voltage integral term k_{iU}	15.99
Switch frequency f_s	10 kHz	Phase margin of voltage loop γ	45°
Filter resistance R_f	78.25 mΩ	Cutoff frequency ω_c	2066.7 rad/s
Filter inductance L_f	0.54 mH	Time constant of LPF τ_f	5 ms
Filter capacitance C_f	9 uF	Virtual#1 impedance Z_{vir1}	2 Ω
Line#1 impedance Z_{line1}	(0.2 + j0.17) Ω	Virtual#2 impedance Z_{vir2}	2 Ω
Line#2 impedance Z_{line2}	0.1 Ω	AC bus voltage sampling frequency f_{sa}	1 kHz
Load#1 impedance Z_{load1}	60 Ω	Initial phase difference $\Delta\varphi_{20}$	50°
Load#2 impedance Z_{load2}	(32 + j16.5) Ω	The synchronization resistance R_{max}	28 Ω

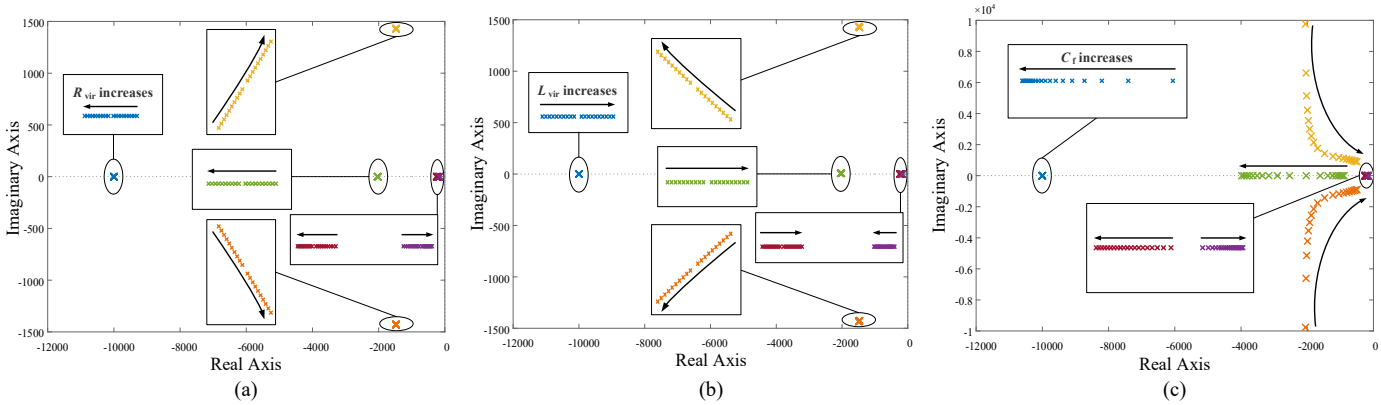


Fig. 8. The system root locus. (a) At L_{vir}=-1 mH, R_{vir}∈[-10 Ω, 10 Ω]. (b) At R_{vir} =1 Ω, L_{vir}∈[-10 mH, 10 mH]. (c) At R_{vir} =1 Ω, L_{vir}=-1 mH, C_f∈[0.1C_{nf}, 2C_{nf}].

due to the dispersion of VSIs, each slave VSI can only synchronize to the AC bus, rather than the master VSI. In this case, the phase of each slave VSI is unable to be equalized to the phase of the master VSI. To tackle this problem, a new synchronization method is proposed, which can precisely synchronize the VSIs. In the proposed method, each VSI has equal status and operates at a constant frequency of 50 Hz.

The schematic diagram of a VSI connecting to a multi-VSIs system is shown in Fig. 9, in which R_L and L_L are load resistance and load inductance respectively. According to Thevenin's theorem, the synchronized VSIs are equivalent to a single VSI#1, while VSI#2 represents the VSI to be connected. Since the synchronized VSIs have the same voltage, it is easy to know that $\dot{U}_1=\dot{U}_3=\dot{U}_4=\cdots=\dot{U}_n$, and $R_1=R_3//R_4//\cdots//R_n$. Therefore, the 2-VSI system based analysis can also be applied to the case where a VSI is connected to a multi-VSI system.

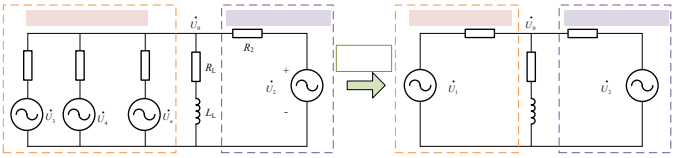


Fig.9. Schematic diagram of the paralleled-VSIs. (a) VSI#2 is connected to a multi-VSI system. (b) VSI#2 is connected to an equivalent VSI.

By using the superposition theorem, the relationship between the AC bus voltage and the output voltages is formulated as

$$\dot{U}_0=\frac{(R_L+j\omega L_L)R_2}{R_1[(R_L+j\omega L_L)+R_2]+(R_L+j\omega L_L)R_2}\dot{U}_1+\frac{(R_L+j\omega L_L)R_1}{R_2[(R_L+j\omega L_L)+R_1]+(R_L+j\omega L_L)R_1}\dot{U}_2 . \quad (21)$$

Since $R_1 \cdot R_2$ is very small relative to $R_1 \cdot (R_L+j\omega L_L)$ and $R_2 \cdot (R_L+j\omega L_L)$, it can be ignored in (21). Assume the power sharing ratio of VSI#1 and VSI#2 is n:1, i.e., $nR_1 = R_2$. Substitute it into (21), and we can get

$$\dot{U}_0=\frac{R_2}{R_1+R_2}\dot{U}_1+\frac{R_1}{R_1+R_2}\dot{U}_2=\frac{n}{n+1}\dot{U}_1+\frac{1}{n+1}\dot{U}_2 . \quad (22)$$

Since $U_1= U_2=U^*$, (22) is further derived as

$$U_0=U^*\sqrt{\frac{1+n^2+2n\cos(\varphi_2-\varphi_1)}{(n+1)^2}} . \quad (23)$$

Due to R_1 is very small relative to $(R_L+j\omega L_L)$, we have $\varphi_1 \approx \varphi_0$. Let $\Delta\varphi_{20}=\varphi_2-\varphi_0$ is the phase difference between VSI#2 and the AC bus, then we have $\Delta\varphi_{20} \approx \varphi_2-\varphi_1$. Substitute it into (23), and U_0 is presented as

$$U_0=U^*\sqrt{\frac{1+n^2+2n\cos\Delta\varphi_{20}}{(n+1)^2}} . \quad (24)$$

Firstly, the maximum value of $\Delta\varphi_{20}$ is derived based on (24). Since

$$\frac{1+n^2+2n\cos\Delta\varphi_{20}}{(n+1)^2} \geq \frac{1+\cos\Delta\varphi_{20}}{2} . \quad (25)$$

Substitute (25) into (24), and we can get

$$U_0 \geq U^*\sqrt{\frac{1+\cos\Delta\varphi_{20}}{2}} . \quad (26)$$

According to [31], the allowable deviation of the AC bus voltage is ±7%. Therefore, let $U_0 \geq 0.93U_N$ and substitute $U^*=1.03U_N$ into (26), then the range of $\Delta\varphi_{20}$ is demonstrated as

$$\Delta\varphi_{20} \leq 50.91^\circ . \quad (27)$$

Equations (26) and (27) indicate that if the phase difference between the newly connected VSI#2 and the AC bus is smaller than 50.91°, the AC bus voltage will maintain above $0.93U_N$ after VSI#2 is joined.

Besides, the circulating current and AC bus voltage are investigated after VSI#2 is put in with a phase difference of $\Delta\varphi_{20}=50^\circ$. In this case, the circulating current is significant if two VSIs are paralleled through a small resistance. To tackle this problem, a large virtual resistance R_{max} is adopted during the synchronization process. However, the large resistance R_{max} also affects the AC bus voltage, which may lead to maloperation of the synchronization control. According to (18), in the normal operating condition, $U_0 \geq 0.97U_N$ is guaranteed by the proper design of R_i. Therefore, U_0 should drop below $0.97U_N$ when VSI#2 is connected. In this way, the normal operating condition and the VSI#2 connecting condition are distinguished. The influences of R_{max} on both circulating current and AC bus voltage are further explored, then the value range of R_{max} is presented.

Based on the aforementioned, when VSI#2 is connected with a phase angle difference of $\Delta\varphi_{20}$, the following two requirements must be satisfied to make it practical.

1) The arm currents of each VSI will not trigger the blocking of IGBTs. In other words, the output current of each VSI must in a reasonable range (2 pu current threshold is typical [33], [34], for a 10kVA/380V VSI, the pu current is 21.4 A). To leave a certain margin, a 1.5 pu current threshold is selected in this paper. It means that the circulating current must be limited within 0.5 pu (10.7 A) when a large resistance R_{max} is applied.
2) The AC bus voltage U_0 must be maintained in the range of [$0.93U_N$, $0.97U_N$), i.e., [289.23 V, 301.67 V), to accurately trigger the synchronization actions.

The circulating current and the AC bus voltage are depicted in Fig. 10 when R_{max} goes from 1 Ω to 50 Ω. It can be seen that when R_{max} is in the dotted range of [21 Ω, 36 Ω], the circulating current and the AC bus voltage are both of the desired range. In this paper, a moderate value of R_{max} =28 Ω is selected.

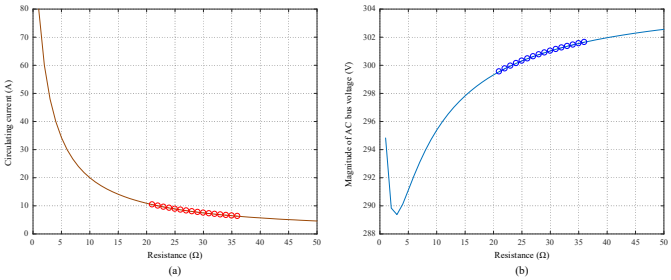


Fig. 10 The circulating current and the AC bus voltage at $R_{max} \in$[1 Ω, 50 Ω]. (a) The circulating current. (b) The magnitude of the AC bus voltage.

B. Proposed Synchronization Control

According to the previous theoretical analysis, a new synchronization method is proposed for VSIs. The action flow

of the proposed method is shown in Fig. 11, in which each VSI operates at a constant frequency of 50 Hz. The phase difference between the new VSI and the AC bus voltage is initially set as $\Delta\varphi_{i0}=50^{\circ}$ and the virtual resistance is selected as $R_{viri}= R_{max}$ when the new VSI is connecting. In this case, U_0 will drop to a range of [$0.93U_N$, $0.97U_N$) and the circulating current is acceptable. If $U_0\in$[$0.93U_N$, $0.97U_N$) is detected within 20 ms continuously, that is, within 20 sampling cycles when the sampling frequency f_{sa} is set as 1 kHz, the temporary disturbances are excluded and it is considered that a new VSI has been connected. Then each VSI collects the phase angle of the AC bus voltage and calculates its new phase difference $\Delta\varphi_i=\varphi_i - \varphi_0$. To ensure that all VSIs have collected their phase differences, another 20 ms delay is augmented. After that, each VSI updates its reference phase to $\varphi_i = \varphi_i - \Delta\varphi_i$ and resets its virtual resistance to achieve the proper power sharing. Thus, the synchronization of each VSI is realized. Although the voltage phases of VSIs and AC bus are time-varying, the phase difference $\Delta\varphi_i$ is a fixed value under the same steady-state. Therefore, the proposed method does not require the simultaneous sampling for the phase of the AC bus voltage, nor need to carry out the synchronous actions at the same time of each VSI.

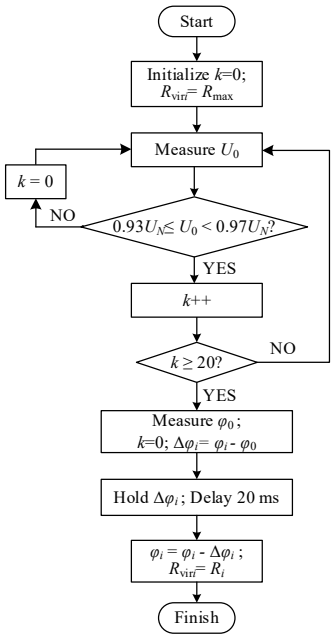


Fig.11. Flow chart of the synchronization actions.

Note that the above analysis gives an optimal synchronization scheme when a new VSI is connecting to the system. However, during the synchronization process, the values of the phase angle difference $\Delta\varphi_{20}$ and the virtual resistance R_{max} are preferred but not mandatory. If $U_0\in$[$0.93U_N$, $0.97U_N$) is not satisfied with the recommend scheme due to large parameters variations, VSI#2 can adjust its $\Delta\varphi_{20}$ and R_{max} to make $U_0\in$[$0.93U_N$, $0.97U_N$). This is practical since U_0 can be measured in real time, while $\Delta\varphi_{20}$ and R_{max} are control parameters that can be easily modified. After the new VSI has been synchronized to the system, the accidental false triggers only increase the synchronous actions, and will not affect the normal operation of the system.

Compared with the PLL-based synchronization method presented in [14], the advantages of this proposed synchronization method include:

1) It can truly realize the synchronization of each VSI, to ensure the accurate sharing of reactive power.
2) The exit of any VSI will not affect the normal operation of other VSIs, so the reliability of the system is improved.
3) Each VSI operates at a constant frequency of 50 Hz, which eliminates the inherent frequency deviation.

However, it also possesses a flaw. Since this synchronization is only a one-time operation, regular synchronization is required. Even so, the proposed method has strong practicability, because regular calibration is commonly adopted in engineering. The accidental false triggers caused by disturbances can even be considered as phase calibrations in the proposed synchronization method. Besides, the event-triggered-based strategies can significantly relax the requirement for precise real-time information transmission and have been widely adopted [35], [36].

V. Simulation Results

To verify the effectiveness of the proposed scheme, a detailed paralleled-2-VSI system is developed in the professional software PSCAD/EMTDC. Both VSIs adopt the proposed DOB-based controller shown in Fig.6 and the synchronization method illustrated in Fig.10. The circuit parameters and control parameters are listed in Table I. Firstly, the performance of the DOB-based feed-forward loop is studied. Then, the effectiveness of the synchronization method is validated. Finally, the current sharing performance is simulated under different scenarios.

A. Performance of Output Impedance Suppression

Firstly, VSI#1 is simulated to validate the effectiveness of the DOB-based current feed-forward loop, in which the virtual impedance Z_{vir1} is set as 0. The simulation starts with VSI#1 operates in no-load circumstance. Then load#1 (Z_{load1} = 60 Ω) is put in at t= 0.2 s and cut off at t= 0.35 s.

Fig. 12 and Fig. 13 respectively present the simulation results with the traditional dual closed-loop controller shown in Fig.5 and with the proposed DOB-based current feed-forward controller presented in Fig.6. With the traditional controller, the magnitude of the output line-to-line voltage drops to about 520 V when load#1 is suddenly put in, and resumes to 537 V after load#1 is removed. The output voltage is affected by the output current, which indicates that the VSI has an inherent output impedance. By contrast, when the proposed controller is applied, the DOB output current I_{fa} enables fast and accurate tracking of the VSI output current I_a. Hence, the output voltage offset is compensated by the feed-forward loop and the output voltage is maintained at 537 V in the steady-state. It can be concluded that the inherent output impedance of the VSI is obviously suppressed by the proposed DOB-based current feed-forward loop.

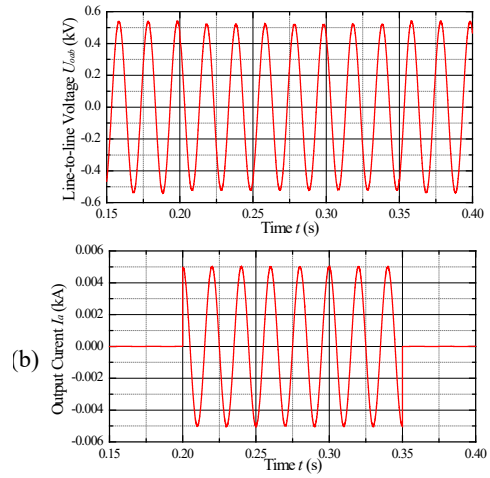


Fig. 12. Simulation waveforms of traditional dual-loop control. (a) The output voltage of VSI#1. (b) The output current of VSI#1.

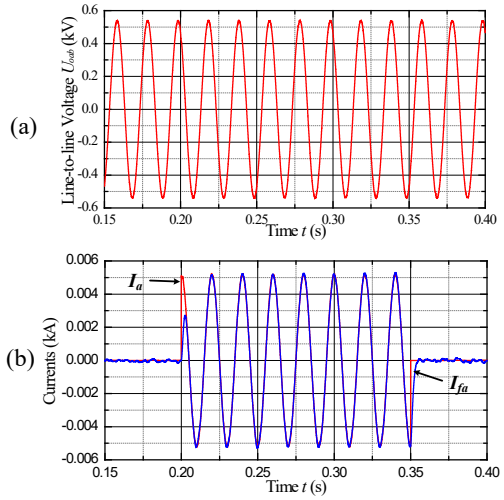


Fig. 13. Simulation waveforms of the proposed feed-forward control. (a) The output voltage of VSI#1. (b) The output current of VSI#1 and the observed current of DOB.

B. *Performance of the Proposed Synchronization Method*

Fig. 14 illustrates the waveforms during the synchronization process. Initially, VSI#1 is connected to load#2 (Z_{load2} = 32 Ω+52.7 mH), while VSI#2 is disconnected. At t = 0.4 s, VSI#2 is connected with a phase difference $\Delta\varphi_{20} = 50^{\circ}$, resulting in the magnitude of AC bus voltage drops from 540V to about 500V, as shown in Fig. 14(b). At t = 0.42s, when the voltage drop is confirmed, VSI#1 and VSI #2 collect the AC bus voltage phase and calculate the phase differences between them and the AC bus respectively. Finally, at t = 0.44s, VSI#1 and VSI#2 achieve synchronization by subtracting the phase differences from their reference phases, as depicted in Fig. 14(a). In this case, the magnitude of AC bus voltage also increases from 500 V to about 540 V. Fig. 14 (c) and Fig. 14 (d) present the direct and quadrature currents output by VSI #1 and VSI #2 during the synchronization process. As can be seen from Fig. 14 (c), the direct current is not evenly shared when VSI #2 is connected at t = 0.4 s, which is caused by the large virtual resistance R_{vir2}= R_{max}. However, proper sharing is achieved when the virtual resistance is reset to the original value. Similarly, the quadrature current is accurately distributed only after the synchronization is completed. It is noted that the quadrature circulating current caused by the phase differences of VSI#1 and VSI #2 between t = 0.4 s and t = 0.44 s is also in an acceptable range, thanks to the increasing of the virtual resistance to the maximum value R_{vir2}= R_{max}. After the synchronization is realized, i.e., after t = 0.44 s, the virtual resistance is reset to achieve the proper sharing of current.

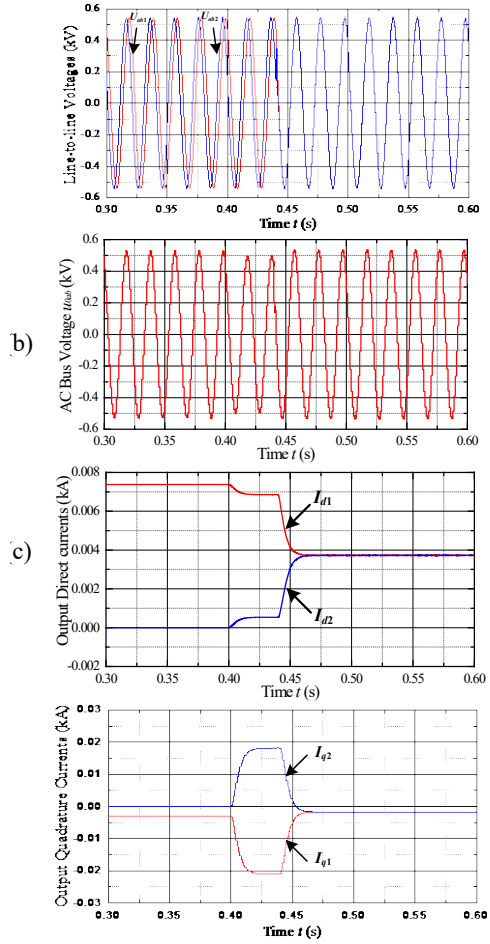


Fig. 14. Simulation waveforms of the proposed synchronization method. (a) The no-load output voltages. (b) The AC bus voltage. (c) The output direct currents. (d) The output quadrature currents.

C. *Performance of Current Sharing*

1) *With the Traditional PLL*

The simulation results are demonstrated in Fig. 15 when the traditional PLL is adopted to synchronize the VSIs. During the whole simulation process, VSI#1 operates at a constant frequency of 50Hz, and VSI#2 synchronizes to the AC bus through a traditional PLL presented in [37]. Initially, VSI#1 is connected to load#2 (Z_{load2} = 32 + j16.5 Ω), while VSI#2 is disconnected. However, at t = 0.4 s, VSI#2 is connected to the AC bus. As can be seen from Fig. 15 (b) and Fig. 15(c), although the direct current is evenly shared and the smooth transition is achieved when VSI #2 is connected, the quadrature current can not be accurately distributed. The reason is that VSI#2 can only synchronize to the AC bus, rather than the master VSI#1. Therefore, VSI#1 affords the whole quadrature current of load. Besides, due to the phase differences of VSI#1 and VSI #2, an additional circulating quadrature current is

required for VSI#1 to supply VSI#2. At t = 0.8 s, VSI#1 (the master VSI) is disconnected due to failures or maintenances, while VSI#2 still tracks the phase of the AC bus voltage. Since the AC bus voltage is generated by VSI#2 itself and the phase of AC bus voltage is always ahead of the phase of VSI#2 under inductive loads, a positive feedback mechanism is formed. Therefore, the system frequency eventually reaches the upper limit of the PLL (selected as 55Hz), which is clearly revealed in Fig. 15(a) and Fig. 15(d). In conclusion, when the traditional PLL is adopted, not only the accurate sharing of reactive current cannot be realized, but also the system will turn to abnormal operation when the master VSI exits.

2) With the Proposed Controller

Different scenarios have been simulated to test the current sharing performances of the proposed controller, including the scenario of load changes, the scenario of current sharing ratio changes, and the scenario of VSI #1 exit.

Fig. 16(a.1) and Fig. 16(a.2) show the transient response during the load changes. In the beginning, VSI#1 and VSI#2 are on parallel operation with the same power rates to supply load#1. At t = 0.4 s, load#2 is connected to the AC bus. The direct currents and quadrature currents output by VSI #1 and VSI #2 both increase to 6.2 A and -1.8 A immediately to supply the needed current, as shown in Fig. 16(a.1) and Fig. 16(a.2). Finally, at t = 0.6 s, when load#2 is disconnected, the output currents of VSI#1 and VSI#2 restore to the original value.

Fig. 16(b.1) and Fig. 16(b.2) exhibit the transient response during current sharing ratio changes of VSI#1 and VSI#2. In the beginning, VSI #1 and VSI #2 are on parallel operation with the same power rates to supply load#1 and load#2. Both output currents of VSI #1 and VSI #2 are approximately 6.2 A of direct current and -1.8 A of quadrature current. At t = 1.0 s, the current sharing ratio has been suddenly changed from 1:1 to 2:1. As illustrated in Fig. 16(b.1) and Fig. 16(b.2), the output currents of VSI#1 and VSI#2 are immediately shifted to the new sharing ratio. This is, the direct current and quadrature current of VSI #1 change to 8.2 A and -2.4 A, while the direct current and quadrature current of VSI #2 change to 4.1 A and -1.2 A respectively. Finally, when the current sharing ratio is changed

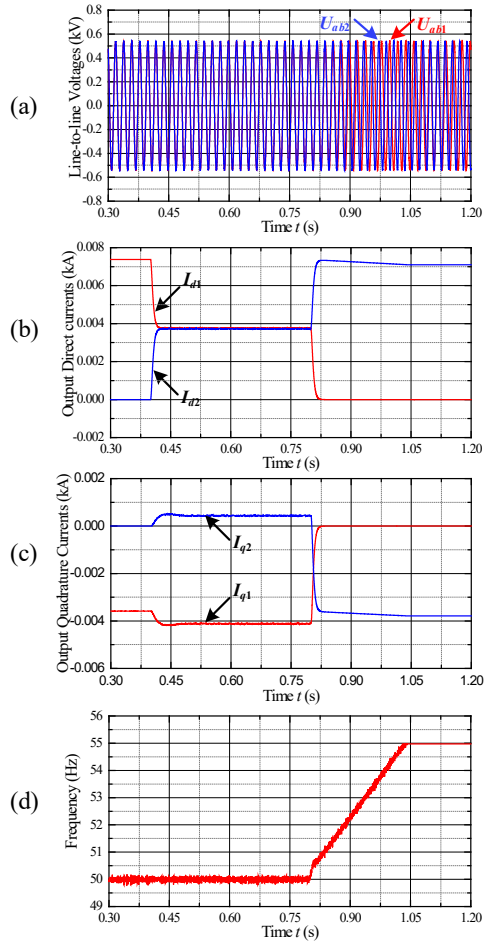


Fig. 15. Simulation waveforms with the traditional PLL. (a) The no-load output voltages. (b) The output direct currents. (c) The output quadrature currents. (d) The frequency of the AC bus voltage.

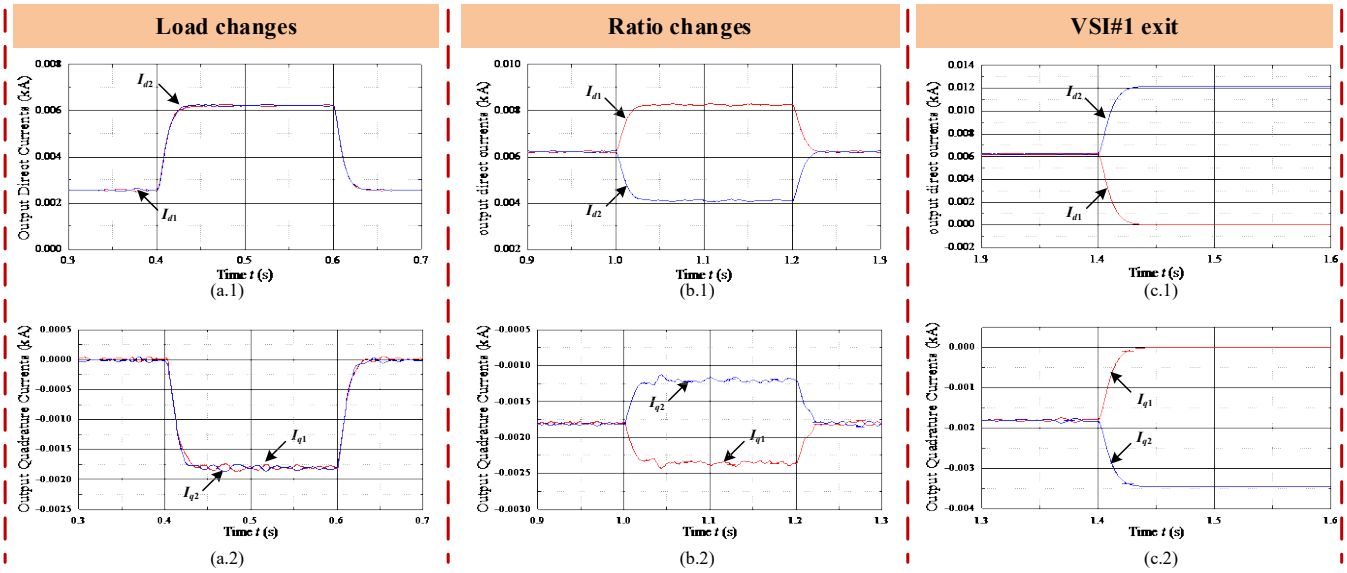


Fig. 16. Simulation results of the current sharing performance in different scenarios. (a.1) The output direct currents in the load changes scenario. (a.2) The output quadrature currents in the load changes scenario. (b.1) The output direct currents in the ratio changes scenario. (b.2) The output quadrature currents in the ratio changes scenario. (c.1) The output direct currents in the VSI #1 exit scenario. (c.2) The output quadrature currents in the VSI #1 exit scenario.

back to 1:1 at t = 1.2 s, the output currents of VSI#1 and VSI#2 restore to the original value.

Fig. 16(c.1) and Fig. 16(c.2) present the transient response during the disconnecting of VSI #1. In the beginning, VSI #1 and VSI #2 are on parallel operation with the same power rates to supply load#1 and load#2. Both VSI #1 and VSI #2 feeds are approximately 6.2 A of direct current and -1.8 A of quadrature current. However, at t = 1.4 s, VSI #1 is disconnected from the AC bus. As depicted in Fig. 16(c.1) and Fig. 16(c.2), the output currents of VSI #2 increase to 12.2 A and -3.5 A respectively to supply the total current.

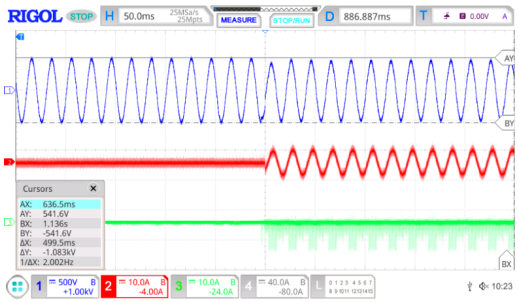
Compared with the traditional PLL method, the proposed synchronization method can achieve the accurate current sharing of VSIs after the synchronization. Besides, with the proposed method, the exit of any VSI does not affect the normal operation of the whole parallel system, since each VSI operates with a constant frequency of 50Hz independently.

VI. Experimental Results

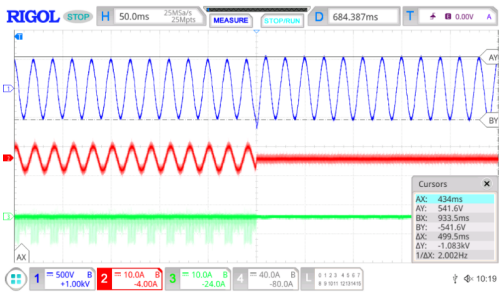
To further validate the effectiveness of the proposed controller, an experimental platform with 2 paralleled-VSIs has also been built based on TI's TMS320F28335. The scenarios and experimental parameters are the same as those in the simulations.

A. Performance of Output Impedance Suppression

In this scenario, the inherent output impedance of VSI is investigated in the presence of load switching. In order to validate the superiority, the experimental results with the proposed DOB-based current feed-forward controller are compared with that of the traditional dual closed-loop controller. Fig. 17 shows the waveforms of the traditional controller, while Fig. 18 depicts the waveforms of the proposed controller. It can be observed from Fig. 17(a) that when load#1 is suddenly connected, the magnitude of the output line-to-line voltage drops from 537 V to around 520 V. Meanwhile, the magnitude of the output line-to-line voltage increases from 520 V to 537 V when load#1 is disconnected, as shown in Fig. 17(b). The VSI has an inherent output impedance when the traditional dual closed-loop controller is adopted. However, when the proposed controller is applied, the output current of VSI is observed by DOB and is feed-forwarded to the export of the voltage compensator. Hence, the output voltage is maintained at 537 V in the steady-state whether with or without load, as shown in Fig. 18. The experimental results are highly consistent with the simulation results.

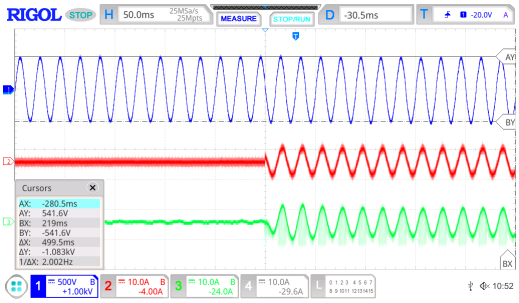


(a)

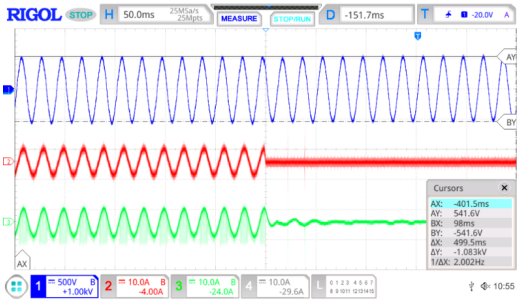


(b)

Fig. 17. Experimental waveforms of traditional dual-loop control. (a) The connection of load# 1. (b) The disconnection of load# 1. CH1, VSI output line-to-line voltage: 500 V/div; CH2, VSI output current: 10 A/div; CH3, DOB output current: 10 A/div.



(a)



(b)

Fig. 18. Experimental waveforms of the proposed feed-forward control. (a) The connection of load# 1. (b) The disconnection of load#1. CH1, VSI output line-to-line voltage: 500 V/div; CH2, VSI output current: 10 A/div; CH3, DOB output current: 10 A/div.

B. Performance of the Proposed Synchronization Method

In this scenario, the effectiveness of the proposed synchronization method is researched. Like in the simulations, VSI#1 is initially connected to load#2, while VSI#2 is disconnected. Then, VSI#2 is put in with a phase difference $\Delta\varphi_{20} = 50^{\circ}$, resulting in the magnitude of AC bus voltage drops to about 500V, as shown in Fig. 19(a). After the voltage drop is confirmed, VSI #1 and VSI #2 collect the AC bus voltage phase and calculate the phase differences between them and the AC bus. Since the phase differences are fixed values under the same steady-state of the system, the proposed method does not need to carry out the synchronous actions at the same time. Therefore, to show the synchronization process more clearly, VSI #2 and VSI#1 conduct their synchronizations in turn. Firstly, VSI #2 subtracts its phase difference from its reference phase, the transient response is depicted in Fig. 19(b). Subsequently, VSI #1 subtracts its phase difference from the reference phase, as depicted in Fig. 19(c). It can be observed from Fig. 19 that the synchronization of VSIs is accurately achieved and the AC bus

voltage restores to about 540 V after VSI #1 finishes its actions. Thanks to the setting of the virtual resistance to the maximum value R_{vir2}= R_{max}, the output currents of VSIs are maintained within a reasonable range during the synchronization process.

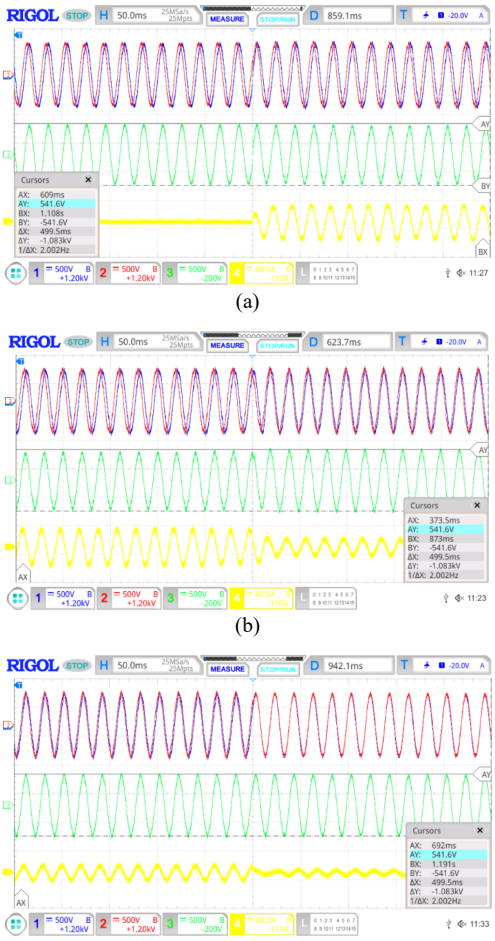


Fig. 19. Experimental waveforms of the proposed synchronization. (a) The connection of VSI #2. (b) The synchronization of VSI #2. (c) The synchronization of VSI #1. CH1, the no-load output voltage of VSI #1: 500 V/div; CH2, the no-load output voltage of VSI #2: 500 V/div; CH3, the AC bus voltage: 500 V/div; CH4, the output current of VSI #2: 40 A/div.

C. Performance of Current Sharing

1) With the Traditional PLL

Experimental results are supplemented in Fig.20 when the traditional PLL is adopted. As can be seen in Fig.20 (a), when VSI#2 is connected to the AC bus through a PLL, the current is not evenly shared. Besides, as depicted in Fig.20 (b), the leading phase of VSI#2 to VSI#1 gradually increases when VSI#1 is removed, indicating that the frequency of VSI#2 is increasing, which eventually causes the frequency exceeding the allowed value. The experimental results are consistent with the simulation results.

2) With the Proposed Controller

Three scenarios have been experimented to test the current sharing performances of the proposed scheme, including the scenario of load changes, the scenario of current sharing ratio changes, and the scenario of VSI #1 exit.

Fig. 21(a.1) and Fig. 21(a.2) show the transient response during the load changes. Initially, VSI #1 and VSI #2 are on parallel operation with the same power rates to supply load#1. Then load#2 is connected to the AC bus, the output currents of VSI #1 and VSI #2 increase accordingly to supply the needed current as shown in Fig. 21(a.1). Whereas, when load#2 is disconnected, the output current of VSI #1 and VSI #2 decrease to the original value, as presented in Fig. 21(a.2). During the whole process, the output currents of VSI #1 and VSI #2 are equally shared.

The current sharing performance during the scenario of current sharing ratio changes is depicted in Fig. 21(b.1) and Fig. 21 (b.2). In the beginning, VSI #1 and VSI #2 operate in parallel with load#1 and load#2. The magnitudes of the output current of both VSI #1 and VSI #2 are approximately 7.2 A. When the current sharing ratio has been suddenly changed from 1:1 to 2:1, the magnitudes of the output currents of VSI #1 and VSI #2 change to 9.6 A and 4.8 A respectively, as shown in Fig. 21(b.1). When the sharing ratio is changed back to 1:1, the output currents of VSI #1 and VSI #2 restore to the original value, as shown in Fig. 21(b.2).

Fig. 21(c) presents the transient response during the exit of VSI#1. In the beginning, VSI#1 and VSI#2 parallel operate with load#2. The magnitudes of the output current of both VSI#1 and VSI#2 are approximately 4.7 A. When VSI#1 is disconnected from the AC bus, the magnitude of the output current of VSI#2 increases to 9.4 A, while the output current of VSI#1 decreases to 0. Note that different with the PLL-based method, the frequency of VSI#2 remains at 50 Hz when VSI#1 exits. With the proposed controller, the exit of any VSI will not affect the normal operation of the parallel system.

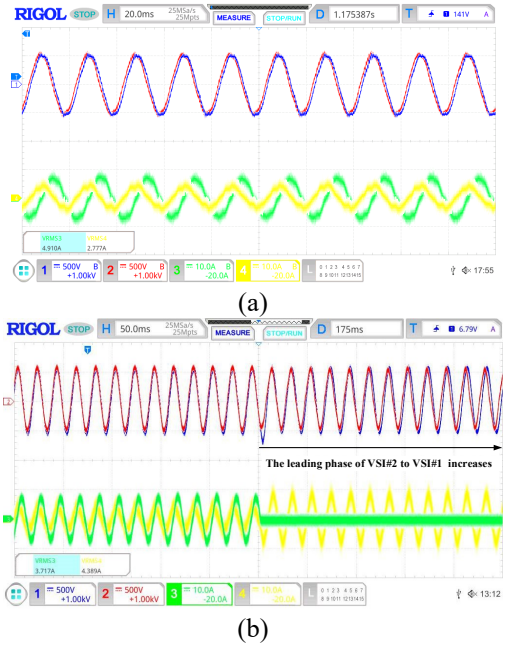


Fig. 20. Experimental waveforms with the traditional PLL. (a) The parallel operation of VSI#1 and VSI#2. (b) The exit of VSI #1. CH1, the no-load output voltage of VSI #1: 500 V/div; CH2, the no-load output voltage of VSI #2: 500 V/div; CH3, the output current of VSI #1: 10 A/div; CH4, the output current of VSI #2: 10 A/div.

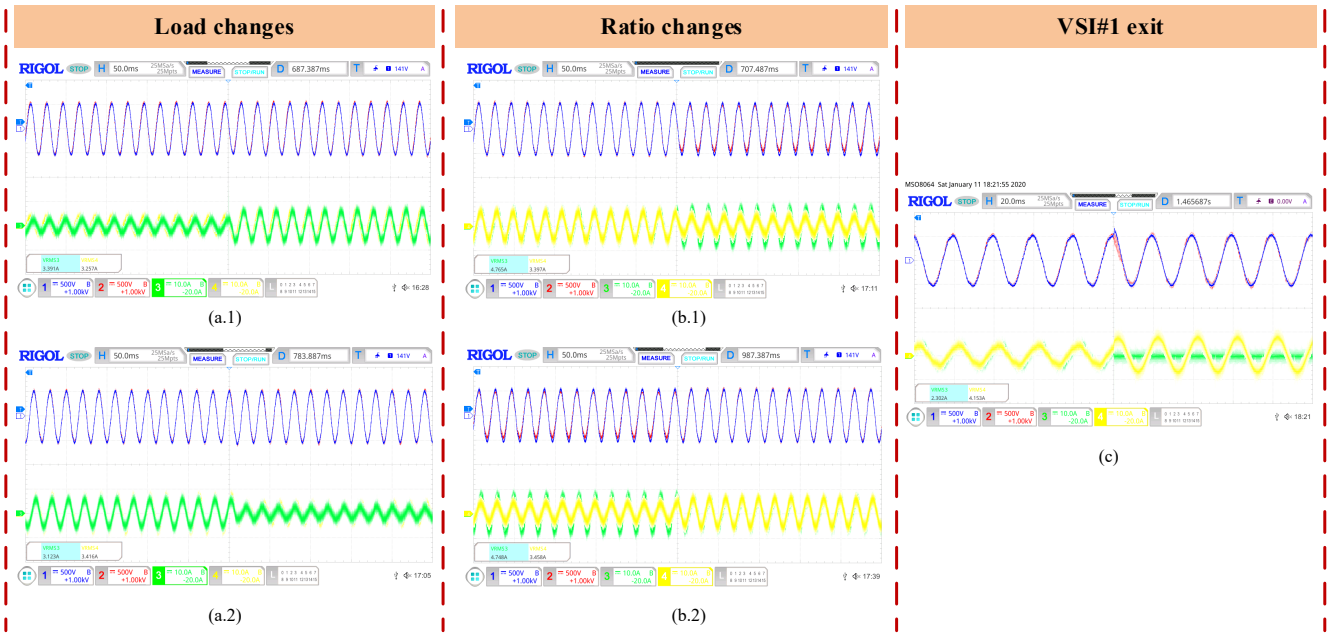


Fig. 21. Experimental results of the current sharing performance in different scenarios. (a.1) The connection of load#2. (a.2) The disconnection of load#2. (b.1) The ratio is changed from 1:1 to 2:1. (b.2) The ratio is changed from 2:1 to 1:1. (c) The exit of VSI #1. CH1, the output voltage of VSI #1: 500 V/div; CH2, the output voltage of VSI #2: 500 V/div; CH3, the output current of VSI #1: 10 A/div; CH4, the output current of VSI #2: 10 A/div.

VII. Conclusion

In this paper, a unified scheme of controlling parallel-operated VSIs is developed, which endows accurate current sharing performance among VSIs and ensures high reliability of the parallel system. By analyzing the power flow of the parallel system, two critical issues are extracted: the control of combined impedance and the synchronization of the VSIs. For the combined impedance control, this paper proposes a novel DOB-based controller that combines a feed-forward loop with a virtual complex impedance loop. The inherent output impedance of VSI is suppressed by the feed-forward loop, while the combined impedance is reconstructed by the virtual complex impedance loop. For the synchronization control, a constant frequency-based method is put forward to synchronize the phases of VSIs by using only local measurements. Each VSI operates at a constant frequency of 50 Hz and the exit of any VSI will not affect the normal operation of the parallel system. Simulation and experimental results validate the excellent behavior of the proposed controller. Concise control principle and clear parameter design method also facilitate engineering promotion of the proposed scheme. However, there are still some limitations of the proposed strategy. The proposed method is applicable to small-scale microgrids, where the line impedances are negligible due to the predominant virtual resistances. If it is to be adopted in large-scale microgrids, the grid parameters are required to obtain the AC bus voltage and achieve accurate power sharing.

References

[1] J. M. Guerrero, M. Chandorkar, T. Lee and P. C. Loh, "Advanced Control Architectures for Intelligent Microgrids—Part I: Decentralized and Hierarchical Control," *in IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1254-1262, April 2013.

[2] J. Rocabert, A. Luna, F. Blaabjerg and P. Rodríguez, "Control of Power Converters in AC Microgrids," *in IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734-4749, Nov. 2012.

[3] J. A. P. Lopes, C. L. Moreira and A. G. Madureira, "Defining control strategies for MicroGrids islanded operation," *in IEEE Transactions on Power Systems*, vol. 21, no. 2, pp. 916-924, May 2006.

[4] T. Wu, Z. Liu, J. Liu, S. Wang and Z. You, "A Unified Virtual Power Decoupling Method for Droop-Controlled Parallel Inverters in Microgrids," *in IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5587-5603, Aug. 2016.

[5] J. M. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *in IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1205-1213, Sept. 2004.

[6] J. He and Y. W. Li, "An Enhanced Microgrid Load Demand Sharing Strategy," *in IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 3984-3995, Sept. 2012.

[7] H. Han, X. Hou, J. Yang, J. Wu, M. Su and J. M. Guerrero, "Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids," *in IEEE Transactions on Smart Grid*, vol. 7, no. 1, pp. 200-215, Jan. 2016.

[8] J. M. Guerrero, Luis Garcia de Vicuna, J. Matas, M. Castilla and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," *in IEEE Transactions on Industrial Electronics*, vol. 52, no. 4, pp. 1126-1135, Aug. 2005.

[9] W. Yao, M. Chen, J. Matas, J. M. Guerrero and Z. Qian, "Design and Analysis of the Droop Control Method for Parallel Inverters Considering the Impact of the Complex Impedance on the Power Sharing," *in IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 576-588, Feb. 2011.

[10] J. M. Guerrero, N. Berbel, J. Matas, L. G. de Vicuna and J. Miret, "Decentralized Control for Parallel Operation of Distributed Generation Inverters in Microgrids Using Resistive Output Impedance," *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics, Paris*, 2006, pp. 5149-5154.

[11] Z. Chen, X. Pei, M. Yang and L. Peng, "An Adaptive Virtual Resistor (AVR) Control Strategy for Low-Voltage Parallel Inverters," *in IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 863-876, Jan. 2019.

[12] Y. W. Li and C. Kao, "An Accurate Power Control Strategy for Power-Electronics-Interfaced Distributed Generation Units Operating in a Low-Voltage Multibus Microgrid," *in IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2977-2988, Dec. 2009.

[13] J. C. Vasquez, J. M. Guerrero, A. Luna, P. Rodriguez and R. Teodorescu, "Adaptive Droop Control Applied to Voltage-Source Inverters Operating

in Grid-Connected and Islanded Modes," *in IEEE Transactions on Industrial Electronics*, vol. 56, no. 10, pp. 4088-4096, Oct. 2009.
[14] Y. Guan, J. M. Guerrero, X. Zhao, J. C. Vasquez and X. Guo, "A New Way of Controlling Parallel-Connected Inverters by Using Synchronous-Reference-Frame Virtual Impedance Loop—Part I: Control Principle," *in IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4576-4593, June 2016.
[15] R. Wai, Q. Zhang and Y. Wang, "A Novel Voltage Stabilization and Power Sharing Control Method Based on Virtual Complex Impedance for an Off-Grid Microgrid," *in IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1863-1880, Feb. 2019.
[16] P. Sreekumar and V. Khadkikar, "Direct Control of the Inverter Impedance to Achieve Controllable Harmonic Sharing in the Islanded Microgrid," *in IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 827-837, Jan. 2017.
[17] W. Chen, J. Yang, L. Guo and S. Li, "Disturbance-Observer-Based Control and Related Methods—An Overview," *in IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1083-1095, Feb. 2016.
[18] G. Lou, W. Gu, J. Wang, J. Wang and B. Gu, "A Unified Control Scheme Based on a Disturbance Observer for Seamless Transition Operation of Inverter-Interfaced Distributed Generation," *in IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 5444-5454, Sept. 2018.
[19] Y. Joo, G. Park, J. Back and H. Shim, "Embedding Internal Model in Disturbance Observer With Robust Stability," *in IEEE Transactions on Automatic Control*, vol. 61, no. 10, pp. 3128-3133, Oct. 2016.
[20] Y. Wu and Y. Ye, "Internal Model-Based Disturbance Observer With Application to CVCF PWM Inverter," *in IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5743-5753, July 2018.
[21] P. P. Das, S. Chattopadhayay and M. Palmal, "A d–q Voltage Droop Control Method With Dynamically Phase-Shifted Phase-Locked Loop for Inverter Paralleling Without Any Communication Between Individual Inverters," *in IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4591-4600, June 2017.
[22] M. S. Golsorkhi and D. D. C. Lu, "A Control Method for Inverter-Based Islanded Microgrids Based on V-I Droop Characteristics," *in IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1196-1204, June 2015.
[23] M. S. Golsorkhi, M. Savaghebi, D. D. Lu, J. M. Guerrero and J. C. Vasquez, "A GPS-Based Control Framework for Accurate Current Sharing and Power Quality Improvement in Microgrids," *in IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5675-5687, July 2017.
[24] Y. Li and L. Fan, "Stability Analysis of Two Parallel Converters With Voltage–Current Droop Control," *in IEEE Transactions on Power Delivery*, vol. 32, no. 6, pp. 2389-2397, Dec. 2017.
[25] Zhao, G.; Yang, H. Parallel Control of Converters with Energy Storage Equipment in a Microgrid[J]. *Electronics*, 2019, 1110 (8), 1-20.
[26] A. Micallef, M. Apap, C. S. Staines and J. M. G. Zapata, "Secondary control for reactive power sharing and voltage amplitude restoration in droop-controlled islanded microgrids," *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Aalborg*, 2012, pp. 492-498.
[27] Q. Shafiee, J. M. Guerrero and J. C. Vasquez, "Distributed Secondary Control for Islanded Microgrids—A Novel Approach," *in IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 1018-1031, Feb. 2014.
[28] X. Lu, X. Yu, J. Lai, Y. Wang and J. M. Guerrero, "A Novel Distributed Secondary Coordination Control Approach for Islanded Microgrids," *in IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 2726-2740, July 2018.
[29] Amirnaser Yazdani; Reza Iravani, "Grid-Imposed Frequency VSC System: Control in dq-Frame," *in Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications, IEEE*, 2010, pp. 219-222.
[30] Amirnaser Yazdani; Reza Iravani, "Controlled-Frequency VSC System," *in Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications, IEEE*, 2010, pp. 256-257.
[31] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, *IEEE Std 1547-2003*, July 2003.
[32] X. Guo, W. Liu, X. Zhang, X. Sun, Z. Lu and J. M. Guerrero, "Flexible Control Strategy for Grid-Connected Inverter Under Unbalanced Grid Faults Without PLL," *in IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1773-1778, April 2015.
[33] N. M. Haleem and A. D. Rajapakse, "Fault-Type Discrimination in HVDC Transmission Lines Using Rate of Change of Local Currents," in IEEE Transactions on Power Delivery, vol. 35, no. 1, pp. 117-129, Feb. 2020.
[34] G Zhou, M Han, S Filizadeh, X Cao and W Huang, "Studies on the combination of RSFCLs and DCCBs in MMC-MTDC system protection," in International Journal of Electrical Power & Energy Systems, vol. 125, pp. 1-9, Nov. 2020.
[35] R. Han, L. Meng, J. M. Guerrero and J. C. Vasquez, "Distributed Nonlinear Control With Event-Triggered Communication to Achieve Current-Sharing and Voltage Regulation in DC Microgrids," *in IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6416-6433, July 2018.
[36] R. C. Francy, A. M. Farid, and K. Youcef-Toumi, "Event triggered state estimation techniques for power systems with integrated variable energy resources," *ISA Trans.*, vol. 56, pp. 165–172, Nov. 2014.
[37] Amirnaser Yazdani, Reza Iravani, "Grid-Imposed Frequency VSC System: Control in dq-Frame," in Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications, IEEE, 2010, pp. 211-212.

Wenyuan Cao (S'19) was born in Hunan, China, in 1994. He received the B. S. degree in North China Electric Power University, Beijing, China, in 2017, where he is pursuing the Ph.D. degree, majoring in electrical engineering.
He is currently a guest Ph.D. student in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His research interests include hybrid AC/DC distribution network and its control.

Minxiao Han (M'05–SM'18) was born in Shannxi, China, in 1963. He received his Ph.D. from North China Electric Power University (NCEPU). He was a visiting Ph.D. student with Queen's University of Belfast, U.K. and a post-doctoral fellow with Kobe University, Japan. He is presently the Director of Institute of Flexible Electric Power Technology of NCEPU. He has been the leader in projects consigned by National Nature Science Foundation of China, National Educational Ministry, and enterprises. He has four published books and more than 100 refereed publications in journals and conferences. His research interests are the applications of power electronics in power system including HVDC, FACTS, power conversion and control.

Xiahui Zhang was born in Zhejiang, China, in 1997. He received the B. S. degree in China University of Geosciences, Beijing, China, in 2019, and he is pursuing the M.D. degree in North China Electric Power University, Beijing, China.
His research interests include DC distribution network and its control.

Wenqiang Xie (S'19) was born in Jiangsu, China, in 1993. He received the B.S. degree in North China Electric Power University, Beijing, China, in 2016, where he is pursuing the Ph.D. degree, majoring in electrical engineering.
His research interests include power electronics, control, and their applications in dc microgrids.

Gibran David Agundis Tinajero received the B.S. degree in mechanical and electrical engineering from the Universidad Autónoma de San Luis Potosí, San Luis Potosí, México, in 2012, and the M.Sc. and Ph.D. degrees in electrical engineering from the Universidad Autónoma de San Luis Potosí, San Luis Potosí, México, in 2014 and 2018, respectively. He is currently working as a Postdoctoral Fellow at the Energy Technology Department, Aalborg University, Denmark, where he contributes in different renewable-energy related projects. His research interests include modelling, analysis, and control of microgrid clusters including LV and MV distribution grids.

Josep M. Guerrero (S'01–M'04–SM'08–F'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. From 2014, he is Chair Professor in Shandong University. Since 2015, he has been a Distinguished Guest Professor at Hunan University. Since 2016, he has been a visiting professor fellow at Aston University, UK, and a guest Professor at the Nanjing University of Posts and Telecommunications. From 2019, he became a Villum Investigator by The Villum Fonden, which supports the Center for Research on Microgrids (CROM) at Aalborg University, where he is the Founder and Director. He has published more than 500 journal papers in the fields of microgrids and renewable energy systems, which are cited more than 50,000 times. His research interests include different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering and the internet of things for ac/dc microgrid clusters and islanded minigrids, with a special focus on microgrid technologies applied to offshore wind and maritime microgrids for electrical ships, vessels, ferries, and seaports. Prof. Guerrero is an Associate Editor for a number of IEEE Transactions. He received the Best Paper Award of the IEEE TRANSACTIONS ON ENERGY CONVERSION for the period 2014–2015, the Best Paper Prize of IEEE-PES in 2015, the Best Paper Award of the IEEE JOURNAL OF POWER ELECTRONICS in 2016. From 2014 to 2019, he was awarded by Clarivate Analytics (former Thomson Reuters) as Highly Cited Researcher. In 2015, he was promoted as a Fellow at the IEEE for his contributions on distributed power systems and microgrids.