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Published in:
Energies

DOI (link to publication from Publisher):
10.3390/en12122434

Publication date:
2019

Document Version
Publisher's PDF, also known as Version of record

energies

MDPI

Article

A Three-Phase Transformerless T-Type- NPC-MLI for Grid Connected PV Systems with Common-Mode Leakage Current Mitigation

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Received: 4 June 2019; Accepted: 21 June 2019; Published: 24 June 2019

Abstract: DC to AC inverters are the well-known and improved in various kinds photovoltaic (PV) and gird tied systems. However, these inverters are require interfacing transformers to be synchronized with the grid-connected system. Therefore, the system is bulky and not economy. The transformerless inverter (TLI) topologies and its grid interface techniques are increasingly engrossed for the benefit of high efficiency, reliability, and low cost. The main concern in the TL inverters is common mode voltage (CMV), which causes the switching-frequency leakage current, grid interface concerns and exaggerates the EMI problems. The single-phase inverter two-level topologies are well developed with additional switches and components for eliminating the CMV. Multilevel inverters (MLIs) based grid connected transformerless inverter topology is being researched to avail additional benefits from MLI, even through that are trust topologies presented in the literature. With the above aim, this paper has proposed three -phase three-level T type NP-MLI (TNP-MLI) topology with transformerless PV grid connected proficiency. The CM leakage current should handle over mitigating CMV through removing unwanted switching events in the inverter pulse width modulation (PWM). This paper is proposes PV connected T type NP-MLI interface with three-phase grid connected system with the help of improved space vector modulation (SVM) technique to mitigate the CM leakage current to overcome the above said requests on the PV tied TL grid connected system. This proposed the SVM technique to mitigate the CM leakage current by selecting only mediums, and zero vectors with suitable current control method in order to maintain the inverter current and grid interface requirements. The proposed PV tied TNP-MLI offering higher efficiency, lower breakdown voltage on the devices, smaller THD of output voltage, good reliability, and long life span. The paper also investigated the CM leakage currents envisage and behavior for the three-phase MLI through the inverter switching function, which is not discussed before. The proposed SVM on TL-TNP-MLI offers the reliable PV grid interface with very low switching-frequency leakage current (200mA) for all the PV and inverter operation conditions. The feasibility and effectiveness of the TLI and its control strategy is confirmed through the MATLAB/Simulink simulation model directly as compared with 2kW roof top PV plant connected TL-TNP-MLI experimentation, showing good accordance with theoretical investigation. The simulation and experimental results are demonstrated and presented in the good stability of steady state and dynamics performances. The proposed inverter reduces the cost of grid interface transformer, harmonics filter, and CMV suppressions choke.

Keywords: Hybrid Microgrid; Battery Electric Vehicle; Energy management strategy; Vehicle-to-Vehicle Charging; Energy Storage Unit

1. Introduction

Photovoltaic (PV) based power generation is an unavoidable segment in the electrical power generation system (PGS) to meet the world power demand. The most recent renewables 2018 global status report indicates that 450GW of new PV plants have been set up worldwide in 2017, a 125% proliferation when compared to 2016 [1]. The reported global electricity generations from renewable energy sources alone in 2017 has been estimated around 26.5%, out of which 1.9% is from PV power generations.

The leading PV power producers were China, European Union, and the United States of America, with 131.1 GW, 108 GW, and 51 GW, respectively [2,3]. Countries like Japan, India, United Kingdom (UK), and Australia are the next pioneers in generating more power from PV planets.

Even though the price of PV panel has been mostly dropped, the complete cost of both the components investment and the generation of grid-tied PV system are quiet high. Hence, the PV tied grid-tied voltage source inverters (VSIs) are need to be prudently designed for accomplishing the low cost, high efficiency, and small size, in addition to low weight. The PV grid-tied VSIs are associated with the line-frequency transformers (LFTs) to afford galvanic-isolation in commercial PV inverter system structures. Nevertheless, LFTs are heavy and large, building the complete system bulky as well as inflexible to install. The use of LFTs for line-frequency isolation in grid-connected inverters, high-frequency isolation transformers are considered for their smaller size, lower cost, as well as total system weight. On the other hand, these high-frequency transformers connect inverter system have different power conversion stages, which affect the system and diminish the system overall efficiency and straightforwardness [4,5]. As a result, the PV grid-tied transformerless inverters (TLIs) are broadly used and installed in the low-power PV distributed generation systems (particularly 5kW and less). However inappropriately, TLIs are producing the common-mode leakage currents, which cause the leakage current flow due to the present PV panel parasitic capacitances [6]. This leakage current leads to serious safety concern and electro magnetics interference issues [7]. Hence, parasitic capacitances leakage current must be able to mitigate within a recommended choice [8]. Furthermore, the PV inverters tied grid-connected system should fulfill the grid interfacing standards and codes, leakage current detection, grid frequency protection, active and reactive control, and power quality standards [9–13]. Hence, the PV large manufacturers companies, such as Fronius international, Sunny boy, and SMA solar technology, are strict with PV standards and codes to satisfy the system safety and reliability requests. These companies are following German codes (VDE0126-1-1, IEC 60755 issued time, 2006 and VDE-AR-N-4105 issued time, 2011) for leakage current (less than 300mA) and grid frequency ($47.5 < f < 51.5$). Hence, over 300 mA leakage current, the PV inverter should be trigger to breakdown within 0.3 sec, as per the VDE 0126-1-1 code standard.

From the above-mentioned investigation, the important concerns in the PV tied transformerless inverters should be considered for efficiency, reliability, and cost. In industry practices, the commercial TLIs are designed with the total efficiency of more than 97% to 98 %. The total efficiency of the distributed PV tied TLI systems are manufactured by Steca's Grid and Good We Technology's, with 97.7% and 96.9%, respectively [14,15]. In view of PV inverters installation, 10%–20% overall installation cost is the initial system cost [16], hence the price drops for PV inverters installations certainly promote the PV product affordability. The U.S. energy department demonstrated that the TLI system for the residential systems (≤ 10 kW) had dropped from nine U.S. dollars to 4.8 U.S. dollars per Watt, since 2009 to 2014 [17].

Most of the installed PV plants are erected by single-phase type two-level voltage source inverter (VSI) topologies [2], which generate pulsating AC output power. Hence, the inverters require large

DC-link capacitors; high collector–emitter voltage based switching devices and bulky filters ensure the grid standard codes. Henceforth for the last quarter decades, three-phase three-level NPC (3L-NPC) inverters are preferred for the alternate of two-level VSIs, which has been the hub of various research studies on PV applications [3–7]. Due to their small DC-link capacitors and the constant ac power on the output, NP-MLIs gave higher efficiency, lower breakdown voltage on the devices, smaller THD of output voltage, good reliability, and long life span [3,18–24]. Three-phase three-level NPC-MLIs are separated into two types (I and T) based on their leg shapes. After the arrival of T-type-NPC-MLI, I-type-NPC-MLI were evaded due to their long current commutation paths, higher stray inductance, and high conduction loss. The T-type 3L-NPC is being explored more to progress the better system efficiency [25–32]. The research on NPC-MLI has been extensively researched in PV and DC Distribution Network due its influencing of the stability, lower total harmonic distortion (THD), and lower electromagnetic noise [32–34]. These improvements mainly focused on DC-link balancing and common-mode voltage mitigations [35,36].

Most of the PV-tied grid connected inverter topologies are transformer based, which isolates the PV panels from the grid. The line-frequency transformer is avoided and high-frequency transformer is preferred due to the size and weight issues. However, the high-frequency transformer degrades the efficiency and makes the system more complex [37,38]. As a result, transformerless (TL) PV tied inverter–grid connection structure is greatly appreciated and studied by the power engineers due its less size, weight, and cost [39,40]. Although the TL inverters are able to gain system efficiencies of up to 97%, due to the absence of galvanic isolation and large stray capacitances, higher common mode voltage (CMV) is generated by VSI, which escorts the higher CM leakage current on the PV modules. Therefore, TL inverters suffer higher THD, ripple in grid current, degrading power quality, and warns of human safety, along with forming worsening EMI issues [41,42]. Figure 1 shows the leakage current bath for the Transformerless PV connected system.

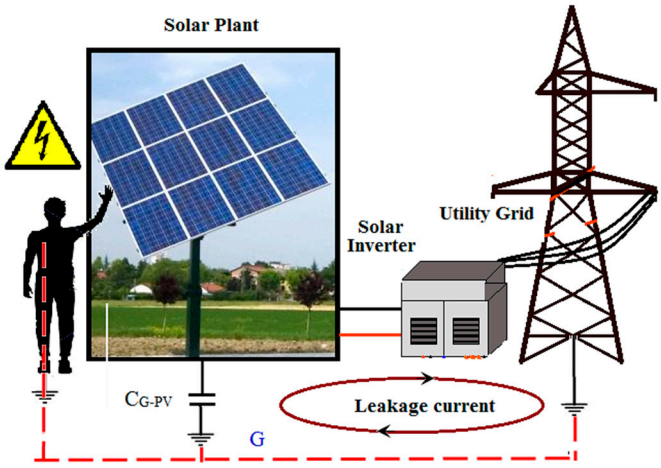


Figure 1. Leakage current for Transformerless photovoltaic (PV) connected system.

The PV commissioning companies recommended limiting the leakage current, for example, in German standard 300mA, is used as the reference value. In order to keep this recommendation, most of the inverter manufacturers maintain expertise in inverter topologies, special controllers, and novel pulse width modulation (PWM) techniques. There are techniques for the TL system to reduce the leakage current through adding up devices in the inverter, such as diodes, switches, and passive elements [43–47]. However, changing the PWM switching pattern is more efficient than adding the devices and increasing the cost and reducing trust on continuous operation [37], which are mainly changing the pulses based on CMV development. When compared to other PWM methods, space vector modulation (SVM) is a pledge PWM to creating different PWM in a binary way. The methods use three medium vectors (3MV), keeps minimal CMV as the constant value, and it does

not root less leakage current. Nevertheless, the maximum fundamental output voltage of the inverter is restricted $V_{DC}/2$. A different method in [45] uses two MVs and one zero vector (ZV) and it does not cause the leakage current. However, similar to 3MV, its limited output voltage, and hence the better dc-link voltage, is compulsory to interface with the grid. Lee. J.S et.al has developed modulation techniques for reducing the leakage current while balancing the DC-link voltages. The method using the medium, zero, and large vectors reduces the CMV voltage that significantly roots the leakage current with better DC-link unitization [47].

Based on the aforementioned recognitions, a novel three-phase three-level TL T-type- NPC-MLI (3L-TL-TNPC-MLI) is proposed for the PV grid connected system with leakage current reduction. The novel TL-TNPC-MLI topology, together with the SVM strategy, have been proposed, aiming to improve system efficiency through the reduction of the commutation and conduction loss on the inverter, and leakage current reduction. The validity of the proposed inverter and its SVM control algorithm is verified for 1.5 kW PV grid connected system via simulation and experiment study. From the results, it is verified that the proposed inverter and PMW algorithm is well set for the perfect grid interface with reducing the leakage current.

The paper is outlined, as follows: nomenclature deals with the List of symbols and abbreviations. Section 2 accomplishes the analytical model and derivation of the leakage current on the three-phase transformerless MLI PV-grid connected system. Section 3 discusses the proposed PV tied three-phase three-level TL-TNP-MLI for th grid connected system. Sections 4 and 5 accomplishes the MATLAB/Simulink simulations and hardware prototype experimentations. In conclusion, the advantages of the proposed system are presented in Section 6.

2. Leakage Current Analysis Transformerless PV Inverter System

In the PV tied grid connected systems, the isolation transformer is connected between the PV inverters and the grid, as shown in Figure 1. The parasitic capacitances ($C_{G\text{-}PV}$) is connected in the 1 (dc^+ terminal) and 2 (dc^-terminal) of the PV array. The mid-point of terminals 1 and 2 is called the neutral point (N). The voltage difference between terminals 1 and 2 is related to ground (G). The L_A, L_B, and L_C are line the inductances of each phase, L_{CA}, L_{CB}, and L_{CC} are the line inductances of each phase with respect to grid and, L_G is the grid inductance. When the variations of the 1 and 2 terminals would source leakage currents from the PV panel to the ground. The leakage current value is depending on the amplitude and frequency of the voltage fluctuations and, in addition to the value of the parasitic capacitance (leakage capacitance) [26]. The leakage capacitance value depends on many factors, such as PV panel and frame structure, dust or salt covering the PV panel, and weather conditions, and so on.

Due to the fact of $C_{G\text{-}PV}$ and inverter topology, common-mode voltage (CMV) is generated, which causes the common-mode current (CMC). The CMC is a danger, and it falloffs the PV lifetime [36]. In a general PV tied grid connected system with isolation transformer, the CMC can only find its path through the stray capacitances of the transformer. Generally, this is the reason why galvanic isolation (with a transformer) based PV systems are not affected due to the low frequency leakage current behavior, irrespective of the converters and their modulation techniques. As per German standard-DIN VDE0126-1-1, when the ground current goes beyond 300 mA (peak), the inverter needs to disconnect within 3 sec, and it furnishes the needs for restrictions concerning ground leakage and fault currents [18]. However, in TLI, due to the transformer absence, the converter and modulation methods can only do the CMC elimination. With this aim, the leakage current model is derived related with three-phase inverter switching. In order to illustrate the path for the common-mode current (CMC), the stray elements are added to the system, as in Figure 2.

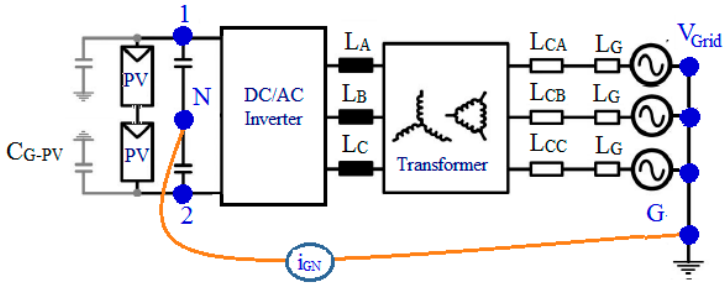


Figure 2. Grid connected PV system including the parasitic capacitance to ground of the PV array.

Figure 3 shows the three-phase PV-grid connected inverter model with $C_{G\text{-}PV}$ and CMV source that individually calculate the CMV and differential mode voltage (DMV), and these can be related with the leakage current model.

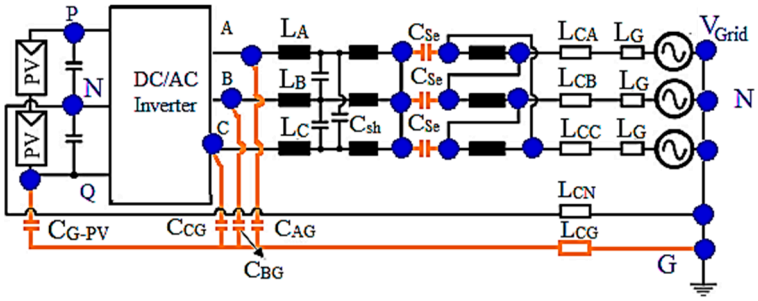


Figure 3. Three-phase PV-grid connected inverter model with stray elements.

Where the parameters are described, as follows; C_{sh} is shunt capacitance; C_{se} is series capacitance; L_{CN} is inductance between inverter neutral point and grid; L_{CG} is inductance between PV terminals and grid; and, C_{AG},C_{BG}, and C_{CG} are the capacitances between each phase with respect to grid ground (see Figure 4).

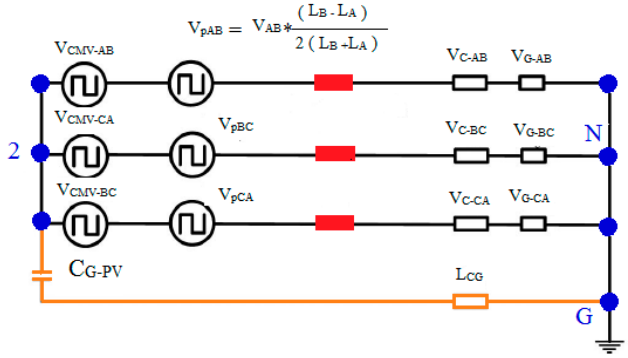


Figure 4. Three-phase PV-grid connected inverter model [5].

In a three-phase system, CMV and differential mode voltage (DMV) calculations between A to B or B to C or C to A phases are same. Thus, only A and phase B investigated in this paper. They calculated as [5],

$$\text{CMV between A and B phases, } V_{CM-AB} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

$$\text{DMV between A and B phases, } V_{DM-AB} = V_{AN} - V_{BN} \quad (2)$$

From (1) and (2), the out voltage expressed as

$$V_{AN} = \frac{V_{DM-AB}}{2} + V_{CM-AB} \tag{3}$$

$$V_{BN} = -\frac{V_{DM-AB}}{2} + V_{CM-AB} \tag{4}$$

By observing the above equations, the CM model for A and B phases are shown in Figures 5 and 6. Inverter stray capacitances are significantly identical, since the output inductances are identical for all three phases; the model can be simplified, as presented in Figure 7a. The final CM equivalent circuit model for the three-phase system is based on the designed two-phase circuit CM model, as shown in Figure 7b.

The CMV for all three phases expressed as [20],

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{5}$$

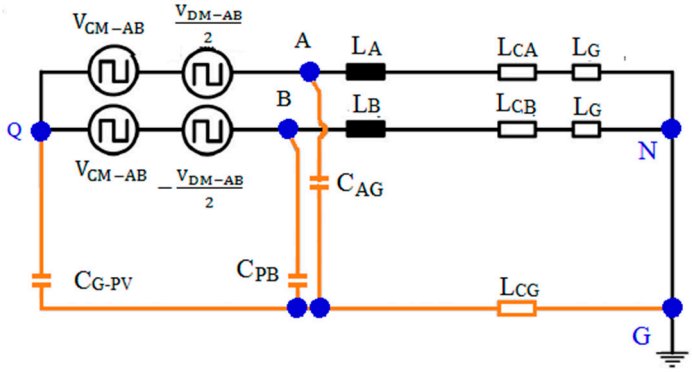


Figure 5. PV-grid connected inverter model only A and B phase [5].

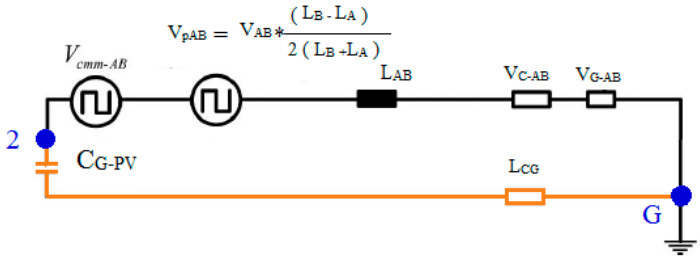
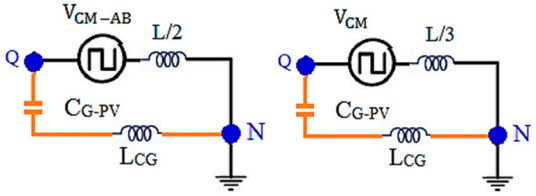


Figure 6. Single line model of total common mode voltage (CMV) [5].



(a) (b)

Figure 7. CMV model (a) two-phase model, and (b) three-phase model.

The output voltages of the three-level VSI are determined, based on the inverter's legs connection with one point among P, N, and Q, as in Figure 3. If the grid ground (G) is the standard, these three connection points' output voltages are $V_{DC} + V_N$, $V_{DC}/2 + V_N$, and V_N, respectively.

The grid currents is expressed as [5],

$$\frac{V_{AN} + V_N - E_a}{z_L} + \frac{V_{BN} + V_N - E_b}{z_L} + \frac{V_{CN} + V_N - E_c}{z_L} = 0 \quad (6)$$

Z_L is the impedance of the L-filter
Sum of grid currents is zero,

$$E_a + E_b + E_c = 0 \quad (7)$$

$$V_N = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \quad (8)$$

From (5) and (8), the V_{CM} is related to the output voltages of inverter, which means that V_{CM} can be influenced by the inverter switching state.

Consider that S_a, S_b, and S_c are the switching states of the inverter legs. Hence, the switching function is defined as,

$$S_{A,B,C}(V_{AN,}\, V_{BN}, V_{CN})_{1,\frac{1}{2},0} = \begin{matrix} V_{DC} & V_{DC}/2 & 0 \\ V_{DC} & V_{DC}/2 & 0 \\ V_{DC} & V_{DC}/2 & 0 \end{matrix} \quad (9)$$

From (6) and (9)

$$V_N \text{ or } V_{CM} = \frac{V_{DC}(S_a) + V_{DC}(S_b) + V_{DC}(S_c)}{3} \quad (10)$$

From (10), the possibilities of the CMV in the inverter switching are $-V_{DC}$, $-5V_{DC}/6$, $-2V_{DC}/3$, $-V_{DC}/2$, $-V_{DC}/3$, $-V_{DC}/6$, and 0. These ac-components of V_N cause the leakage current through the line, including C_{PV}.

Further, the leakage current is calculated, as [5],

$$|I_{CM}| = \frac{|V_{CM}|}{|Z_{PV}|} \quad (11)$$

Due the square wave CMV nature, the total CM leakage current is the addition of odd multiples of switching frequency current components. Hence, the total leakage current (I_{TCM}) is obtained, as [5],

$$I_{TCM} = \sum_{n=1,3,5,7,..}^{\infty} \left|I_{CM}(nf)\right| \quad (12)$$

From (12), if the switching frequency increases, there is an increase in I_{TCM}. However, it is not proportional to the switching frequency due to the damping resistor, the leakage resistor on the PV, R_{PV}. From the above discussion, I_{TCM} is influenced by leakage capacitor C_{PV}, and the switching action of the inverter. Hence, inverter switching based leakage current elimination is the best method, since C_{PV} is decisive by the environmental factors.

3. Proposed PV Tied Three-Phase Three-Level TL-TNPC-MLI for Grid Connected System with Leakage Current Reduction

This section discussed the proposed PV tied grid connected TL-TNPC-MLI, including CM leakage current elimination by using the full CM elimination switching technique with grid interfacing.

3.1. TL-TNPC-MLI Operation for Zero CMV.

Figure 8 shows the three-phase 3L-TL-TMLI power circuit, which has 12-IGBTs (S_{a1}-S_{c4}) and 12-anti-parallel free-wheeling diodes (FWD; D_{a1}-D_{c4}) three-phase 3L-TL-TMLI power circuit. It involves three-phase leg with four IGBTs (S_{a1}-S_{a4}) and four FWD (D_{a1}-D_{a4}) in a leg. Here, the top and bottom switches IGBTs/diodes (S_{a1}/$D_{a1}$and S_{a4}/D_{a4}) that were employed with 1200V and middle switches (S_{a2}

/ D_{a2} and S_{a3} / D_{a3}) operated by two 600V. Hence, due to small blocking voltage, middle switches consume very less switching and conduction losses, even though there are two devices that were connected in series [40]. The inverter includes two dc-link identical capacitors ($C_1 = C_2 = V_{DC}/2$) and six equal value split inductors ($L_{a1} = L_{a2} = L_{b1} = L_{b2} = L_{c1} = L_{c2} = L$). In view of T-MLI with TL concept, the ground connection is the essential one for any TL inverter topologies, while the centre of PV cluster does not ground, the proposed TL-TMLI output terminals can be abundantly associated to the grid; else, mid-point (N) of both the dc-link capacitors (V_{C1} and V_{C2}) must be connected to the PV cluster mid-point and grid neutral (G). Table 1 illustrates the switching operation of TL T-MLI, the modes of operation is situated based on the dc-link mid-point (N) connection to DC^+, N and DC^-. There are 27 possible switching states of operation on 3L-TL-TMLI for the full cyclic operation of one grid cycle. Here, the modes are created based on the switching ON and OFF position on each inverter leg. These modes are categorized in four groups (G-1 to G-4). The possible switching state and its switching groups are tabulated in Table 2.

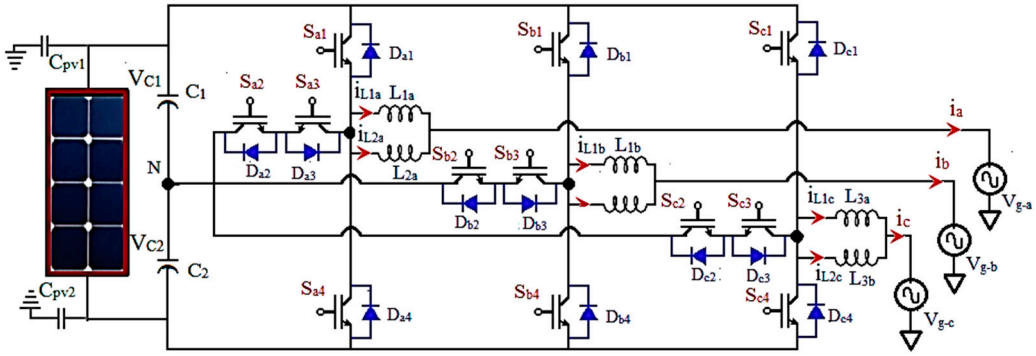


Figure 8. PV tied Three-level TL T- MLI power circuit.

Table 1. PV connected Three-level T-type MLI power circuit.

State	V_{out}	S_{a1}	S_{a2}	S_{a3}	S_{a4}
DC^+	$+V_{dc}/2$	ON	ON	OFF	OFF
N	0	OFF	ON	ON	OFF
DC^-	$-V_{dc}/2$	OFF	OFF	ON	ON

Table 2. Mode of operation of 3L-TL-TMLI.

Groups	Groups	Switching Mode
G-1	Zero Vector (ZV) switching	(000),(111),(-1-1-1)
G-2	Small Vector (SV) switching	{(100),(011)},{(110),(001),{(010),(101)}{(011),(100),{(001),(110)},{(101),(0-10)}
G-3	Medium Vector (MV) switching	(10-1), (01-1), (-110), (-101), (0-11), (1-10)
G-4	Large Vector (LV) switching	(1-1-1), (11-1), (-11-1), (-111), (-1-11), (1-11)

By applying the switching states in equation (10), each switching state has different possibilities of the CMV in the inverter switching are $V_{dc}/6$, $V_{dc}/3$, $V_{dc}/2$, 0, $-V_{dc}/6$, $-V_{dc}/3$, and $-V_{dc}/2$ as shown in Table 3. For example, for the -1-1-1 switching state, the obtained CMV is $V_{com_{[-1-1-1]}} = \frac{1}{3}\cdot(-3)\cdot\frac{V_{dc}}{2} = -\frac{V_{dc}}{2}$. Similarly, the MV 10-1 switching state CMV is $V_{com_{[1\ 0-1]}} = \frac{1}{3}\cdot(0) = 0$. Table 1 illustrates the CMV for the different switching state inverter. For all 27 switching states, the CMVs are summarized as $+V_{dc}/2$, 0, $+V_{dc}/3$, $+V_{dc}/6$. Figure 8 shows the space vector diagram (SVD) for three-level TMLI with their switching and ITS corresponding CMV. The SVD consists of six sectors, 27 switching states, and 24 sub-triangles Here, every switching states has its own CMV, which is tabulated as seven groups and the same represented in three-level SVD, as shown in Figure 8. Here, expect group-D (six MVs and one ZV) all other group

switching states are producing CMV and these CMV components cause the leakage current through the line, including C_{PV}.

Table 3. Switching states and CMV.

Group	Switching States of 3-Level Inverter	CMV Generated
A	(111)	$V_{dc}/2$
B	(110), (101), (011)	$V_{dc}/3$
C	(1-11), (11-1),(-111), (001), (010), (100)	$V_{dc}/6$
D	(000), (01-1), (0 –11), (10-1), (1-10), (–101), (–110)	0
E	(– 1–11),(–11 –1), (1 –1 –1), (00 –1), (0–10), (–1 00)	$–V_{dc}/6$
F	(– 10 –1), (0 –1 –1), (0 –1 –1)	$–V_{dc}/3$
G	(–1 –1 –1)	$–V_{dc}/2$

While operating SVM by selecting D –group-switching sequence, the CMV is fully eliminated, and, as a result, leakage current is fully eliminated. Figure 9 shows the refined SVD with using only D-group switching. When considering the case of V^* moving in sector-1 in order to zero CMV, the suggested switching structure uses zero CMV vectors, as V_Z [000], V_{M1} [10-1], and V_{M2} [01-1]. The uses of MVs with ZV facilitated by fixing/switching at the middle of the sector are 30, 90, 150, 210, 270, 330, (-30). Hence, the proposed scheme trundles on the principle of reference phase angle discrete hoping. Thus, sector-1 is reordered between -30 to 30 ($-30^0 < \theta > 30^0$). Similarly, sector-2 is 30 to 90 ($30^0 < \theta > 90^0$), and so on. This angle determination procedure has expanded for all six sectors in the SVD and each sector consists of the three zero CMV switching vectors (two MVs and one ZV switching state) as shown in Figure 10. Of course, due the absence of LVs, the full CMV elimination limited m_a is to 0.7. Therefore, the inverter output voltages reach up to 70% from the full linear m_a range. The dc-link voltage of the inverter must be increased in order to increase the voltage performance.

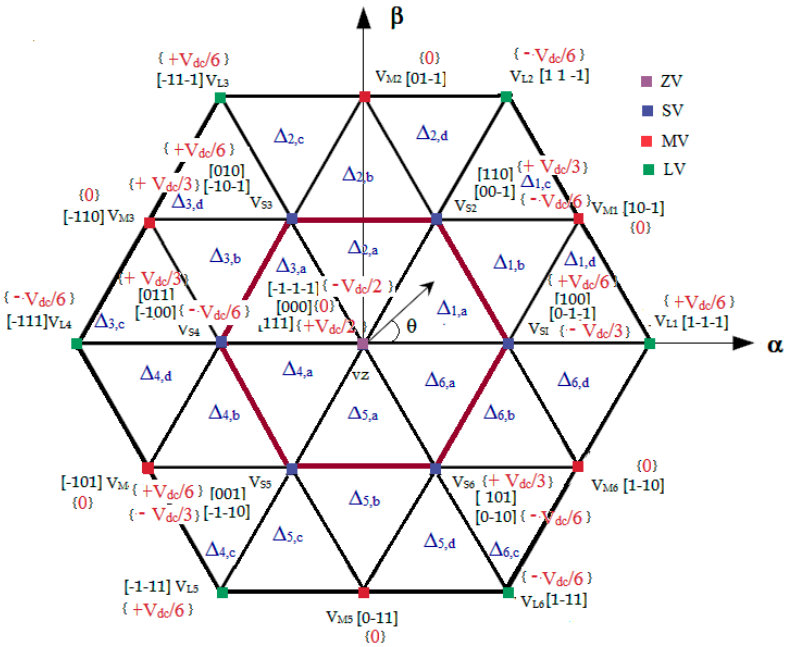


Figure 9. Three-phase space vector diagram (SVD) for three-level MLI.

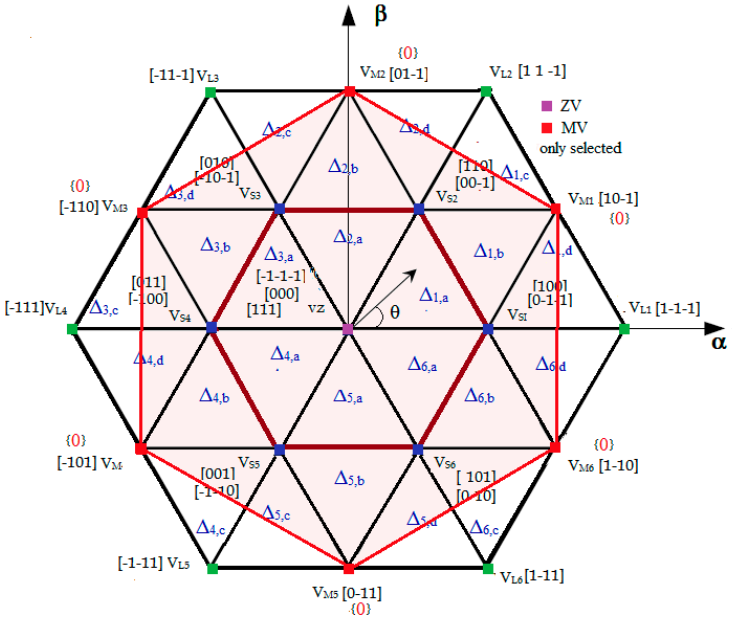


Figure 10. Proposed full mitigation CMV SVD.

3.2. *Proposed Close Loop Grid Connected TL-TNPC-MLI*

Figure 11 shows the proposed control system block. As presented in closed loop system, the PV panels are and controlled by P&O—maximum power point tracking (MPPT) method and the control output drive the boost converter to meet the desired dc-link voltage for the inverter. To connect the inverter power with utility grid, the phase lock loop (PLL) that is used to measure the phase locked angle of the grid voltage (θ) and its nominal frequency (w_r) from the V_g. The three-phase inverter (i_{inv}) and load current (i_L) are converted from abc to dq to match the PV output V_{dc}.

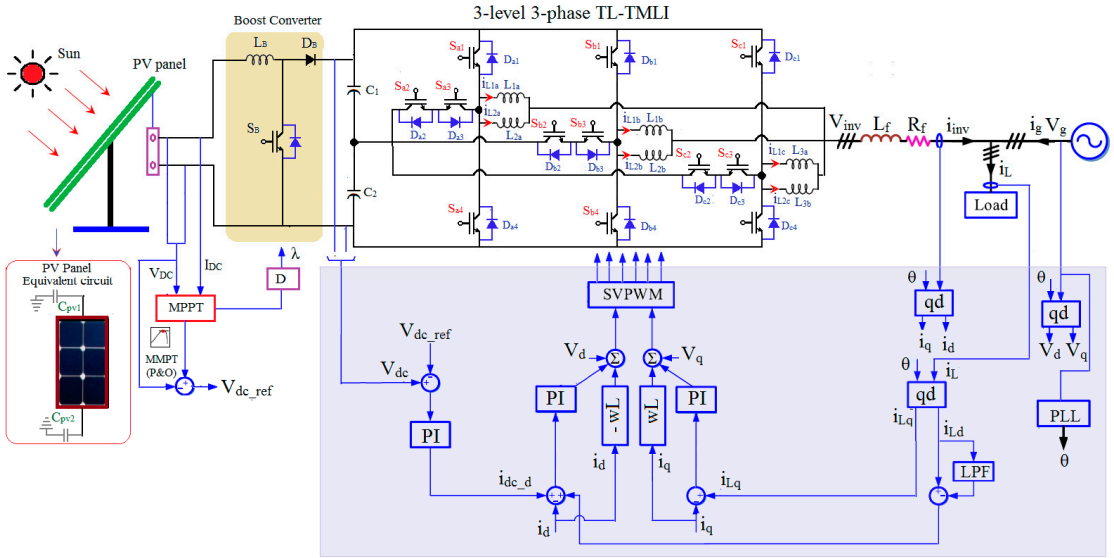


Figure 11. Proposed closed control PV tied grid connected TL-TMLI schematic control block.

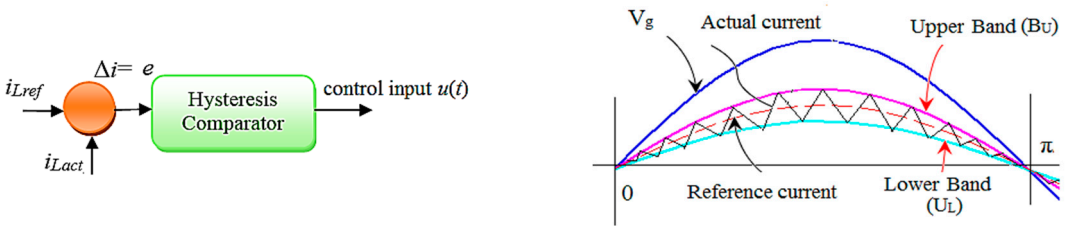
By using (13) and (14), according to [20], reference V_α and V_β are generated, which control the SVM to achieve the inverter grid interface.

$$V_\alpha = -wLi_d + V_d + i'_{dc\_d} \quad (13)$$

$$V_\beta = wLi_q + V_q + i'_{L\_q} \quad (14)$$

Finally, the predetermined component (V_α and V_β) is given to the SVM block, which gives the voltage control reference (V*) with desired modulation index (m_a) to match the grid voltage.

The hysteresis current control (HCC) is used for controlling the inductor current based on the grid current reference. The proposed HCC is giving suitable switching sequence to SVM for controlling inverter. In any HCC, it is necessary to retain the actual load current near the reference load current within the hysteresis boundaries. The main mathematical challenge in current controllers is to generate the reference current components. Figure 12a illustrates the building block of HCC of an inverter. Here, the reference current (i_{ref}) is related with the actual current (i_{act}) to produce the error current, $\vec{\varepsilon_i}$= (i_{Lref} - i_{Lact}), which will produce the error gain (control input u(t)) between the two hysteresis bands B_U and U_L (upper and lower hysteresis bands) [24]. This control signal generates the control input u (t) to drive the inverter.



(a) (b)

Figure 12. Hysteresis current control (HCC) control strategy [24]. (a). HCC comparator, (b). HCC band.

The Sinusoidal PWM (SPWM) based conventional HCC (CHCC) involves three individual references. Therefore, due to the non-interference between the commutation phases, the CHCC deviates from the variable switching frequency over the fundamental frequency cycle, which results in an irregular inverter operation. This happens, because each phase current not only depends on the corresponding phase voltage, but is also affected by the other voltages [23]. However, SVM-based CCs control the current using a single reference vector. Here, the tip of the reference current vector moves around the hexagonal-coordinate system in SVD [20]. Some of the research on HCC for MLI has been attempted through SVM [24,35]. However, these controllers have difficulties in attempting to make a direct current control and they use more numbers of hysteresis bands in order to achieve the results.

Unlike the reported CHCC and SVCC, the proposed HSVCC not only maintains the current, but it also takes care of dc-link capacitor balancing for the inverter, which assures the capacitor balancing within the recommended significance and produces the effective output voltage with current control to the grid. These switching options enables the CC with capacitors balancing throughout the operating condition (change in PV, Inverter, and grid parameters).

Here, when the reference current (i_{Lref}) and actual current (i_{Lact}) lie in SVD, and it is expressed as [24],

$$\vec{i_{Lref}} = i_{Lref\_\alpha} + ji_{Lref\_\beta} \quad (15)$$

$$\vec{i_{Lact}} = i_{Lact\_\alpha} + ji_{Lact\_\beta} \quad (16)$$

Subsequently, the error vector, $\vec{\varepsilon_i}$ is calculated from (2) and (3),

$$\vec{\varepsilon_i} = \vec{i_{Lref}} - j\vec{i_{Lact}} \quad (17)$$

Now, the $\vec{\varepsilon_i}$ expressed in the αβ-vector components frame is

$$\vec{\varepsilon_i} = \vec{\Delta_{i\alpha}} + j\vec{\Delta_{i\beta}} \quad (18)$$

From Equation (5), the position of the $\vec{\varepsilon_i}$ in SVD is calculated and the switching vectors are then selected to keep the $\vec{i}_{Lact}$ close to the $\vec{i}_{Lref}$.

It is assumed that the inverter has unity power factor (PF), i.e., the inverter current i_L is in phase with the grid voltage V_g. This assumption is true for PV grid-connected inverter (unity PF between the in-grid current and the grid voltage). The high frequency inverter switching pulse (f_s) must be stopped at the time $x\pi$ in order to confirm the zero-inverter current beforehand the zero crossing of the V_g, hence the inverter current is forced to zero by the grid voltage, as shown in Figure 13.

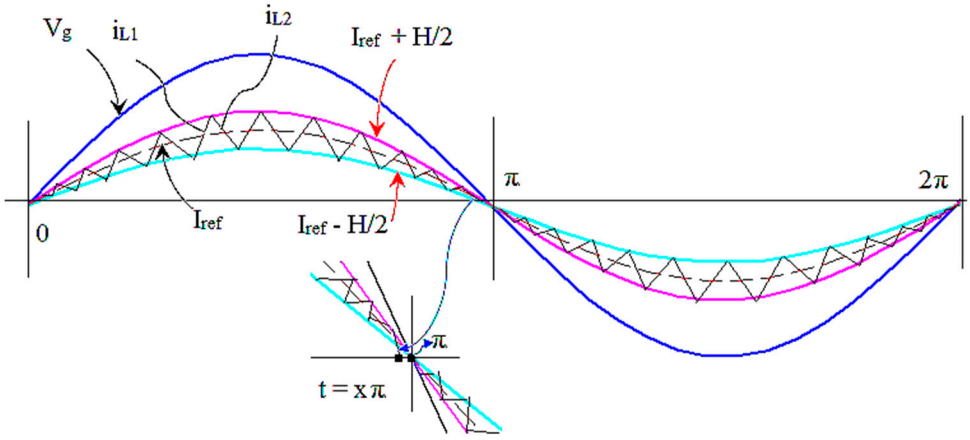


Figure 13. Phase control between grid voltage V_g and inductor current i_{L12}.

The time $x\pi$ to turn OFF the high-frequency inverter switching signals is calculated from the inverter switching action for an interval between x to *x*.

$$\frac{\int_{x\pi}^{\pi}\left[V_{g.}\sin(wt) + V_D(ON) + V_S(ON)\right]}{L} \geq I_{ref.}\sin(x\pi) + \frac{H}{2} \tag{19}$$

Here, V_D (ON) and V_S (ON) are the ON-state voltages of clamping diodes and the power switches, respectively; 'H' is the bandwidth of current hysteresis, i.e., the ripple of inductor current, and *x* is the percent of high-frequency driving signal continuance. HCC is a nonlinear controller, which has high performance, high stability, and fast dynamic response. Nevertheless the output current is widely distributed in the energy of spread-spectrum due to the unfixed switching frequency. Therefore, the filter design is highly difficult. There are many studies on hysteresis band calculation [37]; among them, the real-time regulation method that was based on the switching frequency is the effective method for the calculation of the H value. Fixed frequency HCC can be obtained by calculating the hysteresis band H while using the transient value of the V_g and output voltage of PV array. Based on that, the hysteresis band 'H' is calculated as,

$$H = \frac{V_g\left(V_{PV} - 2.V_g\right)}{V_{PV}.L.f_s} \tag{20}$$

Here, the variant parameters are V_{PV}, V_g, f_S, and fixed one is filter inductor (L)

4. Simulation Validation

The performance of the proposed PV connected three-phase three-level TL-T-MLI simulation models are performed while using MATLAB/Simulink 14.b. Here, the 2 kW PV array module is configured (series model) to feed the power to inverter with each module rated at 152.5W. The T-MLI maintains the dc-link voltage that is close to 456V by the help of two (C1 and C_2) 470μF capacitors. The inverter is connected to 230V/50 Hz utility grid via 4 mH quality split inductors, L_{x1} and L_{x2}

(where. x = a,b,c). The inverter switching frequency (f_{sw}) is maintained throughout the operation of the inverter as 5 kHz. Simulation studies are carried out in two main directions: verifying the validity of the current controller for controlling inductors current and validating the grid connection of PV tied TL inverter with zero circulating current.

Initially, the PV is set to obtain 456V DC-link voltage for T-MLI. The simple boost converter with the P&O Maximum power point tracking (MMPT) method is used to maintain the MLI DC-link as constant. Figure 14 shows the model of the PV array with the MPPT algorithm results, which is taken at various irradiations and constant cell temperature in increasing and decreasing irradiation with the oscillation of MPP voltage. From the results, it could be seen that the MPPT algorithm was able to follow the MPP of PV array within 1.5 times grid period. The inverter operation tested for variable and fixed band hysteresis. In Figures 15 and 16, the current error (Δ_{ei}) trajectory and controlled current trajectory in α-β plane for variable and fixed band hysteresis are shown. These results indicate the HCC characteristic operation and its error minimization are well worked for both bands. When the TL T-MLI operates in the HCC with a fixed band and variable band, the waveforms of i_{Lref} and i_{Lact} are shown in Figure 17. From the results, it can be viewed that i_{Lact} visibly tracks i_{Lref} and minimizes the error by using the proposed HCC for both the fixed band and variable hysteresis band, which ensure the perfect inverter current synchronous with grid voltage. Figure 18a,b shows the inverter leg inductor currents (i_{L1} to i_{L6}) for variable and fixed band hysteresis. It shows that all of the inductors are properly and identically charged. Hence, three-phase inverters current are equal to each other.

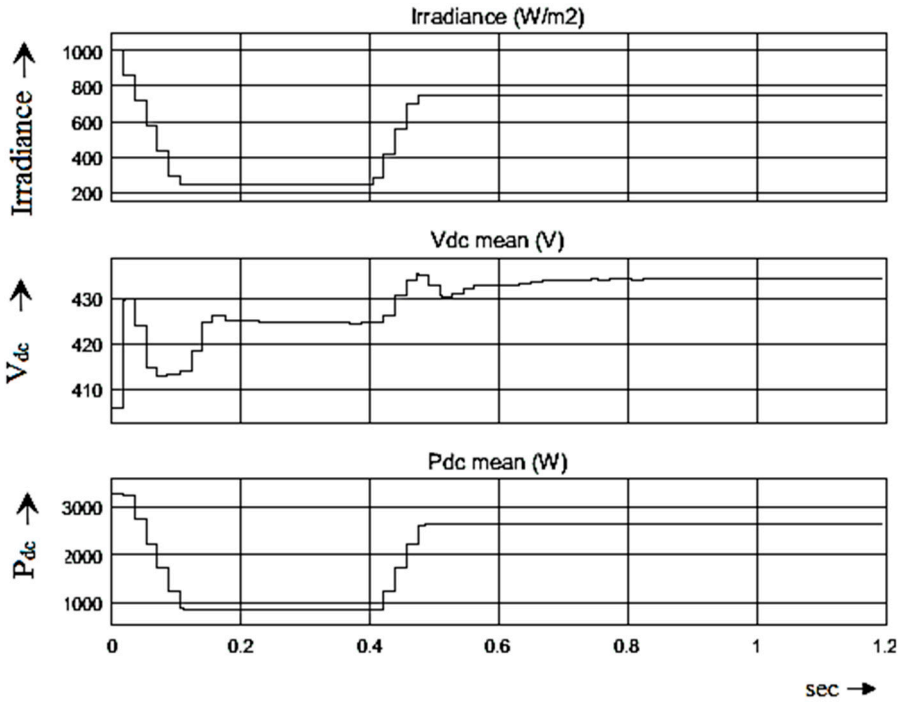
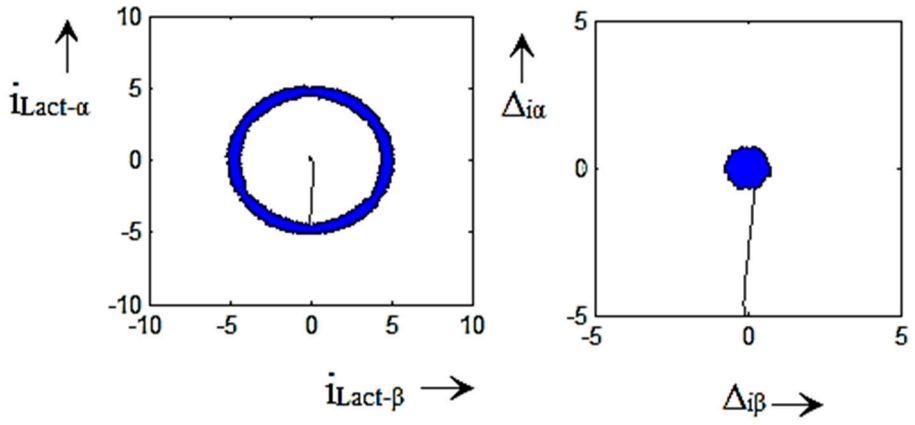
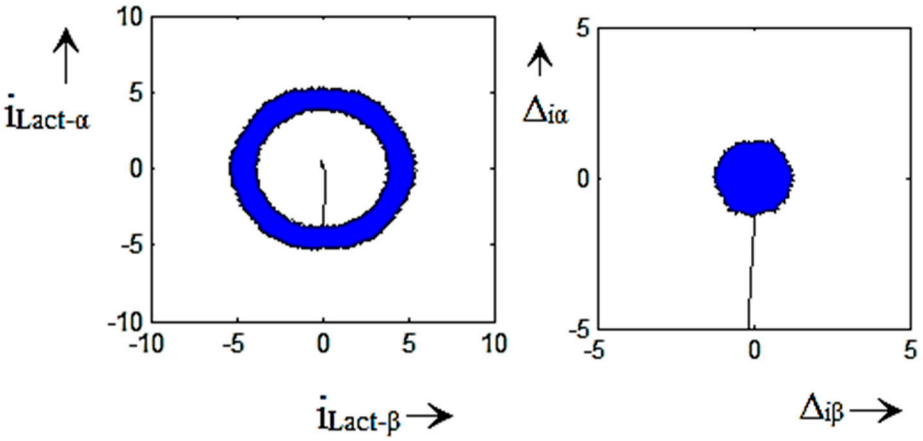


Figure 14. PV array performance for different irradiance.



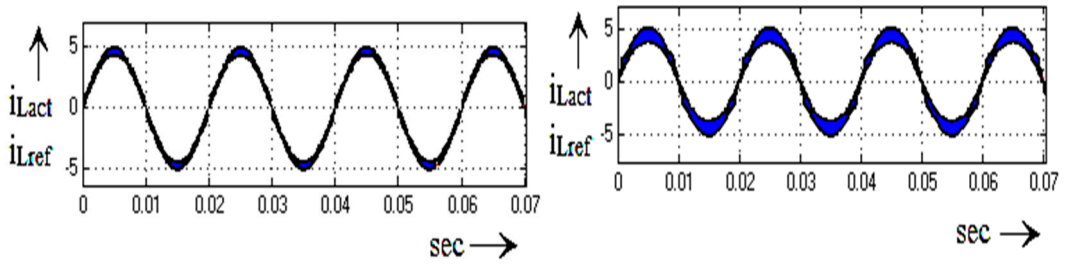
(a) (b)

Figure 15. Current error (Δ_{ei}) trajectory and controlled current trajectory in α-β plane for variable and fixed band hysteresis. (**a**). $i_{Lref-\alpha}$ and $i_{Lact-\beta}$ Trajectory (**b**). $\Delta_{i\ \alpha}$ and $\Delta_{i\ \beta}$ Trajectory.



(a) **(b)**

Figure 16. Current error (Δ_{ei}) trajectory, and controlled current trajectory in α-β plane for variable and variable band hysteresis. (**a**). $i_{Lref-\alpha}$ and $i_{Lact-\beta}$ Trajectory (**b**). $\Delta_{i\ \alpha}$ and $\Delta_{i\ \beta}$ Trajectory.



(a) **(b)**

Figure 17. i_{Lact} and i_{Lref} tracking; (**a**) variable hysteresis band, (**b**) variable and variable band Hysteresis.

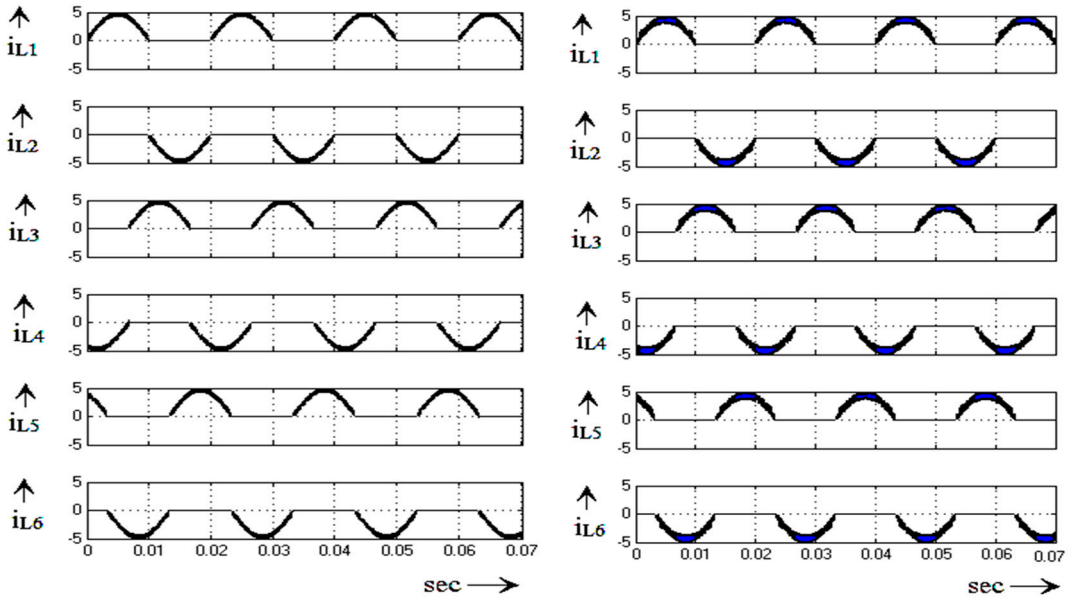


Figure 18. Inverter leg inductor currents (i_{L1} to i_{L6}); (**a**) while applying fixed hysteresis band, (**b**) while applying variable hysteresis band.

Figure 19 shows the waveforms of grid voltage V_a,V_b,V_c and inverter current i_a,i_b,i_c. The one cycle V_g and i_a is given in Figure 20. Based on Figure 20 (zoomed waveform), it could realize that V_g and I_{inv} are meeting together in the zero crossing point for ensuring the perfect grid synchronization. The harmonics spectra of the inverter current and inverter voltage are carried out up to the 500th order (25 kHz/50Hz), as shown Figure 21; it can be seen the THD percentages for both are less, as 14.52% and 9.14%, respectively.

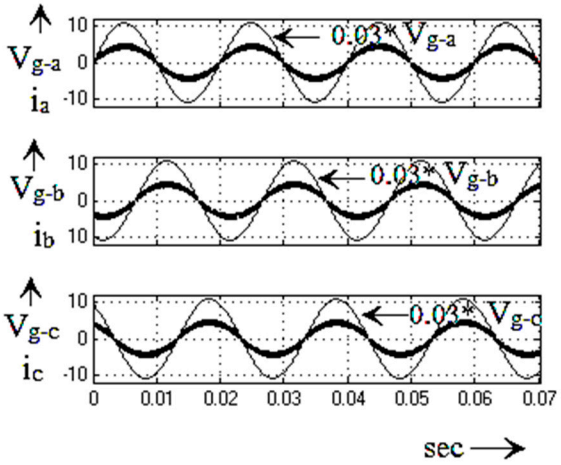


Figure 19. Waveforms of grid voltage V_a,V_b,V_c, and inverter current i_a,i_b,i_c.

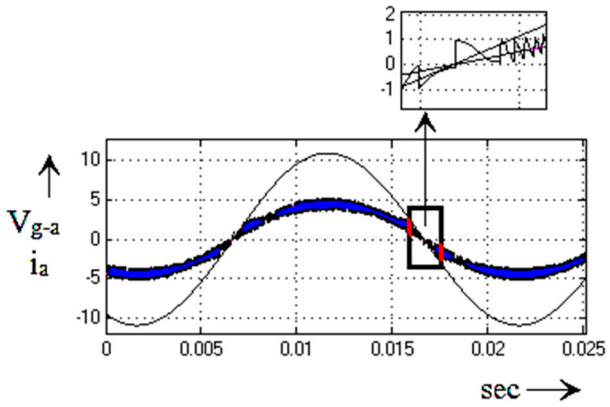


Figure 20. V_g and I_{inv} waveforms of proposed PV-grid connected TL-TNPC-MLI.

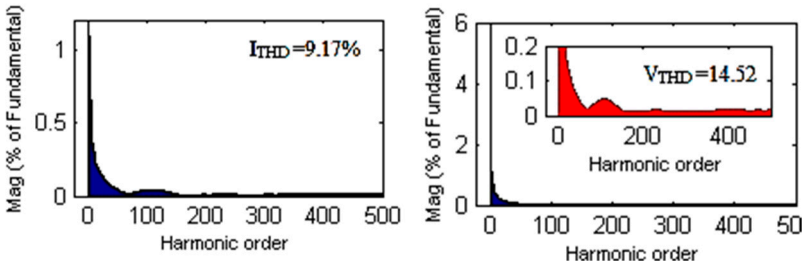


Figure 21. Harmonics spectra of the inverter current and inverter voltage. (**a**). Current THD (**b**). Voltage THD.

Figure 22 shows the performance of the inverter, when there is a change in grid frequency and current magnitudes, here the actual current reaches the reference current by using constant-frequency in 1/5 of the grid frequency interval itself. Figure 23 shows the leakage current of the inverter is observed as very low (100mA), which is close to zero. Based on the waveform, it could clearly understand that the proposed inverter fully mitigates the CM leakage current. Figure 24 shows the performance of the PV tied grid-connected inverter in different grid variations.

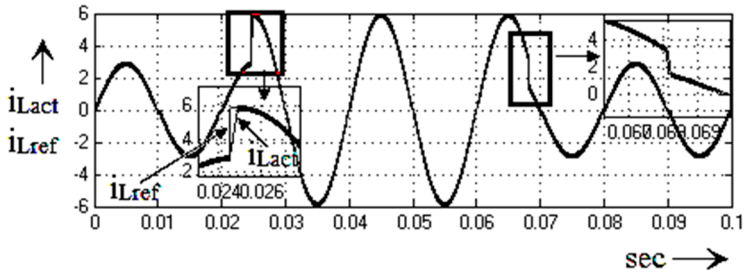


Figure 22. Performance of the PV tied grid connected TL-TMLI by change in grid current i_{Lref}.

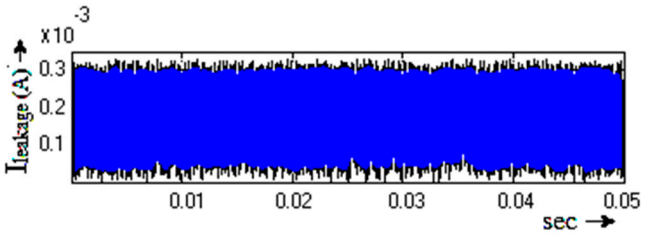


Figure 23. Common-mode, $i_{leakage}$.

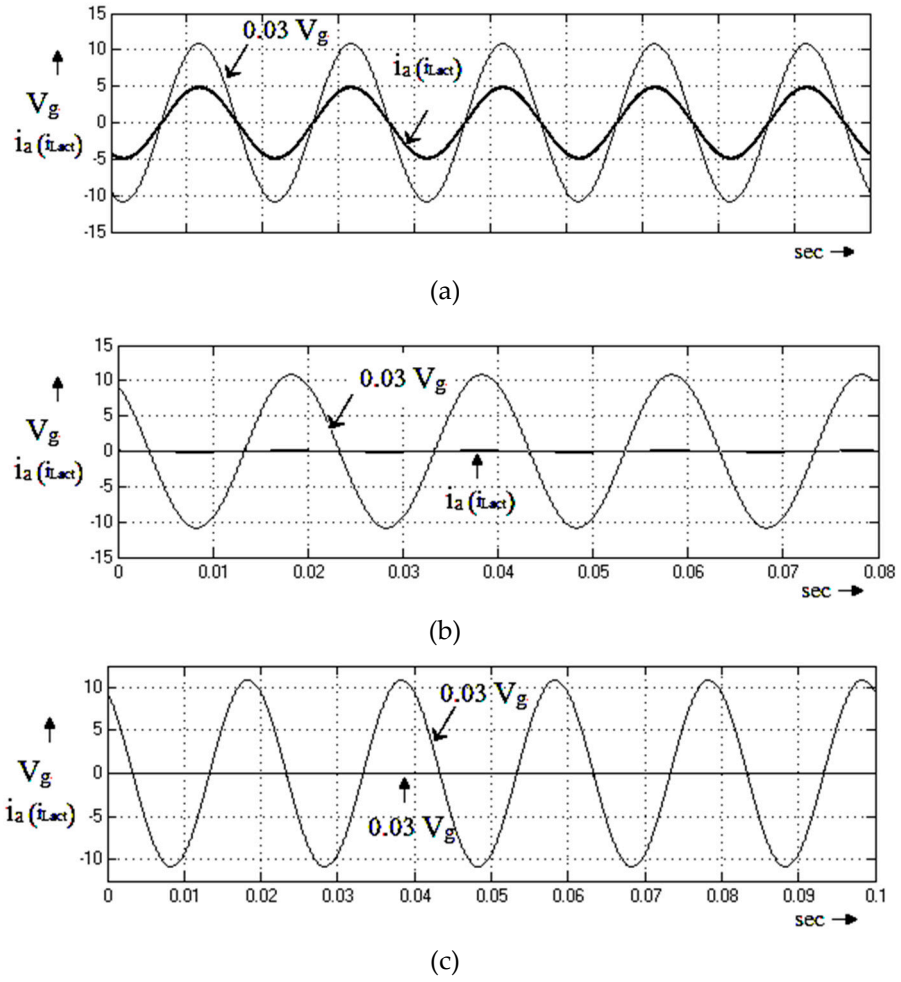


Figure 24. Steady operation waveform with different grid-current command under variable-band constant-frequency HSVCC; (**a**) rated current, (**b**) 5% of rated grid current, and, (**c**) Zero-grid-current reference.

Next, the proposed system is investigated under dynamic condition, when there is an abrupt rise and drop on the grid-current, grid voltage, and PV input voltage, as shown in Figure 25 and 26. Figure 25 illustrates the performance of the PV tied grid connected TL-TMLI by a change in grid voltage V_g. Here, the grid voltage rises at 2.2ms from 230V to 250 V. Figure 26 illustrates the PV voltage variation at 3 msec from 400V to 500V. The proposed controller operated well for both the grid voltage rise and the PV voltage rise. The same way when there are sudden changes in V_g and PV input voltage, the inverter interfacing manipulations on HCC react soon to obtain the actual current matching with the reference current.

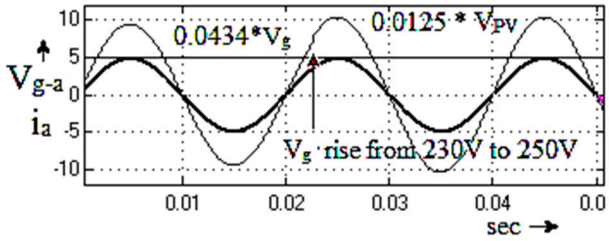


Figure 25. Performance of the PV tied grid connected TL-TMLI by change in grid voltage V_g.

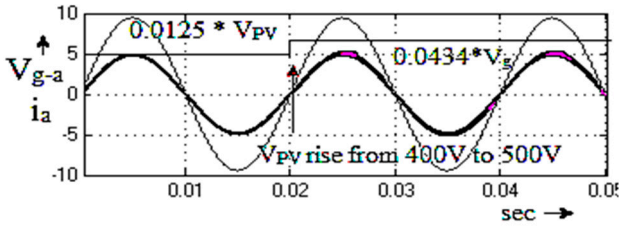


Figure 26. Performance of the PV tied grid connected TL-TMLI by change in PV input voltage V_{PV}.

Next, the inverter performance is tested with HSVCC for different operation frequencies. Figure 27 presents the transient response of current for step change (at 0.023sec from 50Hz to 60Hz) in the frequency of the reference current. From the tested results, it is confirmed that the proposed HSVCC also exhibits superior performance in transient state.

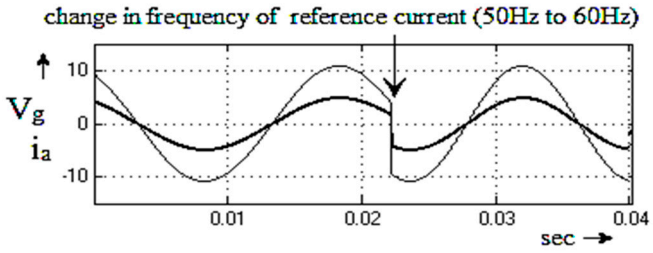


Figure 27. Transient response of the PV tied grid-connected inverter by change grid frequency.

5. Experimental Result

A 1.5kW prototype (shown in Figure 28) is built and CM leakage current elimination SVM signals are produced and tested on a Spartan-III field-programmable gate array (FPGA) board in order to confirm the performance of the proposed topology based 2kW roof-top PV grid connected system, which was programmed through the MATLAB/Simulink-system generated Xilinx tool. The specifications laboratory prototype proposed system parameters are listed; PV output based dc-link voltage = 400, DC-link capacitance C_1=C_2 = 100mF, stray capacitance (used a thin-film capacitor) =100nF, maximum m_a = 0.9, output active, three phase filter inductance L_f=1mH, filter resistance R_f = 10Ω, fundamental frequency f =50Hz, switching frequency f_s = 10kHz, dead time t_D= 4μs. All of the collaborative results were measured by a digital oscilloscope (DSO)) Tektronix MDO4034B-3 and Yokogawa power analyzer. Figure 29 shows the phase-A inverter leg inductor currents (i_{L1a} and i_{L2a}). It shows that the both inductors are charged properly and identically. Similarly, other inverters phase legs -B and C inductors $i_{L1b,}$ i_{L2b} andi_{L1c}, i_{L2c} also maintains identical nature, like phase-A inductors. Hence, the three-phase inverters currents are equal to each other. Figure 30 shows the inverter current (i_{inv}) and Figure 31 shows the inverter voltage. The inverter current harmonics profile is measured and is given in Figure 32. Here, the percentage current THD is observed as 10.251% and all higher harmonics are eliminated. Figure 33 shows the numerical harmonics values for inverter voltage and current. From the results, it could observe that the percentage voltage THD is about 18.051. Here, the third order harmonics is predominant and all other higher orders are very low. Figure 34 shows the i_L and V_g, and inverter $i_{leakage}$. In order to show that the interface between V_g and i_L, the V_g and I_L are measured in the same scope window as 600V/div and 5A/div, respectively. Based on the waveform, it can be seen that V_g and I_L are meeting together in the same zero crossing point for ensuring the grid synchronization. The second scale of Figure 34 showing leakage current of the inverter is observed as very low (200mA), which is close to zero. This value is less than the threshold value referred to VDE0126-1-1, IEC 60755, and VDE-AR-N-4105 PV tied grid connected TLI codes. Figure 35 illustrates the phasor angle of inverter and the grid voltage and current, which confirms the perfect phase sequence of inverter grid interface. With respect to PV input, the proposed PV tied

gird connected T type NP-MLI transformerless topology maintains that the efficiency is more 95% in all PV conditions. Based on the above discussed experimental results of the proposed TL PV tied grid connected system, not only the removing the transformer and inverter leg leakage current. It is also ensuring the enhanced performance such as accuracy in voltage and current waveform, quicker converging speed with smaller amount of response time, no steady-state oscillation around the PVs maximum power point values.

Figure 28. Experimental setup of PV tied reconnected tranformerless T-MLI.

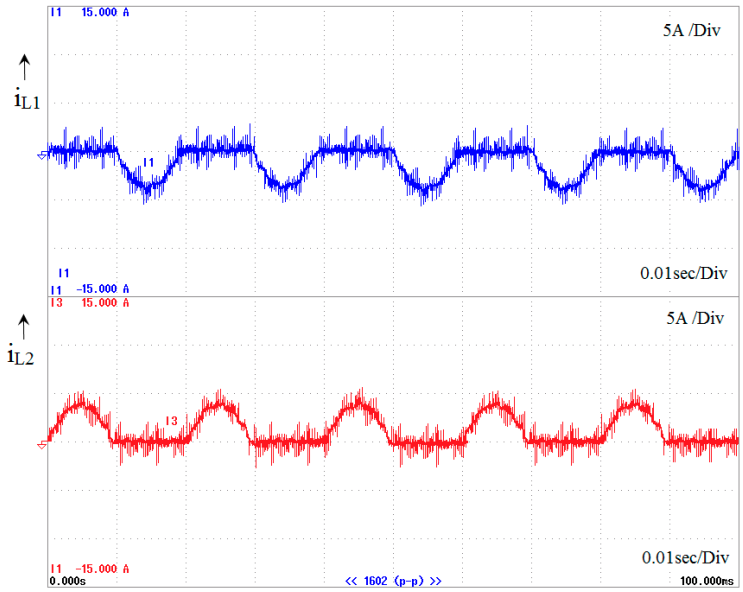


Figure 29. Inverter leg inductor currents ($i_{L1a}$and i_{L2a}).

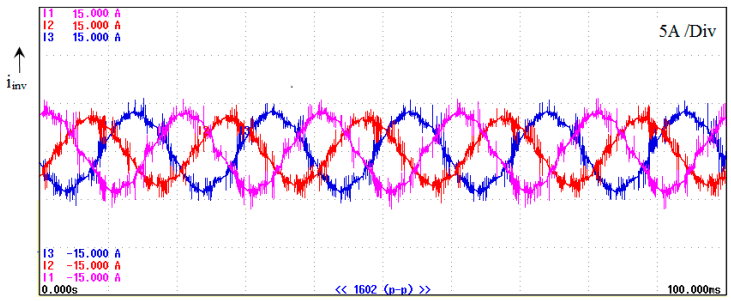


Figure 30. Three phase inverter current (I_{inv}).

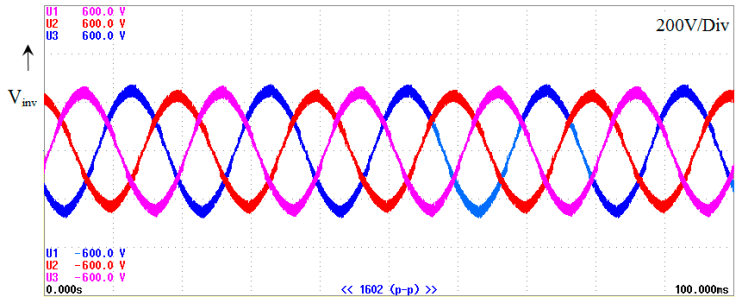


Figure 31. Three phase inverter voltage.

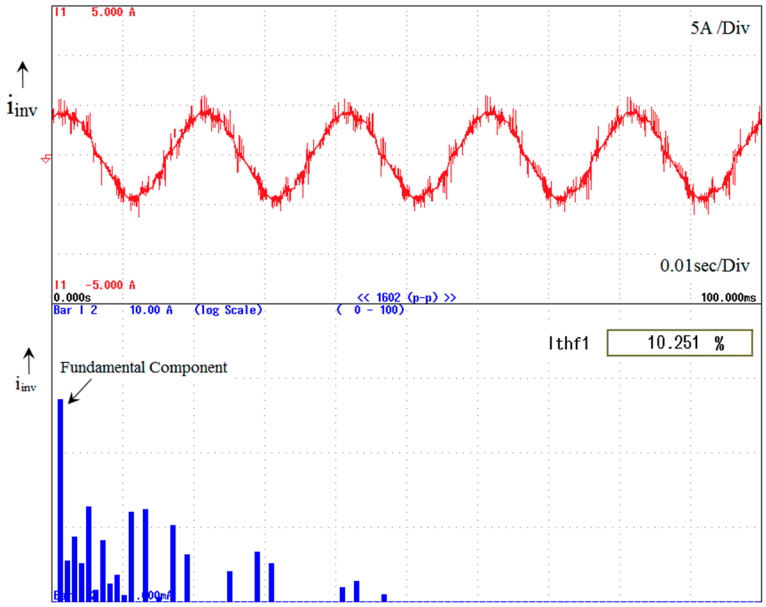


Figure 32. Inverter current (i_L) and harmonics spectra.

			Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]
fPLL1:U1	49.902	Hz	Total	293.51		dc	---------	-------
fPLL2:U2	49.894	Hz	1	288.69	98.357	2	0.54	0.183
			3	3.14	1.068	4	0.40	0.138
Urms1	297.76	V	5	43.20	14.717	6	0.19	0.064
Irms1	0.6413	A	7	21.29	7.253	8	0.41	0.141
P1	123.89	W	9	0.55	0.188	10	0.31	0.107
S1	190.95	VA	11	4.45	1.515	12	0.06	0.020
Q1	145.30	var	13	1.56	0.531	14	0.11	0.037
λ1	0.6488		15	0.52	0.176	16	0.15	0.050
Φ1	G49.55	°	17	1.19	0.406	18	0.19	0.066
			19	2.36	0.806	20	0.20	0.069
Uthd1	18.051	%	21	0.40	0.138	22	0.11	0.037
Ithd1	10.251	%	23	7.02	2.391	24	0.18	0.061
Pthd1	2.340	%	25	8.38	2.855	26	0.24	0.083
Uthf1	11.581	%	27	0.25	0.084	28	0.22	0.075
Ithf1	2.517	%	29	9.50	3.236	30	0.23	0.079
Utif1	---O F---		31	8.71	2.968	32	0.25	0.085
Itif1	---O F---		33	0.07	0.025	34	0.11	0.038
hvf1	7.286	%	35	5.69	1.939	36	0.30	0.101
hcf1	4.419	%	37	3.95	1.344	38	0.36	0.121
Kfact1	1.6793		39	0.10	0.033	40	0.14	0.047
PAGE 1/11							PAGE 1/13	

Figure 33. Numerical harmonics spectra of inverter voltage and inverter current.

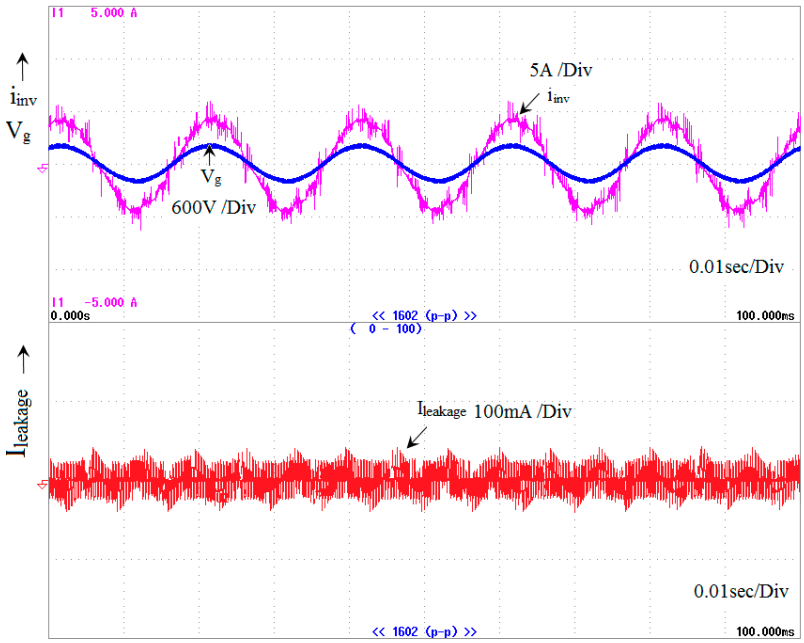


Figure 34. Inverter current (I_L) and grid voltage (V_g), and inverter leakage current.

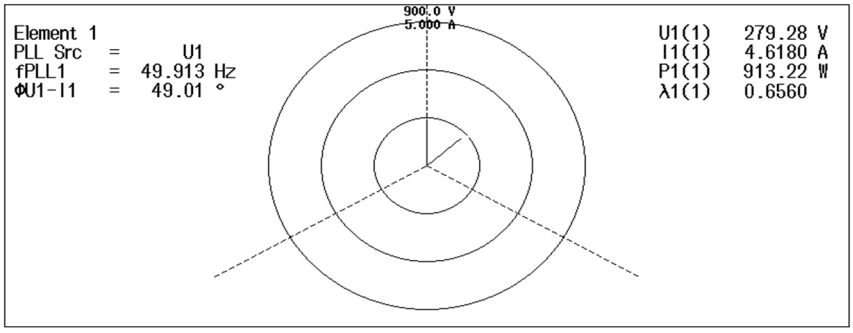


Figure 35. Phasor angle of inverter and grid voltage and current.

6. Conclusions

The interested on photovoltaic tied transformerless inverter topologies and its grid interface techniques are increasingly engrossed for the benefit of high efficiency, reliability, and low cost. The main issue in the transformerless inverter is CMV, which causes the switching-frequency leakage current. The single-phase inverter and two-level topologies are well developed with additional switches and components for eliminating the CMV. Even through there are trust topologies presented in literature, MLIs based grid connected transformerless inverter topology is being researched to avail the additional benefits from MLI, such as lower device breakdown voltage, smaller harmonics effect in the output voltage, good reliability, and long life span.

With above aim, this paper has proposed three-phase three-level T type NP-MLI topology with transformerless PV grid connected proficiency. The proposed MLI is successfully connected with the PV and grid connected system with the help of improved space vector modulation technique to mitigate the CM leakage current.

First, the paper analyzed the three-phase PV tied grid connected transformerless inverter in detail and derived the mathematical model for CMV, DMV, and common mode leakage current. Subsequently, followed by CMV model, the inverter switching function equation is derived for the opportunity of leakage current mitigation. Second, the paper proposed the PV gird interfaced closed model for three-phase three-level T type NP-MLI topology with help of improved space vector modulation technique for controlling the current and mitigating the CM leakage current. The combined space vector

and hysteresis current control has been proposed based on the behavior and requirements of the grid connected standards. The proposed arrangements are confirmed by MATLAB/Simulink simulations and FPGA based 1.5 kW PV tied TL-TNP-MLI grid connected experimentations. The simulation and experimental results significantly recognized that the proposed PV tied gird connected T type NP-MLI transformerless topology is observed as very low CM leakage current (200mA) for all PV and inverter operation conditions. The results are demonstrated and presented in the good stability of steady state and dynamics performances. The proposed inverter reduces current as well as voltage harmonics, and reduction leakage (current near to zero), which makes a significant reduction in harmonics filter and the complete elimination of CMV suppressions choke receptivity.

Author Contributions: All authors are involved developing the concept, simulation and experimental validation and to make the article error free technical outcome for the set investigation work.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

$C_{G\text{-}PV}$	parasitic capacitances
V_{CM}	Common mode voltage
V_{DC}	DC-link voltage
I_{CM}	Leakage current
V*	SVM Reference voltage
V_Z	Zero voltage vector
V_S	Small voltage vector
V_M	Medium voltage vector
V_Z	Large voltage vector
I_{TCM}	Total leakage current
V_α and V_β	α and β SVM coordinated voltage
i_{ref}	Reference current
i_{act}	Actual current
$\vec{\varepsilon_i}$	Error current
u(t))	Control input
m_a	Modulation index
f_s	Frequency inverter switching pulse
f	Grid frequency inverter switching pulse
V_g	Grid voltage
Δ_{ei}	current error
TL	Transformerless inverter
TNP-MLI	Neutral point multilevel inverter
SVM	Space vector modulation
DMV	Common mode voltage
SVD	Space vector diagram
HCC	hysteresis current control
HSVCC	hysteresis Space vector current control
MMPT	Maximum power point tracking

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