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Double Stage Double Output DC–DC Converters for High Voltage Loads in Fuel Cell Vehicles

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Abstract: This article aims to enhance the output voltage magnitude of fuel cells (FCs), since the actual generation is low. The traditional technique is too complicated and has a cascaded or parallel connection solution to achieve high voltage for multiple loads in vehicles. In this case, electronic power converters are a viable solution with compact size and cost. Hence, double or multiple output DC–DC converters with high voltage step up are required to feed multiple high voltage loads at the same time. In this article, novel double stage double output (DSDO) DC–DC converters are formulated to feed multiple high voltage loads of FC vehicular system. Four DSDO DC–DC converters called DSDO L–L, DSDO L-2L, DSDO L-2LC, and DSDO L-2LC are developed in this research work and all the converters are derived based on the arrangement of different reactive networks. The primary power circuitry, conceptual operation, and output voltage gain derivation are given in detail with valid proof. The proposed converters are compared with possible parallel combinations of conventional converters and recently available configuration. Comprehensive numerical simulation and experimental prototype results show that our theoretical predictions are valid and that the configuration is applicable for real time application in FC technologies for 'more-electric vehicles'.

Keywords: DC–DC; double stage; double output; fuel cell; step-up; vehicular system; X–Y converter family

1. Introduction

In electric grid, hybrid 'more-electric vehicles', automobile high-intensity discharge headlamps, uninterruptible power supply, and luxury loads application multiport and multilevel power converters popular solutions [1–4]. Some advanced predictive control based on the multilevel converter is also proposed for energy storage [5,6]. Fuel cells have many features, including compatibility, size, and modularity [7,8]. However, the amalgamation of series and parallel FCs is not a suitable solution for generating high DC voltage/current. Trade-off loss increases the cost of the system and requires a large space. Furthermore, the major obstacles facing FC technology are durability, low generated voltage, and to fulfill the voltage demand of high voltage loads in FC vehicles. In such cases, power electronic DC–DC converters with high voltage conversion ratios and high efficiency play a pivotal control role [9–12]. Theoretically, a moderate or high output voltage is obtained from a traditional boost converter by operating in an extreme duty cycle. Adverse effects at extreme duty ratio lead to reduced controllability, increased switching losses, high conduction losses, large current ripple, high current and voltage ratings, and reverse diode recovery problems [13–16]. Consequently, traditional DC–DC converters are not suitable candidates for FC electric vehicle applications.

Previous research has achieved high voltage conversion ratio by using a cascaded traditional boost converter configuration. However, cascaded converter configurations have low efficiency and high cost due to the increased number of high voltage/current rating semiconductor devices and reactive

elements [17,18]. Further, for implementation, they need complex control logic and increased driver modules to protect and control the semiconductor devices. Quadratic boost converters achieve a high voltage conversion ratio, but high current/voltage rating components/devices and the internal resistance of the inductors limits the output voltage [19]. Multistage diode/capacitor-based DC–DC converters have been proposed to achieve high voltage gain [20–24]. However, multiple discharging/charging loops of the capacitors lead to increased conduction loss, cost, and size, and reduced efficiency due to their parasitic nature. Converters have been proposed to get multiple outputs from a single input source by using push-pull, half-bridge, full-bridge, and fly-back converter topologies [25–27]. In all cases, high voltage is obtained with a high transformer rating on the primary side. Therefore, these converters cannot provide a proper solution for low weight/cost applications.

The parallel configurations of traditional converters such as boost, buck-boost, Cuk, single ended primary inductance converter (SEPIC), and ZETA can be possible solutions to achieve multiple outputs. The power circuitry of possible configurations without common front-end structure are shown in Figure 1a–e. These configurations provide two outputs using two different control switches. However, the voltage gain is not significantly improved, even when using a large number of components and devices. Furthermore, in order to reduce the component or device counts, common front-end structure can be a solution, as shown in Figure 1f–j. These configurations provide dual output using common front-end structures. However, only a few input side components are used, the device count is reduced, and the voltage gain is limited. Moreover, the current rating of the components is increased due to the common structure. In order to reduce the component count, hybrid converters are another possible solution. Moreover, hybrid Cuk, SEPIC, and ZETA converter configurations can achieve multiple outputs. A combination of Cuk and SEPIC converter structure was employed in [28]. Figure 2a shows the SEPIC-Cuk converter circuitry with common front-end design and dual output. A combination of ZETA and buck-boost converter structure was employed in [29].

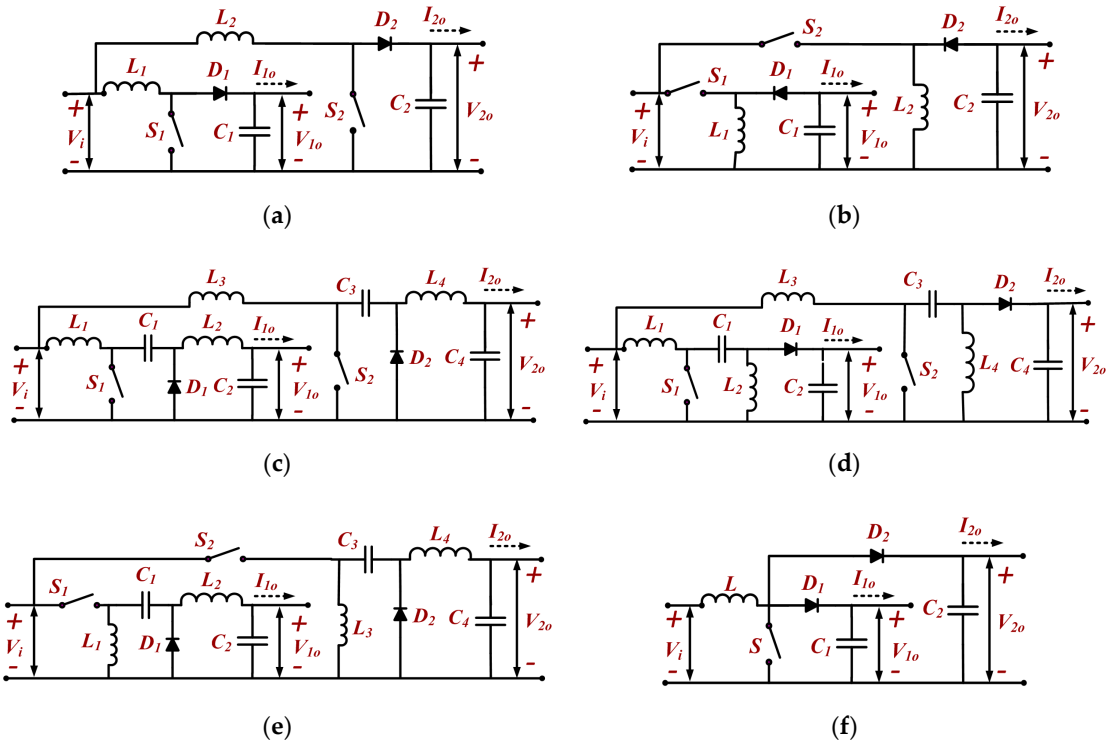


Figure 1. *Cont.*

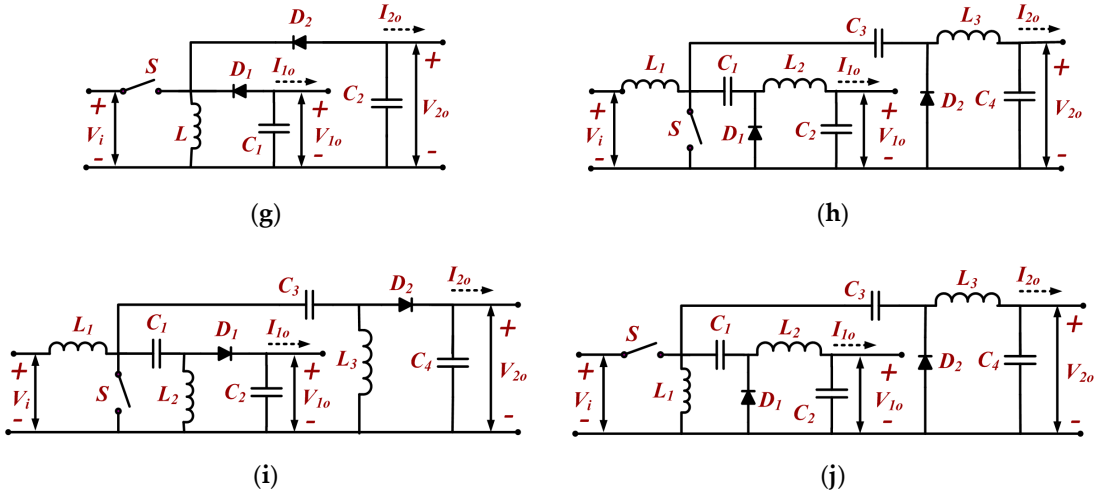


Figure 1. Power circuit of conventional parallel converters: (**a**) boost-boost converter; (**b**) buck-boost-buck-boost converter; (**c**) Cuk-Cuk converter; (**d**) single ended primary inductance converter (SEPIC)-SEPIC converter; (**e**) ZETA-ZETA converter; (**f**) boost-boost converter with common front-end structure; (**g**) buck-boost-buck-boost converter with common front end structure; (**h**) Cuk-Cuk converter with common front-end structure; (**i**) SEPIC-SEPIC converter with common front-end structure; (**j**) ZETA-ZETA converter with common front-end structure.

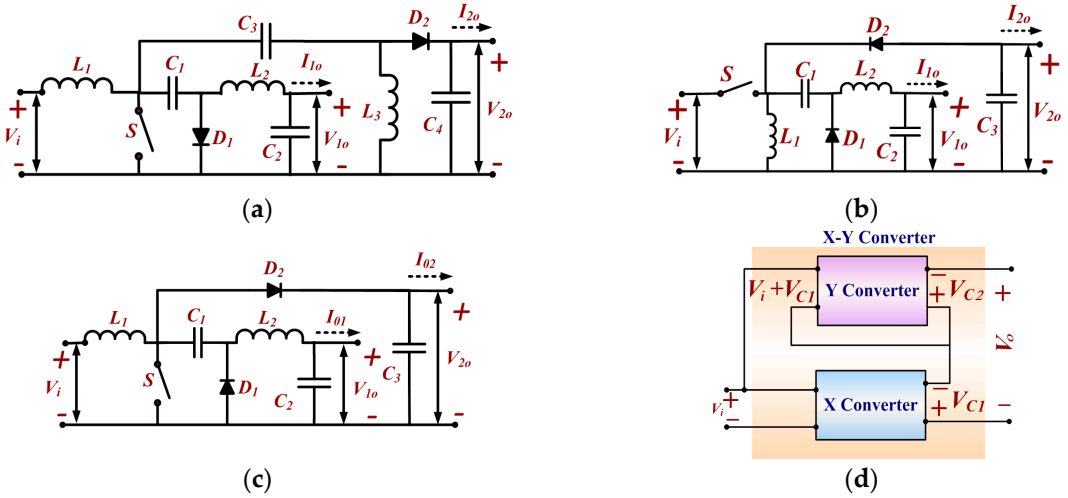


Figure 2. Power circuit of (**a**) SEPIC-Cuk converter, (**b**) ZETA–Buck-boost converter, (**c**) boost-Cuk converter; (**d**) Basic block diagram of the X–Y converter family.

Figure 2b shows the circuitry of a ZETA–Buck-boost converter with common front-end structure and two outputs. The combination of Cuk and boost converters is employed in [30]. The circuitry of a boost-Cuk converter with common front-end and two outputs is shown in Figure 2c. The voltage conversion ratio of these topologies is limited. Furthermore, efforts have been made to reduce the switching and to obtain multiple outputs [31–33]. However, these converters have low voltage conversion ratio and are more suitable for low-power applications. The "X–Y converter family" has been proposed for high voltage output and has single switching and a capacitor stack at the output side [34–38]. The block diagram of the X–Y converter family is depicted in Figure 2d. Notable, in XY converters, the X converter is directly connected to the input supply, and the Y converter is fed from the output voltage of the X converter. The output voltage of an X–Y converter is the sum of the output voltages of the X and Y converters. In order to achieve multiple outputs and high voltage conversion ratio, this article contributes the following:

- The L–Y converters, i.e., an expanded member of the XY converter family that feeds power to two different high voltage loads. At same time, the proposed converter provides high voltage conversion ratio. A diagram of a typical fuel-cell vehicle (FCV) with a DSDO converter is shown Figure 3, where low FC voltage is fed to two high voltage loads.
- Four new original converter configurations (DSDO L–L, DSDO L-2L, DSDO, L-2LC, and DSDO, L-2LC$_m$) are derived from a single switch.
- The modes of operation, characteristics waveform, and voltage gain analysis for each proposed configuration are discussed in detail.
- The performance of the proposed converters is validated through numerical simulation and experimental prototype results.

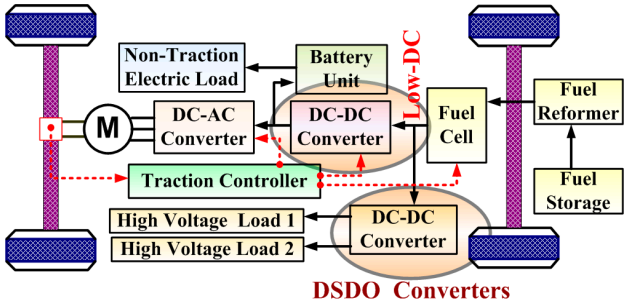


Figure 3. Typical structure of fuel cell (FC) vehicle with double stage double output (DSDO) converters.

2. Double Stage Double Output Converters

2.1. DSDO L–L Converter

Figure 4 depicts the power circuit of a DSDO L–L converter. In a DSDO L–L converter, a single switch S and input voltage V_i are arranged in two stages. Two L–L converters are employed to obtain dual output voltage. The capacitors C_1, C_2, inductors L_1, L_2, and diodes D_1, D_2, D_3 are elements of L–L converter-1. The capacitors C'_1, C'_2, inductors L'_1, L'_2, and diodes D'_1, D'_2, D'_3 are elements of L–L converter-2. The stage-1 and stage-1′ voltages are obtained across capacitors C_1 and C'_1, respectively. The stage-2 and stage-2′ voltages are obtained across capacitors C_2 and C'_2, respectively. The load R_{1o} is connected across capacitors C_1, C2, and load R_{2o} is connected across capacitors C'_1 and C'_2 to achieve double output voltages, i.e., V_{1o} and V_{2o}, from a single source input (V_i) as shown in Figure 4.

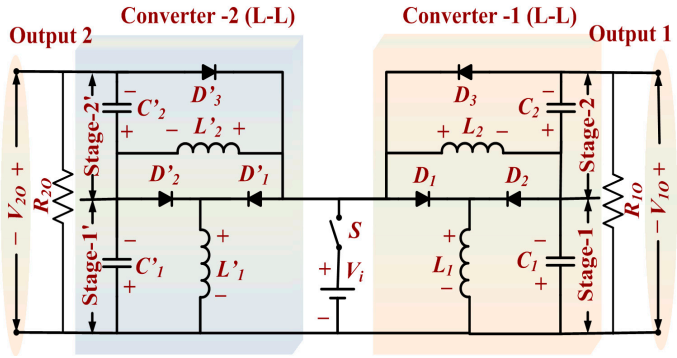


Figure 4. Power circuit of a DSDO L–L converter.

The DSDO L–L converter operates in two modes: switch S turn-ON and another when switch S turn-OFF. Figure 5 shows the characteristics of inductor voltage and current obtained for one switching cycle. Time zone A–B describes the ON time of the switch and time zone B–C describes the OFF time. The equivalent circuit for turn-ON mode is shown in Figure 6a. In this mode, inductor L_1 is magnetized

through switch S and diode D_1 from the input power of voltage V_i. At the same time, input voltage V_i and the voltage across capacitor C_1 magnetizes the inductor L_2. Total energy stored in capacitors C_1 and C_2 provide load R_{1o}. Inductor L'_1 is magnetized through switch S and diode D'_1 by the input voltage V_i. At the same time, input voltage V_i and voltage across capacitor C'_1 magnetizes inductor L'_2. The energy is delivered to load R_{2o} by capacitors C'_1 and C'_2. During turn-ON, capacitors C_1, C'_1, C_2, and C'_2 are discharged, and inductors L_1, L'_1, L_2, and L'_2 are magnetized. Throughout this mode, diodes D_1, D'_1 are forward biased and diodes D_2, D_3, D'_2, D'_3 are reverse biased.

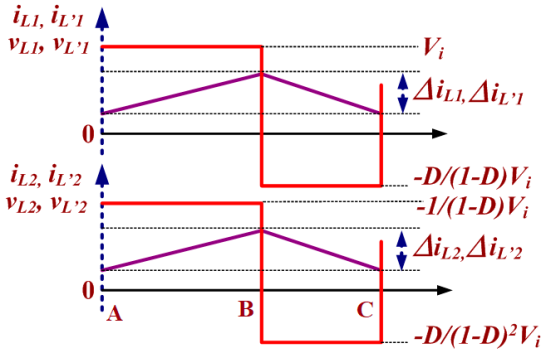


Figure 5. Waveforms of inductor voltages and currents for a DSDO L–L converter.

The voltages across inductors can be obtained as follows,

$$V_{L1} = V_i; V_{L2} = V_{C1} + V_i; V_{L'1} = V_i; V_{L'2} = V_{C'1} + V_i \quad (1)$$

The equivalent circuit for turn-OFF mode is shown in Figure 6b. In this mode, the capacitor C_1 is charged by stored energy in the inductor L_1 through diode D_2. At the same time, capacitor C_2 is charged by stored energy in the inductor L_2 through diode D_3. Energy is provided to load R_{1o} by the connection of inductors L_1 and L_2. Capacitor C'_1 is charged from stored energy in inductor L'_1 through diode D'_2. At the same time, capacitor C'_2 is charged from stored energy in inductor L'_2 through diode D'_3. Energy is provided to load R_{2o} by connection of inductors L'_1 and L'_2. In turn-OFF mode, capacitors C_1, C'_1, C_2, and C'_2 are charged and inductors L_1, L'_1, L_2, and L'_2 are demagnetized. In this mode, diodes D_1, D'_1 are reverse biased and diodes D_2, D_3, D'_2, and D'_3 are forward biased.

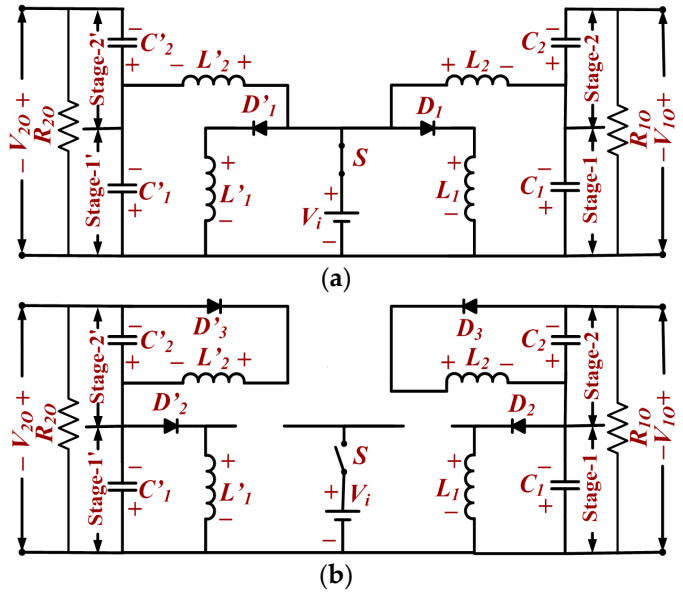


Figure 6. Equivalent circuitry of a DSDO L–L converter: (**a**) ON mode; (**b**) OFF mode.

The voltages across inductors can be obtained as follows,

$$V_{L1} = -V_{C1}; V_{L2} = -V_{C2}; V_{L'1} = -V_{C'1}; V_{L'2} = -V_{C'2} \tag{2}$$

The output voltages V_{1o} and V_{2o} are obtained as follows,

$$\left.\begin{array}{l} \frac{V_{C1}}{V_i} = \frac{V_{C'1}}{V_i} = D(1-D)^{-1}, \frac{V_{C2}}{V_i} = \frac{V_{C'2}}{V_i} = D(1-D)^{-2} \\ V_{1o} = V_{2o} = -V_i \times \left(D(1-D)^{-1} + D(1-D)^{-2}\right) \end{array}\right\} \tag{3}$$

2.2. DSDO L–2L Converter

Figure 7 illustrates the power circuit of a DSDO L–2L converter. A single switch S and input voltage V_i are employed with two-stage L–2L converters to obtain dual output voltage. The capacitors C_1, C_2 inductors L_1, L_2, L_3, and diodes D_1, D_2, … , and D_6 are elements of L–2L converter-1. The capacitors C'_1, C'_2, inductors L'_1, L'_2, L'_3, and diodes D'_1, D'_2, … , and D'_6 are elements of L–2L converter-2. The stage-1 and stage-2 voltages are taken across capacitors C_1 and C_2, respectively. The stage-1′ and stage-2′ voltages are taken across capacitors C'_1 and C'_2, respectively. The two output voltages are taken across capacitors C_1 + C_2 and C'_1 + C'_2, respectively. The load R_{1o} is connected across capacitors C_1 and C_2, and load R_{2o} is connected across capacitors C'_1 and C'_2.

The operation of a DSDO L–2L converter is sectioned into two modes: one when switch S turn-ON and another when switch S turn-OFF. Figure 8 shows the characteristic waveforms of voltage and current of the inductor for one switching cycle. In the characteristic waveform, time zone A–B describes the turn-ON time and time zone B–C describes the turn-OFF time.

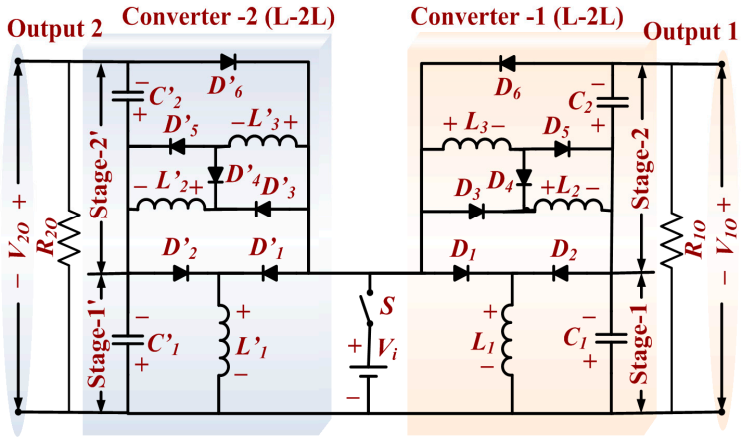


Figure 7. Power circuit of a DSDO L–2L converter.

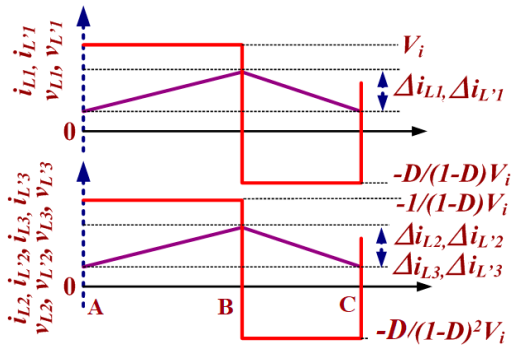


Figure 8. Waveforms of inductor voltage and current for a DSDO L–2L converter.

The equivalent circuit for turn-ON mode is shown in Figure 9a. Inductor L_1 is magnetized by the input voltage V_i. In the same interval, the input voltage V_i and voltage across capacitor C_1 magnetizes inductors L_2 and L_3. Energy is provided to load R_{1o} by capacitors C_1 and C_2. Inductor L'_1 is magnetized by the input voltage V_i. In the same interval, the input voltage V_i and voltage across capacitor C'_1 magnetize inductors L'_2 and L'_3. Energy is provided to load R_{2o} by capacitors C'_1 and C'_2. During turn-ON mode, capacitors C_1, C'_1, C_2, and C'_2 are discharged, and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are magnetized. In this mode, diodes D_1, D'_1, D_3, D'_3, D_5, and D'_5 are forward biased and diodes D_2, D'_2, D_4, D'_4, D_6, and D'_6 are reverse biased.

The voltage across inductors can be obtained as follows,

$$V_{L1} = V_{L'1} = V_i;\ V_{L2} = V_{L'2} = V_{L3} = V_{L'3} = V_{C1} + V_i \tag{4}$$

The equivalent circuit of the turn-OFF mode of a DSDO L–2L converter is shown in Figure 9b. In this mode, capacitor C_1 is charged by the stored energy of inductor L_1. At same time, capacitor C_2 is charged by the series connection of inductors L_2 and L_3. Energy is provided to load R_{1o} by inductors L_1, L_2, and L_3. Capacitor C'_1 is charged by the stored energy of inductor L'_1, whereas the capacitor C'_2 is charged by the series connection of inductors L'_2 and L'_3. Energy is provided to load R_{2o} by inductors L'_1, L'_2, and L'_3. In turn-OFF mode, capacitors C_1, C'_1, C_2, and C'_2 are charged and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are demagnetized. In this mode, diodes D_1, D'_1, D_3, D'_3, D_5, and D'_5 are reverse biased and D_2, D'_2, D_4, D'_4, D_6, and D'_6 are forward biased.

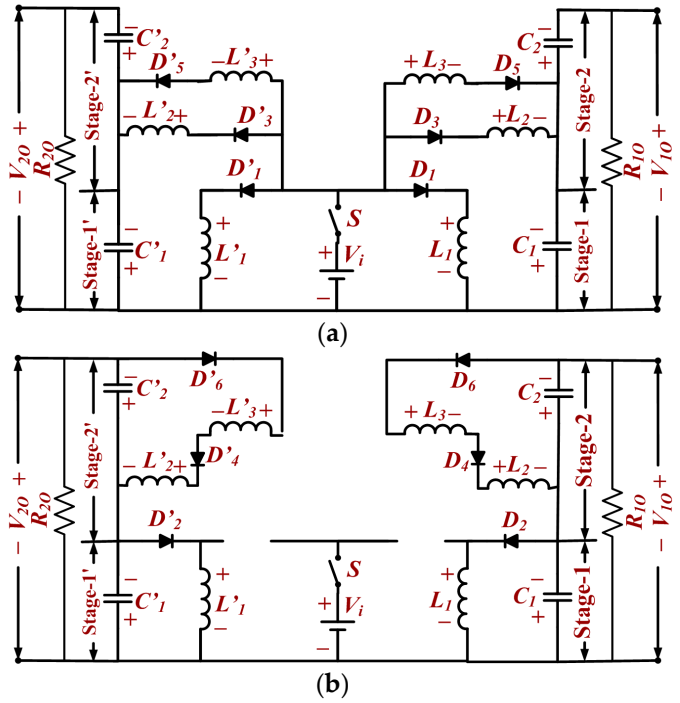


Figure 9. Equivalent circuitry of a DSDO L–2L converter: (**a**) ON mode; (**b**) OFF mode.

The voltage across inductors can be obtained as follows,

$$V_{L1} = V_{L'1} = -V_{C1}; V_{L2} = V_{L'2} = V_{L3} = V_{L'3} = -V_{C2}/2 \tag{5}$$

The output voltages V_{1o} and V_{2o} are obtained as follows,

$$\left.\begin{array}{l} \frac{V_{C1}}{V_i} = \frac{V_{C'1}}{V_i} = D(1-D)^{-1}, \frac{V_{C2}}{V_i} = \frac{V_{C'2}}{V_i} = 2D(1-D)^{-2} \\ V_{1o} = V_{2o} = -V_i \times \left(D(1-D)^{-1} + 2D(1-D)^{-2}\right) \end{array}\right\} \tag{6}$$

2.3. DSDO L–2LC Converter

Figure 10 illustrates the power circuit of a DSDO L–2LC converter. A single switch S and input voltage V_i are employed with two-stage L–2LC converters to obtain dual output voltages. The capacitors C, C_1, and C_2, inductors L_1, L_2, and L_3, diodes D_1, D_2, ... , and D_7 are elements of L–2LC converter-1. The capacitors C′, C'_1, and C'_2, inductors L'_1, L'_2, and L'_3, diodes D'_1, D'_2, ... , and D'_7 are elements of L–2LC converter-2. The stage-1 and stage-2 voltages are taken across C_1 and C_2, respectively. The stage-1′ and stage-2′ voltages are taken across capacitors C'_1 and C'_2, respectively. The load R_{1o} is connected across capacitors C_1 and C_2, and load R_{2o} is connected across capacitors C'_1 and C'_2.

The operation of a DSDO L–2LC converter is sectioned into two modes: one when switch S turn-ON and another when switch S turn-OFF. Figure 11 shows the characteristic waveforms of voltage and current of the inductor for one switching cycle. Time zone A–B describes the turn-ON time and time zone B–C describes the turn-OFF time of the switch. The equivalent circuit for turn-ON mode is shown in Figure 12a. In this interval, inductor L_1 is magnetized by the input voltage V_i. The input voltage V_i and voltage across capacitor C_1 magnetize inductors L_2 and L_3, and charge capacitor C in parallel. Energy is provided to load R_{1o} by capacitors C_1 and C_2. The inductor L'_1 magnetized by the input voltage V_i. The input voltage V_i and voltage across capacitor C'_1 magnetize inductors L'_2 and L'_3 and charge the capacitor C' in parallel. Energy is provided to load R_{2o} by capacitors C'_1 and C'_2. In turn-ON mode, capacitors C_1, C'_1, C_2, and C'_2 are discharged, capacitors C and C' are charged, and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are magnetized. In this mode, diodes D_1, D'_1, D_3, D'_3, D_5, D'_5, D_6, and D'_6 are forward biased and diodes D_2, D'_2, D_4, D'_4, D_7, and D'_7 are reverse biased.

The voltages across the inductors are obtained as follows,

$$V_{L1} = V_{L'1} = V_i;\ V_{L2} = V_{L3} = V_{L'2} = V_{L'3} = V_{C1} + V_i \tag{7}$$

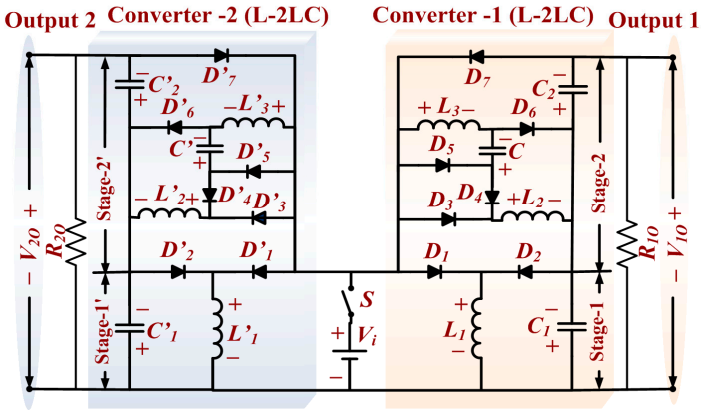


Figure 10. Power circuit of a DSDO L–2LC converter.

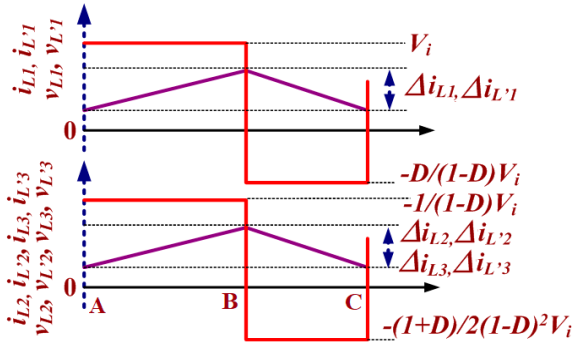


Figure 11. Waveforms of inductor voltage and current for a DSDO L–2LC converter.

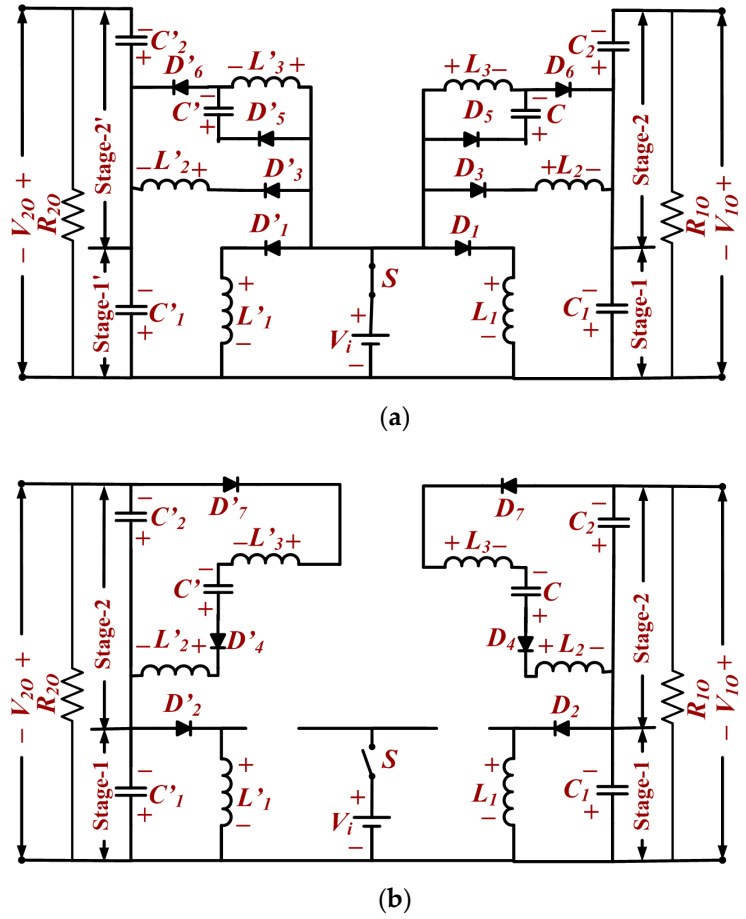


Figure 12. Equivalent circuitry of DSDO L–2LC converter: (**a**) ON mode; (**b**) OFF mode.

The equivalent circuit for turn-OFF mode of a DSDO L–2LC converter is shown in Figure 12b. The capacitor C_1 is charged by energy stored in inductor L_1. The capacitor C_2 is charged by the series connection of inductors L_2, L_3 and capacitor C. Energy is provided to load R_{1o} by inductors L_1, L_2, L_3, and capacitor C. The capacitor C'_1 is charged by stored energy of inductor L'_1. The capacitor C'_2 is charged by the series connection of inductors L'_2, L'_3, and capacitor C'. Energy is provided to load R_{2o} by inductors L'_1, L'_2, L'_3, and capacitor C'. Hence, the capacitors C_1, C'_1, C_2, and C'_2 are charged, capacitors C and C′ are discharged, and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are demagnetized. In this mode, diodes D_1, D'_1, D_3, D'_3, D_5, D'_5, D_6, and D'_6 are reverse biased and diodes D_2, D'_2, D_4, D'_4, D_7, and D'_7 are forward biased.

The voltages across the inductors can be obtained as follows,

$$V_{L1} = V_{L'1} = -V_{C1};\ (V_{L2} = V_{L'2} = V_{L3} = V_{L3}) = \frac{-(V_{C2} - V_C)}{2} = \frac{-(V_{C2} - V_{C'})}{2} \tag{8}$$

The output voltages V_{1o} and V_{2o} are obtained as follows,

$$\left.\begin{array}{l} \frac{V_{C1}}{V_i} = \frac{V_{C'1}}{V_i} = D(1-D)^{-1}, \frac{V_{C2}}{V_i} = \frac{V_{C'2}}{V_i} = \frac{(1+D)}{(1-D)^2} \\ V_{1o} = V_{2o} = -V_i \times \left(D(1-D)^{-1} + (1+D)(1-D)^{-2}\right) \end{array}\right\} \tag{9}$$

2.4. DSDO L–2LC$_m$ Converter

The DSDO L–2LC$_m$ converter is a modified version of the DSDO L–2LC converter, obtained by eliminating two diodes. Figure 13 shows the power circuit of the DSDO L–2LC$_m$ converter in which a single switch S and input voltage V_i are employed with two-stage L–2LC$_m$ converters to obtain dual

output voltages. The capacitors C, C_1, and C_2, inductors L_1, L_2, and L_3, diodes D_1, D_2, ... , and D_5 are elements of L–2LC$_m$ converter-1. The capacitors C', C'_1, and C'_2, inductors L'_1, L'_2, and L'_3, and diodes D'_1, D'_2, ... , and D'_5 are elements of L–2LC$_m$ converter-2. The stage-1 and stage-2 voltages are taken across capacitors C_1 and C_2, respectively. The stage-1′ and stage-2′ voltages are taken across capacitors C'_1 and C'_2, respectively. Load R_{1o} is connected across capacitors C_1 and C_2 and load R_{2o} is connected across capacitors C'_1 and C'_2.

The operation of a DSDO L–2LC$_m$ converter is sectioned into two modes: one when switch S turn-ON and another when switch S turn-OFF. Figure 14 shows the characteristic waveforms of voltage and current for inductors for one switching cycle. The time zone A–B describes the turn-ON time and B–C describes the turn-OFF time. The equivalent circuit for turn-ON mode is shown in Figure 15a. The inductor L_1 is magnetized by the input voltage V_i. In the same interval, the inductor V_i and voltage across capacitor C_1 magnetize inductors L_2 and L_3 and charge capacitor C in parallel. The energy is provided to load R_{1o} by capacitors C_1 and C_2. The inductor L'_1 magnetized by the input voltage V_i. In the same interval, input voltage V_i and voltage across capacitor C'_1 magnetize inductors L'_2 and L'_3 and charge capacitor C' in parallel. The energy is provided to load R_{2o} by capacitors C'_1 and C'_2. Capacitors C_1, C'_1, C_2, and C'_2 are discharged, capacitors C and C' charged, and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are magnetized. In this mode, diodes D_1, D'_1, D_3, D'_3, D_4, and D'_4 are forward biased and diodes D_2, D'_2, D_5, and D'_5 are reverse biased.

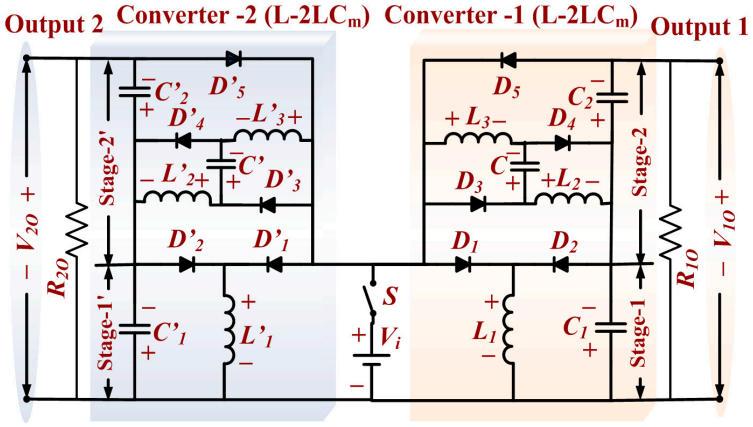


Figure 13. Power circuit of the DSDO L–2LC$_m$ converter.

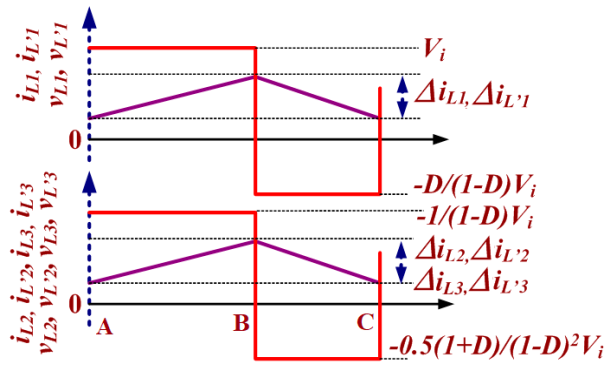


Figure 14. Waveforms of inductor voltage and current for a DSDO L–2LC$_m$ converter.

The voltages across inductors can be obtained as follows,

$$V_{L1} = V_{L'1} = V_i;\ V_{L2} = V_{L3} = V_{L'2} = V_{L'3} = V_{C1} + V_i \tag{10}$$

The equivalent circuit for turn-OFF mode is shown in Figure 15b. Capacitor C_1 is charged by the energy of inductor L_1, and capacitor C_2 is charged by the series connection of inductors L_2, L_3 and

capacitor C. Energy is provided to load R_{1o} by inductors L_1, L_2, L_3, and capacitor C. Capacitor C'_1 is charged by energy of inductor L'_1. Capacitor C'_2 is charged by the series connection of inductors L'_2, L'_3 and capacitor C'. Energy is provided to load R_{2o} by inductors L'_1, L'_2, L'_3, and capacitor C'. The capacitors C_1, C'_1, C_2, and C'_2 are charged, capacitors C and C' are discharged, and inductors L_1, L'_1, L_2, L'_2, L_3, and L'_3 are demagnetized. Throughout this mode, diodes D_1, D'_1, D_3, D'_3, D_4, and D'_4 are reverse biased, and diodes D_2, D'_2, D_5, and D'_5 are forward biased.

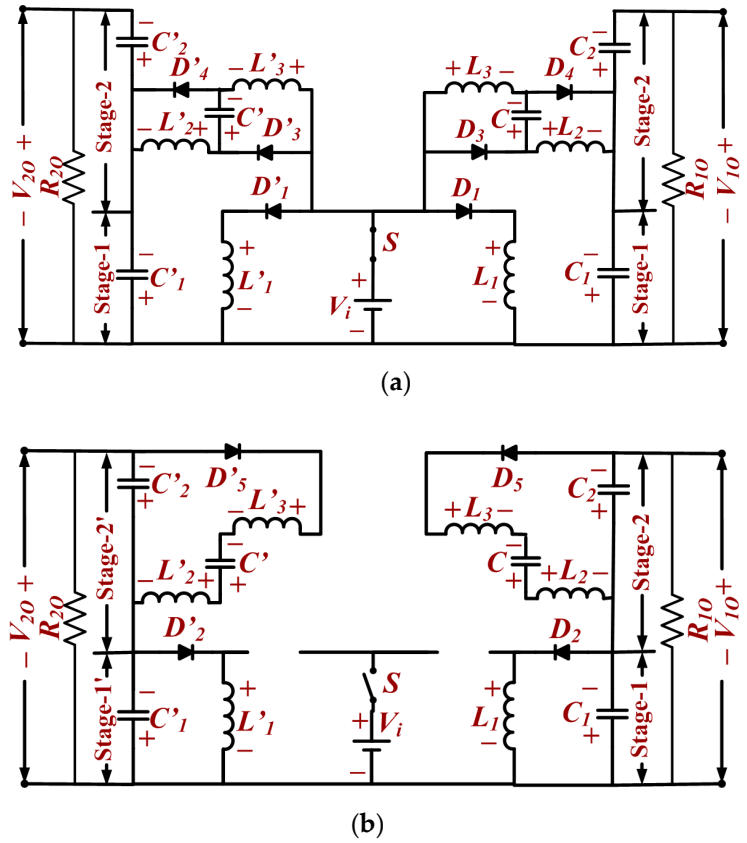


Figure 15. Equivalent circuitry of a DSDO L–2LC$_m$ converter: (**a**) ON mode; (**b**) OFF mode.

The voltages across inductors can be obtained as follows,

$$V_{L1} = V_{L'1} = -V_{C1}; (V_{L2} = V_{L'2} = V_{L3} = V_{L'3}) = \frac{-(V_{C2} - V_C)}{2} = \frac{-(V_{C2} - V_{C'})}{2} \tag{11}$$

The output voltages V_{1o} and V_{2o} are obtained as follows,

$$\left.\begin{array}{l} \frac{V_{C1}}{V_i} = \frac{V_{C'1}}{V_i} = D(1-D)^{-1}, \frac{V_{C2}}{V_i} = \frac{V_{C'2}}{V_i} = \frac{(1+D)}{(1-D)^2} \\ V_{1o} = V_{2o} = -V_i \times \left(D(1-D)^{-1} + (1+D)(1-D)^{-2}\right) \end{array}\right\} \tag{12}$$

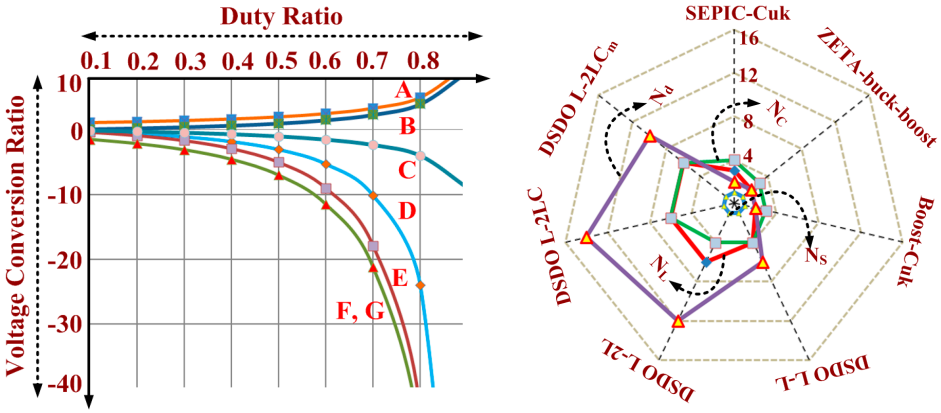
3. Comparative Study

In this section, the new DSDO converter configurations are compared with possible parallel combination of conventional converters and recently addressed DC–DC converters. Table 1 tabulates the comparison in terms of number of components and devices, voltage conversion ratio, and ratio of voltage across switch and input voltage. It is observed that one can achieve multiple output voltages by using conventional converters in parallel. However, the voltage conversion ratio is limited and not suitable for feeding high-voltage loads. Hybrid multiple output converters provide two different voltage levels while using common front-end structure. However, the voltage conversion ratio is not

significantly improved by using a hybrid structure. The proposed converter provides a higher voltage conversion ratio compared to parallel combination of the conventional converters. In Figure 16a, the voltage conversion ratios of the converters are compared graphically. It is notable that all proposed converters provide inverting high voltage with medium duty cycle. It is observed that the DSDO L–2LC and DSDO L–2LC$_m$ converters generate higher voltage conversion ratios compared to the other proposed converters and in comparison to recent DC–DC converters. Figure 16b compares the number of diodes, control switches, inductors, and capacitors. It concludes that the DSDO L–2LC$_m$ converter requires fewer diodes than the DSDO L–2LC converter, while both provide the same voltage conversion ratio.

Table 1. Comparison of Converters.

Converter	Switches	Inductors	Diodes	Capacitors	Voltage Conversion Ratio (V_{1o},V_{2o})	Voltage Stress across Switch (V_s/V_i)
Converter without common front-end structure						
Boost-Boost converter (Figure 1a)	2	2	2	2	1/1-D, 1/1-D	1/1-D
Buck-Boost-Buck-Boost converter (Figure 1b)	2	2	2	2	-D/1-D, -D/1-D	1/1-D
Cuk-Cuk Converter (Figure 1c)	2	4	2	4	-D/1-D, -D/1-D	1/1-D
SEPIC-SEPIC Converter (Figure 1d)	2	4	2	4	D/1-D, D/1-D	1/1-D
ZETA-ZETA Converter (Figure 1e)	2	4	2	4	D/1-D, D/1-D	1/1-D
Converter with common front-end structure						
Boost-Boost converter (Figure 1f)	1	1	2	2	1/1-D, 1/1-D	1/1-D
Buck-Boost-Buck-Boost converter (Figure 1g)	1	1	2	2	-D/1-D, -D/1-D	1/1-D
Cuk-Cuk converter (Figure 1h)	1	3	2	4	-D/1-D, -D/1-D	1/1-D
SEPIC-SEPIC converter (Figure 1i)	1	3	2	4	D/1-D, D/1-D	1/1-D
ZETA-ZETA converter (Figure 1j)	1	3	2	4	D/1-D, D/1-D	1/1-D
Hybrid multi-output converter with common front-end structure						
SEPIC-Cuk converter (Figure 2a)	1	3	2	4	-D/1-D, D/1-D	1/1-D
ZETA–Buck-boost converter (Figure 2b)	1	2	2	3	D/1-D, -D/1-D	1/1-D
Boost-Cuk converter (Figure 2c)	1	2	2	3	-D/1-D, 1/1-D	1/1-D
Proposed DSDO converter configurations						
DSDO L–L converters (Figure 4)	1	4	6	4	$D(1-D)^{-1}$ + $D(1-D)^{-2}$	1+ $D(1-D)^{-1}$ + $D(1-D)^{-2}$
DSDO L–2L converters (Figure 7)	1	6	12	4	$D(1-D)^{-1}$ + $2D(1-D)^{-2}$	1+ $D(1-D)^{-1}$ + $2D(1-D)^{-2}$
DSDO L–2LC converters (Figure 10)	1	6	14	6	$D(1-D)^{-1}$ + $(1 + D)(1-D)^{-2}$	1+ $D(1-D)^{-1}$ + $(1 + D)(1-D)^{-2}$
DSDO L–2LC$_m$ converters (Figure 13)	1	6	10	6	$D(1-D)^{-1}$ + $(1 + D)(1-D)^{-2}$	1+ $D(1-D)^{-1}$ + $(1 + D)(1-D)^{-2}$



(**a**) (**b**)

Figure 16. Comparison of (**a**) voltage conversion ratio versus duty cycle and (**b**) number of diodes (N_d), number of capacitors (N_C), number of Switches (N_S), and number of inductors (N_L). A: Boost, B: SEPIC, C: Cuk or Buck-Boost, D: DSDO L–L, E: DSDO L–2L, F: DSDO L–2LC, G: DSDO L–2LC$_m$ converters.

4. Simulation and Experimental Results

The principle and performance of the proposed DSDO converter configurations are validated through numerical simulation software. The converters were designed and tested with two loads, each rated to 100 W with a single input voltage of 20 V and with 25 kHz switching frequency. For simulation and prototype hardware implementation, the values of the reactive components were 220 µF for capacitors and 700 µH for inductors.

DSDO L–L converter: Figure 17a shows the voltage across the two different loads R_{1o} and R_{2o}. Voltage of −105 V was generated across each load with a fixed 60% duty cycle. Figure 17b,c depicts the voltage across capacitors C_1, C'_1, C_2, and C'_2. The voltage magnitude across capacitors C_1 and C'_1 are the same, i.e., 30 V. The voltage magnitudes across capacitors C_2 and C'_2 are both 75 V. Figure 17d shows that the voltage across switch S of a DSDO L–L converter is 125 V. DSDO L–2L converter: Figure 18a shows the voltage across the two different loads R_{1o} and R_{2o}. Voltage of −180 V was generated across each load with a fixed 60% duty cycle. Figure 18b,c depicts the voltage across capacitors C_1, C'_1, C_2, and C'_2, and shows that the voltage magnitude across capacitors C_1 and C'_1 is 30 V. The voltage magnitudes across capacitors C_2 and C'_2 are 150 V. Figure 18d shows that the voltage across switch S of the DSDO L–2L converter is 200 V. DSDO L–2LC converter: Figure 19a depicts the voltage across the two different loads R_{1o} and R_{2o}. Voltage of −230 V is generated across each load with a fixed 60% duty cycle. Figure 19b,c shows the waveforms of the voltage across capacitors C_1, C'_1, C_2, and C'_2.

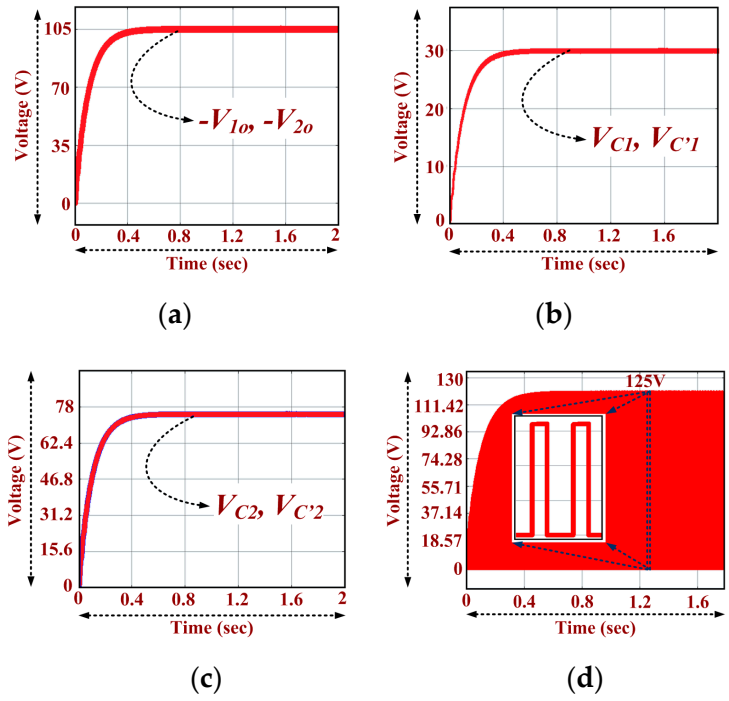


Figure 17. Simulation results of the DSDO L–L converter configuration: (**a**) Output voltages waveforms; (**b**) Voltage waveforms across stage-1 and stage-2; (**c**) Voltage waveforms across stage-1′ and stage-2′; (**d**) Voltage waveform across switch *S*.

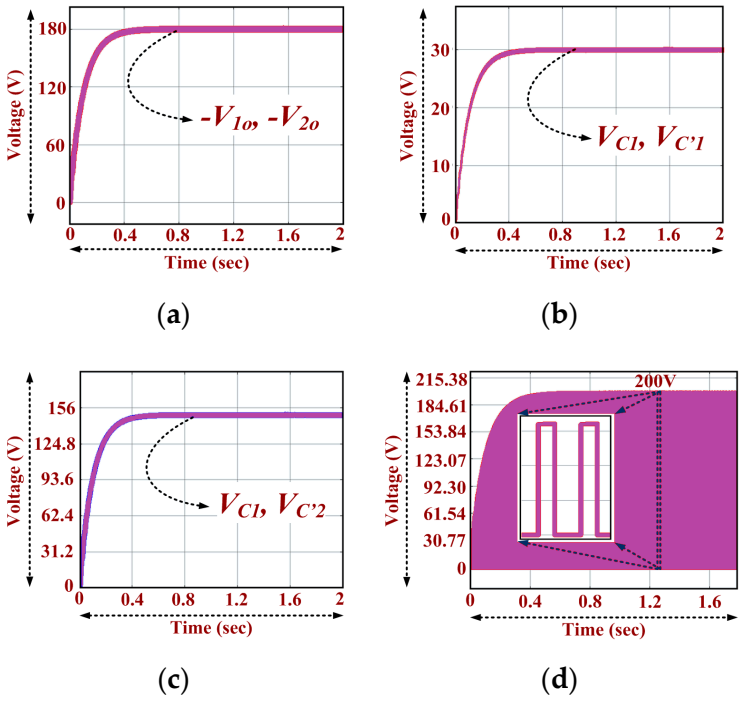


Figure 18. Simulation results of the DSDO L–2L converter configuration: (**a**) Output voltages waveforms; (**b**) Voltage waveforms at stage-1 and stage-2; (**c**) Voltage waveforms at stage-1′ and stage-2′; (**d**) Voltage waveform across switch *S*.

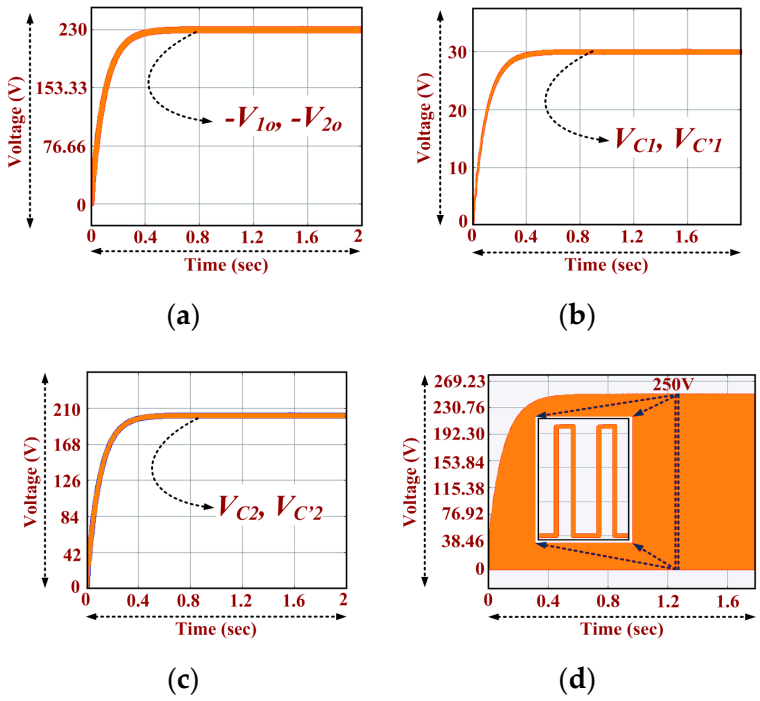


Figure 19. Simulation results of the DSDO L–2LC converter configuration: (**a**) Output voltages waveforms; (**b**) Voltage waveforms across stage-1 and Stage-2; (**c**) Voltage waveforms across stage-1′ and stage-2′; (**d**) Voltage across switch *S*.

The voltage magnitudes across capacitors C_1 and C'_1 are 30 V and the voltage across capacitors C_2 and C'_2 are 200 V. Figure 19d shows the voltage across switch *S* of the DSDO L–2LC converter and its magnitude is 250 V.

DSDO L–2LC$_m$ converter: Figure 20a shows the waveforms of the voltage across the two different loads R_{1o} and R_{2o}. Voltage of −230 V is generated across each load with a fixed 60% duty cycle. Figure 20b,c shows the waveforms of the voltage across capacitors C_1, C'_1, C_2, and C'_2. The voltage magnitudes across capacitors C_1 and C'_1 are 30 V, and voltage across capacitors C_2 and C'_2 are 200 V. Figure 20d shows the voltage across switch *S* of the DSDO L–2LC$_m$ converter and its magnitude is 250 V. Figure 21 shows the preliminary implemented hardware of the DSDO L–L converter. The designed hardware is tested with input voltage of 20 V and the output voltages are controlled at −105 V. Digitally controlled pulses are generated with the help of FPGA (Field Programmable Gate Array). Figures 22a and 22b the voltages across R_{1o} and R_{2o} with the voltage of switch *S*, respectively. Using a 20 V input supply, −104.2 V is successfully generated across each load and the voltage across switch *S* is 124.08 V. Figure 22c depicts the voltage and current waveform of inductors L_1 and L_2, respectively. In the ON state, the voltage across inductor L_1 is 20 V, which confirms that inductor L_1 is magnetized with input voltage. In the OFF state, the voltage across inductor L_1 is −30 V, i.e., inductor L_1 is demagnetized to charge the capacitor C_1. In the ON state, the voltage across inductor L_2 is 50 V, which confirms that the inductor L_2 is magnetized by the input voltage and the voltage across capacitor C_1. In the OFF state, the voltage across inductor L_2 is −75 V, i.e., inductor L_2 is demagnetized to charge capacitor C_2. Figure 22d depicts the voltage and current waveforms of inductor L'_1, L'_2 respectively. In the ON state, the voltage across inductor L'_1 is 20 V, which confirms that inductor L'_1 is magnetized by the input voltage. In the OFF state, the voltage across inductor L'_1 is −30 V, i.e., inductor L'_1 is demagnetized to charge capacitor C'_1. In the ON state, the voltage across inductor L'_2 is 50 V, which confirms that inductor L'_2 is magnetized by the input voltage and the voltage across capacitor C'_1. In the OFF state, the voltage across inductor L'_2 is −75 V, i.e., inductor L'_2 is demagnetized to charge capacitor C'_2.

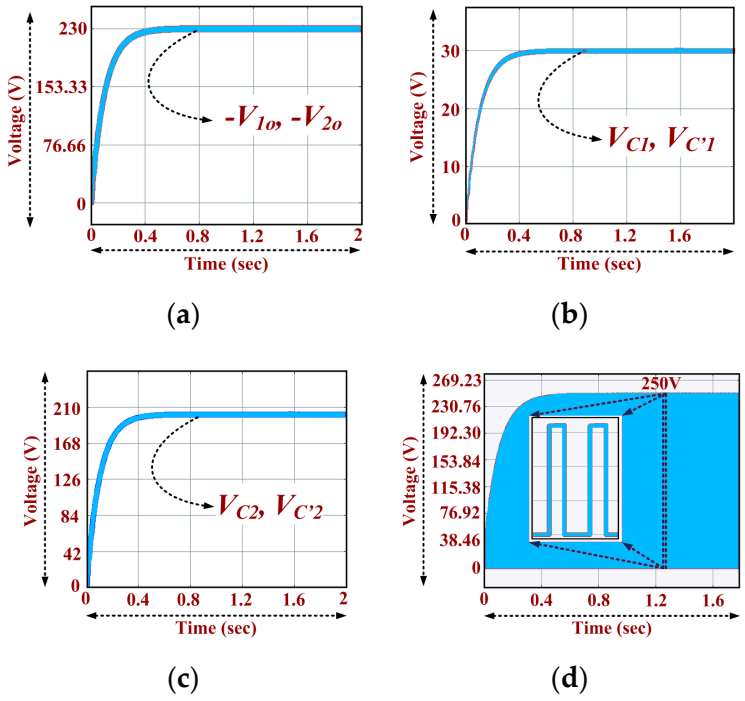


Figure 20. Simulation results of the DSDO L–2LC$_m$ converter configuration: (**a**) Output voltages waveforms; (**b**) Voltage waveforms across stage-1 and Stage-2; (**c**) Voltage waveforms across stage-1′ and stage-2′; (**d**) Voltage across switch *S*.

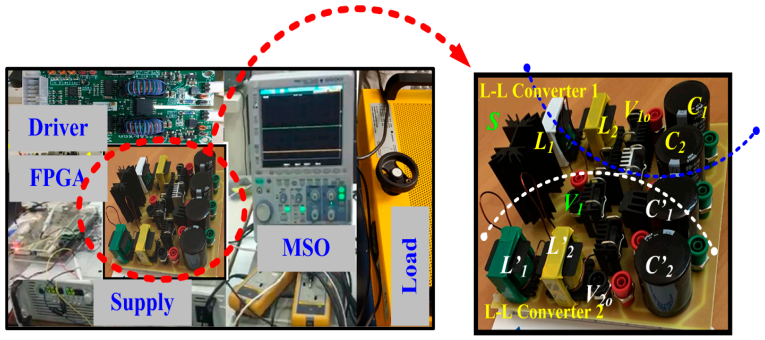


Figure 21. Experimental setup of the DSDO L–L converter configuration.

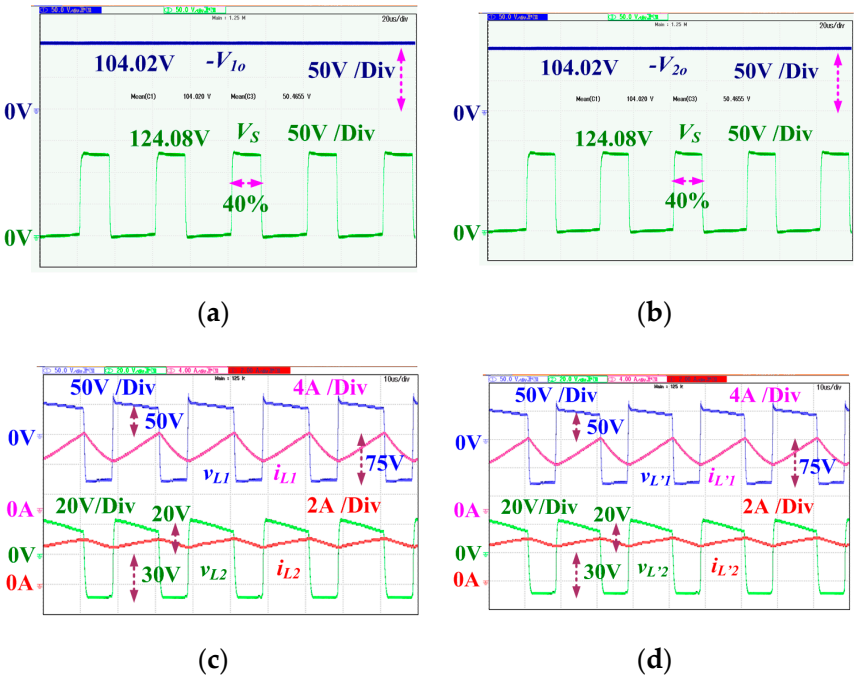


Figure 22. Experimental results of the DSDO L–L converter configuration: (**a**) voltage at load R_{1o} and voltage across switch S waveforms; (**b**) voltage at load R_{2o} and voltage across switch S waveforms; (**c**) inductor voltages and current of L converter-1; and (**d**) inductor voltages and current of L converter-2.

5. Conclusions

This article developed four DSDO converter configurations for high voltage fuel-cell electric vehicular loads. The proposed converters need a single controlling semiconductor switch and are able to feed two loads with high voltage conversion ratio. The circuitry of the DSDO L–L, DSDO L–2L, DSDO L–2LC, and DSDO L–2LC$_m$ converters are developed by merging with two L–L, two L–2L, two L–2LC, and two L–2LC$_m$ converters, respectively. The operating principles of the proposed converters are discussed with detailed theoretical analysis and governing equations for the output voltage conversion ratio. Finally, it is concluded that among the proposed converters, the DSDO L–2LC and DSDO L–2LC$_m$ converters provide higher output voltage and are effective in comparison with DC–DC converters. Both simulation and experimental results show that the proposed DSDO L–L converters had the expected performance.

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