Aalborg Universitet

Equivalent Space Vector Output of Diode Clamped Multilevel Inverters through Modulation Wave Decomposition under Carrier-Based PWM Strategy

He, Yingjie; Liu, Yunfeng; Lei, Chao; Liu, Jinjun

Link to publication from Aalborg University

Equivalent Space Vector Output of Diode Clamped Multilevel Inverters Through Modulation Wave Decomposition Under Carrier-Based PWM Strategy

YINGJIE HE[1,2], **(Member, IEEE), YUNFENG LIU**[1]**, CHAO LEI**[1]**,
AND JINJUN LIU**[1]**, (Fellow, IEEE)**
[1]Department of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China
[2]Department of Energy, Aalborg University, DK-9220 Aalborg, Denmark

Corresponding author: Yingjie He (hyj202411@163.com)

ABSTRACT The carrier-based PWM method (CBPWM) and the space vector PWM method (SVPWM) are two main modulation methods for diode clamped multilevel converters, and there is a certain relationship between these two modulation strategies. For general 8 segments SVPWM modulation sequence in the multilevel inverter, the inherent relationship between these two modulation methods have been researched, but the relationship between CBPWM and SVPWM in an arbitrary level sequence has not been obtained. To solve this problem, an in-depth study of the relationship between the multilevel SVPWM method and the CBPWM method has been made in this paper. By decomposing the modulation wave, and the SVPWM can be achieved by multi-modulation waves CBPWM. And the relationship between SVPWM and CBPWM in N level with an arbitrary number of segments sequence are obtained. Thus, through simple multi-modulation waves CBPWM strategy, less THD in the spectrum and higher DC voltage utilization switching sequences of multilevel inverters can be obtained. The simulation and experimental results illustrate that the relationship between CBPWM and SVPMM is correct.

INDEX TERMS Space vector modulation (SVPWM), decomposing modulation wave, relationship.

I. INTRODUCTION

Multilevel inverters are widely adopted in high-power applications due to their superior performance compared to two-level converters, with advantages such as reduced voltage stress on the power devices, lower harmonics, and lower instantaneous rate of voltage change (dv/dt) [1]–[3]. The modulation strategy is one of the most key technology for multilevel inverters [4]–[8].

Among various modulation strategies for multilevel inverters, space vector pulse width modulation (SVPWM) and carrier-based pulse width modulation (CBPWM) are two main PWM methods, SVPWM attracts much attention because it provides significant flexibility to optimize switching waveforms, and is suitable for implementation in digital signal processors, wide linear modulation range, less

The associate editor coordinating the review of this manuscript and approving it for publication was Zhixiang Zou.

total harmonic distortion (THD) in the spectrum of switching waveform, and higher DC voltage utilization [9], [10], what's more, the redundant switching states can be used for DC voltage balance control [11]. However, despite its significant advantages, SVPWM for more than three-level inverters is still hardly explored, due to the largely increased number of switching states and modulation sequences that accompany the higher number of levels [11], [12]. Due to some drawbacks, however, those schemes are not readily extended to five or higher-level inverters. If the relationship between SVPWM and CBPWM can be obtained, it is easy to achieve the SVPWM which has many advantages by using the CBPWM.

The SPWM modulation method is usually an 8-segment sequence in each switching period, but for SVPWM, it can modulate a special sequence that are more than 8 segments, such as 10, 12 or 14 segments, which is widely used in the practical PWM modulation process. And these

more than 8 segments modulation sequences are called special SVPWM sequence (SSVM) here. Numerous researchers have verified that SSVM can optimize output voltage and current and balance DC power, reduce the THD, control the neutral point voltage in NPC [13]–[15]. Compared with the conventional 8 segments SVPWM sequence, the SSVM is complex and has high switching loss [15].

To achieve the relationship between SVPWM and CBPWM, there have been many pieces of research before. References [16]–[20] studied the equivalent relationship between CBPWM and SVPWM for a three-phase two-level inverter and realized the equivalent SVPWM switching sequence output by injecting a zero-sequence component into the modulated wave of CBPWM. Also, the expression of the zero-sequence component is derived in the above researches. However, the above reference only studied the two-level 8-segment sequence and did not study the three-level and higher-level inverters. Reference [21]–[24] research the relationship between SVPWM of 8-segment modulation sequence and CBPWM in three-phase three-level NPC inverter. By injecting a zero-sequence voltage vector into each phase modulation wave under CBPWM, the equivalent relationship is achieved, and the three-level 8-segment modulation sequence is derived. But this method is limited to 8-segment modulation that means the output level of each phase can only be two levels. And for three-level NPC inverter with more than 8-segment switching sequence has not been realized. Reference [25] achieves the relationship between SVPWM of 8 modulation sequence and CBPWM in three-phase five-level NPC inverter. It just researched the 8-segment SVPWM modulation sequences, but the output modulation sequence of SVPWM can be more than 8 segments in diode clamped multilevel inverters, so the studies of the relationship between the CBPWM and SVPWM is incomplete and needs to be improved. Reference [25] proposed a new method with the zero-sequence component injected, which verified the equivalent relationship between SVPWM and CBPWM. However, it only studies three-level converters with less than 14-segment switching sequence and does not study higher-level output converters. All in all, the previous researches focus on special level inverters, the relationship between CBPWM and SVPWM in an arbitrary level sequence has not been obtained.

This paper comprehensively analyzes the relationship between CBPWM and SVPWM in N level with an arbitrary number of segments sequence. It decomposes the modulation waves of each phase into $(n-1)$ sub-modulation waves, the SVPWM can be achieved by multi-modulation waves CBPWM. Thus, through simple multi-modulation waves CBPWM strategy, less THD in the spectrum and higher DC voltage utilization switching sequences can be achieved and lower THD improves the performance of the high-precision power electronics equipment that widely used in the field of medical Magnetic Resonance Imaging and semiconductor lithography [27]–[29]. Moreover, for three-level or higher
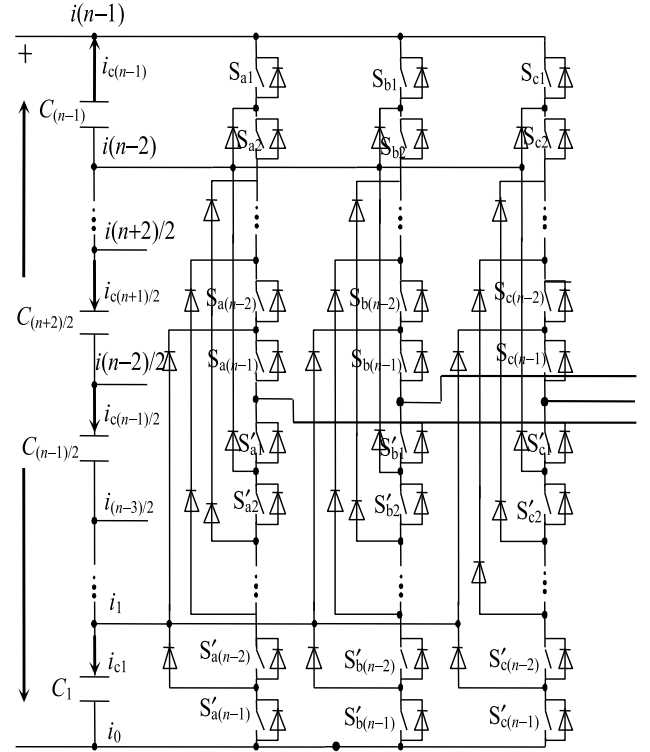

FIGURE 1. The main circuit of diode clamped *N*-level inverter.

inverters with a large number of switching states and modulation sequences, the multi-modulated wave CBPWM strategy can simplify analysis and calculation and is more suitable for the wide application of multi-level converters. The rest of this paper is structured as follows. Section II describes the principle of the SVPWM scheme in detail, including locating the reference vector, calculating the duty cycles, and generating the modulation sequences; Section III presents the strategy of decomposing the modulation wave, and some examples of getting the relationship between CBPWM and SVPWM of different segments sequence is shown in five-level converters. Finally, experimental waveforms are described in section IV, and the conclusions are given in Section V.

II. SVPWM FOR MULTILEVEL INVERTER
A. THE N-LEVEL INVERTER STRUCTURE
The structure of the three phases N-level neutral-point-clamped (NPC) voltage source inverter (VSI) is shown in Fig. 1, DC-link need $(n-1)$ capacitors, the main circuit needs $3 \times 2(n-2)$ clamped diodes and $3 \times 2(n-1)$ power switches. Here defining the n voltage states are 0, 1, 2, …, $(n-1)$, taking the phase A as an example, it has $2(n-1)$ power switches which are expressed by $S_{a1}, S_{a2}, …, S_{a(n-2)}$, $S_{a(n-1)}$ and $S'_{a1}, S'_{a2}, …, S'_{a(n-2)}, S'_{a(n-1)}$ as shown in Fig. 1, the on-off states of switches $S_{a1}, S_{a2}, …, S_{a(n-2)}, S_{a(n-1)}$ and $S'_{a1}, S'_{a2}, …, S'_{a(n-2)}, S'_{a(n-1)}$ are opposite all the time, if $S_{a1}, S_{a2}, …, S_{a(n-2)}, S_{a(n-1)}$ turn off, $S'_{a1}, S'_{a2}, …, S'_{a(n-2)},$

TABLE 1. On-off state of each switch for each voltage state in diode clamped *n*-level inverter.

Output voltage U_{AO}	On-off state of each Switch										Voltage state
	$S_{a1}S_{a2}\ldots S_{a(n-2)}S_{a(n-1)}S_{a'1}S_{a'2} \ldots S_{a(n-2)}S_{a(n-1)}$										$S_x(x=a, b, c)$
$U_n=U_{dc}/2$	1	1	1	1	1	0	0	0	0	0	$(n-1)$
$U_{(n-1)}=(n-3)U_{dc}/2(n-1)$	0	1	1	1	1	1	0	0	0	0	$(n-2)$
...	0	0	...	1	1	1	1	...	0	0	...
$U_{(n-1)/2}=0$	0	0	...	1	1	1	1	...	0	0	$(n-1)/2$
...	0	0	...	1	1	1	1	...	0	0	...
$U_2=-(n-3)U_{dc}/2(n-1)$	0	0	0	0	1	1	1	1	1	0	1
$U_1=-U_{dc}/2$	0	0	0	0	0	1	1	1	1	1	0

FIGURE 2. Space vector diagram of diode clamped *N*-level inverter.

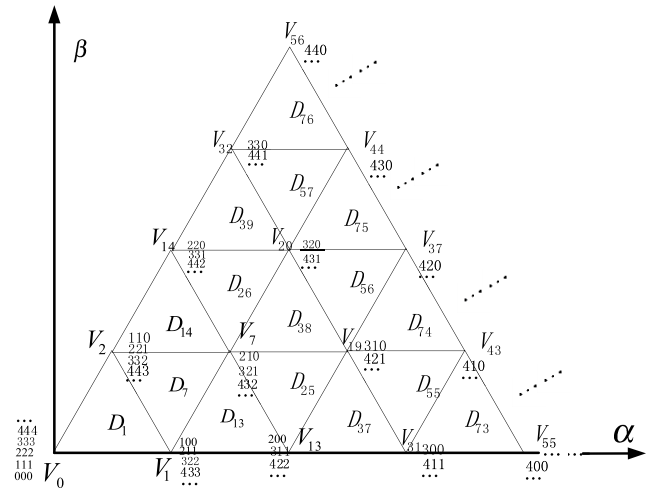**FIGURE 3.** Space vector diagram of the district I in N-level inverter.

$S'_{a(n-1)}$ must turn on, in this case, the voltage states of phase A $S_a = (n-1)$, similarly, the other voltage states can be obtained, if '0' represent the switch turn off, and '1' means switch turn on, the on-off state of each switch for each voltage state shown in table 1. Phase B and phase C are similar to phase A. Since each phase has *n* voltage states, three phases totally have n^3 switching states. As shown in Fig. 2, in *n*-level space vector diagram, three-phase *n*-level inverter totally have $6(n-1)^2(n = 3, 5, 7\ldots)$ small triangle sections, all the n^3 switching states distribute at the position of $[3n(n-1)-1]$ space voltage vectors, so many space vectors have some redundant switching states. For example, the zero-vector located in the center of space vector diagram has *n* switching states that are $(000), (111), (222), \ldots, [(n-1)(n-1)(n-1)]$.

B. THE IMPLEMENTATION OF SVPWM FOR N-LEVEL INVERTER

Generally, For *n*-level inverter shown in Fig. 1, the output voltage vector is defined as

$$\vec{V} = \frac{2}{3}(u_{AN} + u_{BN}e^{j2\pi/3} + u_{CN}e^{-j2\pi/3}) \quad (1)$$

It can be established that $u_{AN} = (S_a-(n-1)/2)U_{dc}/(n-1)$, $u_{BN} = (S_b - (n-1)/2)U_{dc}/(n-1)$, $u_{CN} = (S_c - (n-1)/2)U_{dc}/(n-1)$. S_a, S_b, S_c represent the voltage states output

by three phases respectively, defining the modulation ratio of the *n*-level inverter is

$$m = \frac{|\vec{V}^*|}{2/3 U_{dc}} = \frac{3|\vec{V}^*|}{2U_{dc}} \quad (2)$$

where $|\vec{V}|$ is the amplitude of reference voltage vector $\vec{V}$, and $2U_{dc}/3$ is the magnitude of six large vectors $S((n-1)\ 0\ 0)$, $S(0\ (n-1)\ 0)$, $S(0\ 0\ (n-1))$, $S((n-1)\ (n-1)\ 0)$, $S((n-1)\ 0\ (n-1))$, $S(0\ (n-1)\ (n-1))$.

As shown in Fig. 2, the space vector diagram can be divided into 6 big triangle districts, and each big triangle district can be re-divided to $(n-1)^2$ small triangle sections, taking the innermost small triangle of the district I $(0°-60°)$ as an example as shown in Fig. 3, if the space vector u_{ref} of the reference voltage is located in triangle D_1, it is synthesized by using one zero voltage vectors V_0 and two small voltage vectors V_1, V_2 according to the following equations:

$$\begin{cases} u_{ref} = V_0 \cdot T_0 + V_1 \cdot T_1 + V_2 \cdot T_2 \\ T_0 + T_1 + T_2 = T_S \end{cases} \quad (3)$$

where T_0, T_1, and T_2 are the duration of V_0, V_1, and V_2 within one switching period respectively. T_S is the switching period. As it can be seen from the space vector diagram, zero voltage vector V_0 contains *n* switching states, and each small voltage vectors V_1, V_2 contain $(n-1)$ switching states, so the output modulation sequence is not unique, if all the switching states are been used, then the longest $2\times(3n-2)$ segments sequence in one switching cycle can be expressed as $(0\ 0\ 0)\rightarrow(1\ 0\ 0)\rightarrow(1\ 1\ 0)\rightarrow(1\ 1\ 1)\rightarrow(2\ 1\ 1)\rightarrow\ldots\rightarrow[(n-1)\ (n-1)\ (n-1)]\rightarrow\ldots\rightarrow(2\ 1\ 1)\rightarrow(1\ 1\ 1)\rightarrow(1\ 1\ 0)\rightarrow\rightarrow(1\ 0\ 0)\rightarrow(0\ 0\ 0)$. In practice, it can output any sequence which is less than $2\times(3n-2)$ segments as needed.

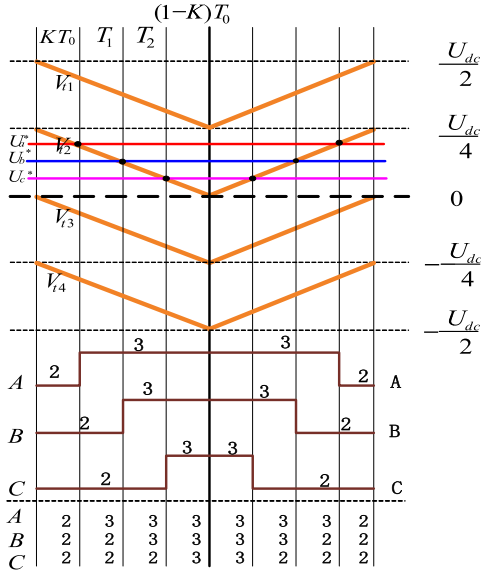Actually, the CBPWM method usually is an 8 segments modulation sequence in each switching cycle, the voltage

FIGURE 4. Relationship between 8 segments SVPWM sequence and CBPWM.

states of each phase just change once and only has two voltage states, so CBPWM is just one special situation of SVPWM.

III. RELATIONSHIP BETWEEN CBPWM AND SVPWM

A. THE RELATIONSHIP FOR 8 SEGMENTS MODULATION SEQUENCE

For general carrier-based modulation, in each switching cycle, there is a corresponding SVPWM sequence, it is usually an 8-segment sequence as shown in Fig. 4, the two modulation strategies can be unified by zero sequence, taking the $n = 5$ as an example, in the district I of the space vector diagram, T_0, T_1 and T_2 are the duty cycle of synthesized voltage vectors V_0, V_1 and V_2, U_a, U_b and U_c are the original three-phase voltage sine modulation waves before injecting the zero sequence component, and $U_a > U_b > U_c$, U_a^*, U_b^*, U_c^* are the three-phase modulation waves after injecting the zero sequence component, U_{ab}, U_{bc} and U_{ca} are the line-to-line voltage of original modulation waves which keep unchanged by injecting any zero sequence components to each phase voltage U_a, U_b and U_c, U_z is the zero sequence component, V_{t1}, V_{t2}, V_{t3}, V_{t4} are the triangle waves, U_{dc} is the DC voltage, K is the duty cycle allocated coefficient of synthesized voltage vectors V_0 which ranges between [0,1], so the duty cycle of each switching states (222) and (333) for zero voltage vector are defined as:

$$\begin{cases} T_{01} = KT_0 \\ T_{02} = (1-K)T_0 \end{cases} \tag{4}$$

According to the principle of voltage-seconds balance within the period of T_s [17], the following relationship can

be obtained:

$$\begin{cases} T_1 \dfrac{U_{dc}}{4} = T_s U_{ab} \\ T_2 \dfrac{U_{dc}}{4} = T_s U_{bc} \end{cases} \tag{5}$$

In one switching cycle, $T_1 + T_2 + T_0 = T_s$, the duty cycle of each voltage vectors can be got:

$$\begin{cases} T_0 = T_s[1 - \dfrac{4U_{ac}}{U_{dc}}] \\ T_1 = \dfrac{4T_s U_{ab}}{U_{dc}} \\ T_2 = \dfrac{4T_s U_{bc}}{U_{dc}} \end{cases} \tag{6}$$

Form Fig. 4, the value of each modulation wave in three phases can be expressed as:

$$\begin{cases} U_a^* = \dfrac{T_s - KT_0}{T_s} \dfrac{U_{dc}}{4} \\ U_b^* = \dfrac{T_s - KT_0 - T_1}{T_s} \dfrac{U_{dc}}{4} \\ U_c^* = \dfrac{(1 - K)T_0}{T_s} \dfrac{U_{dc}}{4} \end{cases} \tag{7}$$

By substituting (6) into (7), finally, the zero-sequence component can be obtained as follows:

$$\begin{cases} U_a^* = U_a + U_z \\ U_b^* = U_b + U_z \\ U_c^* = U_c + U_z \\ U_z = (K - 1) \times U_a - K \times U_c + (1 - K) \times \dfrac{U_{dc}}{4} \end{cases} \tag{8}$$

So, this zero-sequence component U_z connects those two kinds of modulation methods. In the other district, supposing U_{max}, U_{mid}, U_{min} are the maximum, median, minimum value of the original three-phase modulation waves. Then we can get the zero-sequence component in any district as follows:

$$U_z = (K - 1) \times U_{max} - K \times U_{min} + (1 - K) \times \dfrac{U_{dc}}{4} \tag{9}$$

B. THEORY OF MODULATION WAVE DECOMPOSITION

For the conventional CBPWM, after comparing with the triangle carrier wave, each modulation wave can only output two voltage states in one switching cycle and the modulation wave is usually an 8 segments sequence, but for the longest complex SVPWM modulation sequence as mentioned above, each phase contains n voltage states which cannot be achieved by the conventional CBPWM. So, it cannot output any modulation sequence which is more than 8 by using the conventional modulation method in reference [29].

To solve the problem mentioned above, a modified CBPWM modulation method that decomposes the modulation wave is proposed in this part. It can generate more than two voltage states in one switching cycle. Here decomposing each modulation wave into $(n - 1)$
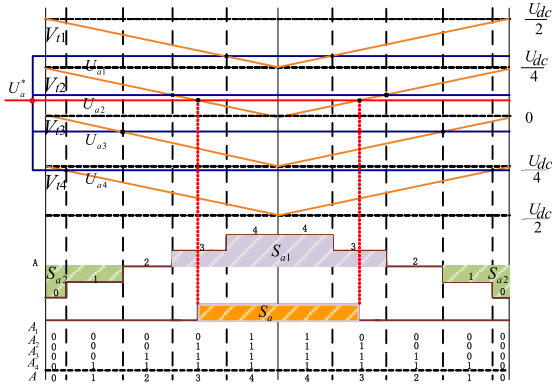
FIGURE 5. Decomposing of modulation wave and the combined pulse.

sub-modulation waves, then summing the output voltage states of each sub-modulation wave by CBPWM, each phase can get n voltage states in each switching cycle.

As shown in Fig. 5, the initial value of modulation wave in phase A is U_a^*, when $n = 5$, the decomposed four sub-modulation waves are U_{a1}^*, U_{a2}^*, U_{a3}^* and U_{a4}^*, each sub-modulation wave just output two voltage states 0 or 1, when compared with the four triangle carrier-based waves V_{t1}^*, V_{t2}^*, V_{t3}^*, and V_{t4}^*, if the sub-modulation waves are bigger than triangle wave, the output voltage state is 1, otherwise, the output voltage states is 0, actually, the sum value of those four sub-modulation waves is equal to the value of original modulation wave U_a^*. From another point of view, in Fig. 5, the area of conventional CBPWM in one switching cycle is equal to modified CBPWM which decomposing the modulation waves, i.e. $S_a = S_{a1} - 2S_{a2}$, so the proposed method has the equivalent effect with the conventional CBPWM. By comparing with triangle carrier wave, four sub-modulation waves can output single phase sequence $(0\to0\to0\to0\to1\to1\to0\to0\to0\to0)$, $(0\to0\to0\to1\to1\to1\to1\to0\to0\to0)$, $(0\to0\to1\to1\to1\to1\to1\to1\to0\to0)$ and $(0\to1\to1\to1\to1\to1\to1\to1\to1\to0)$ respectively, then summing the value of those output voltage states, the five-level SVPWM sequence $(0\to1\to2\to3\to4\to4\to3\to2\to2\to0)$ can be obtained, though the strategy of decomposing the modulation waves, it can output 0, 1, 2, 3 and 4 five voltage states in one switching states. This cannot be achieved by conventional CBPWM.

C. THE RELATIONSHIP BETWEEN TWO MODULATION STRATEGIES

To obtain the relationship between CBPWM and SVPWM, taking the above-decomposed method, here the sum of all those four sub-modulation waves in one fundamental cycle is equal to the sine modulation wave which is injected the zero-sequence component in each phase. Here taking the $n = 5$ as an example, if the reference voltage located in the innermost triangle D_1, K_{01}, K_{02}, K_{03}, K_{04}, K_{11}, K_{12},
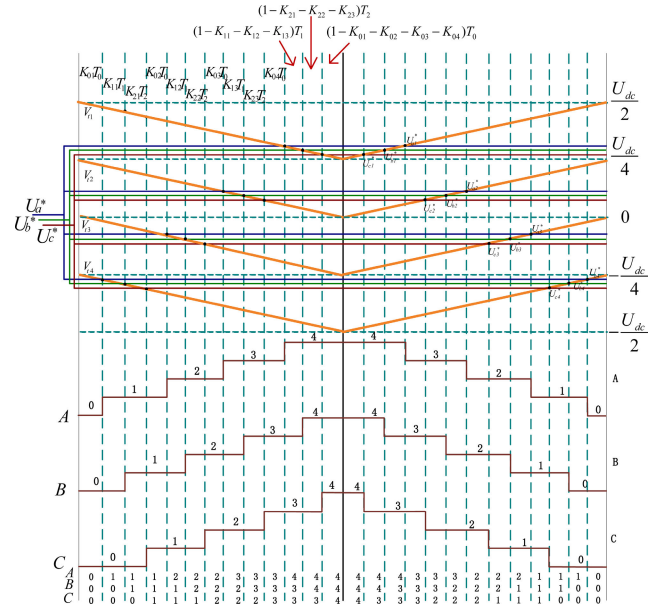

FIGURE 6. Relationship between 26 segments SVPWM sequence and CBPWM.

K_{13}, K_{21}, K_{22}, K_{23} are duty cycle allocated coefficient of three synthesized voltage vectors V_0, V_1 and V_2 respectively which range between [0,1], in Fig. 6, each original modulation wave U_a^*, U_b^*, U_c^* is decomposed to four sub-modulation waves, after comparing with the four triangle carrier waves, it can output five voltage states in one switching cycle. Thus, using the conventional *CBPWM* method to modulate those decomposed sub-modulation waves, the same *SVPWM* modulation sequence can be achieved. Next, it will give the detailed process to obtain the zero sequence which connects the two modulation methods, i.e., *CBPWM* and *SVPWM*.

According to Fig. 6, using the voltage-second balance principle, the following relationship can be obtained:

$$\begin{cases} [(1 - K_{11} - K_{12} - K_{13})T_1 + K_{11}T_1 + K_{12}T_1 \\ \quad + K_{13}T_1]\dfrac{U_{dc}}{4} = T_s U_{ab} \\ [(1 - K_{21} - K_{22} - K_{23})T_2 + K_{21}T_2 + K_{22}T_2 \\ \quad + K_{23}T_2]\dfrac{U_{dc}}{4} = T_s U_{bc} \end{cases} \tag{10}$$

In one switching cycle, $T_1 + T_2 + T_0 = T_s$, the duty cycle of each voltage vectors can be got:

$$\begin{cases} T_0 = T_s(1 - \dfrac{4U_{ac}}{U_{dc}}) \\ T_1 = T_s\dfrac{4U_{ab}}{U_{dc}} \\ T_2 = T_s\dfrac{4U_{bc}}{U_{dc}} \end{cases} \tag{11}$$

According to the geometric principle of similarity triangle, then we can get the equation of U_{x1}^*, U_{x2}^*, U_{x3}^*, and

U_{x4}^* (x =a, b, c) as follows:

$$\begin{cases} U_{a1}^* = \{[(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0 \\ \quad + (1 - K_{11} - K_{12} - K_{13})T_1]/T_s \\ \quad + \dfrac{(1 - K_{21} - K_{22} - K_{23})T_2}{T_s}\}\dfrac{U_{dc}}{4} + \dfrac{U_{dc}}{4} \\ U_{a2}^* = [(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0 + K_{04}T_0 \\ \quad + (1 - K_{11} - K_{12} - K_{13})T_1]/T_s \\ \quad + \dfrac{K_{13}T_1 + (1 - K_{21} - K_{22} - K_{23})T_2 + K_{23}T_2}{T_s})\dfrac{U_{dc}}{4} \\ U_{a3}^* = \dfrac{K_{01}T_0 + K_{11}T_1 + K_{21}T_2 + K_{02}T_0}{T_s}(-\dfrac{U_{dc}}{4}) \\ U_{a4}^* = \dfrac{K_{01}T_0}{T_s}(-\dfrac{U_{dc}}{4}) - \dfrac{U_{dc}}{4} \end{cases} \quad (12)$$

$$\begin{cases} U_{b1}^* = [(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0 + (1 \\ \quad - K_{21} - K_{22} - K_{23})T_2]/T_s\dfrac{U_{dc}}{4} + \dfrac{U_{dc}}{4} \\ U_{b2}^* = \{\dfrac{(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0 + K_{04}T_0}{T_s} \\ \quad + [(1 - K_{11} - K_{12} - K_{13})T_1 + (1 - K_{21} - K_{22} \\ \quad - K_{23})T_2 + K_{23}T_2]/T_s\}\dfrac{U_{dc}}{4} \\ U_{b3}^* = \dfrac{K_{01}T_0 + K_{11}T_1 + K_{21}T_2 + K_{02}T_0 + K_{12}T_1}{T_s} \\ \quad (-\dfrac{U_{dc}}{4}) \\ U_{b4}^* = \dfrac{K_{01}T_0 + K_{11}T_1}{T_s}(-\dfrac{U_{dc}}{4}) - \dfrac{U_{dc}}{4} \end{cases} \quad (13)$$

$$\begin{cases} U_{c1}^* = \dfrac{(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0}{T_s}\dfrac{U_{dc}}{4} + \dfrac{U_{dc}}{4} \\ U_{c2}^* = \{\dfrac{(1 - K_{01} - K_{02} - K_{03} - K_{04})T_0 + K_{04}T_0}{T_s} \\ \quad + [(1 - K_{11} - K_{12} - K_{13})T_1 + (1 - K_{21} - K_{22} \\ \quad - K_{23})T_2]/T_s\}U_{dc}/4 \\ U_{c3}^* = (K_{01}T_0 + K_{11}T_1 + K_{21}T_2 + K_{02}T_0 + K_{12}T_1 \\ \quad + K_{22}T_2)/T_s(-U_{dc}/4) \\ U_{c4}^* = \dfrac{K_{01}T_0 + K_{11}T_1 + K_{21}T_2}{T_s}(-\dfrac{U_{dc}}{4}) - \dfrac{U_{dc}}{4} \end{cases} \quad (14)$$

Then substituting equation (9) into (10), (11), (12), the value of sub-modulation waves can be obtained as follows:

$$\begin{cases} U_{a1}^* = (K_{01} + K_{02} + K_{03} + K_{04} - K_{11} - K_{12} - K_{13}) \\ \quad \times U_a + (K_{11} + K_{12} + K_{13} - K_{21} - K_{22} - K_{23}) \\ \quad \times U_b + (K_{21} + K_{22} + K_{23} - K_{01} - K_{02} - K_{03} \\ \quad - K_{04}) \times U_c + (2 - K_{01} - K_{02} - K_{03} - K_{04}) \times U_{dc}/4 \\ U_{a2}^* = (K_{01} + K_{02} + K_{03} - K_{11} - K_{12}) \times U_a + (K_{11} \\ \quad + K_{12} - K_{21} - K_{22}) \times U_b + (K_{21} + K_{22} - K_{01} \\ \quad - K_{02} - K_{03}) \times U_c + (1 - K_{01} - K_{02} - K_{03}) \times U_{dc}/4 \\ U_{a3}^* = (K_{01} + K_{02} - K_{11}) \times U_a + (K_{11} - K_{21}) \times U_b \\ \quad + (K_{21} - K_{01} - K_{02}) \times U_c - (K_{01} + K_{02}) \times U_{dc}/4 \\ U_{a4}^* = K_{01} \times U_a - K_{01} \times U_c - (1 + K_{01}) \times U_{dc}/4 \end{cases} \quad (15)$$

$$\begin{cases} U_{b1}^* = (-1 + K_{01} + K_{02} + K_{03} + K_{04}) \times U_a \\ \quad + (1 - K_{21} - K_{22} - K_{23}) \times U_b + (K_{21} + K_{22} \\ \quad + K_{23} - K_{01} - K_{02} - K_{03} - K_{04}) \times U_c \\ \quad + (2 - K_{01} - K_{02} - K_{03} - K_{04}) \times U_{dc}/4 \\ U_{b2}^* = (K_{01} + K_{02} + K_{03} - K_{11} - K_{12} - K_{13}) \\ \quad \times U_a + (K_{11} + K_{12} + K_{13} - K_{21} - K_{22}) \times U_b \\ \quad + (K_{21} + K_{22} - K_{01} - K_{02} - K_{03}) \times U_c \\ \quad + (1 - K_{01} - K_{02} - K_{03}) \times U_{dc}/4 \\ U_{b3}^* = (K_{01} + K_{02} - K_{11} - K_{12}) \times V_a + (K_{11} \\ \quad + K_{12} - K_{21}) \times U_b + (K_{21} - K_{01} - K_{02}) \\ \quad \times U_c - (K_{01} + K_{02}) \times U_{dc}/4 \\ U_{b4}^* = (K_{01} - K_{11}) \times U_a + K_{11} \times U_b - K_{01}U_c \\ \quad - (1 + K_{01}) \times U_{dc}/4 \end{cases} \quad (16)$$

$$\begin{cases} U_{c1}^* = (-1 + K_{01} + K_{02} + K_{03} + K_{04}) \times U_a \\ \quad + (1 - K_{01} - K_{02} - K_{03} - K_{04}) \times U_c + (2 \\ \quad - K_{01} - K_{02} - K_{03} - K_{04}) \times U_{dc}/4 \\ U_{c2}^* = (K_{01} + K_{02} + K_{03} - K_{11} - K_{12} - K_{13}) \\ \quad \times U_a + (K_{11} + K_{12} + K_{13} - K_{21} - K_{22} - K_{23}) \\ \quad \times U_b + (K_{21} + K_{22} + K_{23} - K_{01} - K_{02} - K_{03}) \\ \quad \times U_c + (1 - K_{01} - K_{02} - K_{03}) \times U_{dc}/4 \\ U_{c3}^* = (K_{01} + K_{02} - K_{11} - K_{12}) \times U_a + (K_{11} \\ \quad + K_{12} - K_{21} - K_{22}) \times U_b + (K_{21} + K_{22} \\ \quad - K_{01} - K_{02}) \times U_c - (K_{01} + K_{02}) \times U_{dc}/4 \\ U_{c4}^* = (K_{01} - K_{11}) \times U_a + (K_{11} - K_{21}) \times U_b \\ \quad + (K_{21} - K_{01}) \times U_c - (1 + K_{01}) \times U_{dc}/4 \end{cases} \quad (17)$$

According to equation $U_x^* = U_{x1}^* + U_{x2}^* + U_{x3}^* + U_{x4}^*$ (x =a, b, c), finally, the zero-sequence component can be obtained as follows:

$$\begin{cases} U_a^* = U_a + U_z \\ U_b^* = U_b + U_z \\ U_c^* = U_c + U_z \\ U_z = (4K_{01} + 3K_{02} + 2K_{03} + K_{04} - 3K_{11} \\ \quad - 2K_{12} - K_{13} - 1) \times U_a + (3K_{11} + 2K_{12} \\ \quad + K_{13} - 3K_{21} - 2K_{22} - K_{23}) \times U_b + (3K_{21} \\ \quad + 2K_{22} + K_{23} - 4K_{01} - 3K_{02} - 2K_{03} - K_{04}) \\ \quad \times U_c + (2 - 4K_{01} - 3K_{02} - 2K_{03} - K_{04}) \times U_{dc}/4 \end{cases} \quad (18)$$

According to the above analysis, after comparing with the four triangle carrier waves, the four sub-modulation waves of three phases U_{x1}^*, U_{x2}^*, U_{x3}^* and U_{x4}^* (x =a, b, c) can output five voltage states in one switching cycle, in this case, three phases can output 26-segment *SVPWM* modulation sequence, so modulating the four sub-modulation waves by CBPWM which is equivalent to inject the zero sequence component in equation (16) to the three original sine modulation waves, it can get the same effect as 26 segments modulation sequence output by *SVPWM*. This is the longest modulation sequence in a five-level inverter since each phase outputs five voltage levels, and if the voltage reference vector located in

the outermost side in the space vector diagram, it can only output 8 or less than 8 segments modulation sequence. Any other modulation sequences between 8 and 26 segments, the three modulation waves are not completely decomposed, it means each phase output less than five voltage level, for example, if each phase just has four voltage states, the output *SVPWM* modulation sequence are 20 segments if each phase has three voltage states, the output *SVPWM* sequence are 14 segments. So, the other situations can be considered as the special case for the longest 26-segment modulation sequence of *SVPWM*, it means some of the modulation waves are not completely decomposed to four sub-modulation waves. Similarly, the zero-sequence component can also be got.

If each phase just outputs 4 switching states, that means each modulation wave only decomposed to three sub-modulation waves, and the other one sub-modulation wave never intersects with the triangle waves, here setting the value of this sub-modulation wave $U_{x1}^* = U_{dc}/4 (x =$a, b, c). Then the output modulation sequence can be arranged as (000)→(100)→(110) →(111)→(211)→(221)→(222)→ (322) →(332)→(333) →(333) →(332) →(322) →(222) →(221) →(211) →(111) →(110) →(100) →(000), which is 20 segments SVPWM sequence. The sub-modulation waves as shown in Fig. 7.
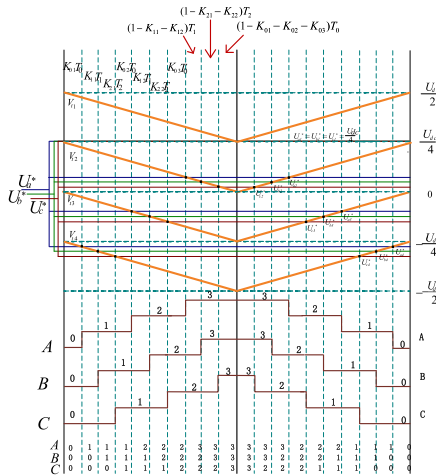

FIGURE 7. Relationship between 20 segments SVPWM sequence and CBPWM.

Similarly, the injected zero sequence component is:

$$
\begin{cases}
U_a^* = U_a + U_z \\
U_b^* = U_b + U_z \\
U_c^* = U_c + U_z \\
U_z = (3K_{01} + 2K_{02} + K_{03} - 2K_{11} - K_{12} - 1) \\
\quad \times U_a + (2K_{11} + K_{12} - 2K_{21} - K_{22}) \times U_b \\
\quad + (2K_{21} + K_{22} - 3K_{01} - 2K_{02} - K_{03}) \\
\quad \times U_c + (1 - 3K_{01} - 2K_{02} - K_{03}) \times U_{dc}/4
\end{cases}
\tag{19}
$$

Meanwhile, the sub-modulation waves U_{x1}^*, U_{x2}^*, U_{x3}^* and U_{x4}^* ($x =$a, b, c) can be obtained as follows:

$$
\begin{cases}
U_{a1}^* = U_{dc}/4 \\
U_{a2}^* = (K_{01} + K_{02} + K_{03} - K_{11} - K_{12}) \times U_a \\
\quad + (K_{11} + K_{12} - K_{21} - K_{22}) \times U_b + (K_{21} \\
\quad + K_{22} - K_{01} - K_{02} - K_{03}) \times U_c + (1 \\
\quad - K_{01} - K_{02} - K_{03}) \times U_{dc}/4 \\
U_{a3}^* = (K_{01} + K_{02} - K_{11}) \times U_a + (K_{11} - K_{21}) \\
\quad \times U_b + (K_{21} - K_{01} - K_{02}) \times U_c - (K_{01} \\
\quad + K_{02}) \times U_{dc}/4 \\
U_{a4}^* = K_{01} \times U_a - K_{01} \times U_c - (1 + K_{01}) \times U_{dc}/4
\end{cases}
\tag{20}
$$

$$
\begin{cases}
U_{b1}^* = U_{dc}/4 \\
U_{b2}^* = (K_{01} + K_{02} + K_{03} - 1) \times U_a + (1 - K_{21} \\
\quad - K_{22}) \times U_b + (K_{21} + K_{22} - K_{01} - K_{02} \\
\quad - K_{03}) \times U_c + (1 - K_{01} - K_{02} - K_{03}) \times U_{dc}/4 \\
U_{b3}^* = (K_{01} + K_{02} - K_{11} - K_{12}) \times U_a + (K_{11} \\
\quad + K_{12} - K_{21}) \times U_b + (K_{21} - K_{01} - K_{02}) \\
\quad \times U_c - (K_{01} + K_{02}) \times U_{dc}/4 \\
U_{b4}^* = (K_{01} - K_{11}) \times U_a + K_{11} \times U_b \\
\quad - K_{01}U_c - (1 + K_{01}) \times U_{dc}/4
\end{cases}
\tag{21}
$$

$$
\begin{cases}
U_{c1}^* = U_{dc}/4 \\
U_{c2}^* = (K_{01} + K_{02} + K_{03} - 1) \times U_a \\
\quad + (1 - K_{01} - K_{02} - K_{03}) \times U_c + (1 - K_{01} \\
\quad - K_{02} - K_{03}) \times U_{dc}/4 \\
U_{c3}^* = (K_{01} + K_{02} - K_{11} - K_{12}) \times U_a + (K_{11} \\
\quad + K_{12} - K_{21} - K_{22}) \times U_b + (K_{21} + K_{22} \\
\quad - K_{01} - K_{02}) \times U_c - (K_{01} + K_{02}) \times U_{dc}/4 \\
U_{c4}^* = (K_{01} - K_{11}) \times U_a + (K_{11} - K_{21}) \times U_b \\
\quad + (K_{21} - K_{01}) \times U_c - (1 + K_{01}) \times U_{dc}/4
\end{cases}
\tag{22}
$$

Similarly, if each phase just decomposed to two sub-modulation waves, each phase only output three-voltage states, the output modulation sequence is 14 segments, and the zero-sequence component is:

$$
\begin{cases}
U_a^* = U_a + U_z \\
U_b^* = U_b + U_z \\
U_c^* = U_c + U_z \\
U_z = (2K_{01} + K_{02} - K_1 - 1) \times U_a + (K_1 - K_2) \times U_b \\
\quad + (K_2 - 2K_{01} - K_{02}) \times U_c - (1 + 2K_{01} + K_{02}) \times \dfrac{U_{dc}}{4}
\end{cases}
\tag{23}
$$

As can be seen from above, the zero-sequence component equation format of 14-segment sequence and 20-segment sequence is similar to 26 segments, actually, any segments sequence between 8−26 segments are the special case of 26 segments sequence.

For the *n*-level inverter, each phase can output *n* voltage states, in the innermost modulation triangles D_1 in Fig. 2, zero voltage vector V_0 have $(n − 1)$ switching states, V_1 and V_2 each have $(n − 2)$ switching states, it can output

TABLE 2. Output current and voltage of three-phase 5-level diode-clamped NPC.

methods		Current		Voltage	
		Amplitude/ A	THD/ %	Amplitude/ V	THD/ %
CBPWM		7.243	1.01	120.7	91.83
CBPWM +U_z	8 segments	7.244	0.95	120.9	91.80
	20 segments	7.249	0.90	120.9	91.76
	26 segments	7.253	0.87	121.0	91.69

Hints: the max frequency used for THD computation is 1000Hz.

$(6n - 4)$ *SVPWM* segments sequence ultimately, by the same way, each modulation wave is decomposed to $(n - 1)$ sub-modulation waves, then the zero-sequence component can be obtained as follows:

$$
\begin{cases}
U_a^* = U_a + U_z \\
U_b^* = U_b + U_z \\
U_c^* = U_c + U_z \\
U_z = ((n-1)K_{01} + (n-2)K_{02} + \cdots + 2K_{0(n-2)} \\
\quad + K_{0(n-1)} - (n-2)K_{11} - (n-3)K_{12} - \cdots \\
\quad -2K_{1(n-3)} - K_{1(n-2)} - 1) \times U_{max} + ((n-2)K_{11} \\
\quad + (n-3)K_{12} + \cdots + 2K_{1(n-3)} + K_{1(n-2)} - (n-2)K_{21} \\
\quad - (n-3)K_{22} - \cdots - 2K_{2(n-3)} - K_{2(n-2)}) \\
\quad \times U_{mid} + ((n-2)K_{21} + (n-3)K_{22} + \cdots \\
\quad + 2K_{2(n-3)} + K_{2(n-2)} - (n-1)K_{01} - (n-2)K_{02} \\
\quad - \cdots - 2K_{0(n-2)} - K_{0(n-1)}) \times U_{min} \\
\quad + ((n-1)/2 - (n-1)K_{01} - (n-2)K_{02} \\
\quad - \cdots \cdots - 2K_{0(n-2)} - K_{0(n-1)}) \times \dfrac{U_{dc}}{n-1}
\end{cases} \tag{24}
$$

The $(n - 1)$ sub-modulation waves can be obtained as follows:

$$
\begin{cases}
U_{max\,1}^* = (K_{01} + K_{02} + \cdots + K_{0(n-1)} - K_{11} \\
\quad - K_{12} - \cdots - K_{1(n-2)}) \times U_{max} \\
\quad + (K_{11} + K_{12} + \cdots + K_{1(n-2)} - K_{21} \\
\quad - K_{22} - \cdots - K_{2(n-2)}) \times U_{mid} \\
\quad + (K_{21} + K_{22} + \cdots + K_{2(n-2)} - K_{01} \\
\quad - K_{02} - \cdots - K_{0(n-1)}) \times U_{min} \\
\quad + ((n-1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-1)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
U_{max\,i}^* = (K_{01} + K_{02} + \cdots + K_{0(n-i)} - K_{11} \\
\quad - K_{12} - \cdots - K_{1(n-i-1)}) \times U_{max} \\
\quad + (K_{11} + K_{12} + \cdots + K_{1(n-i-1)} - K_{21} \\
\quad - K_{22} - \cdots - K_{2(n-i-1)}) \times U_{mid} \\
\quad + (K_{21} + K_{22} + \cdots + K_{2(n-i-1)} - K_{01} \\
\quad - K_{02} - \cdots - K_{0(n-i)}) \times U_{min} \\
\quad + ((n-2i+1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-i)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
U_{max(n-1)}^* = K_{01} \times U_{max} - K_{01} \times U_{min} \\
\quad + (-(n-3)/2 - K_{01}) \times U_{dc}/(n-1)
\end{cases} \tag{25}
$$

$$
\begin{cases}
V_{min\,1}^* = (K_{01} + K_{02} + \cdots + K_{0(n-1)} - 1) \times U_{max} \\
\quad + (1 - K_{01} - K_{02} - \cdots - K_{0(n-1)}) \times U_{min} \\
\quad + ((n-1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-1)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
V_{min\,i}^* = (K_{01} + K_{02} + \cdots + K_{0(n-i)} - K_{11} \\
\quad - K_{12} - \cdots - K_{1(n-i)}) \times U_{max} \\
\quad + (K_{11} + K_{12} + \cdots + K_{1(n-i)} - K_{21} \\
\quad - K_{22} - \cdots - K_{2(n-i)}) \times U_{mid} \\
\quad + (K_{21} + K_{22} + \cdots + K_{2(n-i)} - K_{01} \\
\quad - K_{02} - \cdots - K_{0(n-i)}) \times U_{min} \\
\quad + ((n-2i+1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-i)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
V_{min(n-1)}^* = (K_{01} - K_{11}) \times U_{max} + (K_{11} - K_{21}) \\
\quad \times U_{mid} + (K_{21} - K_{01}) \times U_{min} \\
\quad + (-(n-3)/2 - K_{01}) \times U_{dc}/(n-1)
\end{cases} \tag{26}
$$

$$
\begin{cases}
V_{mid\,1}^* = (K_{01} + K_{02} + \cdots + K_{0(n-1)} - 1) \times U_{max} \\
\quad + (1 - K_{11} - K_{12} - \cdots - K_{1(n-2)}) \times U_{mid} \\
\quad + (K_{21} + K_{22} + \cdots + K_{2(n-2)} - K_{01} \\
\quad - K_{02} - \cdots - K_{0(n-1)}) \times U_{min} \\
\quad + ((n-1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-1)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
V_{mid\,i}^* = (K_{01} + K_{02} + \cdots + K_{0(n-i)} - K_{11} \\
\quad - K_{12} - \cdots - K_{1(n-i-1)}) \times U_{max} \\
\quad + (K_{11} + K_{12} + \cdots + K_{1(n-i)} - K_{21} \\
\quad - K_{22} - \cdots - K_{2(n-i-1)}) \times U_{mid} \\
\quad + (K_{21} + K_{22} + \cdots + K_{2(n-i-1)} - K_{01} \\
\quad - K_{02} - \cdots - K_{0(n-i)}) \times U_{min} \\
\quad + ((n-2i+1)/2 - K_{01} - K_{02} - \cdots - K_{0(n-i)}) \\
\quad \times U_{dc}/(n-1) \cdots \cdots \\
V_{mid(n-1)}^* = (K_{01} - K_{11}) \times U_{max} \\
\quad + K_{11} \times U_{mid} - K_{01} \times U_{min} \\
\quad + (-(n-3)/2 - K_{01}) \times U_{dc}/(n-1)
\end{cases} \tag{27}
$$

where the K_{01}, K_{02} ... $K_{0(n-1)}$ refer to $(n - 1)$ duty cycle allocated coefficient of zero voltage, K_{11}, K_{12}, ..., $K_{1(n-2)}$ and K_{21}, K_{21}, ..., $K_{2(n-2)}$ are the duty cycle allocated coefficient of two small voltage vectors, U_{max}, U_{mid}, U_{min} mean the maximum, median, minimum value of the original three-phase modulation waves. Any modulation sequence between 8 and $(6n - 4)$ can treat similarly as the five-level inverter mentioned above, some modulation waves are not completely decomposed, then the zero-sequence component can be deduced, so the zero-sequence component realizes the unification between CBPWM and any level any SVPWM segments sequence. It completes the relationship between SVPWM and CBPWM.

IV. SIMULATION COMPARISON AND ANALYSIS

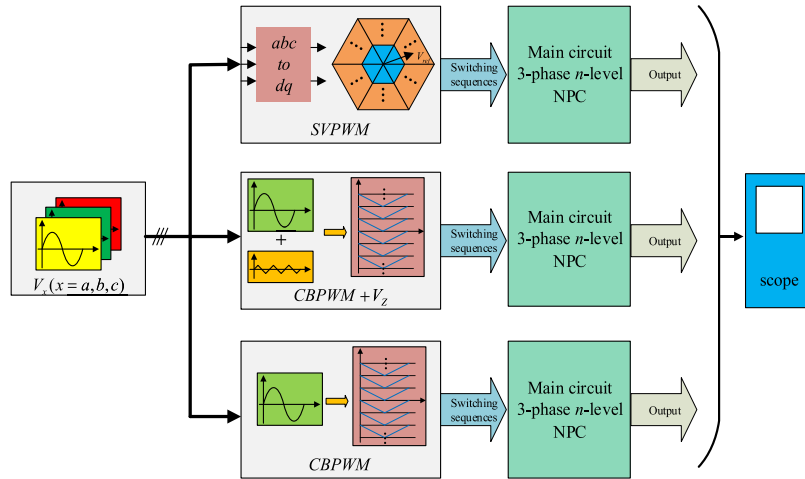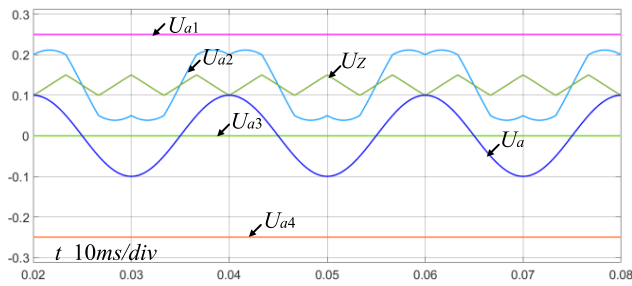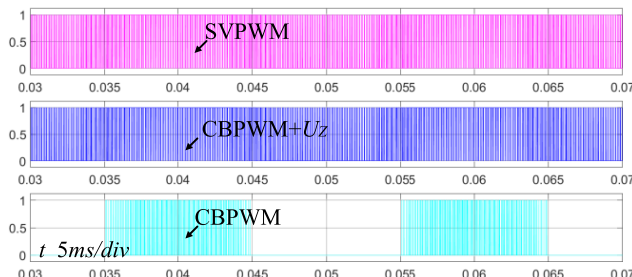Based on the previous theoretical analysis, we set up a simulation model on MATLAB/SIMULINK to verify the
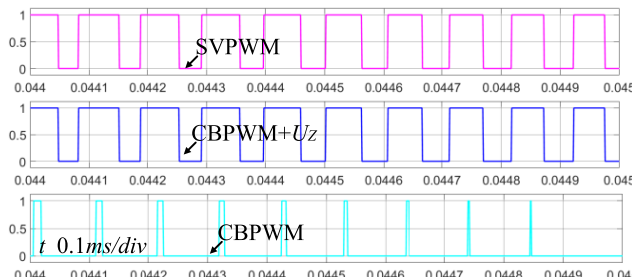
FIGURE 8. Simulation model.

(a). waveforms of U_{a1}, U_{a2}, U_{a3}, U_{a4}, U_Z, and U_a
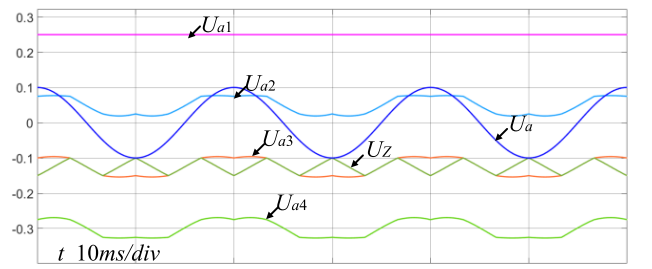

(b). On-off state of phase A S_{a1} by three different modulation strategies

(c). The zoom figure of (b)

FIGURE 9. m=0.2, Output waveforms for 8 segments modulation sequence.

(a). waveforms of U_{a1}, U_{a2}, U_{a3}, U_{a4}, U_Z, and U_a

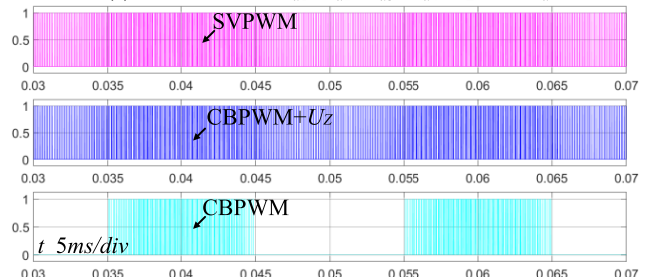(b). On-off state of phase A S_{a1} by three different modulation strategies

(c). The zoom figure of (b)

FIGURE 10. m=0.2, Output waveforms for 20 segments modulation sequence.
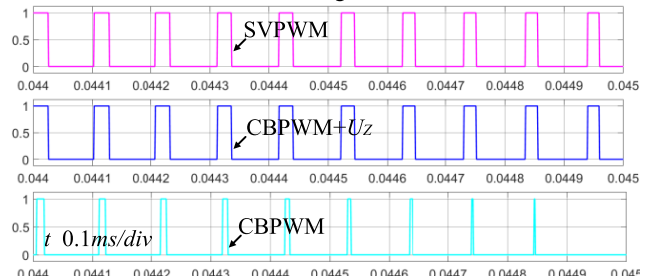
equivalence between CBPWM and SVPWM, as shown in Fig.8. There are three control models in the simulation that are SVPWM, CBPWM+U_Z, and CBPWM. The equivalent

relationship mainly verified by the output switching sequence of CBPWM and SVPWM, i.e., if they output the same switching sequence that means they are equivalent. So, for the control system of the three-phase n-level diode-clamped NPC, the open-loop control is enough. Here, taking the
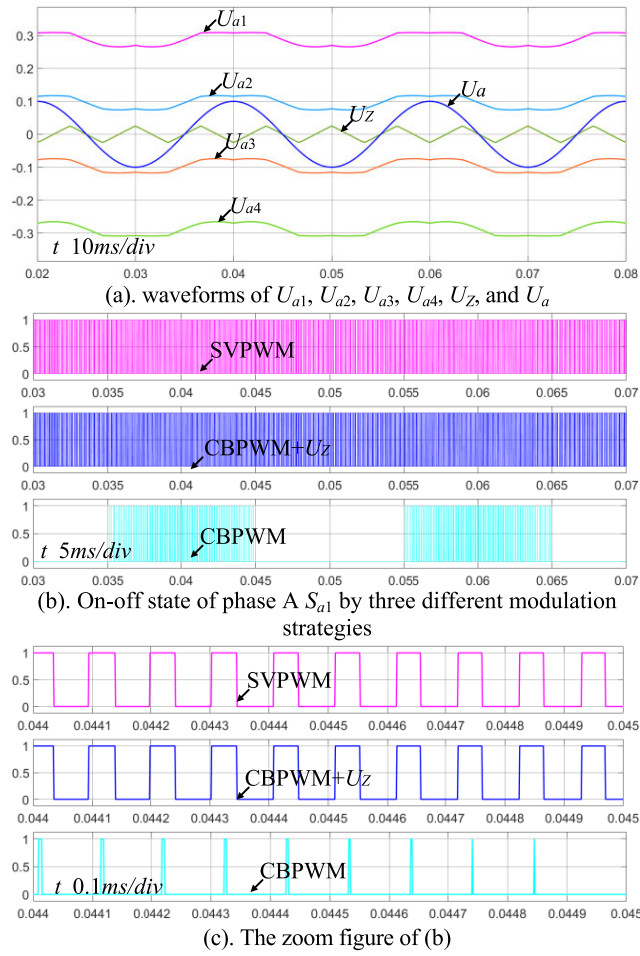
(a). waveforms of U_{a1}, U_{a2}, U_{a3}, U_{a4}, U_Z, and U_a

(b). On-off state of phase A S_{a1} by three different modulation strategies

(c). The zoom figure of (b)

FIGURE 11. m=0.2, Output waveforms for 26 segments modulation sequence.

(a). waveforms of U_a^*, U_Z, and U_a

(b). On-off state of phase A S_{a1} by three different modulation strategies

(c). The zoom figure of (b)

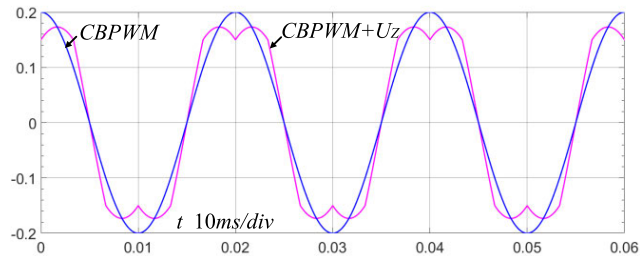**FIGURE 13.** m=1, Output waveforms for 8 segments and 10 segments modulation sequence.

FIGURE 12. m=0.2, Modulation waveforms of CBPWM and 26 segments CBPWM+U_Z.

three-phase 5-level diode-clamped NPC as an example, taking $n = 5$, the modulation ratio $m = 2V_r/U_{dc}$ (V_r represents the command voltage, U_{dc} represents the DC side voltage), assuming that all the redundant switching states have the same working time, for example, if the SVPWM modulation sequence is 26 segments as shown in Fig 6, the switching states 000, 111, 222, 333 and 444 with the working time $K_{01}T_0$, $K_{02}T_0$, $K_{03}T_0$, $K_{04}T_0$ and $(1-K_{01}-K_{02}-K_{03}-K_{04})T_0$ are the same, so, $K_{01} = K_{02} = K_{03} = K_{04} = 0.2$, similarly, $K_{11} = K_{12} = K_{13} = 0.25$, $K_{21} = K_{22} = K_{23} = 0.25$;
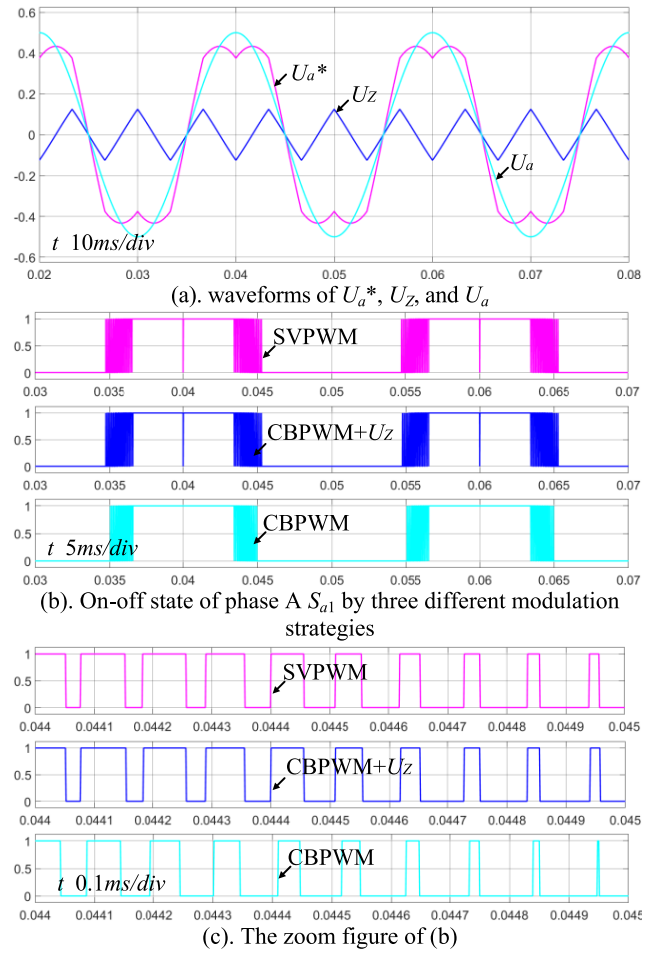
if the SVPWM modulation sequence is 20 segments, $K_{01} = K_{02} = K_{03} = 0.25$, $K_{11} = K_{12} = 1/3$, $K_{21} = K_{22} = 1/3$; if the modulation sequence is only 8 segments, there is only one duty cycle allocated coefficient $K = 0.5$. The longest and difficult 26-segment switching sequence is realized, the switching sequences from 8-segment to 26-segment can also be realized. The switching frequency is 10kHz and the standard modulation wave frequency is 50Hz. The resistance and inductance of the load with the star connection are 1.771Ω and 30mL respectively. And the DC side voltage is 700V.

Fig 9, 10, 11 shows m=0.2, the Output waveforms for 8-segment, 20-segment, and 26-segment modulation sequences, respectively. In Fig.9, to output 8 segments modulation sequence, only one of the four sub-modulated waves needs to inject the zero-sequence component, and the other three modulated waves keep constant that means the same states can be output when compared with the carrier. Similarly, when output 20-segment modulation sequence, there is a sub-modulated wave that keeps constant, and when output 26-segment modulation sequence, there is no sub-modulated wave that keeps constant. The final output on-off switching states show that the same output switching sequences
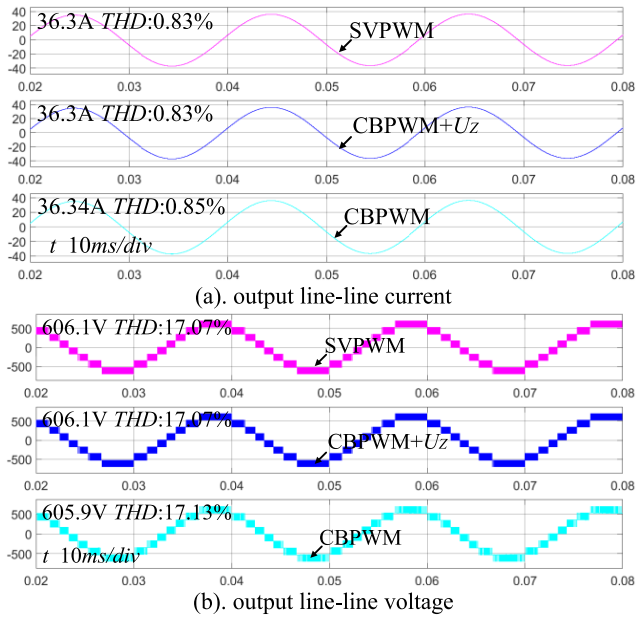
(a). output line-line current

(b). output line-line voltage

FIGURE 14. m=1, output line-line current and line-line voltage of three-phase 5-level diode-clamped NPC.

(a) Waveforms of U^*_a, U_z and U_a

(b) Waveforms of U^*_a, U^*_b, U^*_c

FIGURE 15. Output waveforms for 8 segments *SVPWM* modulation sequence under *CBPWM+Uz* strategy.

(a) Waveforms of U^*_a, U_z, and U_a

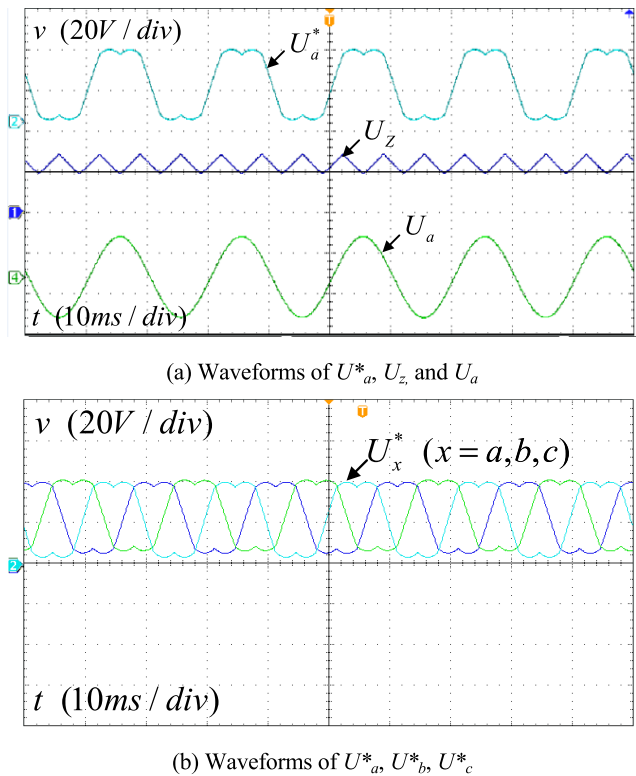(b) Waveforms of U^*_{a1}, U^*_{a2}, U^*_{a3}, and U^*_{a4}

FIGURE 16. Output waveforms for 26 segments *SVPWM* modulation sequence under *CBPWM+Uz* strategy.

as SVPWM can be realized by injecting the zero-sequence component into the modulation waves under CBPWM modulation.

The output line-line current and voltage of three-phase 5-level diode-clamped NPC between CBPWM+U$_Z$ and
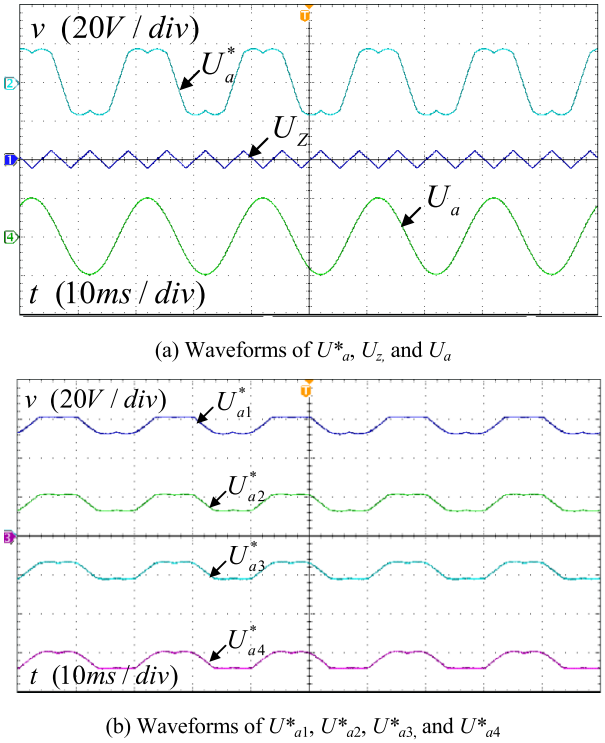
CBPWM are shown in Table 2. It can be seen that the THD of output current and voltage of CBPWM+U$_Z$ is better than CBPWM. And the more segments of switching sequence is, the better output current and voltage are. The ideal output line-line voltage and current values are 121.2436V and 7.2995A respectively. Also, the voltage of CBPWM+U$_Z$ is closer to the ideal value than CBPWM that means the former has better tracking performance. And the more segments of switching sequence is, the better tracking performance is.

Fig.12 shows the modulation waves of CBPWM and 26 segments CBPWM+U$_Z$, with the same command voltage, the amplitude of the modulated wave of CBPWM+U$_Z$ decreases to 0.866 of the commanded voltage after injecting the zero sequence component, while the amplitude of the modulated wave of CBPWM remains unchanged, which means that through CBPWM+U$_Z$, the diode clamped multilevel inverter can output higher line-line voltage.

Fig 13 shows $m = 1$, the Output waveforms for 8-segment and 10-segment modulation sequences. In Fig.13 (a), U_a and U_Z represent the zero-sequence voltage and command voltage respectively, U_a* represents the modulation wave with zero-sequence component injected. It can be seen that after zero-sequence component injected, the amplitude of the modulated wave decreases to 0.866 of the commanded voltage which is similar to Fig.12. Also, Fig.13 (a) (b) show that the same output switching sequences as SVPWM can be realized by injecting the zero-sequence component into the modulation waves under CBPWM modulation. In Fig.3, set $n = 5$, when $m = 1$, reference voltage rotates through
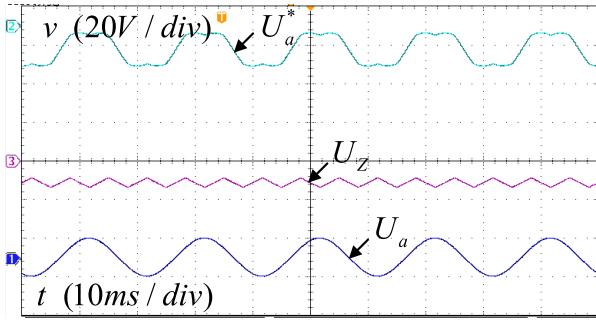
(a) Waveforms of U^*_a, U_z and U_a
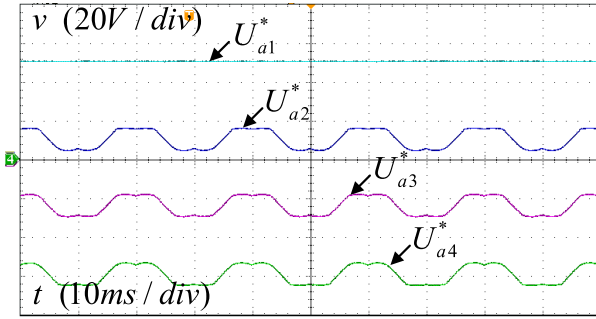
(b) Waveforms of U^*_{a1}, U^*_{a2}, U^*_{a3}, and U^*_{a4}

FIGURE 17. Output waveforms for 20 segments *SVPWM* modulation sequence under *CBPWM+Uz* strategy.
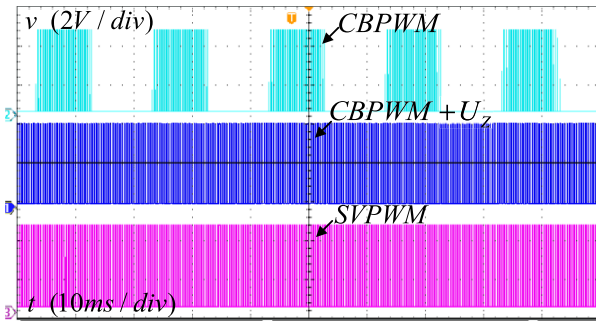
(a) On-off state of phase A S_{a1} by three different modulation strategies
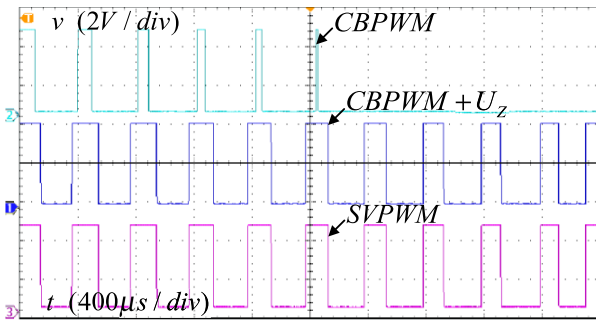
(b) The zoom figure of (a)

FIGURE 18. Switching state of phase A $Sa2$ by three different modulation strategies.

sector D_{55}, D_{56}, D_{57}, D_{74} and D_{75}, so in sector D_{55}, the reference can be composed by voltage vectors V_{19}, V_{31}, V_{43}.
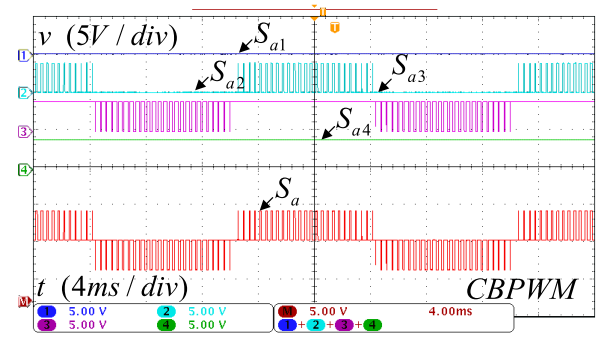
(a) Switching states of S_{a1}, S_{a2}, S_{a3}, S_{a4}, and S_a
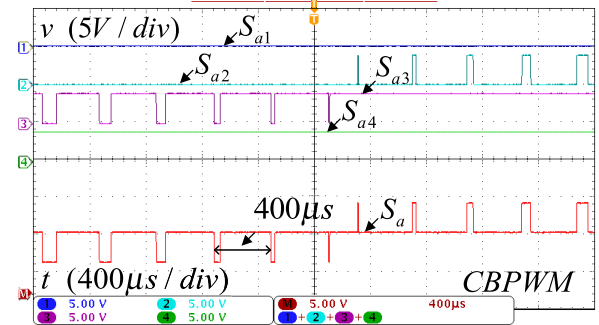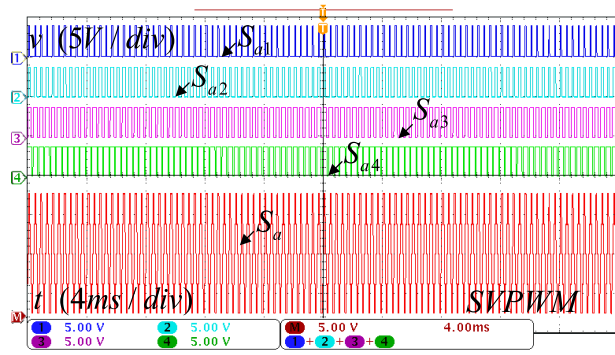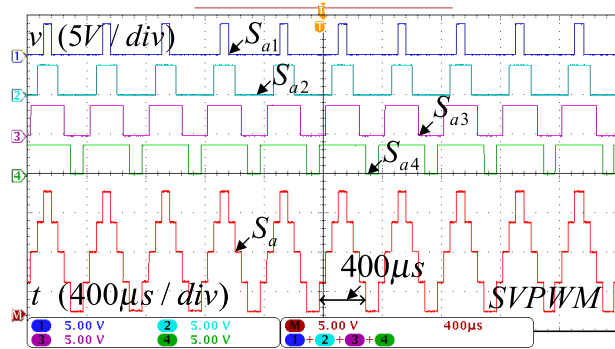

(b) The zoom figure of (a)

FIGURE 19. The waveform of phase A under CBPWM strategy.

and three vectors totally have 5 switching states, considering the symmetry of the modulation sequence, a 10-segment modulation sequence can be formed. Similarly, in sector D_{74}, a 8-segment modulation sequence can be formed and other sectors' analysis are the same. Fig.14 shows the output line-line current and line-line voltage of three-phase 5-level diode-clamped NPC under $m = 1$, similar to $m = 0.2$, SVPWM and CBPWM+U_Z have the same output line-line current and line-line voltage, and both of them are better than CBPWM.

V. EXPERIMENTAL RESULTS

Theoretic analysis results are necessary to further verify by the actual circuits. The main controller of the experiment platform uses DSP and FPGA. DSP is TMS320F28335 of TI Company, which is dedicated to realizing the control algorithm of the entire system. FPGA is the Cyclone II series EP2C35F484C8 of Altera Company, which mainly generates the PWM gating signals and the other achieves communications and protections [30].

To verify the relationship between SVPWM and CBPWM proposed in this paper, taking $n = 5$, injecting the zero-sequence component to original sine modulation waves, the modulation ratio $m = 0.2$, when the SVPWM modulation sequence is longest 26 segments, the four sub-modulation waves can be calculated. All the redundant switching states are assumed to share equivalent interval time. So, $K_{01} = K_{02} = K_{03} = K_{04} = 0.2$, $K_{11} = K_{12} = K_{13} = 0.25$, $K_{21} = K_{22} = K_{23} = 0.25$, if the SVPWM modulation

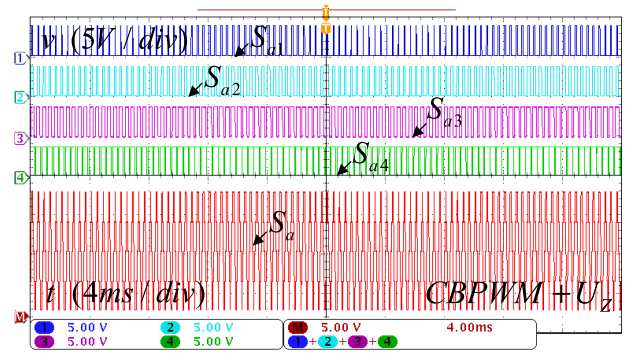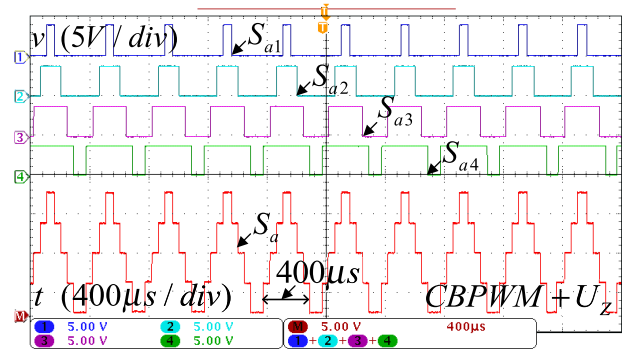(a) Switching states of S_{a1}, S_{a2}, S_{a3}, S_{a4} and S_a

(b) The zoom figure of (a)

FIGURE 20. The waveform of phase A under SVPWM strategy.

(a) Switching states of S_{a1}, S_{a2}, S_{a3}, S_{a4}, and S_a

(b) The zoom figure of (a)

FIGURE 21. The waveform of phase A under CBPWM+U_Z strategy.

sequence is 20 segments, $K_{01} = K_{02} = K_{03} = 0.25$, $K_{11} = K_{12} = 1/3$, $K_{21} = K_{22} = 1/3$, if the modulation sequence is only 8 segments, there is only one duty cycle allocated coefficient $K = 0.5$. The switching frequency is 2.5kHz and the standard modulation wave frequency is 50Hz.

Fig.15 (a) and Fig.15 (b) show the modulation waveforms of phase A by CBPWM+U_z which is corresponding to 8 segments sequence of SVPWM. Fig.15 (a) shows the original modulation waveform of phase A, the zero-sequence component, and the modulation wave of phase A after injected zero-sequence component. Fig.15 (b) shows the three-phase modulation waves after injecting the zero-sequence component. Fig. 16 (a) and Fig. 16 (b) show the output waveforms for 26 segments *SVPWM* modulation sequence under the *CBPWM+Uz* strategy, Fig. 16 (b) shows the four sub-modulation waves of phase A. Fig. 17 shows the output waveforms for 20 segments *SVPWM* modulation sequence under *CBPWM+Uz* strategy, in this situation, the value of the first sub-modulation wave equals to $U_{dc}/4$.

Fig. 18 shows the on-off state of switching state S_{a1} in phase A by three different modulation strategies, i.e. SVPWM, CBPWM with zero-sequence component injected CBPWM+U_z, and CBPWM without zero-sequence component injected. It can be seen that the on-off state of Switching state S_{a2} between the SVPWM and CBPWM+U_z is totally the same, but totally different from CBPWM.

Fig.19, Fig.20 and Fig.21 shows the on-off state of switching states S_{a1}, S_{a2}, S_{a3}, S_{a4}, and output voltage state S_a of phase A under three different modulation strategies, i.e. CBPWM, SVPWM, and CBPWM+U_z. It can be seen that the output switching sequences of SVPWM and CBPWM+U_z are almost the same and both of them can output five levels in each 400μs switching cycle. However, the CBPWM can only output two levels in each 400μs switching cycle that is different from the output of SVPWM and CBPWM+U_z. In one word, by using the multi-modulation waves with a zero-sequence component injected to modulate, the CBPWM can output the same switching sequence as SVPWM that verifies the equivalent relationship between SVPWM and CBPWM proposed in this paper.

VI. CONCLUSION

This paper comprehensively analyzes the relationship between SVPWM and CBPWM in n level NPC inverter. For general 8 segments SVPWM modulation sequence in the multilevel inverter, the relationship between two modulation methods have been many researched, but for much longer SVPWM modulation sequences more than 8 segments, it has not been researched before, and it cannot be achieved by the conventional analytic technique of CBPWM modulation method. In addition, the previous researches focus on specific level inverters, the relationship between CBPWM and SVPWM in an arbitrary level sequence has not been obtained. In this paper, by the strategy of decomposing the modulation

waves, The SVPWM in N level with an arbitrary number of segments sequence can be obtained by the multi-modulation wave CBPWM method. At last, the experiment results verify the correctness and validity of the method.

REFERENCES

[1] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, "Single-phase dual-mode interleaved multilevel inverter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2905–2915, Apr. 2020.

[2] B. Sharma and J. Nakka, "Single-phase cascaded multilevel inverter topology addressed with the problem of unequal photovoltaic power distribution in isolated DC links," *IET Power Electron.*, vol. 12, no. 2, pp. 284–294, Feb. 2019.

[3] R. Castillo, B. Diong, and P. Biggers, "Single-phase hybrid cascaded H-bridge and diode-clamped multilevel inverter with capacitor voltage balancing," *IET Power Electron.*, vol. 11, no. 4, pp. 700–707, Apr. 2018.

[4] X. Zeng, D. Gong, M.-L. Wei, and J. Xie, "Research on novel hybrid multilevel inverter with cascaded H-bridges at alternating current side for high-voltage direct current transmission," *IET Power Electron.*, vol. 11, no. 12, pp. 1914–1925, Oct. 2018.

[5] J. Amini, "An effortless space-vector-based modulation for *N*-level flying capacitor multilevel inverter with capacitor voltage balancing capability," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6188–6195, Nov. 2014.

[6] H. P. Vemuganti, D. Sreenivasarao, G. S. Kumar, and A. S. Spandana, "Reduced carrier PWM scheme with unified logical expressions for reduced switch count multilevel inverters," *IET Power Electron.*, vol. 11, no. 5, pp. 912–921, May 2018.

[7] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[8] I. Ahmed, V. B. Borghate, A. Matsa, P. M. Meshram, H. M. Suryawanshi, and M. A. Chaudhari, "Simplified space vector modulation techniques for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8483–8499, Dec. 2016.

[9] K. Nishizawa, J.-I. Itoh, A. Odaka, A. Toba, and H. Umida, "Current harmonic reduction based on space vector PWM for DC-link capacitors in three-phase VSIs operating over a wide range of power factor," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4853–4867, May 2019.

[10] J. Biswas, M. D. Nair, V. Gopinath, and M. Barai, "An optimized hybrid SVPWM strategy based on multiple division of active vector time (MDAVT)," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4607–4618, Jun. 2017.

[11] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.

[12] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. IA-37, no. 2, pp. 637–641, Mar./Apr. 2001.

[13] H. L. Liu and G. H. Cho, "Three-level space vector PWM in low index modulation region avoiding narrow pulse problem," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 481–486, Sep. 1994.

[14] L. Lin, Y. Zou, Z. Wang, and H. Jin, "A simple neutral-point voltage balancing control method for three-level NPC PWM VSI inverters," in *Proc. IEEE Int. Conf. Electr. Mach. Drives*, San Antonio, TX, USA, May 2005, pp. 828–833.

[15] W. Tian, J. Zhang, and Z. Zhang, "Research on energy feedback based on SVPWM algorithm for three-level," in *Proc. Int. Symp. Intell. Inf. Process. Trusted Comput.*, Huanggang, China, Oct. 2010, pp. 110–113.

[16] K. Ma and F. Blaabjerg, "Unifying and generating of space vector modulation sequences for multilevel converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 196–201.

[17] S. R. Bowes and Y.-S. Lai, "The relationship between space-vector modulation and regular-sampled PWM," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 670–679, Sep. 1997.

[18] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis [three-phase inverters]," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.

[19] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May/Jun. 1997.

[20] X.-L. Wen and X.-G. Yin, "The unified PWM implementation method for three-phase inverters," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, May 2007, pp. 241–246.

[21] H. Fang, X. Ge, W. Song, R. Ding, and X. Feng, "Relationship between two-level space-vector pulse-width modulation and carrier-based pulse-width modulation in the over-modulation region," *IET Power Electron.*, vol. 7, no. 1, pp. 189–199, Jan. 2014.

[22] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.

[23] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. IA-38, no. 2, pp. 500–506, Mar./Apr. 2002.

[24] D.-P. Cao, W.-X. Song, H. Xi, G.-C. Chen, and C. Chen, "Research on zero-sequence signal of space vector modulation for three-level neutral-point-clamped inverter based on vector diagram partition," in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, vol. 3, May 2009, pp. 1435–1439.

[25] H. Wu and X. He, "Inherent correlation between multilevel carrier-based PWM and space vector PWM: Principle and application," in *Proc. 4th IEEE Int. Conf. Power Electron. Drive Syst. (IEEE PEDS Indonesia)*, vol. 1, Oct. 2001, pp. 276–281.

[26] J. Chen, Y. J. He, S. U. Hasan, and J. J. Liu, "A comprehensive study on equivalent modulation waveforms of the SVM sequence for three-level inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7149–7158, Dec. 2015.

[27] B. J. D. Vermulst, "Compensating baseband distortion of regularly sampled pulsewidth modulators for high-precision power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6257–6263, Jul. 2019.

[28] J. M. Schellekens, H. Huisman, J. L. Duarte, M. A. M. Hendrix, and E. A. Lomonova, "An analysis of the highly linear transfer characteristics of dual-buck converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4681–4690, Jun. 2018.

[29] E. Lemmen, J. M. Schellekens, C. G. E. Wijnands, and J. L. Duarte, "Advances in high-precision amplifiers—The extra L opposed current converter," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5691–5700, Oct. 2015.

[30] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1873–1886, Mar. 2016.

YINGJIE HE (Member, IEEE) was born in Henan, China, in 1978. He received the B.S., M.S., and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 1999, 2003, and 2007, respectively.

From May 2007 to May 2009, he was with the Power Electronics and Renewable Energy Center, Xi'an Jiaotong University, Xi'an, China, as a Postdoctoral Research Scholar. He is currently an Associate Professor with Xi'an Jiaotong University. His current research interests include power quality control, multilevel inverters, and the application of power electronics in power systems.

YUNFENG LIU is currently pursuing the M.S. degree with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China.

His main research interests include the hybrid multilevel, multilevel converter, power quality, and the applications of power electronics in power systems.

CHAO LEI was born in Shanxi, China, in 1997. He received the B.S. degree in electrical engineering from the Hefei University of Technology, Anhui, China, in 2019. He is currently pursuing the M.S. degree with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China.

His main research interests include the hybrid multilevel, multilevel converter, power quality, and the applications of power electronics in power systems.

JINJUN LIU (Fellow, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), China, in 1992 and 1997, respectively.

He then joined the School of Electrical Engineering, XJTU, as a Faculty Member. From late 1999 to early 2002, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, USA, as a Visiting Scholar. In late 2002, he was promoted to a Full Professor and then the Head of the Power Electronics and Renewable Energy Center, XJTU, which currently comprises 16 faculty members and around 100 graduate students and carries one of the leading power electronics programs in China. He served as an Associate Dean of the School of Electrical Engineering, XJTU, from 2005 to early 2010, and the Dean for Undergraduate Education, XJTU, from 2009 to early 2015. He is currently a XJTU Distinguished Professor of power electronics, sponsored by the Chang Jiang Scholars Program, Chinese Ministry of Education. He has coauthored three books, including one textbook, published over 300 technical papers in peer-reviewed journals and conference proceedings, holds 39 invention patents (China/U.S.), and delivered plenary keynote speeches for many times at comprehensive IEEE conferences or China national conferences in power electronics area. His research interests include power quality control and utility applications of power electronics, microgrids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu received governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements for seven times. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award. He has served the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for ten years. He has been serving as an Associate Editor for the IEEE Transactions on Power Electronics, since 2006. Since 2015, he has been the Vice President of the Membership of IEEE PELS. He is on the Board of China Electrotechnical Society (CES) and was elected as the Vice President of the CES Power Electronics Society, in 2013. He has been the Vice President for International Affairs, China Power Supply Society (CPSS), since 2013, and the inaugural Editor-in-Chief of the CPSS Transactions on Power Electronics and Applications, since 2016. He has been serving as the Vice Chair of the Chinese National Steering Committee for College Electric Power Engineering Programs, since 2013.

・・・