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Modeling and Analysis of 2/3-Level Dual-Active-Bridge DC-DC Converters with the Five-Level Control Scheme

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Abstract— Two-three (2/3)-level dual-active-bridge (DAB) DC-DC converters have high potential to become a promising solution for medium-voltage DC (MVDC) systems. In this paper, the operating constraints based on the switching characteristics of the 2/3-level DAB converters are analyzed comprehensively with a five-level control scheme, in order to ensure stable and reliable operation. Furthermore, to reduce the complexity of the modeling, a unified power-transfer model is derived based on an equivalent method, and five operating modes are divided, being the references for reliable and efficient control. Simulation results verify the effectiveness of the operating constraints and accuracy of the proposed model.

Keywords—Multilevel DAB converter, DC-DC converters, phase-shift control, modeling, operating constraints.

I. INTRODUCTION

Recently, the DAB converters have been widely applied in several applications due to the advantages such as high power density, galvanic isolation, inherent soft-switching capability, and high efficiency [1]. To satisfy various applications like energy storage systems, uninterrupted power supplies, and solid-state transformers, different DAB converters have been proposed. Compared with the two-level DAB converters, which was proposed in [2], multilevel DAB converters provide several benefits when being applied in mediumvoltage DC (MVDC) systems, e.g., higher voltage blocking capability, higher step-up ratio, and more control degrees of freedom (DoFs) to further improve the performance of the converters. Among various multilevel DAB converters, the topology in [3] is more applicable in the case where the rated voltages of the input and output sides are considerably different, as shown in Fig. 1. This topology is referred to as two-three (2/3)-level DAB converter, which consists of a twolevel full-bridge in the low-voltage (LV) side, a three-level neutral point-clamped (NPC) full-bridge in the high-voltage (HV) side, and an isolated transformer in between.

Phase-shift control is one of the most popular control schemes for the DAB converters, in which the magnitude and direction of the transferred power are determined by the phase-shift ratios among different gate-driving signals [4]. Single-phase-shift control is the simplest control scheme. However, when the two terminal voltages of the transformer mismatches, which means the voltage conversion ratio is far away from unity, the performance of the converters will be degraded due to a narrow soft-switching range, high current stress, etc [5], [6]. To overcome these limitations, multiphase-shift (MPS) control schemes have been proposed. Among various MPS control schemes, the five-level control scheme is a promising solution to the NPC-based DAB converters due to more DoFs [7]-[9]. Unfortunately, in the literature, most research on the five-level control focuses on the neutral-point balancing issues to avoid capacitor voltage imbalance and the overvoltage of power devices [8]-[10].

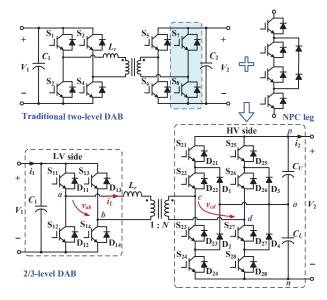


Fig. 1. A two-three-level dual-active-bridge DC-DC converter.

However, other important aspects like operating constraints and power-transfer model have not been investigated yet.

The analysis of the operating constraints is the mandatory to avoid maintain the performance and stable operation of the converters. For two-level DAB converters, as long as the gate-driving signals of the two switches in the same bridge leg are complementary, the terminal voltages of the transformer will only be determined by the phase-shift ratios. However, for the NPC-based DAB converters, the voltages will also be affected by the polarity of the inductor current, which may lead to voltage distortions and other issues when the current polarity changes. Unfortunately, the operating constraints are rarely considered so far in previous studies.

In addition to the operating constraints, modeling is another basis for the reliable and efficient modulation. There are two main modeling methods for the two-level DAB converters using: 1) the integration of the voltage and current piece-by-piece; 2) the Fourier analysis [11]-[13]. However, these methods lose the advantages when applied in multilevel DAB converters due to a large number of switching combinations. A novel equivalent method is developed in [14] which equates the terminal voltages of the transformer with two square waveforms. The modeling effort can be significantly simplified by only calculating the integration of the square waveforms. However, when this method is applied to the 2/3-level DAB converters, the gate-driving signals of the NPC legs are not square waveforms the duty cycle being 50%, leading to complicated equivalent square waveforms. Thus, the equivalent signals and calculating process should be reconsidered.

In light of the above, this paper explores the operating constraints of the 2/3-level DAB converter with a five-level control scheme by analyzing the switching characteristics. Furthermore, a unified power-transfer model is proposed. The rest of the paper is organized as follows. The switching characteristics of the 2/3-level DAB converters and the operating constraints are analyzed in Section II. The modeling process based on the equivalent method is given and the power-transfer model under different operating modes is derived in Section III. Section IV presents the simulation results to verify the effectiveness of the theoretical analysis. Finally, a conclusion is provided in Section V.

II. OPERATING CONSTRAINTS OF FIVE-LEVEL CONTROL SCHEME FOR DAB CONVERTERS

A. Operating principle

In Fig. 1, the topology of the 2/3-level DAB converters is shown, where V_1 and V_2 are the input and output DC voltages, respectively. v_{ab} and v_{cd} are two terminal AC voltages of the transformer with the turns-ratio being N. L_r is the sum of the leakage inductor and auxiliary inductor, and i_L is the current of the inductor L_r . p, o, and n are the positive point, neutral point and negative point of the NPC bridge. When applying the phase-shift control scheme to the 2/3-level DAB converters, the waveforms of v_{ab} and v_{cd} are affected by the polarity of i_L , in addition to the phase-shift ratios.

Fig. 2 gives a typical example where the waveform of v_{cd} is affected by the polarity of i_L [7]. In Fig. 2, the solid line denotes the waveform of v_{cd} when i_L is positive at the interval [A, B], and the dotted line denotes that when i_L is negative, where the gate-driving signals of the two cases are the same. Note that due to the symmetry of the waveforms during one switching cycle, the polarities of i_L during the intervals [A, B] and [C, D] are opposite. During the interval [A, B], the gate drive signals of S_{21} , S_{28} , S_{23} and S_{26} are at a high level. If i_L is positive (from the LV side to the HV side) during this interval, the current will flow through D₃, S₂₆, S₂₃, D₂, and finally go back to the neutral point o, as shown in Fig. 3 (a). As a consequence, the voltage v_{cd} is equal to 0 under this condition. However, if i_L is negative, as shown in Fig. 3 (b), the current will flow through D_{24} , D_{23} , D_{26} , and D_{25} , and the voltage v_{cd} is equal to $-V_2$. Similarly, the current conduction paths at the interval [C, D] can be obtained as shown in Fig. 3 (c) and (d) with the positive and negative i_L , respectively, and the corresponding values of v_{cd} are equal to V_2 and 0. Therefore, if the polarity of i_L changes at the intervals [A, B] and [C, D], the waveform of v_{cd} will be distorted, affecting the normal operation and performance of the converters. Unfortunately, the polarity of i_L in most cases cannot be determined directly, especially when the operating conditions changes frequently, since it is affected by several parameters, such as the phaseshift ratios, the input and output DC voltages, and the value of the transferred power. Therefore, to avoid the distortion caused by the modulation scheme, the operating constraints should be discussed to decouple the waveform of v_{cd} and the polarity of i_L . It should be noted that the coupling between the waveform of v_{ab} and the polarity of i_L does not exist. Therefore, only the switching characteristics in the HV side is

Considering v_{cn} and v_{dn} are the midpoint voltages for the two legs in the HV side. Due to $v_{cd} = v_{cn} - v_{dn}$, if the waveforms of v_{cn} and v_{dn} are not affected by the polarity of i_L , the terminal voltage v_{cd} will also be independent of it. Table I shows the

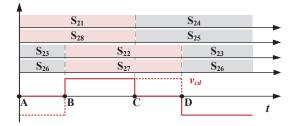


Fig. 2. A typical modulation scheme where the waveforms are dependent of the polarity of i_L with the same gate-driving signals.

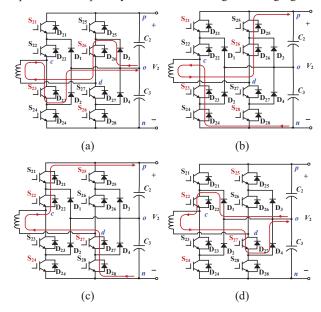


Fig. 3. Current conduction paths when: (a) i_L is positive during [A, B], (b) i_L is negative during [A, B], (c) i_L is positive during [C, D], and (d) i_L is negative during [C, D].

switching characteristics for the first leg of the NPC bridge (composed of S₂₁, S₂₂, S₂₃ and S₂₄). At any moment, the gate drive signals of two power switches are at the high level. From Table I, it can be seen that under some switching states, the values of v_{cn} are identical with different polarities of i_L . For instance, when the switching state is $\{S_{21}, S_{22}\}$, and if the polarity of i_L is positive, the current flows through D_{22} and D_{21} , as shown in Fig. 4 (a), and the value of v_{cn} is equal to the output voltage V_2 due to $v_{cn} = v_{pn}$. When the polarity of i_L is negative, the current flows through S₂₁ and S₂₂, as shown in Fig. 4 (b), and the value of v_{cn} is also equal to V_2 . However, in other states, the value of v_{cn} will be affected by the polarity of i_L . For instance, when the switching state is $\{S_{21}, S_{23}\}$, the current conduction paths are shown in Fig. 4 (c) and (d) when i_L is positive and negative, respectively, and the corresponding values of v_{cn} are $0.5V_2$ and 0. As a result, from Table I, it can be seen that there are only three switching states which can decouple v_{cn} from the polarity of i_L , e.g., $\{S_{21},$ S_{22} }, $\{S_{22}, S_{23}\}$, and $\{S_{23}, S_{24}\}$. The switching characteristics for the second leg (composed of S_{25} , S_{26} , S_{27} and S_{28}) can be analyzed similarly, and there are also three switching states: $\{S_{25}, S_{26}\}, \{S_{26}, S_{27}\}, \text{ and } \{S_{27}, S_{28}\} \text{ can decouple the value}$ of v_{dn} from the polarity of i_L . In summary, to avoid the voltage distortion caused by the changing polarity of i_L , no matter which modulation scheme is employed for the NPC bridge, the switching states must be $\{S_{2i}, S_{2(i+1)}\}\$, (i = 1, 2, 3 for the)first arm, and i = 5, 6, 7 for the second arm) at any moment.

TABLE I
SWITCHING CHARACTERISTICS FOR THE FIRST LEG

Switching states	Polarity of i_L	Value of <i>v_{cn}</i>
$\{S_{21},S_{22}\}$	+	V_2
	-	V 2
$\{S_{21},S_{23}\}$	+	$0.5V_{2}$
	-	0
$\{S_{21},S_{24}\}$	+	V_2
	-	0
$\{S_{22}, S_{23}\}$	+	$0.5V_2$
	-	0.372
$\{S_{22},S_{24}\}$	+	V_2
	-	$0.5V_{2}$
$\{S_{23},S_{24}\}$	+	0
	-	U

This is defined as the general operating principle of the control scheme for the 2/3-level DAB converters.

B. Operating constraints

Fig. 5 shows the typical waveforms with the five-level control scheme, in which T_{hs} is a half switching cycle. There are four control variables D_1 , D_2 , D_0 , and D in the five-level control scheme, which are defined as: D_1 , D_2 and D_0 are three phase-shift ratios between S_{14} and S_{11} , S_{27} and S_{11} , S_{22} and S_{11} , respectively. D denotes the duty-cycle ratio of the power switches in the HV side, where 1-D is the duty cycle of the four outer switches S_{21} , S_{24} , S_{25} and S_{28} , and 1+D is the duty cycle of the four inner switches S₂₂, S₂₃, S₂₆ and S₂₇. From the switching sequences of the HV side, it can be seen that the operating principle can be satisfied at any moment. Therefore, by using this control scheme, the waveforms of the voltages will be independent of the polarity of i_L , and only determined by the switching sequences, which are controlled by the phase-shift ratios and duty-cycle ratio. The ranges of the four control variables are defined as $0 \le D_1$, D_2 , D_0 , $D \le 1$. Note that whether D_2 is larger or less than D_0 , the waveforms of v_{ab} , v_{cd} , and i_L remain, which means the power model will not change. A similar condition applies in different relationships between D_2 and $D_0 + D$. For convenience, we only consider the condition $D_0 \le D_2 \le D_0 + D$ in this paper.

Furthermore, from Fig. 5, it can be seen that $D_2 + D$ is the largest phase-shift ratio, whose upper boundary should be discussed. Fig. 6 shows the waveforms when $D_2 + D > 1$, from which, it can be seen that the highest voltage levels $\pm V_2$ will not appear. That is because the voltage level V_2 corresponds to the switching state $\{S_{21}, S_{22}, S_{27}, S_{28}\}$, and V_2 corresponds to the switching state $\{S_{23}, S_{24}, S_{25}, S_{26}\}$, which can be seen in Fig. 5. However, when $D_2 + D > 1$, there are no such switching states. As a result, the waveforms with the five-level control scheme will be degraded, and the power transmission capacity will also be damaged. Based on the above analysis, the operating constraints for the five-level control scheme can be summarized as

$$\begin{cases} 0 \le D_1, D_2, D_0, D \le 1, \\ D_0 \le D_2 \le D_0 + D, D_2 + D \le 1 \end{cases}$$
 (1)

III. MODELING OF 2/3-LEVEL DAB CONVERTERS

A. Unified power-transfer model

From Fig. 5, it can be seen that v_{ab} and v_{cd} are three-level and five-level symmetric square waveforms, respectively.

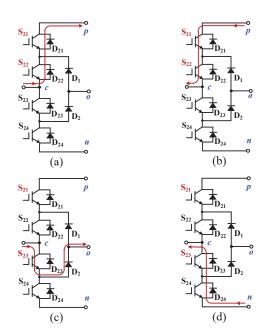


Fig. 4. Current conduction path under different operating conditions. (a) S_{21} and S_{22} are turned on, and i_L is positive. (b) S_{21} and S_{22} are turned on, and i_L is negative. (c) S_{21} and S_{23} are turned on, and i_L is positive. (d) S_{21} and S_{23} are turned on, and i_L is negative.

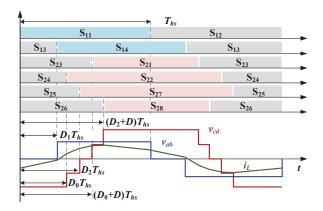


Fig. 5. Typical waveforms of the voltages and inductor current with the five-level control scheme.

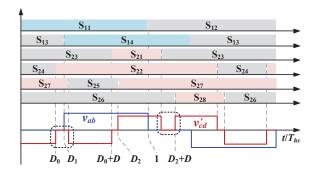


Fig. 6. Waveforms for the DAB converters when $D_2 + D > 1$.

According to the Kirchhoff Voltage Law (KVL), the inductor current i_L can be expressed as

$$\frac{di_L(t)}{dt} = \frac{v_{ab}(t) - v_{cd}(t)/N}{L_r}$$
 (2)

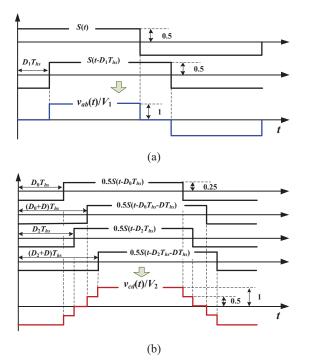


Fig. 7. Equivalent waveforms for the terminal voltages v_{ab} and v_{cd} . (a) Equivalent waveforms for v_{ab} . (b) Equivalent waveforms for v_{cd} .

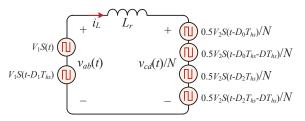


Fig. 8. Equivalent circuit of the 2/3-level DAB converters by using the equivalent-waveform method.

The transferred power of the converters is expressed as

$$P = \frac{1}{T_{hs}} \int_{0}^{T_{hs}} v_{ab}(t) i_{L}(t) dt$$
 (3)

From (2) and Fig. 5, it can be seen that the waveform of i_L is divided into many pieces with different slopes. Therefore, to calculate the power model, the slopes, initial and final values of i_L in each piece should be calculated, and then integrated piece by piece by using the traditional modeling method. It leads to heavy computation and complicated calculating process.

In the equivalent-waveform method, the waveforms of v_{ab} and v_{cd} can be composed of two and four square waveforms with 50% duty cycle, respectively, as shown in Fig. 7. S(t) denotes the basic waveform, whose cycle is equal to the switching cycle of $2T_{hs}$ of the converters, and the amplitude is 0.5. Other waveforms are obtained by phase shifting of S(t), expressed as S(t-x), where x denotes the phase-shift ratios. For the LV-side voltage v_{ab} , there is one phase-shift ratio D_1 , and therefore, it can be equivalent to two waveforms S(t) and $S(t-D_1T_{hs})$. However, there are four phase-shift ratios in the HV-side voltage v_{ab} , and thus, it is equivalent to four waveforms $S(t-D_0T_{hs})$, $S(t-D_2T_{hs})$, $S(t-D_0T_{hs}-DT_{hs})$, and $S(t-D_2T_{hs}-DT_{hs})$. The amplitude of each waveform should be 0.25 to guarantee that the highest level of v_{cd} is equal to

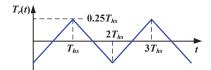


Fig. 9. Waveform of $T_r(t)$.

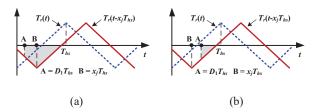


Fig. 10. Two conditions for calculating the transferred power. (a) $D_1 \le x_j$. (b) $D_1 > x_j$.

the output voltage V_2 . In this way, the equivalent circuit of the 2/3-level DAB converters can be depicted as shown in Fig. 8.

According to (2) and the equivalent circuit, the unified expression of i_L can be obtained as

$$i_{L}(t) = \frac{1}{L_{r}} \{ V_{1} \sum_{r} T_{r}(t - x_{i}) - \frac{V_{2}}{2N} \sum_{r} T_{r}(t - x_{j}) \}$$
 (4)

where $x_i \in \{0, D_1 T_{hs}\}\ (i = 1, 2)$ denotes the phase-shift ratios in the LV side, and $x_j \in \{D_0 T_{hs}, D_2 T_{hs}, (D_0 + D) T_{hs}, (D_2 + D) T_{hs}\}\ (j = 1, 2, 3, 4)$ denotes the phase-shift ratios in the HV side. $T_r(t)$ is the integration of S(t), as shown in Fig. 9, which can be expressed in one switching cycle as

$$T_r(t) = \begin{cases} 0.5t - 0.25T_{hs}, & 0 \le t < T_{hs} \\ -0.5t + 0.75T_{hs}, & T_{hs} \le t < 2T_{hs} \end{cases}$$
 (5)

Combining (3) and (4), the unified power-transfer model can be calculated as

$$P = \frac{-V_1 V_2}{2NL_r T_{hs}} \int_{D_1 T_{hs}}^{T_{hs}} \sum_{T_r} T_r (t - x_j) dt$$
 (6)

B. Power-transfer calculation

From (6), it can be seen that there are only two conditions for calculating the intergration of $T_r(t - x_j)$, e.g., $D_1 \le x_j$ and $D_1 > x_j$, as shown in Fig. 10. If $D_1 \le x_j$, two intervals $[D_1 T_{hs}, x_j T_{hs}]$ and $[x_j T_{hs}, T_{hs}]$ should be considered due to the piecewise expressions of $T_r(t - x_j)$, as shown in Fig. 10 (a), while only one interval $[D_1 T_{hs}, T_{hs}]$ should be considered if $D_1 > x_j$, as shown in Fig. 10 (b). Based on (5), intergration of $T_r(t - x_j)$ of the two conditions can be given as

$$\int_{D_{l}T_{hs}}^{T_{hs}} T_{r}(t-x_{j})dt =
\begin{cases}
0.25(2x_{j}^{2}+D_{l}^{2}-2x_{j}D_{l}-2x_{j}+D_{l})T_{hs}^{2}, & D_{l} \leq x_{j} \\
0.25(-D_{l}^{2}+2x_{j}D_{l}-2x_{j}+D_{l})T_{hs}^{2}, & D_{l} > x_{j}
\end{cases} (7)$$

Therefore, according to the relationships between D_1 and the four phase-shift ratios x_j of the HV side, each integration of $T_r(t-x_j)$ can be calculated based on (7), and the power model can be further obtained by adding the four integration parts together. In this way, the relationships between D_1 and x_j is the only factor to be considered rather than the slopes, initial and final values of i_L in modeling process.

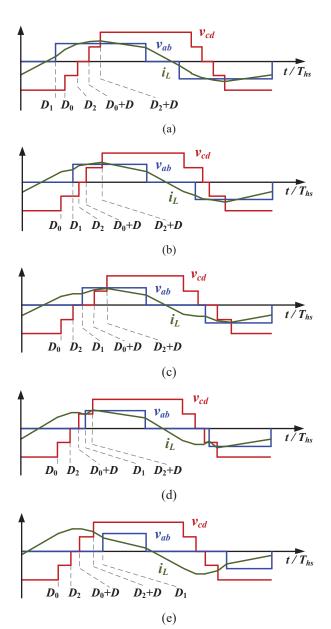


Fig. 11. Operating modes divided by different mode constraints. (a) Mode 1: $D_1 \le D_0 \le D_2 \le D_0 + D \le D_2 + D$. (b) Mode 2: $D_0 \le D_1 \le D_2 \le D_0 + D \le D_2 + D$. (c) Mode 3: $D_0 \le D_2 \le D_1 \le D_0 + D \le D_2 + D$. (d) Mode 4: $D_0 \le D_2 \le D_0 + D \le D_1 \le D_2 + D$. (e) Mode 5: $D_0 \le D_2 \le D_0 + D \le D_2 + D \le D_1 \le D_0 + D \le D_2 + D \le D_1$.

From the above analysis, with various relationship between D_1 and x_j , the power-transfer expressions will be different, which means the DAB converters work at different operating modes. From the operating constraints shown in (1), it can be seen that the relationship among the phase-shift ratios of the HV side is determined as $D_0 \le D_2 \le D_0 + D \le D_2 + D$. Thus, by taking D_1 into consideration, five operating modes can be obtained, i.e., Mode 1: $D_1 \le D_0 \le D_2 \le D_0 + D$

TABLE II
PARAMETERS OF THE SIMULATION MODEL

Parameters	Values
Input volatge V_1	200 V
Transformer turns-ratio N	1
Inductor L_r	100 μΗ
Switching frequency f_s	10 kHz
Input-side capacitor C_1	1 mF
Output-side capacitors C_2 , C_3	1 mF

 $\leq D_2 + D$; Mode 2: $D_0 \leq D_1 \leq D_2 \leq D_0 + D \leq D_2 + D$; Mode 3: $D_0 \leq D_2 \leq D_1 \leq D_0 + D \leq D_2 + D$; Mode 4: $D_0 \leq D_2 \leq D_0 + D \leq D_1 \leq D_2 \leq D_0 + D \leq D_1 \leq D_2 \leq D_0 + D \leq D_2 \leq D_0 + D \leq D_2 \leq D_0 + D \leq D_1$. The waveforms of the five operating modes are shown in Fig. 11, where the mode constraints are also given for each operating mode. Subsequently, the normalized power model of each mode can be calculated according to (6) and (7), as shown in (8), where $P_N = V_1 V_2 T_{hs} / (4NL_r)$ is the maximum transferred power.

IV. SIMULATION RESULTS

In order to verify the effectiveness of the operating constraints and accuracy of the proposed model, simulations are performed. The key parameters are shown in Table II.

Fig. 12 illustrates the simulation results of the five operating modes, in which the reference output voltage V_2^* is set as 400V. It can be seen that with different relationship of the phase-shift ratios, the waveform of v_{cd} can be maintained at five-level under all operating modes, and there is no waveform distortion, e.g., during the change in the polarity of the inductor current, indicating the effectiveness of the principle and operating constraints.

A comparison between the theoretical-calculated power based on the model and simulated power is shown in Fig. 13, where $D_2 = 0.2$, $D_0 = 0.1$, D = 0.1, $V_2^* = 400$ V, and D_1 is regulated from 0 to 0.35. It indicates that the results match well under different operating modes and the whole range of the transmission power. Therefore, the accuracy of the power model proposed in this paper is verified.

V. CONCLUSION

This paper investigated the phase-shift control scheme for the 2/3-level DAB converters by analyzing the switching characteristics. Firstly, a general operating principle for different phase-shift control schemes of the 2/3-level DAB converters was presented. Under such a principle, the steady-state waveforms can be decoupled from the inductor current polarity, and become only dependent of the sequences of the drive signals. In this way, the transferred power can be controlled by the phase-shift ratios without waveform distortions. Based on this principle, the operating constraints of the five-level control scheme for the 2/3-level DAB

$$P_{0} = \frac{P}{P_{N}} = \begin{cases} 2(-D_{1}^{2} - D_{2}^{2} - D_{0}^{2} - D^{2} + D_{1}D_{2} + D_{1}D_{0} + D_{1}D - D_{0}D - D_{2}D - D_{1} + D_{2} + D_{0} + D), & \text{Mode 1} \\ 2(-0.5D_{1}^{2} - D_{2}^{2} - 0.5D_{0}^{2} - D^{2} + D_{1}D_{2} + D_{1}D - D_{0}D - D_{2}D - D_{1} + D_{2} + D_{0} + D), & \text{Mode 2} \end{cases}$$

$$2(-0.5D_{2}^{2} - 0.5D_{0}^{2} - D^{2} + D_{1}D - D_{0}D - D_{2}D - D_{1} + D_{2} + D_{0} + D), & \text{Mode 3}$$

$$2(0.5D_{1}^{2} - 0.5D_{2}^{2} - 0.5D^{2} - 0.5D^{2} - D_{1}D_{0} - D_{2}D - D_{1} + D_{2} + D_{0} + D), & \text{Mode 4}$$

$$2(D_{1}^{2} - D_{1}D_{0} - D_{1}D_{2} - D_{1}D - D_{1} + D_{2} + D_{0} + D), & \text{Mode 5}$$

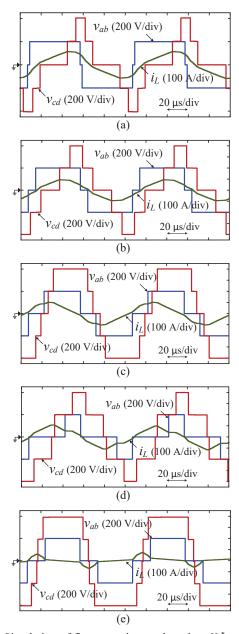


Fig. 12. Simulation of five operating modes when $V_2^* = 400$ V. (a) Mode 1. (b) Mode 2. (c) Mode 3. (4) Mode 4. (5) Mode 5.

converters were obtained to maintain the effectiveness of this modulation scheme. In addition, a unified power-transfer model was proposed according to an equivalent method, which simplifies the model compared with traditional methods. Simulation results have confirmed that the operating constraints of the 2/3-level DAB converters under the five-level control scheme can be ensured, and the accuracy of the proposed power model is adequate under the entire power-transfer range.

REFERENCES

[1] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified Triple-Phase-Shift Control to Minimize Current Stress and Achieve Full Soft-Switching of Isolated Bidirectional DC–DC Converter," *IEEE Trans. Ind. Electron*, vol. 63, no. 7, pp. 4169-4179, Jul. 2016.

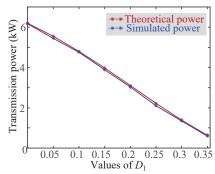


Fig. 13. Comparative results between theoretical power and simulated power.

- [2] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl*, vol. 27, no. 1, pp. 63-73, Jan.-Feb. 1991.
- [3] M. A. Moonem and H. Krishnaswami, "Analysis and Control of Multi-Level Dual Active Bridge DC-DC Converter," in *Proc. ECCE*, Raleigh, 2012, pp. 1556-1561.
- [4] H. Shi, H. Wen, and Y. Hu, "Deadband Effect and Accurate ZVS Boundaries of GaN-Based Dual-Active-Bridge Converters With Multiple-Phase-Shift Control," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9886-9903, Sept. 2020.
- [5] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148-3172, Mar. 2020.
- [6] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link powerconversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091-4106, Aug. 2014.
- [7] P. Liu, C. Chen, S. Duan, and W. Zhu, "Dual Phase-Shifted Modulation Strategy for the Three-Level Dual Active Bridge DC-DC Converter," *IEEE Trans. Ind. Appl.*, vol. 64, no. 10, pp. 7819-7830, Oct. 2017.
- [8] A. Filba-Martinez, S. Busquets-Monge, J. Nicolas-Apruzzese, and J. Bordonau, "Operating principle and performance optimization of a three-level NPC dual-active-bridge DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 678-690, Feb. 2016.
- [9] A. Filba-Martinez, S. Busquets-Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of multilevel NPC dual active bridge DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2499-2510, Apr. 2020.
- [10] M. A. Moonem, T. Duman, and H. Krishnaswami, "Capacitor voltage balancing in a neutral-point clamped multilevel dc-dc dual active bridge converter," in *Proc. PEDG*, Florianopolis, 2017, pp. 1-7.
- [11] B. Zhao, Q. Song, W. Liu, G. Liu, and Y. Zhao, "Universal high frequency- link characterization and practical fundamental-optimal strategy for dual-active-bridge dc-dc converter under PWM plus phaseshift control," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6488– 6494, Dec. 2015.
- [12] D. Mou, Q. Luo, Z. Wang, J. Li, Y. Wei, H. Shi, and X. Du, "Optimal asymmetric duty modulation to minimize inductor peak-to-peak current for dual active bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4572-4584, Apr. 2021.
- [13] C. Wang, G. Sha, H. Cheng, and Q. Deng, "Unified phasor analytical method for dual-active-bridge dc/dc converter under phase-shift control," in *Proc. IPEMC-ECCE Asia.*, Hefei, 2016, pp. 348–355.
- [14] A. Tong, L. Hang, X. Jiang, and S. Gao, "Modeling and analysis of dual-active-bridge isolated bidirectional DC-DC converter to minimize RMS current With Whole Operating Range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302-5316, Jun. 2018.