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Reliability Analysis of Capacitors in Voltage Regulator Modules with Consecutive Load Transients

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***Abstract*—Capacitors are critical in voltage regulator modules (VRMs) which contribute to store energy and stabilize the output voltage during load transients. Usually, VRMs work with consecutive load transients, which would bring more electro-thermal stress to capacitors and affect the reliability of capacitors compared with the steady-state operation. Recently, some efforts have been made to investigate the reliability of capacitors in power electronic converters. Unfortunately, transient processes are commonly ignored, which can impair the accuracy of the lifetime estimation. Regarding this issue, this paper investigates the influence of transients on the damage of capacitors in VRMs. A 150 W VRM is introduced as a case study. Firstly, the electro-thermal stresses during steady state and transients are analyzed. Then, the lifetime calculation is considered from a single capacitor to hybrid capacitor banks. In addition, a suitable capacitor configuration of capacitor banks is also provided, in order to maximize its lifetime.**

***Index Terms*—Capacitors, voltage regulator module (VRM), reliability evaluation, load transients.**

I. Introduction

VOLTAGE regulator modules (VRMs) are widely used as power supplies for modern electronic applications with continuously varying loading conditions, such as digital signal processors, microprocessors, etc. [1]. In order to store energy and stabilize the output voltage during transients, a large capacity filter capacitor bank consisting of Aluminum Electrolytic Capacitors (Al-Caps) and Multi-Layer Ceramic Capacitors (MLC-Caps) is commonly applied at the output side of VRMs. However, capacitors are often considered to be the weakest components in power electronic systems [2]. For reliability reasons, it is important to investigate the lifetime of capacitors to provide a reference for capacitor sizing.

Usually, capacitor manufacturers provide a lifetime calculation model for their products [3]. However, the capacitor lifespan is estimated under a special condition with a given ambient temperature, ripple current, and capacitor voltage. The estimation result can not accurately represent the lifetime of capacitors in the actual operation with varied electro-thermal stress.

To improve the evaluation accuracy, some mission profile based reliability assessment methods have been presented in recent years. In [4], [5], a real mission profile and statistical approaches are used to evaluate the lifetime of capacitors. However, there is a lack of research focusing on the reliability evaluation of capacitors in VRMs, and some limitations exist in applying the above-mentioned methods in VRMs.

1) Few research efforts have investigated the lifespan of hybrid capacitor banks consisting of Al-Caps (non-solid or polymer Al-Caps) and MLC-Caps, which are widely used in VRMs.
2) Low sampling-rate mission profiles (the sampling rate is usually in the order of minutes, and it is in the order of hours in [4]) cannot represent the actual operation state of VRMs (the loading step frequency is usually larger than 1kHz [6]), which results in some important loading information are ignored.
3) The loading profiles in [4], [5] are sampled in steady state, which ignores the transient processes. For VRM applications, the current and voltage stresses of capacitors during transients are usually larger than that for steady state. Ignoring the transient processes would result in inaccurate estimation results.
4) There is a lack of a thermal model to describe the temperature dynamic for capacitors. In [4], [5], the hotspot temperature is calculated using the steady-state thermal resistance of capacitors, which is inaccurate for capacitors in VRMs.

In order to fill up the gap of reliability analysis of capacitors in VRMs, this paper investigates the lifetime of hybrid capacitor banks in VRMs. The main contributions are given as follows.

1) A thermal model is proposed to describe the temperature dynamic of capacitors in VRMs with consecutive load transients.
2) The electro-thermal stresses of capacitors during steady-state and transient processes are analyzed. Then the annual damage of different types of capacitors including non-solid Al-Caps, polymer Al-Caps, and MLC-Caps are investigated.
3) A reliability-oriented design method is used to investigate the lifetimes of capacitor banks with different configurations, which provides a reference for capacitor sizing.

The rest of this paper is organized as follows: Section II describes the capacitors functions in VRMs. A reliability analysis procedure of capacitors in VRMs is presented in Section III. Finally, conclusions are drawn in Section IV.

II. Capacitors in Voltage Regulator Modules

A. Electrical Stress of Capacitors in VRMs

In VRM applications, synchronous buck converters are the most preferred topology, as shown in Fig. 1(a), where the output capacitor bank is composed of Al-Caps and MLC-Caps. The total equivalent series resistance (ESR) of the capacitor bank C_o is defined as R_{bank}, the total equivalent series inductance (ESL) is L_{bank}, and its capacitance is defined as C_{bank}. For VRMs, the amplitude and frequency of loading current (i_o) step are variable, a typical example of which is shown in Fig. 1(b).

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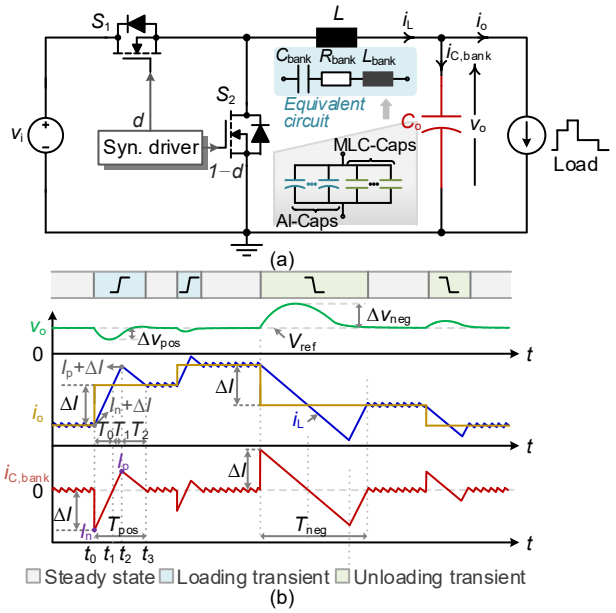

Fig. 1. Topology and key waveforms of a VRM. (a) Topology of a synchronous buck converter. (b) Key waveforms.

In order to achieve an optimal transient performance, some state-of-the-art control techniques including V^2 control [7], time-optimal control [1], [8], etc., have been widely used in VRMs. These control techniques have pushed the transient performance of a VRM close to its physical limit, as shown in Fig. 1(b), where v_i, v_o, i_L, $i_{C,bank}$ represent the input voltage, output voltage, inductor current, and capacitor current of a capacitor bank, respectively. Before the instant t_0, the converter works in steady state, the root mean square (RMS) of steady-state capacitor current is calculated as [9],

$$I_{RMS\_steady} = v_o(1-d)\Big/\left(f_s\sqrt{12}L\right) \tag{1}$$

where f_s, d, and L denote the switching frequency, duty cycle, and inductance, respectively.

At t_0, a positive load current step ΔI occurs (i.e., a loading transient), which causes a capacitor current step. At t_3, the output voltage again reaches to the reference voltage V_{ref}. The RMS value of the capacitor current during the loading transient is calculated as [9]

$$I_{RMS\_pos} = \sqrt{\frac{I_n^2 + I_p^2 + I_n I_p}{3}\times\frac{T_0+T_1}{T_{pos}} + \frac{I_p^2}{3}\times\frac{T_2}{T_{pos}}} \tag{2}$$

where the current peak values I_p, I_n are

$$I_n = -\Delta I,\quad I_p = (v_i - v_o)(T_0+T_1)/L - \Delta I \tag{3}$$

The transient period T_{pos}, and the durations T_0 (t_0 to t_1), T_1 (t_1 to t_2), T_2 (t_2 to t_3) can be obtained from [1].

Referring to Fig. 1, the RMS value of the capacitor voltage during steady state equals to V_{ref}. During transients, the voltage trajectory can be approximated to a half-wave sine curve. The RMS value during the loading transient is calculated as

$$V_{RMS\_pos} = V_{ref} - \Delta v_{pos}/\sqrt{2} \tag{4}$$

where, Δv_{pos} represents the voltage undershoot [1], i.e.,

$$\Delta v_{pos} = \frac{R_{ESR}^2 C_{bank}^2 (v_i^2 - 2v_i v_o + v_o^2) + \Delta I^2 L^2}{2(v_i - v_o)LC_{bank}}. \tag{5}$$

Similarly, the RMS values I_{RMS_neg} and V_{RMS_neg} of capacitor current and capacitor voltage during unloading transients can be calculated in the same way.

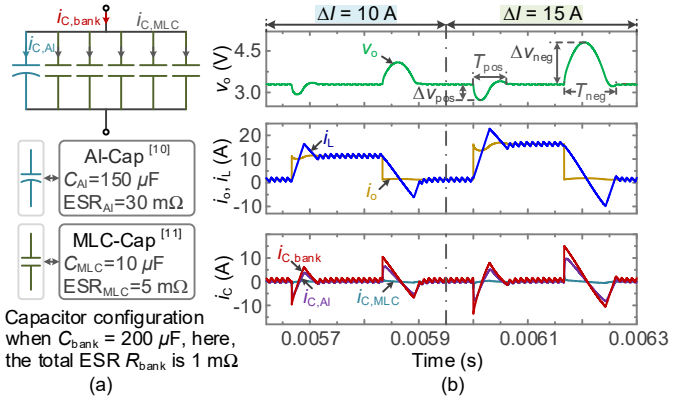

Fig. 2. Simulation results. (a) Capacitor configuration of the capacitor bank when C_{bank} = 200 μF. (b) Simulation waveforms of a VRM under different transients.

TABLE I
SIMULATION RESULTS OF THE CAPACITOR CURRENTS

Operating state	Total RMS current	RMS value of $i_{C,Al}$	RMS value of $i_{C,MLC}$
Steady state	0.62 A	0.32 A	0.06 A
ΔI = +15 A	4.96 A	3.68 A	0.26 A
ΔI = − 15 A	7.89 A	5.97 A	0.39 A

Considering the current distribution of individual capacitor in capacitor banks, the transient current of k-th capacitor in the bank is calculated as [5]

$$I_{k\_pos} = I_{RMS\_pos} \times C_k \Big/ \sum_{i=1}^{n} C_n \tag{6}$$

where C_k represents the capacitance of k-th capacitor in the bank, and n is the number of capacitors. Similarly, the current distribution of capacitors during steady state can be calculated using the impedance at the switching frequency.

B. Simulation Validation

A 150 W VRM is built in the PSIM simulation environment, the key parameters are given as follows: V_i = 12 V, V_o = 3.3 V, L = 13 μH, f_s = 100 kHz. Taking a 200 μF (R_{bank} ≈1 mΩ) capacitor bank as an example, Fig. 2(a) shows the capacitor configuration, where two different types of capacitors are considered. The types of Al-Caps and MLC-Caps are PSLP8075105142006 (150 μF/ 6.3 V, ESR_{Al} = 30 mΩ [10]) and GRM185R60J106ME15 (10 μF/ 6.3 V, ESR_{MLC} = 5 mΩ [11]), respectively. Notice that the capacitor current of these four MLC-Caps $i_{C,MLC}$ are the same due to the same capacitor parameters, the capacitor current of the Al-Caps is denoted as $i_{C,Al}$. Two different load steps are chosen as examples, i.e., ΔI = 10 A and ΔI = 15 A, Fig. 2(b) shows the steady-state and transient waveforms of v_o, i_L, i_o, $i_{C,bank}$, $i_{C,Al}$, and $i_{C,MLC}$. It is found that the voltage deviations Δv_{pos}, Δv_{neg} and setting time T_{pos}, T_{neg} for different transients are different.

To verify the current distribution of the capacitor bank, Table I lists the simulation results of the capacitor current during steady-state and the 15 A load transient, which are approximately equal to the calculation results in (6). Moreover, Fig. 2(b) illustrates that $i_{C,bank} = i_L - i_o$, so the total RMS values of capacitor banks can be calculated using i_L and i_o.

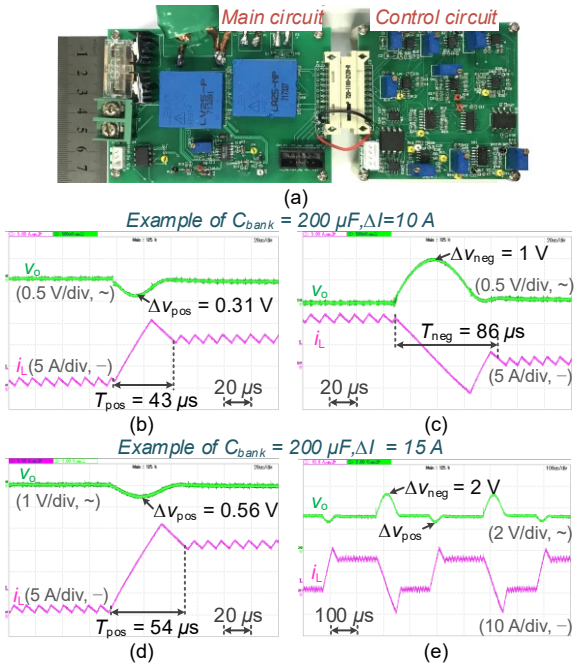

Fig. 3. Experimental results (a) Photo of the built VRM. (b) Loading transient when ΔI = 10 A. (c) Unloading transient when ΔI = 10 A. (d) Loading transient when ΔI = 15 A. (e) Repetitive transient when ΔI = 15 A.

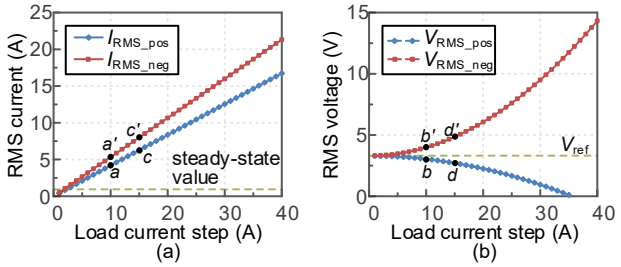

Fig. 4. Capacitor current and capacitor voltage RMS values under different load current steps. (a) Capacitor current RMS values. (b) Capacitor voltage RMS values.

C. Experimental Validation

Fig 3(a) shows the built VRM, which uses the same parameters in simulation. Figs. 3(b) and (c) show the experimental results of loading transient and unloading transient when ΔI = 10 A. Figs. 3(d) and (e) show the experimental results of loading transient and repetitive transient when ΔI = 15 A [8]. Referring to Figs. 3(b) and (d), it is found that the voltage undershoots Δv_{pos} and setting time T_{pos} for different transients are different. Moreover, the calculated RMS values for a 10 A load transient are I_{RMS_pos} = 3.45 A, I_{RMS_neg} = 4.82 A, V_{RMS_pos} = 3.1 V, V_{RMS_neg} = 4.0 V, which are consistent with the theoretical values in Fig. 4 (i.e., points *a*, *a'*, *b*, and *b'*). The calculated RMS values for a 15 A load transient are I_{RMS_pos} = 5.61 A, I_{RMS_neg} = 7.51 A, V_{RMS_pos} = 2.9 V, V_{RMS_neg} = 4.71 V, which are also consistent with the theoretical values in Fig. 4 (i.e., points *c*, *c'*, *d*, and *d'*). Based on the calculated I_{RMS_pos} and I_{RMS_neg}, the RMS current for each individual capacitor can be derived using (6).

Moreover, the theoretical results in Fig. 4 illustrate that the RMS currents during transients are larger than for the steady-state. For capacitor current during transients, the RMS current increases as the load current step increases. For capacitor voltage during transients, RMS voltage during unloading transients increases as the load step ΔI increases. And, the RMS voltage during loading transients decreases as ΔI increases.

III. Reliability-Oriented Design of Capacitors in VRMs

The procedure for designing the capacitor bank of VRMs is shown in Fig. 5, which are detailed discussed in the following.

A. Mission Profile and Capacitor Types Selection

VRMs are widely used as power supplies for various node components in data centers. The daily ambient temperature of a data center [12] with a sample rate of one hour is shown in Fig. 6(a). In order to obtain the detailed load transient information, a short time-scale loading profile is considered, as shown in Fig. 6(b) [13], it is found that the load current fluctuates continuously. As the loading step frequency of VRMs is usually larger than 1 kHz [6], here, the sampling frequency f_{samp} is defined as 2 kHz.

Referring to Fig. 5, the capacitor types can be selected based on the mission profile and system specifications. In this case study, the output voltage of the VRM is 3.3 V, three different types of capacitors with a rated voltage of 6.3 V are considered. Detailed parameters of capacitors are shown in Table II, where R_{ha} and τ_{ha} represent the thermal resistance and thermal time constant from the hotspot to ambient, respectively.

Assuming the design aim of the VRM is to keep the maximum voltage undershoot (e.g., ΔI = 15 A) within 5% of the steady-state reference value.

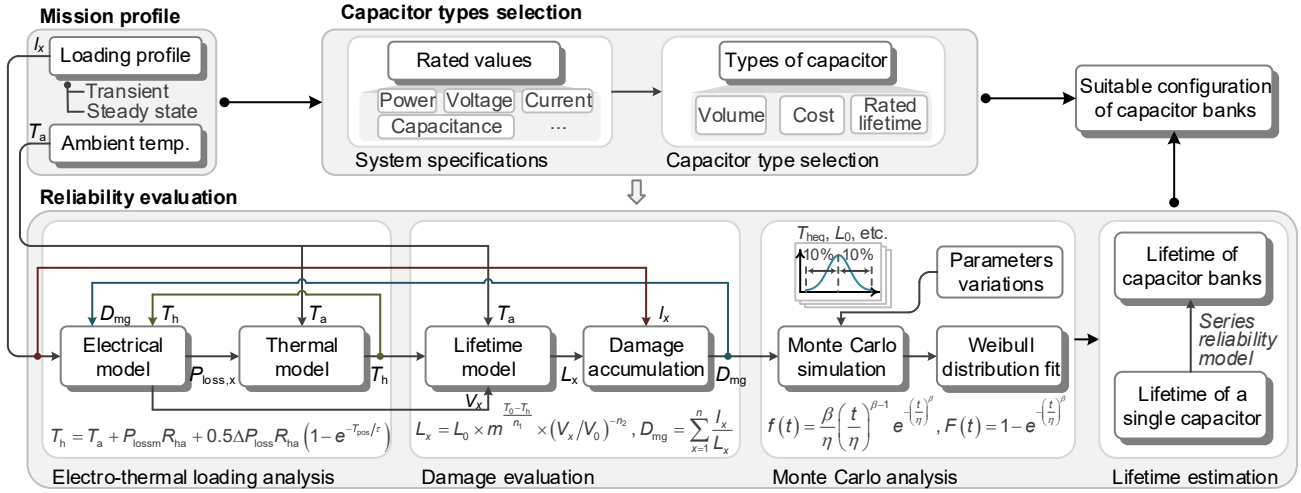

Fig. 5. Reliability-oriented design of capacitor banks in VRMs.

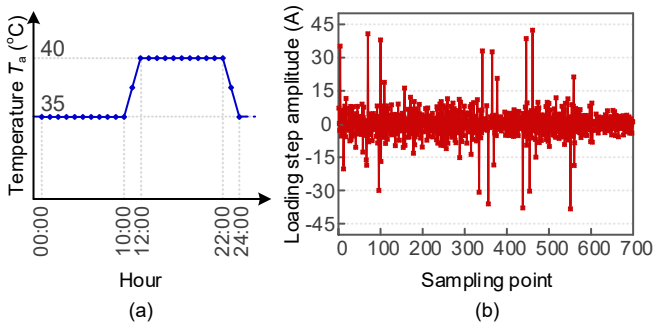

Fig. 6. Mission profile of VRMs in a data center. (a) Daily ambient temperature in a data center. (b) Loading profile of a VRM in a specified period.

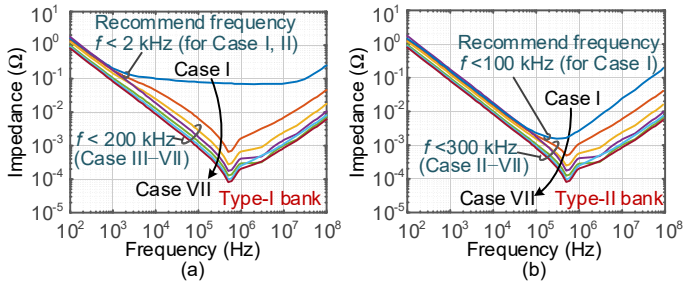

Fig. 7. Impedance characteristics of hybrid capacitor banks. (a) Capacitor banks consisting of non-solid Al-Caps and MLC-Caps. (b) Capacitor banks consisting of polymer Al-Caps and MLC-Caps.

TABLE II
SPECIFICATIONS AND PARAMETERS OF EMPLOYED AL-CAPS AND MLC-CAPS

Parameter	Non-solid Al-Cap: WCAP-ASLI 865060143005 [10]	Polymer Al-Cap: WCAP-PSLP 875105142006 [10]	MLC-Cap: ZRB GRM185R60J106ME15, GRM21BR60J107ME15 [11]
Dimension	43.6×5.5 mm	28.1×5.5 mm	1.3×0.5 mm 2.5×1.25 mm
Rated capacity	150 μF/6.3V	150 μF/6.3 V	10μF/6.3 V 100μF/6.3 V
Initial ESR	510 mΩ @ 100 kHz, 20 °C	30 mΩ @ 100 kHz, 20 °C	5 mΩ, 1 mΩ @ 100 kHz, 25 °C
Rated lifetime	2000 h [10] @ +105 °C, 6.3 V	2000 h [10] @ +105 °C, 6.3 V	1000 h [14] @ +85 °C, 12.6 V
R_{ha} [15]	55.6 °C/W	133.1 °C/W	22.9 °C/W
τ_{ha} [16],[17]	40 s	83.9 s	0.14 s

According to the calculation results in (5), a 1000 μF capacitor bank is required. The possible combinations of capacitor bank are listed in Table III. Notice that the configurations of capacitor banks consider the influence of voltage on the capacitance of MLC-Caps. There exist 7 different configurations, the impedance characteristics of these capacitor banks are shown in Fig. 7, where Fig. 7(a) shows the impedance characteristics for capacitor banks consisting of non-solid Al-Caps and MLC-Caps (i.e., Type I), Fig. 7(b) shows that for capacitor banks consisting of polymer Al-Caps and MLC-Caps (i.e., Type II). It should be noted that the impedance data of MLC-Caps are obtained at 0 V/25 °C [11]. Generally, the recommended operating frequencies f of capacitor banks are at the frequency band in which the impedance is dominated by capacitance, as shown in Fig. 7.

B. Reliability Analysis of a Single Capacitor

The procedure to assess reliability is shown in the bottom of Fig. 5, which mainly includes four steps. Notice that the feedback loops from the hotspot temperature T_h and the accumulated damage D_{mg} to the electrical model represent ESR and C degradation. Taking the capacitor bank configuration in Case IV as an example, the reliability evaluation process is given as follows.

1) Electro-thermal loading analysis

Thermal stress is the critical stressor of capacitors' wear-out failure, which is mainly caused by the rise of the hotspot temperature of capacitors. Taking an AL-Cap as an example, the electro-thermal model is shown in Fig. 8(a) [4], the hotspot temperature T_h of capacitors is affected by the ambient temperature T_a and power loss of capacitors. Taking the loading transient as an example, Fig. 8(b) shows the electro-thermal response waveforms of capacitors.

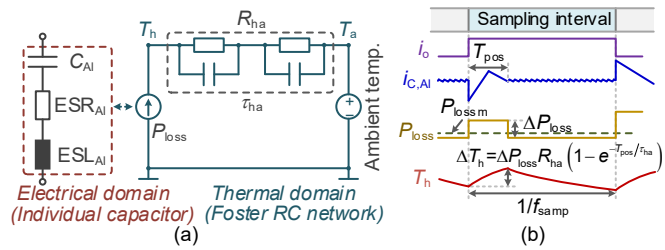

Fig. 8. Electro-thermal models and response waveforms of an individual capacitor under consecutive load transients. (a) Electro-thermal models. (b) Electro-thermal response waveforms.

TABLE III
DIFFERENT CONFIGURATIONS OF CAPACITOR BANKS

Capacitor types [10], [11]	Number of capacitors in different configuration cases						
	Case I	Case II	Case III	Case IV	Case V	Case VI	Case VII
150 μF Non-solid or Polymer Al-Cap	7	6	5	4	3	2	1
100μF MLC-Cap (35μF @ 3.3V)	0	3	7	11	15	20	24
10μF MLC-Cap II (3.5μF @ 3.3V)	0	0	2	5	8	0	3

Based on the Foster RC network model, the hotspot temperature fluctuation caused by step loss ΔP_{loss} is calculated as [18]

$$\Delta T_h = \Delta P_{loss} R_{ha}\left(1-e^{-T_{pos}/\tau_{ha}}\right) \tag{7}$$

According to Fig. 8(b), T_h during one sampling interval (i.e., one load step period, $1/f_{samp}$) is approximately calculated as

$$T_h = T_a + P_{lossm} R_{ha} + 0.5\Delta P_{loss} R_{ha}\left(1-e^{-T_{pos}/\tau_{ha}}\right) \tag{8}$$

where P_{lossm} represents the mean loss and step loss of capacitors during this sampling interval, which can be calculated based on P_{loss}. Furthermore, P_{loss} is calculated as $P_{loss} = ESR_{Al} \cdot I_{RMS,Al}^2$, where $I_{RMS,Al}$ represents the RMS current of an individual Al-Cap at different transient modes. T_h can be approximate as $T_h = T_a + P_{lossm} \times R_{ha}$ when $\tau_{ha} >> T_{pos}$. Here, the mean loss P_{lossm} can be calculated using the mean value of multiple sampling intervals. Then, T_h represents the hotspot temperature for multiple intervals. Notice that the thermal model is also suitable for other types of capacitors in capacitor banks.

Based on the foregoing analysis, the hotspot temperature of capacitors can be calculated using the sampling interval as unit. Referring to Fig. 6(b), the current during sampling points 230 to 270 are repetitive with ±10 A steps. Taking these sampling intervals as an example, Fig. 9(a) shows the power loss (the top part) and temperature profile (the bottom part) of individual Al-Cap in the capacitor bank (i.e., Case IV). Here, the current distribution of different capacitors is considered. Referring to Fig. 9(a), P_{lossm} for an unloading transient interval and a loading transient interval are 0.19 W and 0.08 W, respectively. Based on (8), T_h for these two intervals are 35.56 °C and 29.45 °C, respectively. The mean value of T_h during these two intervals is 32.5 °C, which is consistent with the simulated T_h based on the total interval (i.e., sampling point from 230 to 270). The simulation results are consistent with the theoretical results from

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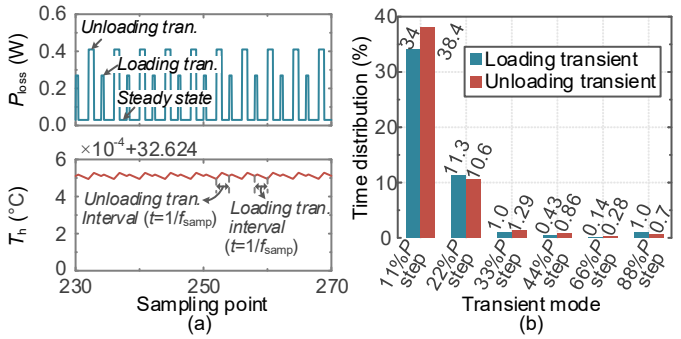


Fig. 9. Thermal simulation waveforms and transient mode distribution. (a) Simulation waveforms of the non-solid Al-Cap in the bank (Case IV). (b) Transient mode distribution.

TABLE IV
SUMMARY OF THE LIFETIME MODEL PARAMETERS USED IN (9)

Parameters	Non-solid Al-Cap [4]	Polymer Al-Cap [3]	MLC-Cap [19]
m	2	10	2
n_1	10	20	8
n_2	0	0	3

(8), which illustrates the feasibility of this thermal model.

In this case study, the power steps are divided into six typical values for the sake of simplicity, i.e., 11%P, 22%P, 33%P, 44%P, 66%P, and 88%P, where P represents the rated power of a VRM. Assuming that the mission profile in Fig. 6(b) is repeated every 0.35 s, the time distribution of different transient models is shown in Fig. 9(b).

2) Accumulated damage evaluation

The widely used lifetime model and accumulated damage model for lifetime evaluation of capacitors are [3], [4], [19]

$$L_x = L_0 \times m^{\frac{T_0 - T_h}{n_1}} \times \left(V_x / V_0\right)^{-n_2},\ D_{mg} = \sum_{x=1}^{n} \frac{l_x}{L_x} \tag{9}$$

where L_0, V_0, and T_0 denote the rated lifetime, rated voltage, and hotspot temperature under the reference condition, l_x, L_x, V_x, and T_h represent the operation time, calculated lifetime, capacitor voltage, and hotspot temperature under the used conditions. The coefficient m, n_1, and n_2 denote the temperature coefficient, temperature-dependent constant, and voltage stress exponent respectively, which are summarized in Table IV.

According to the mission profile, the annual damage of each type of capacitor cell can be calculated, as shown in Fig. 10, where Fig. 10(a) shows the result for the non-solid Al-Cap in Type-I bank, Figs. 10(b)−10(d) show the results for the polymer Al-Cap and the MLC-Cap (100 μF and 10 μF) in Type-II bank. Referring to Fig. 10(a), it can be seen that the damage consumption of the non-solid Al-Cap (D_{mg} = 13.7) is larger than 1, which illustrates that its lifetime is shorter than 1 year.

From Figs. 10(b)−10(d), it is found that the polymer Al-Cap (D_{mg} = 3.14×10^{-2}) has relatively low annual damage. And the damage for the MLC-Caps (D_{mg} equals to 7.87×10^{-3} and 7.81×10^{-3}) are the lowest. For Al-Caps, the wear-out failure is mainly caused by the current stress [2]. From Fig. 10, it is easily found that the majority of damage consumption of Al-Caps occurs during the 88%P step period due to the highest current stress [i.e., thermal stress, c.f. (8)] on capacitors in this mode. Different from that, the majority of damage consumption of MLC-Caps mainly occurs during the 11%P step period due to the operation time of this mode is longest. Here, the failure is dominated by voltage stress due to the thermal stress on MLC-Caps is relatively small (as the ESR is very small). Taking 22%P step as an example, it is found that the damage consumption during unloading transient is larger than that during loading transient due to larger voltage and current stresses on capacitors.

3) Monte Carlo analysis and lifetime evaluation

To address the uncertainty in the above mentioned accumulated damage estimation process, a statistical approach based on Monte Carlo simulation is introduced to the estimation process. Assuming that all the variations of parameters obey the normal distribution, 100000 samples are chosen to analyze the time-to-failure of capacitors, as shown in Fig. 11. Here, T_{heq}, L_0, and V_0 (similar to the distribution of T_{heq} and L_0, which is not shown in Fig. 11) are considered to have a 10% variation, respectively. Notably T_{heq} is the equivalent hotspot temperature calculated from D_{mg}. Usually, the time-to-failure of samples obey with Weibull distribution [4], i.e.,

$$f(t) = (\beta/\eta)\cdot(t/\eta)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}},\ F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{10}$$

where β and η represent the shape parameter and the scale parameter, respectively. Based on this, the histograms of years to failure and failure probability for different types of capacitors are shown in Fig. 11. It is found that the B_1 lifetimes of polymer Al-Caps and MLC-Caps are approximately equaled to 16.6 and 85.7 (or 87) years, respectively.

4) Reliability analysis of hybrid capacitor banks

Table V lists the total volumes and costs for each capacitor bank configuration (i.e., Case I to Case VII in Table III), where the non-solid Al-Cap is not considered due to its lifetime is less than 1 year. In Table V, the total volume is approximately calculated as the total base area of capacitors multiply the maximum height.

Based on the series reliability model in Fig. 12(a) [4], the wear-out failure probability curves of capacitor banks are shown in Fig. 12(b). It is found that the lifetime of the capacitor bank

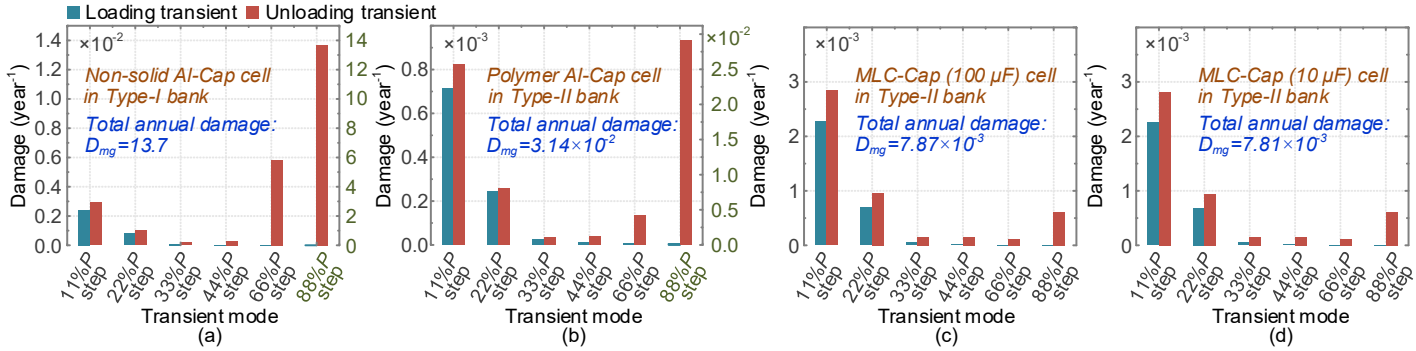


Fig. 10. Annual damage for different types of capacitor cells. (a) Annual damage of non-solid Al-Cap cell in Type-I bank. (b) Annual damage of polymer Al-Cap cell in Type-II bank. (c) Annual damage of MLC-Cap (100 μF) cell in Type-II bank. (d) Annual damage of MLC-Cap (10 μF) cell in Type-II bank.

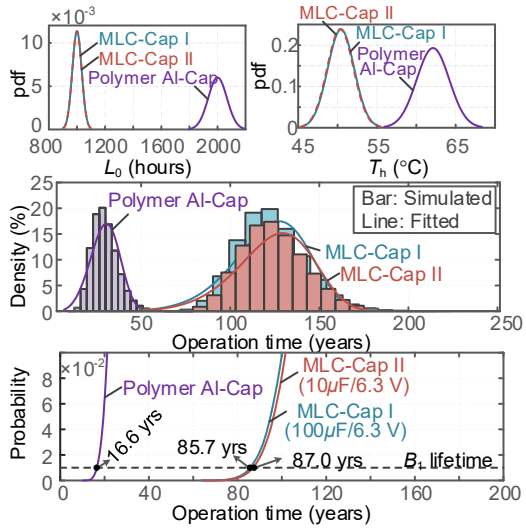
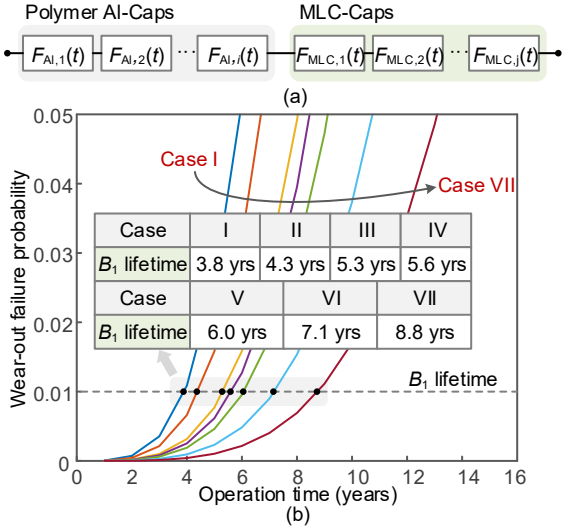


Fig. 11. Monte Carlo simulation results for capacitors in a bank (Case IV).



Case	I	II	III	IV
B_1 lifetime	3.8 yrs	4.3 yrs	5.3 yrs	5.6 yrs
Case	V	VI	VII	
B_1 lifetime	6.0 yrs	7.1 yrs	8.8 yrs	

Fig. 12. Wear-out probability curves of different capacitor bank configurations. (a) Series reliability model. (b) Wear-out probability curves.

TABLE V
COMPARISON OF THE TOTAL VOLUMES AND COSTS FOR EACH CASE

Capacitor types	Case I	Case II	Case III	Case IV	Case V	Case VI	Case VII
Total volume (base area × height, mm)	196.7 × 5.5	176.1 × 5.5	160.1 × 5.5	146.3 × 5.5	132.1 × 5.5	106.2 × 5.5	91.9 × 5.5
Cost (USD)	3.57	3.69	6.25	8.89	11.53	13.96	16.6

increases as the number of employed polymer Al-Caps decreases. For Case I, the B_1 lifetime is 3.8 years, which is significantly shorter than 8.8 years for Case VII. Moreover, the total volume of Case VII is smaller than that for Case I. However, the total cost of Case VII is higher than that for Case I. From the perspective of reliability, it is recommended to reduce the number of polymer Al-Caps to improve the reliability of the capacitor bank.

IV. CONCLUSION

This paper investigates the lifetime of capacitors in VRMs with consecutive load transients. Based on a case study (a 150 W VRM), the electro-thermal stresses, annual damage, estimated lifetime of capacitors are analyzed. The main conclusions are as follows:

1) The damage consumption of Al-Caps mainly occurs during the transient with higher current stress. The majority of damage consumption of MLC-Caps occurs during the transient with longer operation time.

2) The lifetime of non-solid Al-Cap in VRMs is less than 1 year, which illustrates that it is not suitable for VRMs.

3) For hybrid capacitor banks consisting of polymer Al-Caps and MLC-Caps, reduction of the number of polymer Al-Caps can improve the reliability of capacitor banks while reducing the total volume of capacitors. However, the total cost of capacitor banks is increased.

4) For VRMs consisting of multiphase buck converters with different types of capacitors and different rated power, the evaluation method of lifetime for capacitors is the same.

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