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MODELING AND REDUCING THE PARASITIC CAPACITANCES IN MEDIUM-VOLTAGE INDUCTORS

BY
HONGBO ZHAO

DISSERTATION SUBMITTED 2021

AALBORG UNIVERSITY
DENMARK

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AALBORG UNIVERSITY
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“I think, therefore I am”

— *Rene Descartes*

ENGLISH SUMMARY

With the recent advancements of medium-voltage (MV) Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) technology, the MV converters are benefited from simpler circuit topologies, lower switching energy dissipation, and higher switching frequency than conventional Silicon devices. However, the fast switching behaviors (high *dv*/*dt*) introduced by MV SiC MOSFETs pose several challenges to the MV inductors, which can introduce significant capacitive current into the system due to the parasitic capacitance of MV inductors. To deal with this challenge holistically, this Ph.D. thesis focuses on developing physics-based and behavior-based modeling methods to characterize the capacitive couplings as well as approaches to reduce the parasitic capacitance of inductors.

The equivalent parasitic capacitance of inductors is frequency-dependent. The physics-based modeling method can predict the equivalent parasitic capacitance of inductors according to the geometrical structure and material parameters before the first resonant frequency. The improper assumptions for physically modeling the equivalent capacitance of inductors at the first resonant frequency is critiqued firstly. Then, a physics-based modeling method for calculating the parasitic capacitance of inductors considering the grounding effects is developed, which uses a three-terminal equivalent circuit to characterize the capacitive couplings of inductors instead of the conventional two-terminal equivalent circuit. Furthermore, the modeling methods of parasitic capacitance considering the fringe electrical field in copper-foiled MV inductors are presented.

In addition to the physics-based modeling, the behavior-based modeling method can represent the actual couplings by using the time-domain or frequency domain response of the inductors, where the valid frequency range is limited by the bandwidth of the devices that measure the time-domain or frequency-domain signals. A behavioral model of MV inductors is developed. It is firstly obtained from the impedance of the inductor measured by an impedance analyzer. Then, the capacitive coupling between terminal and core of inductors is characterized by using a multi-stage RLC circuit, the parameters of which are analytically calculated according to the measured impedance. The derived behavior-based model of inductors is finally used to build a digital twin of a double-pulse-test setup, where the simulated ground current shows good agreement with the measurements.

The approaches of reducing parasitic capacitance in MV inductors with multiple windings are further proposed. The physics-based modeling indicates that parasitic capacitance can be reduced by changing the geometrical structures, electrical connections, and winding layout. According to analytical calculations, several prototypes of inductors are manufactured, whose parasitic capacitance is reduced

significantly by using the proposed technologies. However, some of the technologies will sacrifice the power density of winding and may increase the manufacturing cost.

Finally, the remained challenges of modeling the parasitic capacitance of medium-voltage inductors are summarized. Conclusions and future research are given at the end of this thesis.

The thesis is in a paper-collection type, which is basically combined by five journal papers, two conference papers, and one filed patent by Danish Patent and Trademark Office.

DANSK RESUME

Grundet de seneste forbedringer i teknologien bag mellemspændings siliciumkarbid (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET), har mellemspændings strømforsyninger set forbedringer i form af simplere kredsløbstopologier, lavere skiftetab og operation ved højere frekvenser, sammenlignet med mellemspændings-systemer baseret på traditionelle silicium komponenter. Men de høje spændingshældninger under tænd/sluk (høj dv/dt), der kan opnås med nye mellemspændings SiC MOSFETs, skaber adskillige udfordringer for mellemspændings-spoler og filtre, da det via spolens kapacitive koblinger kan skabe høje jordstrømme i de effektelektroniske systemer. For at undersøge og klarlægge denne udfordring, fokuserer PhD-afhandlingen på udvikling af både fysik-baserede og system dynamiske modelleringsmetoder, for at kunne karakterisere og løse udfordringerne med kapacitive koblinger i mellemspændings-spoler.

Den ækvivalente kapacitive kobling af en spole er frekvensafhængig. Den fysik-baserede modelleringsmetode kan estimere den ækvivalente kapacitive kobling med udgangspunkt i den geometriske struktur og materiale-parametre gældende op til den første resonansfrekvens. En række unøjagtige antagelser om den fysik-baserede model op til første resonansfrekvens adresseres. Dernæst præsenteres en fysik-baseret modelleringsmetode til at udregne den kapacitive kobling i spoler, inklusiv dets effekter ved jording. Metoden bruger et tre-terminals ækvivalentkredsløb til at karakterisere de kapacitive koblinger, i stedet for det konventionelle to-terminals ækvivalentkredsløb for en spole. Herefter præsenteres en modelleringsmetode af den kapacitive kobling, som også tager højde for kant-effekter i de elektriske felter i kobberfolie mellemspændingsspoler.

I tillæg til den fysik-baserede model, kan system-dynamikken af de faktiske koblinger modelleres ved brug af tids- og frekvens-responset af spolen. Modellens nøjagtighed er begrænset af båndbredden af det udstyr der måler tids- eller frekvens-responset. En model af mellemspændings-spolens dynamik præsenteres, udregnet fra den målte frekvensafhængige impedans. Dernæst er den kapacitive kobling mellem spolens terminaler og kerne karakteriseret, ved brug af et stigenetværk af RLC-kredsløb, hvor dets parametre er analytisk udregnet fra det målte impedans-respons. Den udviklede model af spolen benyttes slutteligt, til at opbygge en digital tvilling af en double-pulse-test opstilling, hvor den simulerede strøm i spolens jordforbindelse viser god overensstemmelse med de eksperimentielle målinger.

Herefter præsenteres teknikker til at reducere de kapacitive koblinger i mellemspændings-spoler med flere viklinger. Den fysik-baserede modelleringsmetode indikerer at den kapacitive kobling kan reduceres ved at ændre den geometriske struktur, de elektriske forbindelser og viklings-layout. Med udgangspunkt i analytiske udregninger, og ved brug af de præsenterede teknikker,

fremstilles adskillige prototyper af spoler, hvis kapacitive koblinger er reduceret markant. Men nogle af de fremsatte teknikker sker på bekostning af nedsat effektdensitet af vindingerne eller en forøgelse af fremstillingsomkostningerne.

Til slut er de tilbageværende udfordringer ved modellering af kapacitive koblinger i mellemspændingsspoler opsummeret. Konklusioner og fremtidig forskning er givet sidst i afhandlingen.

Afhandlingen er opbygget på baggrund af en samling af videnskabelige artikler, herunder: fem tidsskrift-bidrag, to konference-artikler og et ansøgt patent indsendt til Patent- og Varemærkestyrelsen i Danmark.

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Hongbo Zhao

TABLE OF CONTENTS

Chapter 1. Introduction..17

1.1 Background and motivation 17

1.2 State of the art 18

1.2.1 Physics-based modeling methods... 18

1.2.2 Behavior-based modeling methods 21

1.2.3 Methods for reducing parasitic capacitance 22

1.3 Reminded challenges 22

1.4 Objectives 23

1.5 Hypothesis and methodology 24

1.6 Thesis outline and contributions 24

1.7 Related publications and patents 26

Chapter 2. Physics-Based Modeling Method 29

2.1 Proper and improper assumptions 29

2.1.1 The original equivalent circuit 29

2.1.2 Contradiction.. 31

2.1.3 Evaluation of model assumptions.. 32

2.1.4 Summary 36

2.2 Physics-based modeling methods with considering ground effects 37

2.2.1 Capacitive couplings in a typical Medium Voltage inductor 37

2.2.2 Static and dynamic capacitance.. 39

2.2.3 Experimental verifications 42

2.2.4 Summary 45

2.3 Physics-based modeling methods with considering electrical fringe field..... 45

2.3.1 An medium-voltage copper-foiled inductor 45

2.3.2 The electrical Fringe field 47

2.3.3 Static and dynamic capacitance contributed by electrical Fringe field ... 48

2.3.4 Experimental verification.. 53

2.3.5 Summary 55

2.4 Physics-based modeling methods without using floating voltage potential ... 55
  2.4.1 Improved physics-based modeling method ... 55
  2.4.2 Experimental verifications ... 58
  2.4.3 Summary ... 59

Chapter 3. Behavior-Based Modeling Method ... 61

3.1 Measurement of common-mode impedance by using double-pulse-test setup ... 61
  3.1.1 Double-pulse-test setup ... 62
  3.1.2 Principle of the impedance measurement ... 63
  3.1.3 Experimental verifications ... 64
  3.1.4 Summary ... 65
3.2 Behavior-based modeling method using transfer functions ... 66
  3.2.1 Basic Principle ... 66
  3.2.2 Simulations and experimental verifications ... 67
  3.2.3 Summary ... 69
3.3 Behavior-based modeling method using equivalent circuit ... 69
  3.3.1 Derivation of the proposed equivalent circuit ... 70
  3.3.2 Digital-twin simulations and experimental verifications ... 73
  3.3.3 Summary ... 76

Chapter 4 Reducing Parasitic Capacitance in MV Inductors ... 77

4.1 Case studies ... 77
  4.1.1 Conventional design ... 77
  4.1.2 Improved design ... 79
  4.1.3 Calculations and verification ... 85
4.2 Design-oriented guidelines ... 87
4.3 Summary ... 88

Chapter 5. Conclusions and Prospects ... 89

5.1 Conclusions ... 89
5.2 Prospects ... 90

Bibliography ... 93

Appended Publications ... 103

TABLE OF FIGURES

Fig. 1-1 3-dimension CAD model of a toroid inductor 19
Fig. 1-2 Simplified equivalent circuit using the lumped-capacitor-network-based method 19
Fig. 1-3 Simplified equivalent circuit using the energy-conservation based method20
Fig. 2-1 Equivalent circuit of a single-layer inductor... 30
Fig. 2-2 Simplified equivalent circuit using the lumped-capacitor-network-based method 30
Fig. 2-3 Simplified equivalent circuit using the energy-conservation-based method 31
Fig. 2-4 Comparison of simulated impedance using LTSpice and calculated impedance using the energy-conservation-based method and lumped-capacitor-network method (N = 10 is used in this case). 33
Fig. 2-5 Simulated voltage potential distribution of Turn 1-10 in LTSpice............. 34
Fig. 2-6 Comparison of the calculated and simulated capacitance of the equivalent circuit with different number of turns 34
Fig. 2-7 Inductor with adjustable number of turns.. 35
Fig. 2-8 Comparison of theoretically calculated capacitance and measured capacitance 36
Fig. 2-9 Schematics for deriving geometrical parameters of the MV inductor. (a) CAD model and capacitive couplings. (b) Cross section A (horizontal cross section) . (c) Cross section B (vertical cross section).. 38
Fig. 2-10 Schematic of the inner layer and core with different configurations. a) Case 1: core is floating; b) Case 2: core is clamped to the hot terminal; c) core is clamped to the cold terminal 40
Fig. 2-11 Derivation of the three-terminal equivalent circuit schematic. (a) is the schematic. (b), (c) and (d) are the representation of three cases with different terminal connections 42
Fig. 2-12 Pictures of the researched MV inductor 43

Fig. 2-13 Schematic of the medium-voltage copper-foiled inductor. (a) Front view. (b) Cross-sectional view 46
Fig. 2-14 Electrical field simulation of the 2-dimension copper-foil inductor......... 48
Fig. 2-15 Identify the capacitive couplings in copper-foiled MV inductors 48
Fig. 2-16 Schematic of a chip and ground in VLSI applications 49
Fig. 2-17 Elementary capacitances contributed by the fringe field. (a) elementary capacitance between the sidewall and core; (b) elementary capacitance between the top-surface and core. 51
Fig. 2-18 Comparison of the static capacitances obtained using the FEM simulation, the empirical equations, and the proposed modeling method 52
Fig. 2-19 Schematic of the copper-foiled inductor with different configurations. a) Case 1: core is floating; b) Case 2: core is clamped to the hot terminal; c) core is clamped to the cold terminal.. 53
Fig. 2-20 Pictures of the manufactured copper-foiled MV filter inductor 54
Fig. 2-21 Schematics for the three configurations of the improved modeling method. a) Configuration 1; b) Configuration 2; c) Configuration 3. 57
Fig. 2-22 Converting the three-terminal equivalent circuit of an inductor into two-terminal equivalent circuit when the core/frame is floating 58
Fig. 3-1 A DPT setup enabled by 10 kV SiC MOSFETs. a) Picture. b) Schematic. 62
Fig. 3-2 Measured voltage and currents from the DPT at 3 kV/12 A 63
Fig. 3-3 Schematic of the DPT setup with inductor represented by a three-terminal equivalent circuit... 64
Fig. 3-4 Measured voltage and ground current in DPT setup with triple pulse and t_w = 120μs.. 65
Fig. 3-5 Comparsion between the calculated impedance using DPT setup and measured impedance using impedance analyzer 65
Fig. 3-6 Equivalent circuit representation of an inductor. (a) Schematic of the inductor with ground connection. (b) General three-terminal equivalent circuit 66
Fig. 3-7 Comparison between the measured and fitted admittance.......................... 67

Fig. 3-8 Comparison between the simulation and experiments using the actual measured voltage as the excitation. a) First turn-off transition. b) Second turn-on transition 68
Fig. 3-9 Comparison between the simulation and experiments using a ramp signal as the excitation. a) First turn-off transition. b) Second turn-on transition.................. 69
Fig. 3-10 The exampled medium-inductor with labeling terminals and ground 70
Fig. 3-11 Measured impedance of the capacitive coupling between Terminal A and Ground in the exampled medium-voltage inductor with selected frequencies......... 70
Fig. 3-12 High-frequency RLC-based equivalent circuit of a medium-voltage inductor 71
Fig. 3-13 A comparison between the fitted impedance by using the derived equivalent circuits and measurement... 73
Fig. 3-14 Image of digital-twin of the double-pulse-test in LTSpice....................... 74
Fig. 3-15 Measured and simulated ground current according to digital-twin simulation in LTSpice. a) during the first turn-off transition. b) during the second turn-on transition. 75
Fig. 3-16 Measured and simulated ground current from the digital-twin simulation in LTSpice using a damping resistance... 75
Fig. 3-17 Measured and simulated ground current from the digital-twin simulation in LTSpice swapping the connections of the medium-voltage inductor 76
Fig. 4-1 Schematic of Case 1 77
Fig. 4-2 Complete schematic of Case 1.. 78
Fig. 4-3 Schematic of Case 2 79
Fig. 4-4 Schematic of Case 3 80
Fig. 4-5 Schematic of Case 4 81
Fig. 4-6 Schematic of Case 5 82
Fig. 4-7 Schematic of Case 6 82
Fig. 4-8 Schematic of Case 7 83
Fig. 4-9 Schematic of Case 8 84
Fig. 4-10 Schematic of Case 9 84
Fig. 4-11 Schematic of Case 10 85

CHAPTER 1. INTRODUCTION

> *"A human is a reed, the weakest thing in nature, but it is a thinking reed."*
> *— Blaise Pascal*

1.1 BACKGROUND AND MOTIVATION

In the past few years, researchers and engineers have witnessed the exponential growth of applying wide-band-gap (WBG) devices in power electronics converters. The WBG semiconductor material of devices can enable the converters to operate at the higher switching frequency, higher blocking voltage, higher ambient temperature, and less switching losses [1]-[8]. As one of the novel wide-band-gap devices, the 10 kV SiC MOSFETs show promising features, e.g. simpler topology of converters in high voltage applications, reduced complexities of system, and higher efficiency [9]-[13], and show potentials in applying in power generation system [14], power distribution system [15], data centers [16], railway applications [17], and etc.

However, the fast switching speed with high dv/dt value of medium-voltage SiC MOSFETs (up to 250 V/ns [18]) poses several challenges to the components in the system [19]. The parasitic capacitive couplings of power components can introduce large capacitive current under the high dv/dt switching transition, e.g. the common-mode current in gate drivers [20], the ground current in heatsink [21], the capacitive current in power modules [22], transformers and inductors [23]-[26]. Especially for medium-voltage inductors, it is reported that the value of parasitic capacitance is usually larger due to the high inductance value and extra insulation compared to low-voltage inductors [25]. The capacitive current contributed by the parasitic capacitive couplings in medium-voltage inductors will circulate in the power converter, which can cause electro-magnetic interference issues [27], and extra losses on transistors as well as degradation of the transistors [28]. The parasitic capacitance of medium-voltage inductors can limit the expected performance of the medium-voltage SiC MOSFETs.

In order to research the parasitic capacitance of inductors (or transformers), both physics-based and behavior-based modeling methods have been reported in previous research. The physics-based modeling method can be used to obtain the equivalent parasitic capacitance of inductors using the geometrical and material parameters [23],

[29]-[31]. Therefore, the physics-based modeling method can predict the value of the parasitic capacitance prior to manufacturing [32], which provides possibilities reiterate the design of inductors for reducing the parasitic capacitance during the design process. The behavior-based modeling method is usually derived by using the measured frequency-domain or time-domain response of long cables [33]-[36], but further extended to characterize the inductors [37]-[39]. The behavior-based modeling method cannot predict the performance of inductors before manufacturing, but it can simulate the actual response of inductors with circuit simulation tools [40].

The motivations of this PhD thesis are listed as below:

Firstly, there is a typical difference between medium voltage and low voltage applications. In medium-voltage applications, the core and frame of magnetics are required to be grounded due to the safety considerations [41], while in low-voltage applications, the frame and core can be floated if sufficient insulation is applied. When, the core and frame of the inductor is grounded in introduces the third terminal to the system. Therefore, it is not clear that if the previous modeling methods are still applicable in the inductors when their core and frame are grounded.

Secondly, the digital twin of the converter is desired for investigating the system-level performance. The behavior-based models of inductors can be integrated with the behavior-based models of other power components, and the digital twin of the system can be built in circuit simulators. The digital twin simulations can significantly reduce the lab work and accelerate the design and development phase.

Lastly, the methods for reducing the parasitic capacitance in medium-voltage inductors are gaining attention. Although some methods for reducing the parasitic capacitance of inductors have been reported in low-voltage low-power inductors, it is still questionable if the conventional methods are scalable and applicable in the case of medium-voltage inductors.

1.2 STATE OF THE ART

The modeling of capacitive couplings in inductors has been studied in the following three aspects: a) how to develop the physics-based models for inductors; b) how to develop the behavior-based models for inductors; c) how to reduce the capacitive couplings in inductors.

1.2.1 PHYSICS-BASED MODELING METHODS

The physics-based modeling methods of parasitic capacitance in inductors have been researched for almost half a century. The parasitic capacitance of inductors can be modeled by using the finite-element-method (FEM) [42]-[46], which should be accurate with precise geometrical and material parameters and proper configurations and clear definitions of the physics. However, the FEM-based simulations cannot provide the explicit expression of parasitic capacitance, and the factors influencing the magnitude of the parasitic capacitance are difficult to be identified.

In order to obtain the explicit expressions of parasitic capacitance, two modeling methods: a) lumped-capacitor-network-based method [31], [47]-[49] and b) energy-conservation-based method [23], [29], [52]-[58], are derived in previous research. Both methods can be regarded as a simplification of the FEM-based methods, where more assumptions are applied to reduce the complexity and computation of the physics-based models.

1.2.1.1 LUMPED-CAPACITOR-NETWORK-BASED METHOD

A single-layer inductor with a ferrite core is taken as an example in this section. Fig. 1-1 shows the 3-dimension CAD model of the inductor.

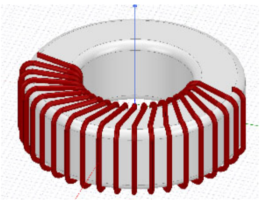


Fig. 1-1 3-dimension CAD model of a toroid inductor

Accurately, there are infinite elementary capacitive couplings within the inductor. By using FEM analysis, the infinite elementary capacitive couplings are simplified into finite couplings based on the mesh theory, and acceptable errors are introduced. In the lumped-capacitor-network method, the capacitive couplings within the inductor are further reduced [31], [47]-[49]. The simplified equivalent circuit of the illustrated single-layer inductor using this method is shown in Fig. 1-2. The capacitive couplings between non-adjacent turns are not considered since these couplings have limited impacts in most situations.

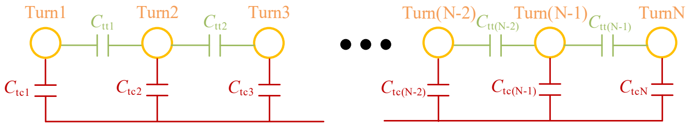


Fig. 1-2 Simplified equivalent circuit using the lumped-capacitor-network-based method

In the lumped-capacitor-network method, the capacitive coupling between two neighbor turns is simplified as a single capacitor C_{tt}(N), the capacitive coupling between turn and core is simplified as a single capacitor C_{tc}(N), where the equivalent inductance and resistance of each turn is neglected. C_{tt}(N) and C_{tc}(N) can be derived using the geometrical and material parameters. Thus, the complex capacitive couplings of the illustrated inductor are simplified into a pure capacitor network, where the total equivalent capacitance can be calculated and explicitly solved using delta-star transformation [31], [47]-[49]. However, this method is limited in inductors with simple geometrical structures, e.g., single-layer inductor or air-coiled inductor. For inductors or transformers with more complex structure, e.g., multi-layer inductor or transformers, the equivalent capacitance can be solved by Spice simulators according to the equivalent circuit representation [50]. The core and frame of inductors are assumed to be floating in lumped-capacitor-network modeling methods [31], [47]-[49], whose applications are limited to two-terminal components.

1.2.1.2 ENERGY-CONSERVATION-BASED METHOD

Taking a single-layer inductor as an example, the energy-conservation-based method is also started with an equivalent circuit representation of the single-layer inductor, as shown in Fig. 1-3.

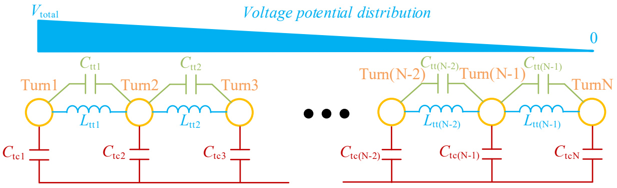


Fig. 1-3 Simplified equivalent circuit using the energy-conservation based method

The energy-conservation-based method tries to solve the equivalent capacitance of the circuit by calculating the total energy stored in the electrical field [23] [29], [51]-[57]. It assumes that the voltage potential is linearly distributed in the winding [58], [59], and is contributed by the elementary inductance L_{tt} between two turns. Therefore, the equivalent capacitance calculated by this method is only valid before the first resonant frequency [29]. Since C_{tt}(N) and C_{tc}(N) are known according to the geometrical and material parameters, the equivalent capacitance of the simplified circuit at the first resonant frequency can be explicitly solved.

The energy-conservation-based modeling method has been applied in inductors or transformers with complex structures [52]-[59], which means this method can be applied into multi-terminal components, e.g., four-terminal transformers [23], [59],

[60]. The six individual capacitances of a four-terminal transformer are analytically calculated using the method based on energy-conservation [60].

In high frequency applications, the skin-effects and proximity effects on the parasitic capacitance in inductors are considered using energy-conservation-based method [61]. For high-voltage and high-power applications, the core and frame are grounded [62], according to safety considerations and standards[41]. In [60], the parasitic capacitances of a transformer with grounded core/frame are calculated. However, one terminal of the transformer is assumed to be grounded with core/frame during the modeling process [60], where the equivalent capacitance between terminals and core/frame cannot be characterized.

1.2.2 BEHAVIOR-BASED MODELING METHODS

According to the introduction in previous sections, the physics-based modeling methods can only predict a single equivalent capacitor (lumped-capacitor-network-based method) or the equivalent capacitor at the first resonant frequency (energy-conservation-based method).

In practice, there are multiple resonances and anti-resonances according to the measured impedance of inductors and transformers [63], which means the capacitance predicted by physics-based modeling methods cannot reveal the complete behaviors of inductors and transformers at the wide frequency range. Besides, the actual behaviors of inductors and transformers are ruled by not only parasitic capacitance but also resistance and inductance at each frequency.

The behavioral model represented by transfer functions are widely used in the modeling of the long cable [33]-[35], where the time-domain or frequency-domain response of the cable is measured first. The behavioral model can also be represented by a circuit, which is more intuitive in comparison to its presentation transfer functions in Spice-based simulators [64]. In [65]-[67], the behavioral models represented by equivalent circuits of chokes are imported into Spice-based simulators, where the common-mode and differential-mode current are simulated. The common-mode and differential-mode impedance of chokes are inductive before the first resonant frequency, where the impedance keeps increasing with the increase of frequency [37], [38]. In [40], the impedance of a common-mode choke is measured first, and a multi-stage RLC circuit is proposed for fitting the measured impedance. The parameters of the multi-stage RLC circuit can be analytically calculated by identifying the frequency and magnitude of resonances and anti-resonances [40]. [37]- [40] introduce a scalable solution for behaviorally modeling the impedance with inductive characteristics before the first resonant frequency.

The behavior-based model can be integrated into the circuit simulator with the behavior-based models of other power components, where a digital-twin of the circuit is possible to be implemented for system-level simulations. However, such behavior-based models are dependent on the electrical measurements on the actual components, which requires to manufacture the prototype before modeling.

1.2.3 METHODS FOR REDUCING PARASITIC CAPACITANCE

The inductors with a low value of the parasitic capacitance can reduce the capacitive current within the circuit. The equivalent parasitic capacitance and thereby the capacitive current of the inductor can be reduced by paralleling another inductor with a smaller parasitic capacitance[68], however, it requires extra components and can cause more losses due to the use of damping resistance. Therefore, it is desired to reduce the parasitic capacitance of inductors by improving their designs.

Using a larger distance to weaken the couplings between two adjacent planes is one of the solutions. In [69], spacers are used between two adjacent layers to reduce the parasitic capacitance contributed by the electrical-field energy stored between them. The parasitic capacitance can also be reduced using applying different winding patterns [29], e.g., by changing the original winding layout to flyback winding layout [70]. These methods are developed at the cost of sacrificing the power density of the inductor and increased manufacturing complexity.

1.3 REMINDED CHALLENGES

The previous research mainly focuses on low-power and low-voltage inductors, where the core and frame of inductors are usually floating in these applications. Therefore, the previous modeling methods assume that the inductor is a two-terminal component [71], where there is only one capacitive coupling that needs to be characterized.

However, in high-power or medium-voltage applications, the core and frame of magnetic devices are required to be grounded since the high floating voltage potential can cause safety hazards. Although the ground effects are considered in modeling parasitic capacitance of transformers [60], where the core and frame have the same ground potential as one of the four terminals of transformers, however the equivalent capacitance between terminals and core/frame are not revealed.

Therefore, the medium-voltage inductors should be characterized as the three-terminal passive components instead of the conventional two-terminal components, where the core/frame need to be considered as an individual terminal. Thus, the equivalent capacitance between two terminals of inductors, as well as the equivalent capacitance between terminal and core is possible to be characterized. Therefore, the first research gap is to develop a physics-based modeling method for characterizing the three parasitic capacitances in inductors considering the core and frame as a separation terminal.

Then, most research analyzes the parasitic capacitance constructed by round-cable and litz wire. However, for high-power applications, the inductors based on copper-foils are more popular due to the low cost and high scalability. Thus, the second gap is to verify whether the physics-based modeling methods developed for inductors with round cables are still valid for copper-foiled inductors.

Besides, the conventional behavior-based modeling method focuses on characterizing the inductive impedance, where the magnitude of impedance keeps increasing with increased frequency before the first resonance. However, according to the experimental measurements, the impedance between the terminal and core(frame) is capacitive, where the impedance drops with increasing the frequency. Therefore, the traditional behavioral modeling methods cannot be directly applied in characterizing the capacitive couplings between terminal and core(frame). Thus, the third research gap is to develop a behavior-based modeling method for characterizing the capacitive impedance.

Finally, the proposed methodologies/approaches to reduce the parasitic capacitance in previous research are only reported in the situations where the core and frame of inductors are floating. Therefore, only the equivalent capacitance between the two terminals of inductors needs to be reduced in previous research. However, this is not sufficient for the inductors with grounded core and frame, since the other two capacitive couplings between each terminal and core needs to consider. Besides, the medium-voltage inductors usually have multiple windings, and the methodologies for reducing inductors with multiple windings are not discussed in previous research. Thus, the fourth research gap is to develop methodologies/approaches of reducing parasitic capacitance in medium-voltage inductors with grounded core and frame.

1.4 OBJECTIVES

Considering the research gaps and unsolved challenges in the modeling and methods of reducing the parasitic capacitance in medium-voltage inductors, this Ph.D. thesis focus on the following specific objectives:

- To develop physics-based modeling methods that can be applied to the inductors with grounded core and frame.
- To develop behavior-based modeling methods that can characterize the capacitive impedance in inductors.
- To propose approaches for reducing parasitic capacitance in medium-voltage inductors with multiple windings and grounded core and frame.

1.5 HYPOTHESIS AND METHODOLOGY

This Ph.D. thesis deals with the modeling methods and approaches for reducing parasitic capacitance in medium-voltage inductors, which is based on the following hypothesis:

- The medium-voltage inductors can be modeled by both physics-based and behavior-based modeling methods. The capacitive couplings between the terminal and core (and frame) can be individually characterized.
- The behavior-based modeling method can develop a circuit-based solution for importing the derived model into circuit simulations.
- By analyzing the developed physics-based and behavior-based model of medium-voltage inductors, several approaches can be proposed for reducing the parasitic capacitance of medium-voltage inductors with multiple windings and grounded core/frame.

Based on the above assumptions, the following methods will be adopted in this thesis:

- The medium-voltage inductors are modeled by an equivalent circuit with finite elementary capacitors and inductors.
- The geometry theory, charge-conservation theory, energy-conservation theory, and multi-terminal circuit theory is applied in calculating the equivalent capacitance between any two terminals of the medium voltage inductors.
- Advanced mathematics is applied to develop the derived models.
- Matlab is used in solving the derived models.
- The FEM simulation, ANSYS, and COMSOL, are used in order to verify the derived models.
- Some prototypes of medium-voltage inductors are designed and manufactured, where the derived model can be experimentally verified by impedance analyzer and double-pulse-test.

1.6 THESIS OUTLINE AND CONTRIBUTIONS

This Ph.D. thesis is divided into five chapters. The main chapters are related to seven publications [J1]-[J5], [C1]-[C2] and one filed patent [P1].

Chapter 1 is the introduction.

Chapter 2 develops the physics-based modeling method for medium-voltage inductors. Chapter 2 is further divided into four subsections:

- Section 2.1 [J1]: *Proper and Improper assumptions in modeling parasitic capacitance of inductors*
  The proper and improper assumptions for physically modeling the parasitic capacitance in inductors are classified, where the assumptions used in the lumped-capacitor-network method is the improper assumption for modeling the equivalent capacitance at the first resonant frequency. The assumption of linear voltage potential distribution is proper in the energy-conservation-based modeling method, although this assumption can introduce some acceptable errors.
- Section 2.2 [J2]: *Physics-based modeling method for medium-voltage inductors with considering the ground effects*
  This subsection extends the conventional physics-based modeling method of parasitic capacitance for two-terminal inductors (core and frame are floating) to three-terminal inductors (core and frame are grounded), where the three individual capacitance between any two terminals of the three-terminal inductor can be analytically calculated.
- Section 2.3 [J3]: *Physics-based modeling method for copper-foiled medium-voltage inductors with considering fringe electrical field*
  It is found that the energy stored in electrical fringe field is significant for copper-foiled medium-voltage inductors. Thus, the parasitic capacitance contributed by the stored energy in the fringe electrical field of the windings is considered and modeled.
- Section 2.4 [J4]: *Improved physics-based modeling method without using the floating core voltage potential*
  The previous modeling methods require knowing the floating core voltage potential as model input for calculating the parasitic capacitance of inductors with floating or grounding cores. In this section, an improved modeling method is proposed without using the floating core voltage potential. The modeling method can also be extended for the transformers.

Chapter 3 develops the behavior-based modeling method for medium-voltage inductors. Chapter 3 is further divided into three subsections:

- Section 3.1[C1]: *Measurements of the capacitive impedance in medium-voltage inductor with using double-pulse-test setup*
  The impedance of the capacitive couplings in medium-voltage inductors is measured using a double-pulse-test setup, which enables the measurement of the impedance under high-voltage and high-current operating conditions. It is found that the impedance of the capacitive couplings is current- and voltage-independent.
- Section 3.2 [C2]: *Behavior-based modeling methods of the capacitive impedance in medium-voltage inductors with using transfer functions.*
  The capacitive coupling in medium-voltage inductors is measured using the impedance analyzer. Then the measured impedance is fitted by a transfer

function using Matlab system identification toolbox. The time-domain simulations of the transfer function-based behavioral model show good agreement with the experimental results.

- Section 3.3 [J5]: *Behavioral Modeling and Analysis of Ground Current in Medium-Voltage Inductors*
  The measured impedance of the capacitive couplings in medium-voltage inductors is fitted by using a multi-stage RLC circuit, whose parameters can be analytically calculated according to the measured impedance. The derived RLC circuit is imported into LTSpice, where a digital twin of the double-pulse-test is simulated. The digital twin simulations of the ground current in the medium-voltage inductor show good agreement with the experimental results.

Chapter 4 introduces the approaches for reducing parasitic capacitance for medium-voltage inductors. The multiple winding arrangements, winding layout, and geometrical improvements are discussed in this chapter, where multiple solutions and case studies are presented. This chapter is supported by [P1].

Chapter 5 discusses the conclusions and future work of this thesis.

1.7 RELATED PUBLICATIONS AND PATENTS

The publications related to this Ph.D. thesis are listed as follows:

Journal Publications:

[J1] Hongbo Zhao et al., “Proper and Improper Assumptions in Modeling Parasitic Capacitance of Inductors,” ***IEEE Transactions on Power Electronics***, submitted.

[J2] Hongbo Zhao et al., “Physics-based Modeling of Parasitic Capacitance in Medium-Voltage Filter Inductors,” ***IEEE Transactions on Power Electronics***, vol. 36, no. 1, pp. 829 – 843, Jan. 2021.

[J3] Hongbo Zhao et al., “Parasitic Capacitance Modeling of Copper-Foiled Medium-Voltage Filter Inductors Considering Fringe Electrical Field,” ***IEEE Transactions on Power Electronics***, vol. 36, no. 7, pp. 8181 – 8192, Jul. 2021.

[J4] Hongbo Zhao et al., “Parasitic Capacitance Modeling of Inductors Without Using the Floating Voltage Potential of Core,” ***IEEE Transactions on Industrial Electronics***, doi: 10.1109/TIE.2021.3068677, early access.

[J5] Hongbo Zhao et al., “Behavioral Modeling and Analysis of Ground Current in Medium-Voltage Inductors,” ***IEEE Transactions on Power Electronics***, vol. 36, no. 2, pp. 1236 – 1241, Feb. 2021.

Conference Publications:

[C1] Hongbo Zhao et.al., “Terminal-to-Core Impedance measurements of the Filter Inductors by Using Double-Pulse-Test”, *in Proc.* ***2020 IEEE Workshop on Control and Modeling for Power Electronics***, pp. 1-6, 2020.

[C2] Hongbo Zhao et.al., “Behavioral Modeling of the Ground Current in Filter Inductors for MV SiC-MOSFET-Based Converters”, *in Proc.* ***2020 IEEE Applied Power Electronics Conference (APEC)***, pp. 1972-1978, 2020.

Patent:

[P1] Hongbo Zhao et al., “Reducing Parasitic Capacitance in Medium-Voltage Inductors, ***filed in Danish Patent and Trademark Office***, 75792DK01, 2021-03-23.

CHAPTER 2. PHYSICS-BASED MODELING METHOD

> *"Thoughts without content are empty, intuitions without concepts are blind.*
> *— Immanuel Kant*

This chapter develops the physics-based modeling method for analytically deriving the individual parasitic capacitances in medium-voltage inductors. First, the proper and improper assumptions used in previous research are clarified and verified in Section 2.1. Then, the developed modeling method considering the ground effects is introduced in Section 2.2. The proposed modeling method for copper-foiled inductors considering the electrical fringe field effects is introduced in Section 2.3. Finally, an improved physics-based modeling method without using the floating core voltage potential is introduced in Section 2.4.

2.1 PROPER AND IMPROPER ASSUMPTIONS

Two different modeling methods, the lumped-capacitor-network method, and energy-conservation-based method are reported in previous research for solving the equivalent capacitance of inductors at the first resonant frequency. However, these two methods show a significant contradiction in the conclusions. Therefore, the proper and improper assumptions applied in these two methods are classified in this section.

2.1.1 THE ORIGINAL EQUIVALENT CIRCUIT

The single-layer inductor can be expressed as the equivalent circuit is shown in Fig. 2-1, using the following assumptions.

- Each turn is simplified to a 2D element in Fig. 2. 1. The capacitive coupling between two adjacent turns is simplified as a single capacitor C_{tt} [72]. The capacitive couplings between each turn and core are simplified as the single capacitor C_{tc} [72].

- Between two adjacent turns, there is an elementary inductor L_{tt} [50], [72]. The capacitive couplings between non-adjacent turns are neglected [73]. Losses are also neglected.
- The core is assumed as a perfect conductor [58], as is commonly done. Even high-resistivity cores often have relatively high permittivity [20], [74], which has a similar effect when modeling electric field distributions.

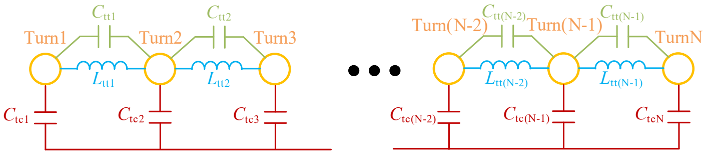

Turn1
Turn2
Turn3
Turn(N-2)
Turn(N-1)
TurnN
C_{tt1}
C_{tt2}
$C_{tt(N-2)}$
$C_{tt(N-1)}$
L_{tt1}
L_{tt2}
$L_{tt(N-2)}$
$L_{tt(N-1)}$
C_{tc1}
C_{tc2}
C_{tc3}
$C_{tc(N-2)}$
$C_{tc(N-1)}$
C_{tcN}

Fig. 2-1 Equivalent circuit of a single-layer inductor

The lumped-capacitor-network modeling method and energy-conservation-based method are original from the equivalent circuit representation of the exampled inductor shown in Fig. 2-1. The lumped circuit assumes that the turn-to-turn inductance L_{tt} can be assumed as open since the frequency at the first resonant frequency is high enough. Therefore, the equivalent circuit shown in Fig. 2-1 can be simplified as Fig. 2-2, where L_{tt} is neglected. Therefore, in the lumped-capacitor-network method, the equivalent capacitance of the pure capacitor-network can be solved by using delta-star circuit transformation according to [72].

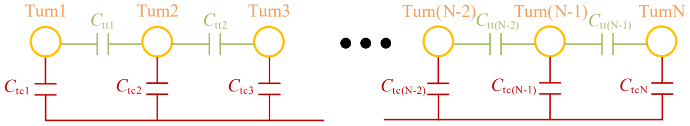

Turn1
Turn2
Turn3
Turn(N-2)
Turn(N-1)
TurnN
C_{tt1}
C_{tt2}
$C_{tt(N-2)}$
$C_{tt(N-1)}$
C_{tc1}
C_{tc2}
C_{tc3}
$C_{tc(N-2)}$
$C_{tc(N-1)}$
C_{tcN}

Fig. 2-2 Simplified equivalent circuit using the lumped-capacitor-network-based method

Although L_{tt} is not considered directly in the energy-conservation-based modeling method, the voltage potential distribution introduced by L_{tt} is considered, which is shown as Fig. 2-3. The voltage potential is assumed to be linearly distributed at the first resonant frequency, where the equivalent capacitance of the equivalent circuit can be obtained by calculating the total stored electrical-field energy.

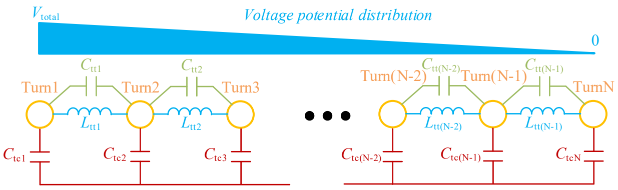

V_{total}
Voltage potential distribution
0
C_{tt1}
C_{tt2}
$C_{\text{tt(N-2)}}$
$C_{\text{tt(N-1)}}$
Turn1
Turn2
Turn3
Turn(N-2)
Turn(N-1)
TurnN
L_{tt1}
L_{tt2}
$L_{\text{tt(N-2)}}$
$L_{\text{tt(N-1)}}$
C_{tc1}
C_{tc2}
C_{tc3}
$C_{\text{tc(N-2)}}$
$C_{\text{tc(N-1)}}$
C_{tcN}

Fig. 2-3 Simplified equivalent circuit using the energy-conservation-based method

2.1.2 CONTRADICTION

By using the lumped-capacitor-network method [72], the total equivalent capacitance $C_{\text{total}}(\text{N})$ of the inductor with a different number N of turns can be calculated [47], which is given in eq. (2.1).

$$\begin{aligned} C_{\text{total}}(2) &= C_{\text{tt}} + \frac{C_{\text{tc}}}{2} \\ C_{\text{total}}(3) &= \frac{C_{\text{tt}}}{2} + \frac{C_{\text{tc}}}{2} \\ C_{\text{total}}(\text{N}) &= \frac{C_{\text{total}}(\text{N - 2}) \times \frac{C_{\text{tt}}}{2}}{C_{\text{total}}(\text{N - 2}) + \frac{C_{\text{tt}}}{2}} + \frac{C_{\text{tc}}}{2}, \quad \text{if N} > 3 \end{aligned} \tag{2.1}$$

If N > 3, $C_{\text{total}}(\text{N})$ is an iterative sequence. According to [47], $C_{\text{total}}(\text{N})$ is convergent when N is large enough, which is given as the equation presented eq. (2.2).

$$C_{\text{total}}(\infty) = \frac{C_{\text{tt}}}{4}(\alpha + \sqrt{\alpha^2 + 4\alpha}), \ \alpha = \frac{C_{\text{tc}}}{C_{\text{tt}}} \tag{2.2}$$

For example, if α = 2, the total capacitance between Turn1 and Turn N is convergent to 1.366 C_{tt} when N is larger than 10.

However, using the energy-conservation-based method, the total equivalent capacitance at the first resonant frequency of the circuit shown in Fig. 2. 3 is presented in eq. (2.3).

$$C_{\text{total}}(\text{N}) = \sum_{n=1}^{\text{N}} \left(\frac{(\text{N} - \text{n})V_{\text{total}}}{\text{N} - 1} - \frac{V_{\text{total}}}{2}\right)^2 \frac{C_{\text{tc}}}{V_{\text{total}}^2} + \sum_{n=1}^{\text{N-1}} \left(\frac{V_{\text{total}}}{\text{N} - 1}\right)^2 \frac{C_{\text{tt}}}{V_{\text{total}}^2} \tag{2.3}$$

Due to the discrete voltage potential distribution in Fig. 2. 3, the total equivalent capacitance is represented by a sum sequence. If the number of turns is large enough, the total equivalent capacitance can be approximated as an integral, and then the total capacitance can be represented as eq. (2.4).

$$\begin{aligned} C_{\mathrm{total}}(\mathrm{N}) &= \frac{\mathrm{N}C_{\mathrm{tc}}}{12} + \frac{C_{\mathrm{tt}}}{\mathrm{N}-1} \\ C_{\mathrm{total}}(\infty) &= \infty \end{aligned} \tag{2.4}$$

Although both methods are aiming to model the total equivalent capacitance at the first resonant frequency, the results and conclusions in (2.2) and (2.4) are quite different. The lumped-capacitor-network method claims that C_{total}(N) will be convergent when N is infinite, where the energy-conservation-based methods claims that C_{total}(N) is infinite when N is infinite. Therefore, these two methods have a contradiction in the final results, and one or both methods is improper in calculating the total equivalent capacitance at the first resonant frequency of inductors.

2.1.3 EVALUATION OF MODEL ASSUMPTIONS

Since both the lumped-capacitor-network method and the energy-conservation-based method originate from the same equivalent circuit, as the circuit shown in Fig. 2-1 is used as the reference circuit for evaluating the model assumptions.

There is a significant difference between the two modeling methods. In the lumped-capacitor-network method, it assumes that the first resonant frequency is high enough that the elementary inductance between adjacent turns is neglected, where the impacts raised by inductance are completely not considered. However, the energy-conservation-based method assumes the linear voltage distribution within the winding, where the voltage distribution is caused by the elementary inductance between adjacent turns. This section will prove that the lumped-capacitor-network-based method has used the improper assumption due to the overlook of impacts raised by turn-to-turn inductance at the first resonant frequency.

The two different modeling methods are compared in LTSpice, where L_{tt} = 1 mH, C_{tt} = 5 pF, C_{tc} = 10 pF, N = 10. The impedance of the equivalent circuit with calculated capacitance at the first resonant frequency is compared with the measured impedance of the original circuit in LTSpice. The calculated capacitance using the lumped-capacitor-network method is 6.9 pF at the first resonant frequency, where the calculated capacitance using the energy-conservation-based method is 10.8 pF at the first resonant frequency. The measured impedance of the original circuit in LTSpice can be fitted with L_{total} = 9 mH and C_{total} = 11.9 pF. Therefore, the calculated capacitance using the lumped-capacitor-network method has a larger error.

In further, the impedances calculated by the lumped-capacitor-network method and energy-conservation-based method are compared with the measured impedance of the original circuit. It can be found that the lumped-capacitor-network-based method actually calculates the total equivalent capacitance after the last resonant frequency. At the first resonant frequency, the turn-to-turn inductance of the original equivalent circuit still has some impacts. Therefore, the turn-to-turn inductance cannot be neglected at the first resonant frequency of inductors.

The voltage potential at Turn 1 ~ N of the original circuit is simulated in LTSpice, which is given in Fig. 2-5. The voltage potential distribution is not absolutely linear at the first resonant frequency, which is however, can introduce some errors to the calculated capacitance at the first resonant frequency compared to the original circuit. Since the variation of voltage potential distribution is relatively small, the assumption claimed by the energy-conservation-based method is more reasonable compared to the assumption claimed by the lumped-capacitor-network method.

The calculated and simulated capacitance are also compared under a different number of turns, which is shown in Fig. 2-6. The calculated capacitance using lumped-capacitor-network method at the first resonant frequency is constant with the increase of turns, where the measured capacitance at the first resonant frequency of the original circuit keeps increasing. Due to the non-linear voltage distribution at the first resonant frequency, there are some errors between the calculated capacitance using the energy-conservation-based method and the measured capacitance of LTSpice, however, the energy-conservation-based method is much more accurate compared to the calculated capacitance using the lumped-capacitor-network method.

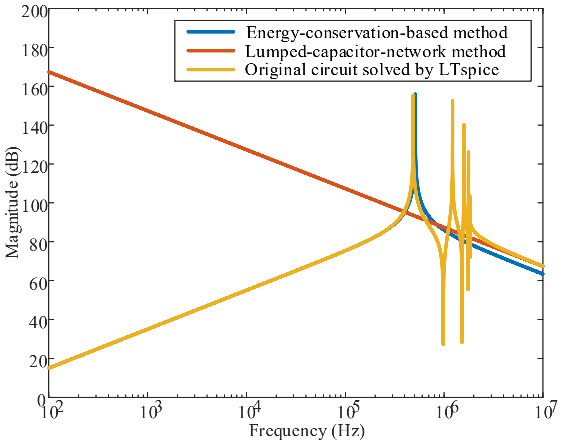


Fig. 2-4 Comparison of simulated impedance using LTSpice and calculated impedance using the energy-conservation-based method and lumped-capacitor-network method (N = 10 is used in this case).

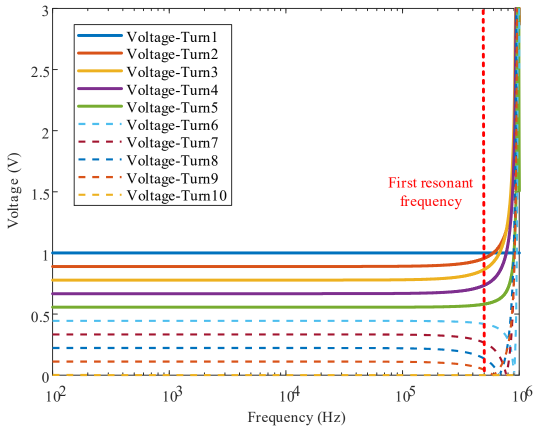


Fig. 2-5 Simulated voltage potential distribution of Turn 1-10 in LTSpice.

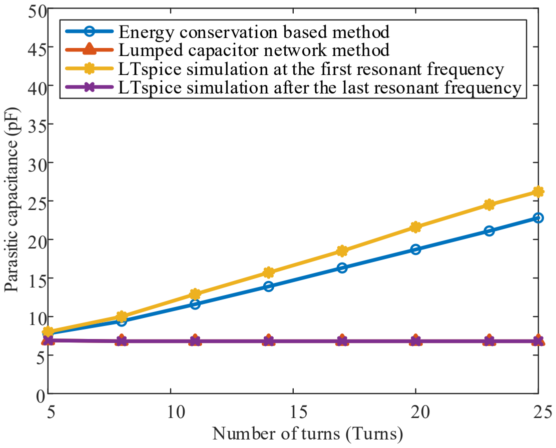


Fig. 2-6 Comparison of the calculated and simulated capacitance of the equivalent circuit with different number of turns

The theoretical analysis is also verified by experimental results. An inductor with a different number of turns is taken as an example, where Fig. 2-7 is the picture of the test inductor and Table 2-I lists its geometrical and material parameters.

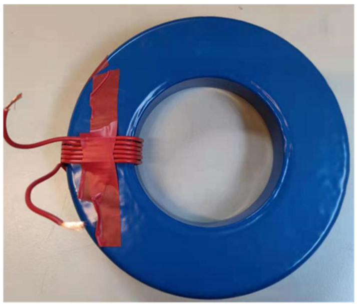


Fig. 2-7 Inductor with adjustable number of turns

The impedance of the test inductor is measured using Keysight E4990 impedance analyzer [75] and its adapter 16047E [76]. By using the geometrical and material parameters, the calculated capacitance of the test inductor at the first resonant frequency using lumped-capacitor-network method and energy-conservation-based method are calculated, and the measured capacitances of the test inductor at the first resonant frequency using impedance analyzer are compared in Fig. 2-8.

In Fig. 2-8, the measured capacitance of test inductors at the first resonant frequency keeps increasing when the number of turns is increased, which means the lumped-capacitor-network method fails to predict the equivalent capacitance of inductors at the first resonant frequency. The energy-conservation-based method predicts the capacitance with an error that is still within the tolerance of geometrical and material parameters as well as the nonlinear voltage distribution at the first resonant frequency of inductors.

Table 2-I Geometrical and material parameters of the test inductor

Core size (Outer diameter/Inner diameter/Height)	75mm/40mm/25mm
Core material	MnZn
Mean length of per turn	120 mm
Number of turns	6-25
Average distance of the airgap between the winding and core	1.75 mm
Average distance of the airgap between two adjacent turns	0.2 mm
Diameter of conductor	0.5mm
Thickness of the insulation	0.6mm
Relative permittivity of the turn coating (PVC [77])	3.1

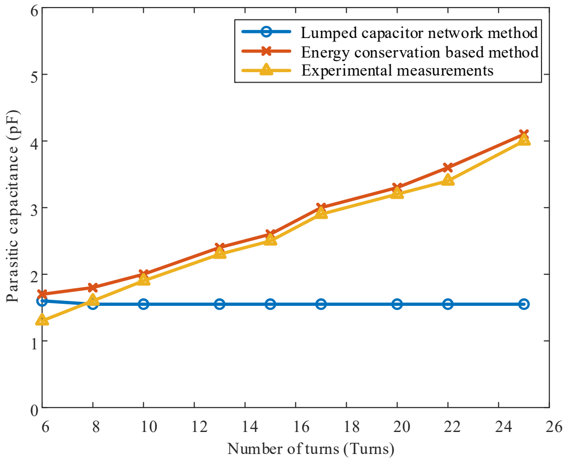


Fig. 2-8 Comparison of theoretically calculated capacitance and measured capacitance

2.1.4 SUMMARY

This section is supported by [J1]. Two widely used modeling methods for characterizing the equivalent capacitance of inductors at the first resonant frequency are classified:

- The lumped-capacitor-network method assumes that only capacitive impedance is significant. This method predicts the capacitance at a very high frequency, and therefore, is improper to predict the equivalent capacitance at the first resonant frequency.
- The energy-conservation-based method assumes that the voltage distribution between turns is uniform and is shown to be more proper for analytically calculating the parasitic capacitance at the first resonant frequency. However, the voltage potential distribution of winding is shown to be non-uniform at the first resonant frequency according to the LTSpice simulations of the equivalent circuit, though by a relatively small amount, which can introduce errors in predictions.

The two modeling methods are compared by experiments. The lumped-capacitor approach is confirmed to be inappropriate, while the errors of the energy-conservation method are found to be within acceptable tolerance in one example.

2.2 PHYSICS-BASED MODELING METHODS WITH CONSIDERING GROUND EFFECTS

The conventional physics-based modeling methods of parasitic capacitance in inductors usually assume that the inductor is a two-terminal component where the core is floating. However, in medium-voltage and high-power applications, the core and frame of magnetic devices are required to be grounded due to safety considerations. Therefore, three individual capacitances between any two terminals of the three-terminal component need to be characterized, respectively.

2.2.1 CAPACITIVE COUPLINGS IN A TYPICAL MEDIUM VOLTAGE INDUCTOR

A typical medium-voltage inductor is used as an example in this paper, where the 3-dimension CAD model is shown in Fig. 2-9 (a). The medium-voltage inductor is designed for a five kHz two-level voltage source converter enabled by 10 kV SiC MOSFETs. The medium-voltage inductor is constructed by two U-type amorphous cores[78], with a 2 mm air gap in between. The geometrical structure of the windings is illustrated in Fig. 2-9 (b) and (c). The geometrical and material parameters are listed in Table 2-II and Table 2-III.

Table 2-II. Key parameters of the MV inductor

Description	Symbol	Value
Diameter of the cable	d_0	1.4 mm
Length of the air gap between the bobbin and core	p_1	0.75 mm
Thickness of the bobbins between the inner layer and core	d_1	2 mm
Length of the air gap between two adjacent layers	p_2	5.7 mm
Average length of the air gap between two turns in the same layer	p_3	0.45 mm
Height of the windings	h	11.9 cm
Width of the spacers between two adjacent layers	w_b	4.8 mm
Length of the outer layer per turn	l_1	24.7 cm
Length of the middle layer per turn	l_2	22.2 cm
Length of the inner layer per turn	l_3	19.7 cm
Average length of per turn for three layers	l	22.2 cm
Average length of the air gap between the two windings	p_4	3 mm
Number of turns of per layers	n	63

Number of layers	m	3
Number of the winding	w	2
Total inductance	L	30 mH

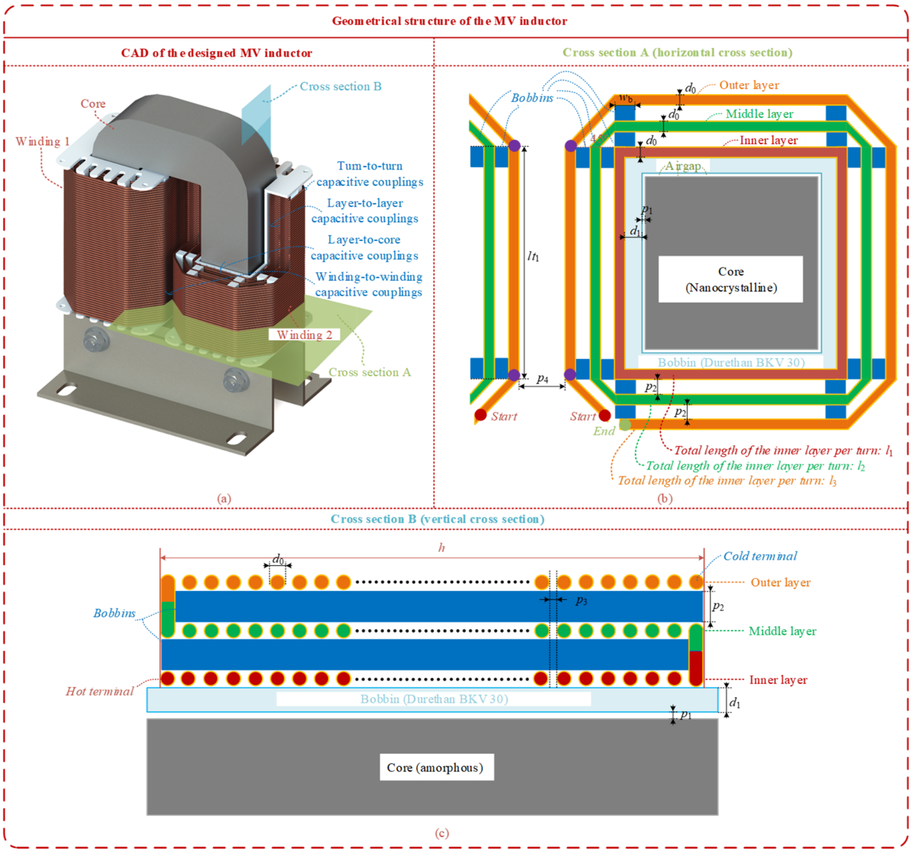

Geometrical structure of the MV inductor
CAD of the designed MV inductor
Cross section A (horizontal cross section)
Core
Winding 1
Cross section B
Turn-to-turn capacitive couplings
Layer-to-layer capacitive couplings
Layer-to-core capacitive couplings
Winding-to-winding capacitive couplings
Winding 2
Cross section A
(a)
Bobbins
w_b
d_0
Outer layer
Middle layer
Inner layer
Airgap
p_1
d_1
lh_1
Core (Nanocrystalline)
Bobbin (Durethan BKV 30)
p_4
p_2
Start
Start
End
Total length of the inner layer per turn: l_1
Total length of the inner layer per turn: l_2
Total length of the inner layer per turn: l_3
(b)
Cross section B (vertical cross section)
h
d_0
Cold terminal
Outer layer
p_3
p_2
Bobbins
Middle layer
Hot terminal
Inner layer
Bobbin (Durethan BKV 30)
d_1
p_1
Core (amorphous)
(c)

Fig. 2-9 Schematics for deriving geometrical parameters of the MV inductor. (a) CAD model and capacitive couplings. (b) Cross section A (horizontal cross section) . (c) Cross section B (vertical cross section).

TABLE II. Relative permittivity of the material

Description	Symbol	Value
The permittivity of the bobbins [79], [80]	ε_b	4.0
The permittivity of the coating of cables [81], [82]	ε_r	3.7 (average value)
The permittivity of vacuum [83]	ε_0	8.82×10^{-12} F/m

According to Fig. 2-10, four basic capacitive couplings of the researched medium-voltage inductor can be identified as follows [J2]:

- The turn-to-turn capacitive coupling between two adjacent turns at the same layer.
- The layer-to-layer capacitive coupling between two adjacent layers.
- The layer-to-core capacitive coupling between the inner layer and core.
- The winding-to-winding capacitive couplings occurred between the two windings.

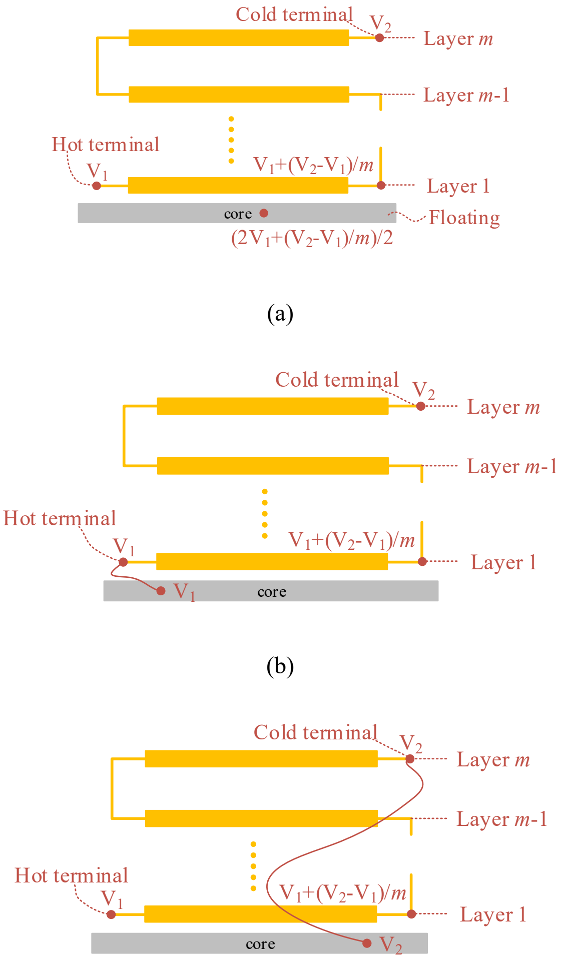
Due to the limited impacts, the capacitive couplings between two non-adjacent turns and between two not-adjacent layers are neglected in this thesis.

2.2.2 STATIC AND DYNAMIC CAPACITANCE

Two different capacitances, static and dynamic capacitance, need to be defined before modeling. The static capacitance is only dependent on the geometrical and material parameters, e.g., C_{tc} and C_{tt} showed in Fig. 2-1. The dynamic capacitance is the equivalent capacitance of the inductor when the inductor is under normal operations, where the current flows through the winding. The dynamic capacitance is the overall performance of the inductor, which is represented by the actual stored electrical-field energy, e.g. C_{total} solved in eq. (2.3). Since in the previous section, the thesis has revealed that the lumped-capacitor-network method is the improper solution for calculating the parasitic capacitance of inductors at the first resonant frequency, the dynamic capacitance (total equivalent capacitance of inductor) will be solved using the energy-conservation-based method. Therefore, the dynamic capacitance of the inductor is dependent on both static capacitance and voltage distribution within the winding, which is represented by the total stored electrical field energy of the static capacitance. Thus, the static capacitance and dynamic capacitance need to be solved in sequence.

The derivations of static capacitance for the considered medium-voltage inductor have been elaborated in [J2]. The four static capacitances, corresponding to the four basic capacitive couplings of the exampled medium-voltage inductor, $C_{\mathrm{sta\_turn\text{-}to\text{-}turn}}$ (static capacitance between two adjacent turns), $C_{\mathrm{sta\_layer\text{-}to\text{-}layer}}$ (static capacitance between two adjacent layers), $C_{\mathrm{sta\_layer\text{-}to\text{-}core}}$ (static capacitance between inner layer and core), $C_{\mathrm{sta\_winding\text{-}to\text{-}winding}}$ (static capacitance between two windings), are derived based on the geometrical and material parameters. The detailed derivations of the four static capacitance are given in [J2]

In order to calculate the three individual capacitance of the medium-voltage inductor considering the ground effects, three different configurations are implemented, which are shown in Fig. 2-10. Each configuration is a two-terminal network, where the voltage potential on the core is different. The voltage potential on the core is assumed to be equal, where the voltage potential of the winding is assumed to be equal to one of the terminals. The voltage potential on the two terminals is V_1 and V_2, respectively. In Case 1, the floating voltage potential on the core is $(2V_1+(V_2-V_1/m))/2$, which is assumed to be the average voltage potential of Layer 1. The voltage potential on core is V_1 in Case 2, which is V_2 in Case 3.


Cold terminal
V2
Layer m
Layer m-1
Hot terminal
V1
V1+(V2-V1)/m
Layer 1
core
Floating
(2V1+(V2-V1)/m)/2
Cold terminal
V2
Layer m
Layer m-1
Hot terminal
V1
V1+(V2-V1)/m
Layer 1
V1
core
Cold terminal
V2
Layer m
Layer m-1
Hot terminal
V1
V1+(V2-V1)/m
Layer 1
core
V2

(a)

(b)

(c)

Fig. 2-10 Schematic of the inner layer and core with different configurations. a) Case 1: core is floating; b) Case 2: core is clamped to the hot terminal; c) core is clamped to the cold terminal

In these three configurations, the dynamic capacitance $C_{\text{dyn\_turn-to-turn}}$ between two adjacent turns, $C_{\text{dyn\_layer-to-layer}}$ between two adjacent layers, and $C_{\text{dyn\_winding-to-winding}}$ between two windings are the same since the voltage potential within the winding is the same. The only difference is the dynamic capacitance between the inner layer and core, since the voltage potential difference between the inner layer and core is different in the three configurations [J2].

The three dynamic capacitance $C_{\text{dyn\_layer-to-core}}$ between the inner layer and core in the three configurations are given in eq. (2.5).

$$\begin{aligned}
C_{\text{dyn\_layer-to-core1}} &= 2\times\frac{1}{12m^2}\times C_{\text{sta\_layer-to-core}}\\
C_{\text{dyn\_layer-to-core2}} &= 2\times\frac{1}{3m^2}\times C_{\text{sta\_layer-to-core}}\\
C_{\text{dyn\_layer-to-core3}} &= 2\times\frac{3m^2-3m+1}{3m^2}\times C_{\text{sta\_layer-to-core}}
\end{aligned}\tag{2.5}$$

It is noted that there is a coefficient of 2 in eq. (2.5), since there are two windings in the researched medium-voltage inductors. The detailed derivations of $C_{\text{dyn\_turn-to-turn}}$, $C_{\text{dyn\_layer-to-layer}}$, $C_{\text{dyn\_winding-to-winding}}$, and $C_{\text{dyn\_layer-to-core}}$ are elaborated in [J2].

The total dynamic capacitance of the researched inductor in three configurations can be obtained as eq. (2.6), based on energy-conservation law.

$$\begin{aligned}
C_{\text{dyn1}} &= C_{\text{dyn\_turn-to-turn}} + C_{\text{dyn\_layer\_to\_layer}} + C_{\text{dyn\_layer\_to\_core1}} + C_{\text{dyn\_winding\_to\_winding}}\\
C_{\text{dyn2}} &= C_{\text{dyn\_turn-to-turn}} + C_{\text{dyn\_layer\_to\_layer}} + C_{\text{dyn\_layer\_to\_core2}} + C_{\text{dyn\_winding\_to\_winding}}\\
C_{\text{dyn3}} &= C_{\text{dyn\_turn-to-turn}} + C_{\text{dyn\_layer\_to\_layer}} + C_{\text{dyn\_layer\_to\_core3}} + C_{\text{dyn\_winding\_to\_winding}}
\end{aligned}\tag{2.6}$$

The three configurations of the medium-voltage inductors can also be presented at the circuit-level, as shown in Fig. 2-11. The three configurations are three special cases of the three-terminal inductor, where the three-terminal inductor is reduced to three two-terminal circuits in each configuration.

C_{tt}, C_{tc1}, and C_{tc2} are the three individual capacitances in the three-terminal equivalent circuit. The dynamic capacitance in Case 1-3 can also be represented by the three individual equivalent capacitances based on the series/parallel connection of the capacitances derived using the circuit theory, which is given as eq. (2.7).

$$\begin{cases} C_{\mathrm{dyn1}} = C_{\mathrm{tt}} + \dfrac{C_{\mathrm{tc1}} C_{\mathrm{tc2}}}{C_{\mathrm{tc1}} + C_{\mathrm{tc2}}} \\ C_{\mathrm{dyn2}} = C_{\mathrm{tt}} + C_{\mathrm{tc2}} \\ C_{\mathrm{dyn3}} = C_{\mathrm{tt}} + C_{\mathrm{tc1}} \end{cases} \tag{2.7}$$

Since C_{dyn1}, C_{dyn2}, and C_{dyn3} are derived, C_{tt}, C_{tc1}, and C_{tc2} can be solved according to eq. (2.7). Thus, the three individual capacitances in the medium-voltage inductors are analytically derived [J2].

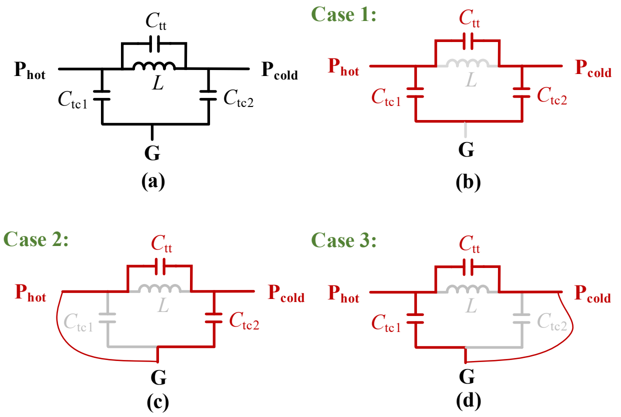


Fig. 2-11 Derivation of the three-terminal equivalent circuit schematic. (a) is the schematic. (b), (c) and (d) are the representation of three cases with different terminal connections

2.2.3 EXPERIMENTAL VERIFICATIONS

The theoretical derivations are verified by a prototype of the medium-voltage inductors. Fig. 2-12 shows the pictures of the medium-voltage inductor.

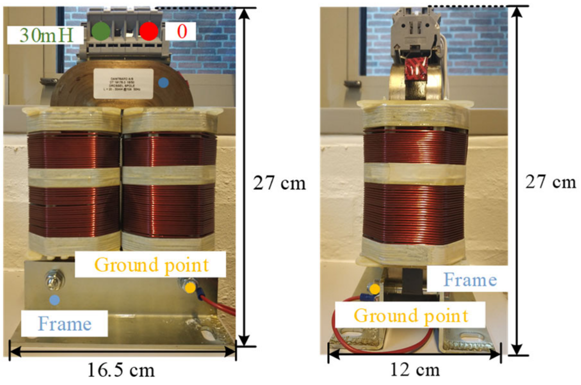


Fig. 2-12 Pictures of the researched MV inductor

The theoretically calculated C_{tt}, C_{tc1}, and C_{tc2} of the medium-voltage inductor can be calculated using the derived equations (2.5)-(2.7) and the given parameters in Table 2. II and III, where the results are listed in Table 2-IV (A). According to he calculations, the equivalent two-terminal circuit and three-terminal circuit are obtained in Table 2-IV (B).

The equivalent capacitance between any two terminals of the medium-voltage inductor is measured by using Keysight E4990 impedance analyzer and its adapted 16047, where the measured capacitance of the three cases are listed in Table 2-V (A). Both the original measurement method and measurement method using guarding technology are compared [84]. The original measurement method can only measure the impedance of a two-terminal network, where the measurement method using guarding technology can measure the individual impedance between any two terminals of a multi-terminal network [J2]. Similarly, the equivalent two-terminal circuit and three-terminal circuit are obtained in Table 2-V (B) using the measured capacitance of the three cases.

Both calculations and measurements are only valid up to the first resonant frequency of inductors.

Table 2-IV (A) Numerical comparisons of calculated parasitic capacitances in three configurations

Case	Calculations (Proposed method)	Calculations (method [29])	Calculations (method [71])
Case 1	48.76 pF (C_{dyn1})	27.63 pF	43.22 pF
Case 2	56.90 pF (C_{dyn2})	Not valid	Not valid
Case 3	252.54 pF (C_{dyn3})	Not valid	Not valid

Table 2-IV (B) Comparisons of the calculated equivalent circuit

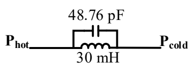
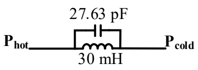
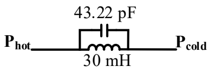
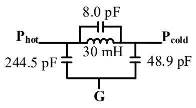
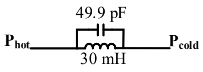
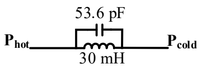
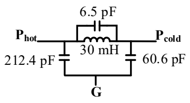
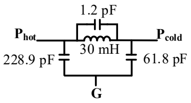
	Calculations (Proposed method)	Calculations (method [29])	Calculations (method [71])
Two-terminal equivalent circuit	 48.76 pF P_{hot} P_{cold} 30 mH	 27.63 pF P_{hot} P_{cold} 30 mH	 43.22 pF P_{hot} P_{cold} 30 mH
Three-terminal equivalent circuit	 8.0 pF P_{hot} P_{cold} 30 mH 244.5 pF 48.9 pF G	Not valid	Not valid

Table 2-V (A) Numerical comparisons of measured parasitic capacitances in three configurations

Case	Measured capacitance (Normal measurements)	Converted capacitance based on the measurements with guarding method
Case 1	49.9 pF	53.6 pF
Case 2	63.0 pF	67.1 pF
Case 3	230.1 pF	218.9 pF

Table 2-V (B) Comparisons of the measured equivalent circuit

	Measured capacitance (Normal measurements)	Converted capacitance based on the measurements with guarding method
Two-terminal equivalent circuit	 49.9 pF P_{hot} P_{cold} 30 mH	 53.6 pF P_{hot} P_{cold} 30 mH
Three-terminal equivalent circuit	 6.5 pF P_{hot} P_{cold} 30 mH 212.4 pF 60.6 pF G	 1.2 pF P_{hot} P_{cold} 30 mH 228.9 pF 61.8 pF G

Comparing Table 2-IV and -V, it can be concluded that the calculations using the proposed modeling method can predict the three individual capacitances of a three-terminal inductor. The maximum error for the three cases is around 15%, which is tolerable compared to previous research in this field. It is found that the two capacitances between terminals and core are not identical due to the unsymmetrical geometrical structure of the winding [J2].

2.2.4 SUMMARY

This section is mainly supported by [J2]. A physics-based modeling method of parasitic capacitance in inductors with considering ground effects is proposed, where the inductor is modeled as a three-terminal component instead of the conventional two-terminal component. The ground/frame of inductor is considered as an individual terminal. The three individual capacitances in the three-terminal equivalent circuit, which are valid up to the first resonant frequency of inductors, are analytically derived. One prototype of the medium-voltage inductor is manufactured, where the accuracy of the proposed modeling method is verified.

2.3 PHYSICS-BASED MODELING METHODS WITH CONSIDERING ELECTRICAL FRINGE FIELD

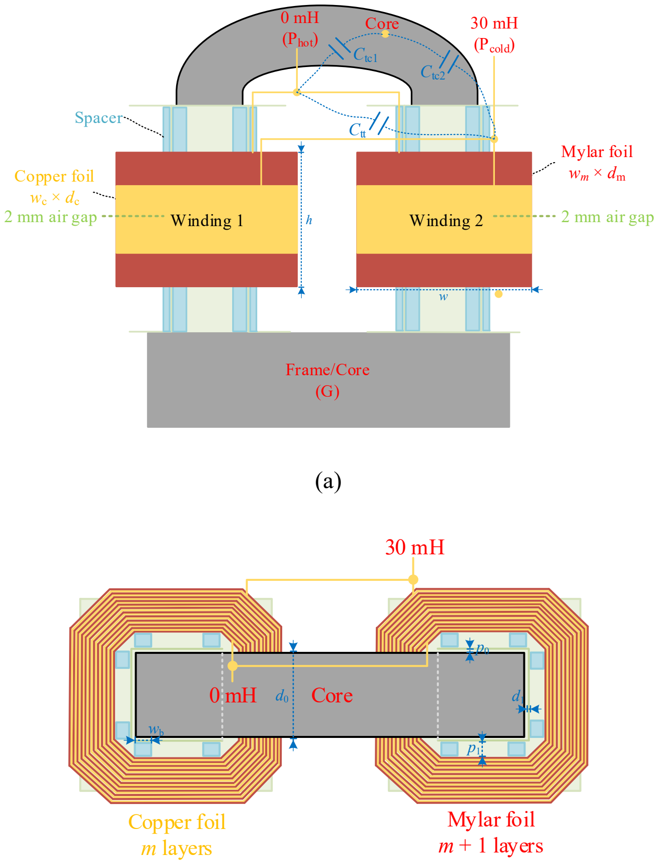
The dynamic capacitance contributed by the electrical fringe field between the winding and core is modeled in this section. The electrical fringe field has more effects in copper-foiled inductors, compared to the conventional inductors constructed by the round cables.

2.3.1 AN MEDIUM-VOLTAGE COPPER-FOILED INDUCTOR

The copper-foiled inductors are widely used in high-power applications since they offer higher power density and more flexibility than round-cable-based inductors [86]-[89]. It is known that the magnetic devices constructed by copper-foils may have a larger parasitic capacitance due to the extensive interleaving of windings [86]. However, only a few works have introduced the physics-based modeling methods for copper-foiled inductors, where the electrical fringe field introduced by the special geometrical structure is not investigated.

The schematic of a medium-voltage copper-foiled inductor are given in Fig. 2-13. As similar to the medium-voltage inductor introduced and presented in the previous section, the core and frame of the medium-voltage copper-foiled inductor will be grounded in practice due to the safety considerations. Therefore, three individual capacitances, C_{tt} between two terminals, C_{tc1} between one terminal and core, and C_{tc2} between the other terminal and core, are considered to be identified by using a physics-based modeling method.

The geometrical parameters and material parameters of the researched medium-voltage copper-foiled inductor are presented in Table 2-VI and -VII, respectively.


0 mH
(P_hot)
Core
30 mH
(P_cold)
C_tc1
C_tc2
C_tt
Spacer
Mylar foil
w_m × d_m
Copper foil
w_c × d_c
2 mm air gap
Winding 1
h
Winding 2
2 mm air gap
w
Frame/Core
(G)
30 mH
p_0
0 mH
d_0
Core
d_1
w_b
p_1
Copper foil
m layers
Mylar foil
m + 1 layers

(a)

(b)

Fig. 2-13 Schematic of the medium-voltage copper-foiled inductor. (a) Front view. (b) Cross-sectional view.

Table 2-VI. Key parameters of the medium-voltage copper-foiled inductor

Description	Symbol	Value
Thickness of the copper foil	d_c	0.05 mm
Width of the copper foil	w_c	30 mm
Thickness of the mylar foil	d_m	0.05 mm
Width of the mylar foil (Height of the winding)	w_m (h)	60 mm
Distance between the two windings	p_w	19 mm
Width of the winding	w	55.5 mm
Width of the spacer	w_b	10 mm

Thickness of the core	d_0	40 mm
Distance of the air gap between the bobbin and core	p_0	1.5 mm
Distance between the inner layer and bobbin	p_1	12 mm
Thickness of the bobbin	d_1	2 mm
Number of layers	m	190
Total inductance (designed value)	L	30 mH

Table 2-VII. Relative permittivity of the material

Description	Symbol	Value
Relative permittivity of the mylar foil [85]	ε_m	3.25
Relative permittivity of the bobbins and spacers [79], [80]	ε_b	4.0
The permittivity of vacuum [83]	ε_0	8.82×10^{-12} F/m

2.3.2 THE ELECTRICAL FRINGE FIELD

A FEM simulation is given in this section to identify the electrical fringe field. In Ansys Maxwell, a 2-dimension copper-foiled inductor is modeled, where the voltage potential on the winding is configured as 1 V, the voltage potential on the core is configured as 0 V. There are 19-layers of copper-foil and 20-layers of mylar-foil, where the thickness of the copper-foil and mylar-foil is 0.5 mm, respectively [J3]. The distance between the inner layer and the core is 4 mm. In the simulation, the width of copper-foil is configured as 30 mm, where the width of mylar-foil is 60 mm [J3]. The simulated electrical field distribution of the 2-dimension copper-foiled inductor is shown in Fig. 2-14.

Since the voltage potential on the copper-foils is the same in this simulation, there is no electrical field between two adjacent copper-foils. According to the FEM simulations, it can be identified that there is a strong electrical coupling between the inner copper-foil and core. Besides, there are some electrical couplings between the sidewall of the inductor and core, and between the top surface and core, which are actually contributed by the electrical fringe field [J3]. Usually, the electrical fringe field is neglected in previous research of modeling the parasitic capacitance in inductors. However, the electrical fringe field in copper-foiled inductors cannot be neglected due to the extensive area of the sidewall and top surface. Therefore, the impacts of the electrical fringe field should be considered in the modeling of parasitic capacitance in copper-foiled inductors [J3].

Then the electrical field contributed by the five basic capacitive couplings in copper-foiled medium-voltage inductors are identified in Fig. 2-15. In order to calculate the three individual capacitances, C_{tt}, C_{tc1}, and C_{tc2}, the static and dynamic capacitance contributed by the five electrical fields needs to be modeled in sequence [J3].

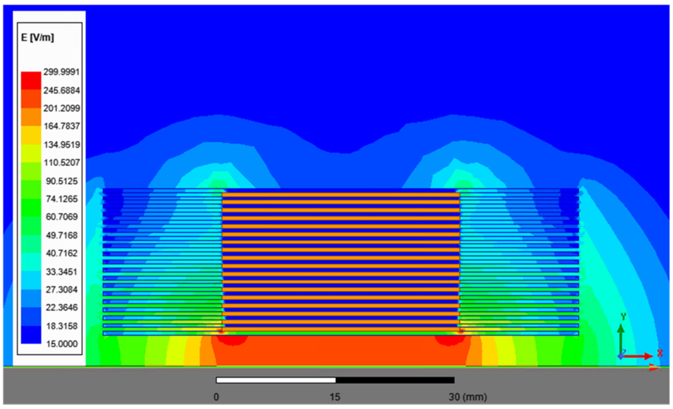


Fig. 2-14 Electrical field simulation of the 2-dimension copper-foil inductor

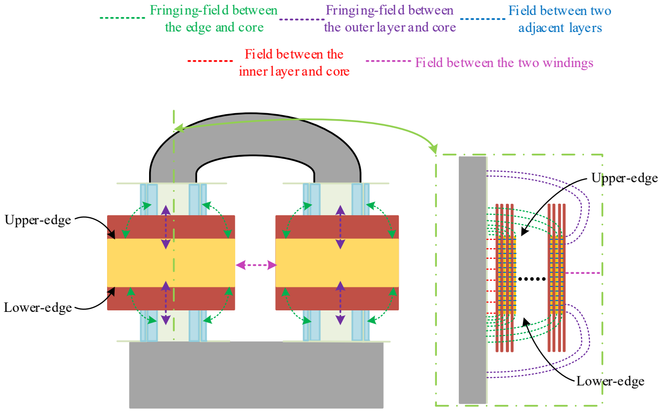

Fringing-field between the edge and core
Fringing-field between the outer layer and core
Field between two adjacent layers
Field between the inner layer and core
Field between the two windings
Upper-edge
Lower-edge
Upper-edge
Lower-edge

Fig. 2-15 Identify the capacitive couplings in copper-foiled MV inductors

2.3.3 STATIC AND DYNAMIC CAPACITANCE CONTRIBUTED BY ELECTRICAL FRINGE FIELD

Since the static and dynamic capacitance contributed by the electrical field between the two adjacent layers, the inner layer and core, and the two windings have been elaborated in previous sections, this section will focus on physics-based modeling of the static and dynamic capacitance contributed by the electrical fringe field [J3].

The capacitance contributed by electrical fringe-field has been researched in transmission line system [90], antenna applications [91], very-large-system-integration (VLSI) applications [92], [93]. The electrical fringe field effects have been also considered in high-voltage transformer applications [94], which is however, directly using the empirical equations derived for VLSI applications.

In VLSI applications, shown in Fig. 2-16, the parasitic capacitance contributed by the electrical fringe field is characterized by an empirical equation [93] shown in eq. (2.8).

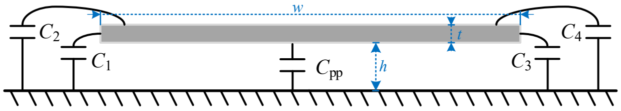


Fig. 2-16 Schematic of a chip and ground in VLSI applications

$$\begin{aligned} C_{\text{total}} &= C_1 + C_2 + C_3 + C_4 + C_{\text{pp}} \\ &\approx \varepsilon_0 \varepsilon_r \times \left(\frac{w}{h} + 0.77 + 1.06 \times \left(\frac{w}{h} \right)^{0.25} + 1.06 \times \left(\frac{t}{h} \right)^{0.5} \right) \end{aligned} \tag{2.8}$$

The empirical eq. (2.8) is only applicable for the cases with special structures. As shown in Fig. 2-16, the applications in VLSI only have one layer, where the chip is assumed to be surrounded by the same material. As illustrated in [93], eq. (2.8) is only valid when $w/h > 0.3$ and $t/h < 10$. According to Fig. 2-13, copper-foiled medium-voltage inductors have multiple layers with a more complex geometrical structure. Besides, the voltage potential is different on each copper foil. Therefore, using the empirical equation shown in eq. (2.8) cannot accurately calculate the dynamic capacitance in copper-foiled medium-voltage inductors [J3].

The static capacitance contributed by the electrical fringe field in the copper-foiled inductors is modeled first. Before modeling the fringe field capacitance, a few necessary assumptions are made, which has been elaborated in [J3].

The schematics of the elementary capacitance contributed by the fringe field are shown in Fig. 2-17. The static capacitance $C_{\text{2d\_sc}}$ between the sidewall of winding and core is calculated as eq. (2.9), based on the geometrical structures and material information [J3].

$$\begin{cases} C_{\mathrm{ele\_sc}} = \dfrac{2\varepsilon_{\mathrm{d1}}\varepsilon_0 dl_1}{\pi(l_1 + p_1 + d_1)} \\ \varepsilon_{\mathrm{d1}} \approx \dfrac{p_1 + d_1 + \dfrac{1+\varepsilon_{\mathrm{c}}}{2} l_1}{l_1 + p_1 + d_1} \\ C_{\mathrm{2d\_sc}} = 2\displaystyle\int_0^{t_{\mathrm{winding}}} C_{\mathrm{ele\_sc}} \\ \qquad = 2\displaystyle\int_0^{t_{\mathrm{winding}}} \dfrac{2\varepsilon_{\mathrm{d1}}\varepsilon_0}{\pi(l_1 + p_1 + d_1)} dl_1 \end{cases} \tag{2.9}$$

The static capacitance $C_{\mathrm{2d\_tc}}$ between the top surface and core is calculated as eq. (2.10).

Similarly, the static capacitance between the inner layer and core is derived as eq. (2.11). The electrical field between inner layer and core is assumed as the uniform electrical field.

$$\begin{cases} C_{\mathrm{2d\_lc}} = \dfrac{\varepsilon_{\mathrm{s1}}\varepsilon_0 w_{\mathrm{foil}}}{d_{\mathrm{m}} + p_1 + d_1} \\ \varepsilon_{\mathrm{s1}} = \dfrac{d_1\varepsilon_b + p_1 + d_{\mathrm{m}}\varepsilon_m}{d_{\mathrm{m}} + p_1 + d} \end{cases} \tag{2.11}$$

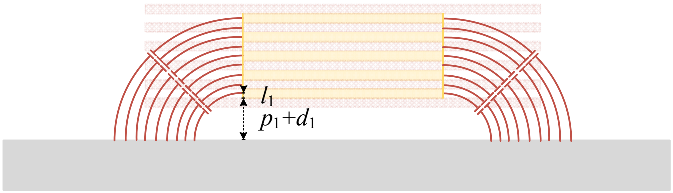
Thus, the total capacitance $C_{\mathrm{2d\_total}}$ in a 2D copper-foiled inductor can be presented as eq. (2.12), as a sum of $C_{\mathrm{2d\_sc}}$, $C_{\mathrm{2d\_tc}}$, and $C_{\mathrm{2d\_lc}}$.

$$C_{\mathrm{2d\_total}} = C_{\mathrm{2d\_sc}} + C_{\mathrm{2d\_tc}} + C_{\mathrm{2d\_lc}} \tag{2.12}$$

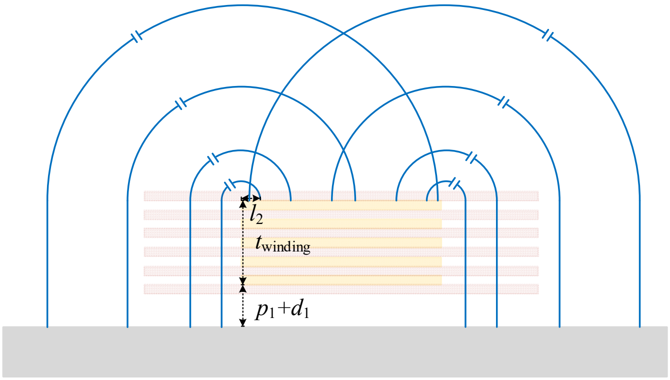
By substituting the geometrical and material information listed in Table II-VI and -VII, a comparison of parasitic capacitance simulated using FEM tool, calculation using empirical equations, and the proposed method is shown in Fig. 2-18. According to Fig. 2-18, the proposed modeling method shows better accuracy in predicting the static capacitance of 2-dimension copper-foiled inductors [J3].

It is worth to mention that in both eq. (2.9) and eq. (2.10), the integrating path of electrical field intensity is assumed as the red and blue curve in Fig. 2-17, respectively. The electric field strength is assumed as a constant value at each path of electrical field intensity.

$$\begin{cases} C_{\text{ele\_tc}} = \dfrac{\varepsilon_{\text{d2}}\varepsilon_0 dl_2}{\pi l_2 + p_1 + d_1 + t_{\text{winding}}} \\ \varepsilon_{\text{d2}} = \dfrac{p_1 + d_1 + \dfrac{1+\varepsilon_{\text{c}}}{2} t_{\text{winding}} + \pi l_2}{p_1 + d_1 + t_{\text{winding}} + \pi l_2} \qquad (l_2 < \dfrac{w_{\text{m}} - w_{\text{c}}}{2}) \\ \varepsilon_{\text{d2}} = 1 \qquad (l_2 \geq \dfrac{w_{\text{m}} - w_{\text{c}}}{2}) \\ C_{\text{2d\_tc}} = 2\displaystyle\int_0^{w_{\text{foil}}} C_{\text{ele\_tc}} \\ \quad = 2\displaystyle\int_0^{w_{\text{foil}}} \dfrac{\varepsilon_{\text{d2}}\varepsilon_0}{\pi l_2 + p_1 + d_1 + t_{\text{winding}}} dl_{21} \end{cases} \tag{2.10}$$



(a)



(b)

Fig. 2-17 Elementary capacitances contributed by the fringe field. (a) elementary capacitance between the sidewall and core; (b) elementary capacitance between the top-surface and core.

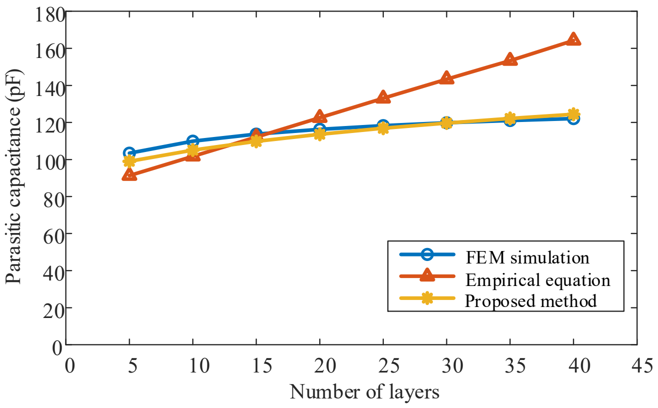
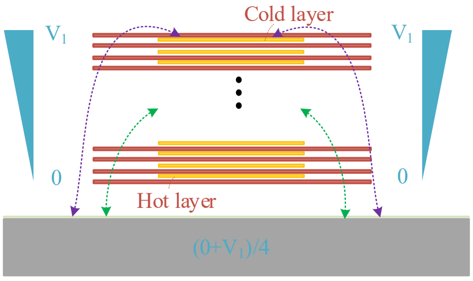


Fig. 2-18 Comparison of the static capacitances obtained using the FEM simulation, the empirical equations, and the proposed modeling method

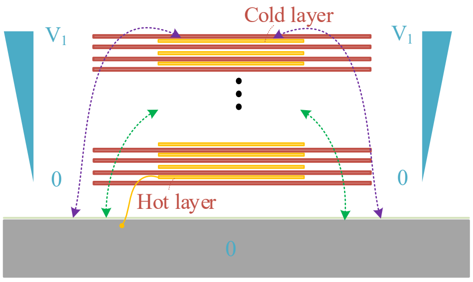
Similar to the previous section, three configurations are selected for calculating the three individual capacitance of the three-terminal copper-foiled inductor [J3]. The schematics of the three configurations are shown in Fig. 2-19. The voltage potential at the inner layer is 0, where the voltage potential at the outer layer is V_1.

- Case 1: Core is floating, where the core potential is around $(0+V_1)/4$ in inductors with multiple layer structures [58].
- Case 2: Core is connected to the hot layer, where the voltage potential is V_1.
- Case 3: Core is connected to the cold layer, where the voltage potential is 0.

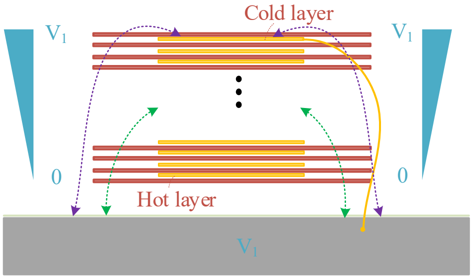
The total dynamic capacitance in these three configurations can be derived according to the derived static capacitance and voltage potential distribution. The detailed derivations of the total dynamic capacitance in the three configurations are elaborated in [J3]. Similar to Fig. 2-11 and eq. (2.7), C_{tt}, C_{tc1}, and C_{tc2} can be solved using the derived total dynamic capacitance for the three configurations [J3].



(a)


Cold layer
V1
V1
0
0
Hot layer
0

(b)

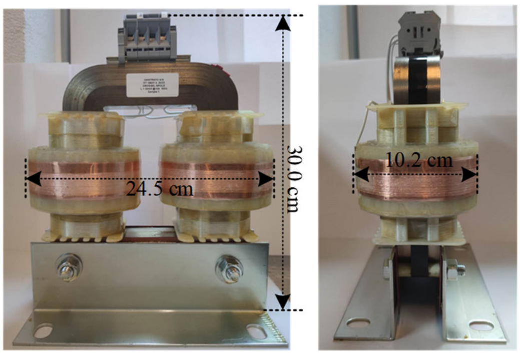

Cold layer
V1
V1
0
0
Hot layer
V1

(c)

Fig. 2-19 Schematic of the copper-foiled inductor with different configurations. a) Case 1: core is floating; b) Case 2: core is clamped to the hot terminal; c) core is clamped to the cold terminal

2.3.4 EXPERIMENTAL VERIFICATION

A prototype of 10 kV/8A copper-foiled inductor with the parameters shown in Table 2-VI and -VII is manufactured. The pictures are presented in Fig. 2-20.



(a) Front view (b) Side view

Fig. 2-20 Pictures of the manufactured copper-foiled MV filter inductor

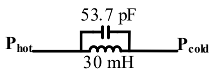
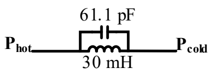
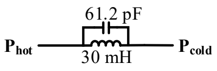
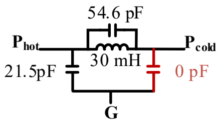
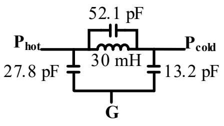
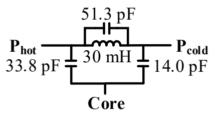
The calculated capacitance with and without considering the electrical fringe field is compared with the measurement results, which are shown in Table 2-VIII (A). The parasitic capacitance of the copper-foiled inductor is measured by Keysight E4990 impedance analyzer and its adapter 16047E. Using the calculated and measured capacitance of Case 1-3, the two-terminal equivalent circuit and three-terminal equivalent circuit are obtained in Table 2-VIII (B).

It can be found that the equivalent capacitance between P_{cold} and G is 0 pF predicted by the conventional modeling methods without considering the electrical fringe field effects, which is very inaccurate compared to the measurement results. Using the proposed modeling method with considering the electrical fringe field effects, the equivalent capacitance between P_{cold} and G is calculated, which shows good agreement with the measurement results. More details regarding experimental verifications can be found in [J3].

Table 2-VIII (A) Numerical comparisons of parasitic capacitances between the measurements and calculations

Case	Calculations (without considering the fringe field [J2])	Calculations (Proposed method)	Measured capacitance (Normal measurements)
Case 1	53.7 pF	61.1 pF	61.2 pF
Case 2	53.7 pF	65.3 pF	65.3 pF
Case 3	75.1 pF	80.0 pF	85.1 pF

Table 2-VIII (B) Comparisons of the calculated and measured equivalent circuit

	Calculations (without considering the fringe field [J2])	Calculations (Proposed method)	Measured capacitance (Normal measurements)
Two-terminal equivalent circuit			
Three-terminal equivalent circuit	 54.6 pF P_{hot} P_{cold} 21.5pF 30 mH 0 pF G	 52.1 pF P_{hot} P_{cold} 27.8 pF 30 mH 13.2 pF G	 51.3 pF P_{hot} P_{cold} 33.8 pF 30 mH 14.0 pF Core

2.3.5 SUMMARY

This section is mainly supported by [J3]. The modeling method for medium-voltage copper-foiled inductors is proposed in this section, where the effects of electrical fringe field are considered. The theoretical analysis proves that the energy stored in the electrical fringe field is significant for correctly characterize the parasitic capacitance between terminals and core. The experimental results show the effectiveness of the proposed modeling method.

2.4 PHYSICS-BASED MODELING METHODS WITHOUT USING FLOATING VOLTAGE POTENTIAL OF CORE

There is a common constraint in previous modeling methods. The floating voltage potential is required to be known, not only for the modeling of the inductors with floating core and frame, but also for the inductors with grounded core and frame. In this section, an improved physics-based modeling method without using floating voltage potential is proposed. The "perfect conductor" assumption is still used in this section, where the voltage potential on the core is assumed to be a constant value during the modeling process.

2.4.1 IMPROVED PHYSICS-BASED MODELING METHOD

For two-terminal inductors, the core of the inductors is always floating. Therefore, the core/frame of inductor is unnecessary to be considered as an individual terminal. In these inductors, the floating core voltage potential is required to know for calculating the energy stored between the winding and core.

For three-terminal inductors, the core/frame of inductors is usually grounded, where the core/frame is required to be modeled as an individual terminal. Although the core and frame of inductors are grounded, the floating core voltage potential is still required to be pre-known, as shown in Fig. 2-11 and Fig. 2-19, where the inductor with a floating core is considered as one of the three configurations for calculating the three individual capacitances in the three-terminal equivalent circuit.

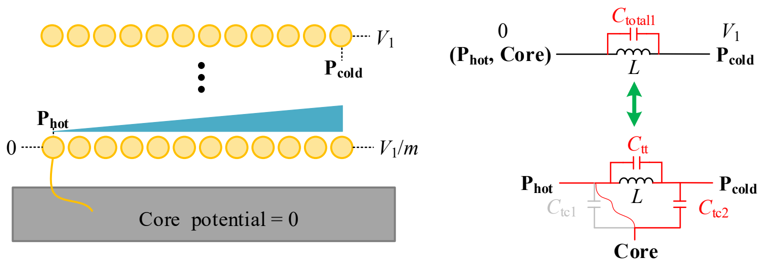
The three-terminal equivalent circuit is able to be converted to the corresponding two-terminal circuit by assuming the ground point in the three-terminal equivalent circuit is floating, which means, the inductor with a floating core can still be represented by a three-terminal equivalent circuit by considering the core/frame is an individual terminal [J4].

Thus, if another configuration without using the floating core voltage potential, could be proposed by replacing the configuration that requires to pre-know the floating core voltage potential, which can model the parasitic capacitance of inductors with floating or grounding core/frame without using the floating core voltage potential. The impacts of the uncertainty of floating core voltage potential on the calculated capacitance have been elaborated in [J4], where the dynamic capacitance between the winding and core will change under different floating core voltage potential.

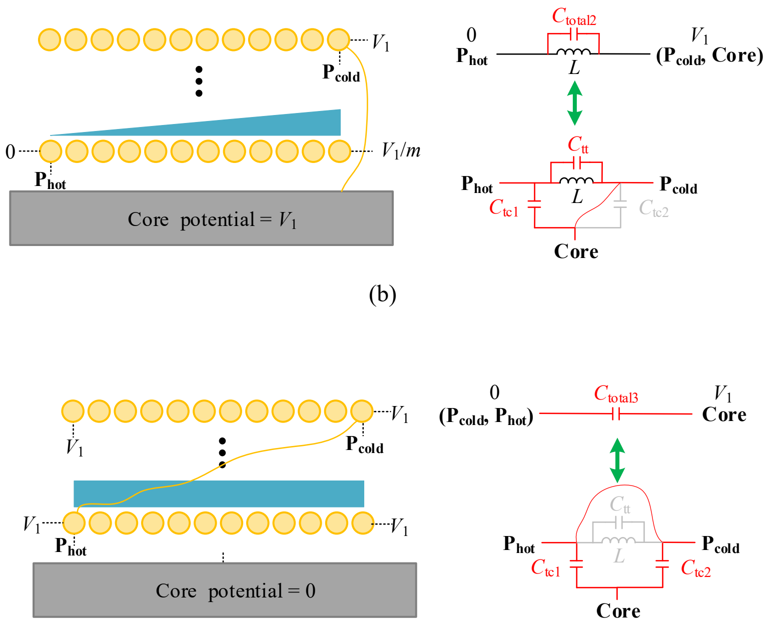
The three configurations for modeling the three individual capacitances with a new configuration, for both inductors with grounding core/frame or floating core/frame, are proposed, which are shown in Fig. 2-21.

In order to simplify the derivations, the voltage potential at the two ends of inductor is assumed to be 0 and V_1, as shown in Fig. 2-21. In this section, the terminal voltage potential 0 and V_1 is used for simplifying the derivation.

Similar to the previous section, the three-terminal inductor is simplified to three configurations that can be represented by two-terminal equivalent circuits. Compared to the proposed modeling method in previous section, Fig. 2-21 (c) is the new configuration, where the three configurations illustrated in Fig. 2-21 do not require the knowledge of the floating core voltage potential [J4].



(a)


V_1
$\mathbf{P}_{\text{cold}}$
0
V_1/m
$\mathbf{P}_{\text{hot}}$
Core potential = V_1
0
$\mathbf{P}_{\text{hot}}$
C_{total2}
L
V_1
($\mathbf{P}_{\text{cold}}$, Core)
C_{tt}
$\mathbf{P}_{\text{hot}}$
$\mathbf{P}_{\text{cold}}$
C_{tc1}
L
C_{tc2}
Core
V_1
V_1
$\mathbf{P}_{\text{cold}}$
V_1
V_1
$\mathbf{P}_{\text{hot}}$
Core potential = 0
0
($\mathbf{P}_{\text{cold}}$, $\mathbf{P}_{\text{hot}}$)
C_{total3}
V_1
Core
C_{tt}
$\mathbf{P}_{\text{hot}}$
L
$\mathbf{P}_{\text{cold}}$
C_{tc1}
C_{tc2}
Core

(b)

(c)

Fig. 2-21 Schematics for the three configurations of the improved modeling method. a) Configuration 1; b) Configuration 2; c) Configuration 3.

These three configurations provide the overview of voltage potential distribution for both winding and core [J4]. Thus, using the developed modeling methods for deriving the dynamic capacitance in three configurations, C_{tt}, C_{tc1}, and C_{tc2} in the three-terminal equivalent can be calculated by eq. (2.13).

$$\begin{aligned} C_{\text{total1}} &= C_{\text{tt}} + C_{\text{tc2}} \\ C_{\text{total2}} &= C_{\text{tt}} + C_{\text{tc1}} \\ C_{\text{total3}} &= C_{\text{tc1}} + C_{\text{tc2}} \end{aligned} \tag{2.13}$$

With the known C_{tt}, C_{tc1}, and C_{tc2}, the three-terminal equivalent circuit when the core is floating can also be derived by Fig. 2-22 and eq. (2.14), where the floating core voltage potential is not used in the proposed modeling method.

$$C_{\text{float}} = C_{\text{tt}} + \frac{C_{\text{tc1}} C_{\text{tc2}}}{C_{\text{tc1}} + C_{\text{tc2}}} \tag{2.14}$$

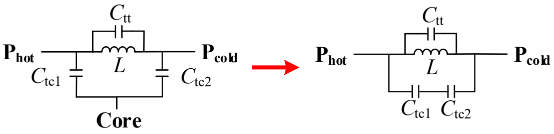


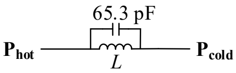
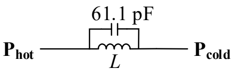
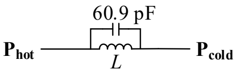
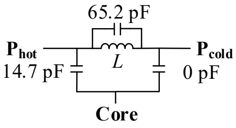
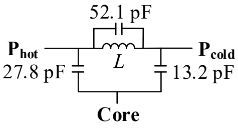
Fig. 2-22 Converting the three-terminal equivalent circuit of an inductor into two-terminal equivalent circuit when the core/frame is floating

2.4.2 EXPERIMENTAL VERIFICATIONS

The medium-voltage copper-foiled inductor shown in Section 2.3 is also used as an example in this section.

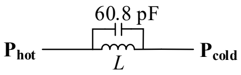
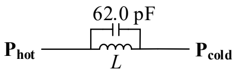
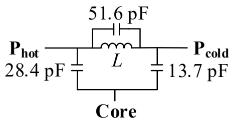
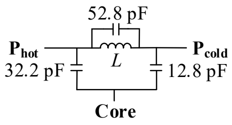
The calculated parasitic capacitances using the previous modeling methods [J2], [J3], and [58] are compared in Table 2-IX. In [J2], the floating voltage potential is assumed to be the average voltage potential of the inner layer. In [J3], the floating voltage potential is assumed to be 25% of the total winding voltage drop. In [58], the floating voltage potential is calculated based on a simplified circuit model and charge-conservation law, which is however, only the capacitance in a two-terminal equivalent circuit is obtained.

Table 2-IX Numerical comparisons of the parasitic capacitances for the different modeling methods

Methods	Model in [J2]	Model in [J3]	Model in [58]
Floating core potential	By estimating the value as the average potential in the inner layer	By estimating the value as 25% of the total winding voltage drop	By calculating the value based on the simplified circuit model and charge-conservation law
Two-terminal equivalent circuit			
Three-terminal equivalent circuit	 65.2 pF P_{hot} P_{cold} L 14.7 pF 0 pF Core	 52.1 pF P_{hot} P_{cold} L 27.8 pF 13.2 pF Core	Not valid

The calculated parasitic capacitance using the improved modeling method proposed in this section and measured parasitic capacitance using impedance analyzer is compared in Table 2-X. It can be found that, for calculating the two-terminal equivalent of inductor (core/frame is floating) and the three-terminal equivalent of inductor (core/frame is grounded), the floating voltage potential is not used. According to Table 2-X, the calculated capacitance using the improved modeling method shows good agreement with the measurements, even without using the floating core voltage potential.

Table 2-X Numerical comparisons of the parasitic capacitances using the improved modeling method and measurement results

Methods	Improved modeling method proposed in this section	Experimental measurements
Floating core potential	Not needed	Not needed
Two-terminal equivalent circuit		
Three-terminal equivalent circuit	 51.6 pF P_{hot} P_{cold} L 28.4 pF 13.7 pF Core	 52.8 pF P_{hot} P_{cold} L 32.2 pF 12.8 pF Core

2.4.3 SUMMARY

This section is supported by [J4]. The improved modeling method proposed in this section does not require the knowledge of the floating voltage potential of the core, which can avoid the uncertainties introduced by estimating the floating core voltage potential. For the magnetic devices with a more complex structure, e.g., transformers, it might be even more difficult to predict an accurate value of the floating core voltage potential. Thus, the improved modeling method can also be extended to transformers or other magnetics with multiple terminals.

CHAPTER 3. BEHAVIOR-BASED MODELING METHOD

> *"Behavior is the mirror in which everyone shows their image."*
>
> *— Johann Wolfgang von Goethe*

This chapter introduces the behavior-based modeling method of the common-mode impedance in inductors with grounded core and frame. Although the physics-based modeling method can predict the common-mode capacitive coupling between and core using a single capacitor (C_{tc1} and C_{tc2} illustrated in Fig. 2-11 and Fig. 2-21), it is only accurate up the first resonant frequency. Therefore, the physics-based modeling results are not sufficient if the research interests above the first resonant frequency. This chapter is divided into three sections. Section 3.1 introduces a measurement method of the common-mode impedance in inductors using a double-pulse-test setup. Section 3.2 introduces a behavior-based modeling method using transfer functions fitted by the system identification toolbox in Matlab. Section 3.3 introduces a behavior-based modeling method using a multi-stage RLC circuit, where a digital twin of the common-mode coupling of medium-voltage inductors is simulated in LTSpice.

3.1 MEASUREMENT OF COMMON-MODE IMPEDANCE BY USING DOUBLE-PULSE-TEST SETUP

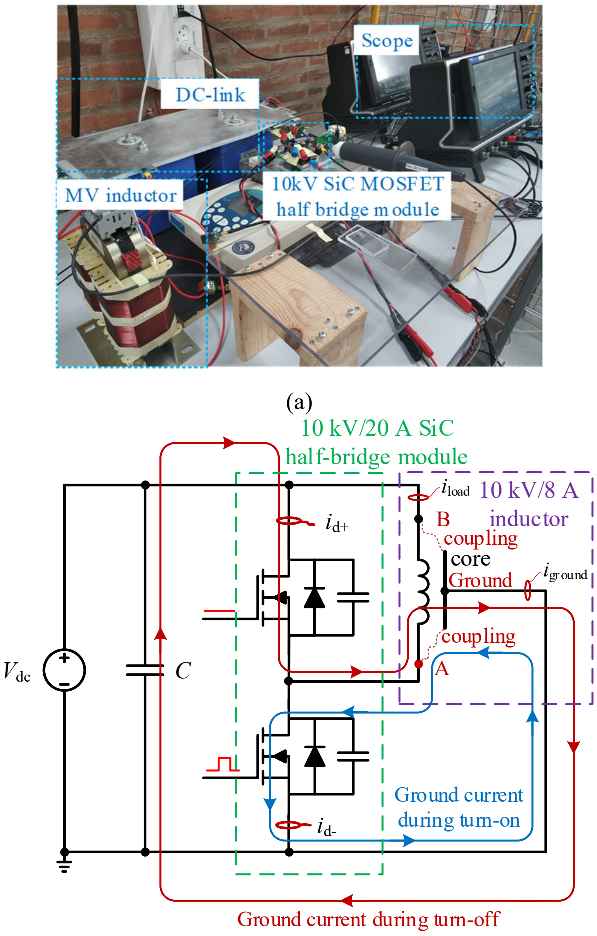
The impedance of inductors is usually measured using an impedance analyzer. Due to the limited power level of the injected perturbations of impedance analyzers, the impedance is measured under low-current, and -voltage level [75], [76], which cannot completely represent the actual behaviors of inductors under high-voltage and high-current level. The impedance of a power converter can be measured under the rated current and voltage [95], by injecting small perturbations at the operating points [96]. However, an extra converter is required for injecting the perturbations [97], which is inconvenient and add more costs to the testing.

In order to fill this gap, an impedance measurement method is proposed using the double-pulse-test setup, where the inductors can be subjected to rated current and voltage level with a compact solution.

3.1.1 DOUBLE-PULSE-TEST SETUP

Double-pulse-test (DPT) is widely used for characterizing the device performance under different voltage and current level. A picture of the double-pulse-test setup enable by 10 kV SiC MOSFETs is given in Fig. 3-1(a), where the schematic is shown in Fig. 3-1(b). The medium-voltage inductor used in this setup is the same inductor introduced in Section 2.2. A custom-packaged 10 kV/ 20A half-bridge power module is used in the DPT setup [98].

In order to guarantee the high accuracy of the measurement signal, the current and voltage measurement probes and oscilloscope in the DPT setup are selected with high-band width, which are listed in Table 3-I.


Scope
DC-link
MV inductor
10kV SiC MOSFET half bridge module
10 kV/20 A SiC half-bridge module
i_{load}
10 kV/8 A inductor
B
coupling
core
Ground
i_{ground}
i_{d+}
coupling
A
V_{dc}
C
Ground current during turn-on
i_{d-}
Ground current during turn-off

(a)

(b)

Fig. 3-1 A DPT setup enabled by 10 kV SiC MOSFETs. a) Picture. b) Schematic

Table I Measurement devices used in the double-pulse-test setup

	Devices	Maximum bandwidth
i_{d+}, i_{d-}, i_{load}	Pearson 2878 [99]	70 MHz
i_{ground}	Pearson 2877 [100]	200 MHz
v_{out}	Lecroy PPE 20 kV [101]	100 MHz
Oscilloscope	Lecroy HRO64zi [102]	400 MHz

Fig.3-2 shows the measured voltage and currents from the DPT at 3 kV/12 A. By changing the time period of the first turn-on time, the current level can be adjustable.

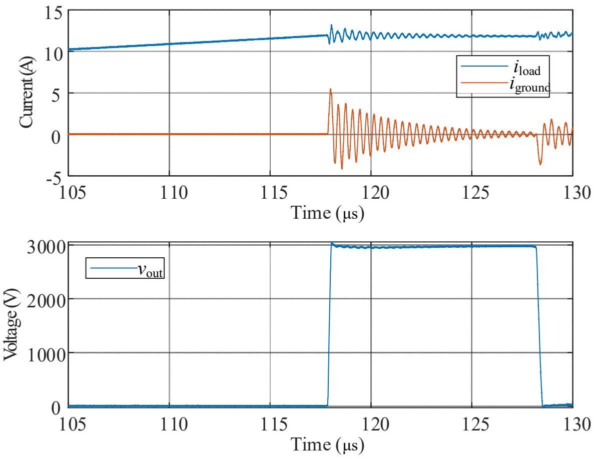


Fig. 3-2 Measured voltage and currents from the DPT at 3 kV/12 A

3.1.2 PRINCIPLE OF THE IMPEDANCE MEASUREMENT

According to Fig. 3-2, the PWM voltage should include the infinite harmonics up to a very high frequency. Thus, the basic principle of the impedance measurement method with using the double-pulse-test setup is to use the PWM voltage signal as the voltage excitation.

The DPT setup with the three-terminal equivalent circuit representation of medium-voltage inductor is shown in Fig. 3-3. Since the voltage variation between terminal 2 and 3 of the inductor is almost zero, the current i_{23}(t) through the terminal 2 and 3 is negligible. Thus, i_{ground}(t) is fully contributed by the current i_{13}(t). The voltage drop on Z_{13} is the same as v_{out}(t).

The fast Fourier-Transformation (FFT) is used to extract the harmonics of measured voltage and current. The sampling frequency of signal is defined as f_s, which is limited by the sampling frequency of scope. The number of datasets is defined as N. The length of time window t_w is defined as N/f_s, where the resolution R is calculated as

$1/t_w$. Therefore, the impedance of inductor at frequency nR is calculated as eq. (3.1), where n is the n^{th} harmonic.

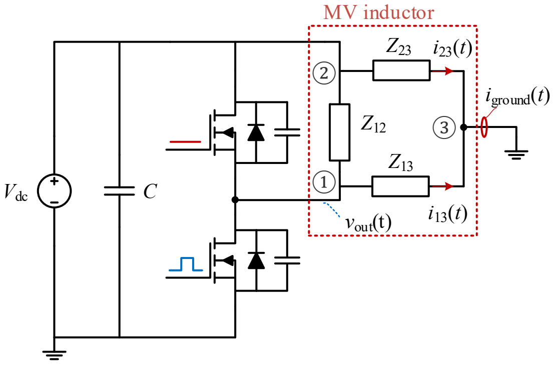


Fig. 3-3 Schematic of the DPT setup with inductor represented by a three-terminal equivalent circuit

$$Z(s,nR) = \frac{\mathcal{F}(v_{\text{out}}(t),nR)}{\mathcal{F}(i_{\text{ground}}(t),nR)} \tag{3.1}$$

The impedance of Z_{13} is obtained by mapping the calculated impedance in the interested frequency range according to (3.1).

3.1.3 EXPERIMENTAL VERIFICATIONS

The medium-voltage inductor is tested with the DPT setup under 3kV and 12 A in this section. In order to enhance the resolution, a longer time window with triple-pulse instead of the double-pulse, is selected. The measured time-domain waveforms of the triple-pulse are shown in Fig. 3-4.

The impedance can be calculated by the time-domain signal in Fig. 3-4 and eq (3.1), which is plotted as the blue curve in Fig. 3-5. The measured impedance by using the impedance analyzer and with guarding technology is the red curve shown in Fig. 3-5.

Comparing the two curves, which are measured at high voltage/current and low voltage/current level, the impedance does not have significant changes in terms of current and voltage. More experimental results could be found from [C1].

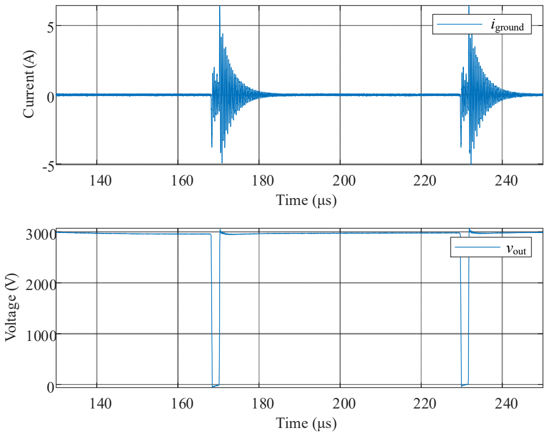


Fig. 3-4 Measured voltage and ground current in DPT setup with triple pulse and $t_w = 120\mu s$

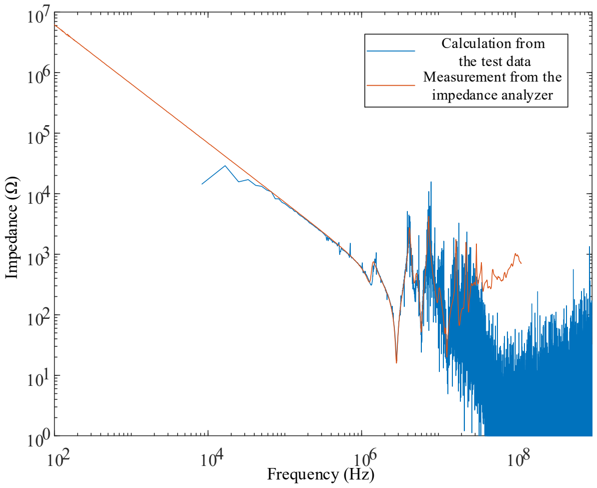


Fig. 3-5 Comparsion between the calculated impedance using DPT setup and measured impedance using impedance analyzer

3.1.4 SUMMARY

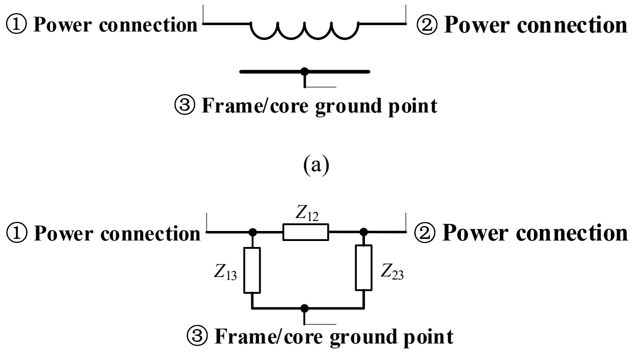
This section is supported by [C1]. It is known that the inductors will be saturated under a large current. However, using a developed impedance measurement method, the common-mode impedance of inductors can be measured with DPT setup, under high-current and -voltage operations. According to experimental results, the common-mode impedance of inductors is stable under different current and voltage.

3.2 BEHAVIOR-BASED MODELING METHOD USING TRANSFER FUNCTIONS

The behavior-based modeling method is usually developed on the measured time-domain or frequency-domain signal. In this section, the behavior-based model of common-mode impedance in inductors is developed, by fitting the measured impedance with transfer functions. According to Section 3.1, the fitted transfer function should work under a wide current and voltage range.

3.2.1 BASIC PRINCIPLE

An MV inductor and its general three-terminal equivalent circuit are shown in Fig. 3-6, where the common-mode impedance is Z_{13} and Z_{23}. Z_{13} and Z_{23} are measured with guarding technology by impedance analyzer Keysight E4990 and its adapter 16047.



(a)

(b)

Fig. 3-6 Equivalent circuit representation of an inductor. (a) Schematic of the inductor with ground connection. (b) General three-terminal equivalent circuit

According to Fig. 3-3, the ground current i_{ground} can be simulated if the excitation v_{out} and the transfer function of impedance Z_{13} is known since $i_{23}(t)$ is approximate to zero. It can be mathematically represented by eq. (3.2). Therefore, only Z_{13} is behaviorally modeled for simulating the ground current.

$$v_{\text{out}}(t) \times \frac{1}{\text{tf}(Z_{13})} = i_{\text{ground}}(t) \tag{3.2}$$

In order to avoid the right-half-plane poles in eq. (3.2), the right-half-plane zeros need to be avoided in tf(Z_{13}). However, in the identification toolbox of Matlab [103], only the right-half-plane poles of a transfer function can be avoided.

Hence, a simple method for avoiding the right-half-plane zeros in tf(Z_{13}) is introduced. Firstly, the measured impedance from the impedance analyzer needs to be converted to admittance. Then, the amplitude, phase, and frequency of the converted admittance need to be imported into the system identification toolbox in Matlab. Then, the fitted frequency range, the number of zeros and poles of the fitted transfer function is configured in the toolbox. Finally, the fitted transfer function is obtained.

Using the system identification toolbox to fit the admittance can avoid the right-half-plane poles in eq. (3.2). If the measured impedance is fitted directly, then the right-half-plane poles will occur in eq. (3.2), which may cause instability during the time-domain simulations.

3.2.2 SIMULATIONS AND EXPERIMENTAL VERIFICATIONS

The medium-voltage inductor used in this section is the same inductor introduced in Section 2.2. Using the system identification toolbox of Matlab, the extracted transfer function is fitted with 32 zeros and 31 poles, where the fitted frequency range is from 500 Hz to 100 MHz, with consideration of the measured noise at low frequency. Fig. 3-7 shows the comparison between the fitted admittance and measured admittance, where a close agreement can be observed.

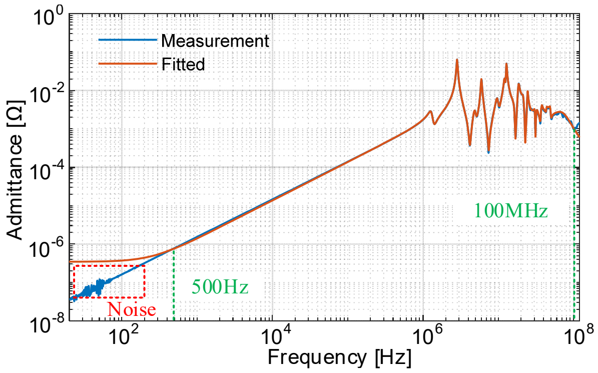
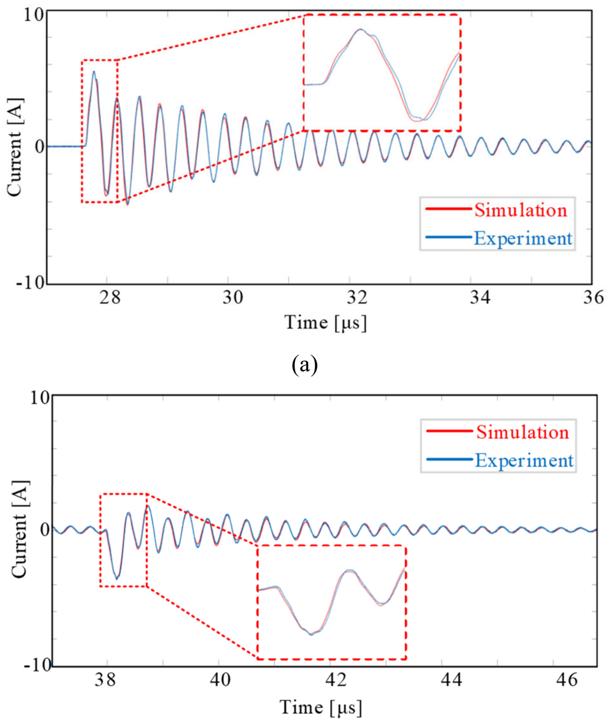


Fig. 3-7 Comparison between the measured and fitted admittance

The measured voltage v_{out}(t) is selected as the voltage excitation to verify the fitted transfer function in the time-domain in Matlab Simulink. According to eq. (3.2), the ground current could be simulated, which are shown in Fig. 3-8.



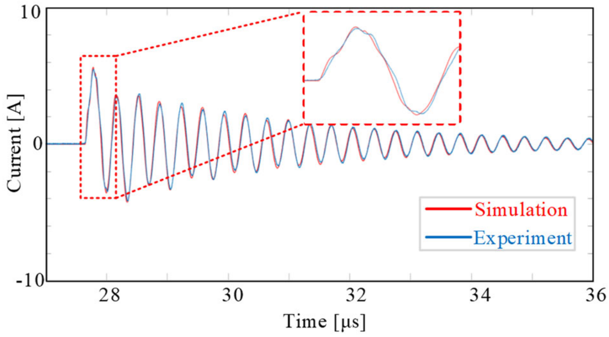
(a)

(b)

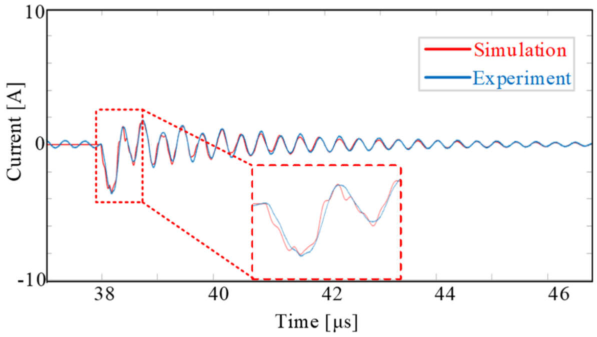
Fig. 3-8 Comparison between the simulation and experiments using the actual measured voltage as the excitation. a) First turn-off transition. b) Second turn-on transition

The ground current is also simulated using a ramp signal. In Fig. 3-9, the ground current is simulated with a ramp signal from 0 V to 3 kV with a slope of 18.8 kV//μs, and 3 kV to 0 V with a slope of 10.8 kV//μs.

Both Fig. 3-8 and Fig. 3-9 show good agreements with the experimental results. However, there is still some difference in the simulations due to the different voltage excitations used in the two simulations, where the ramp signal used in simulations is not exactly same as the actual voltage excitation. Using the measured voltage waveforms as the excitation for the fitted transfer functions can achieve more accurate simulation results.



(a)



(b)

Fig. 3-9 Comparison between the simulation and experiments using a ramp signal as the excitation. a) First turn-off transition. b) Second turn-on transition

3.2.3 SUMMARY

This section is supported by [C2]. The measured admittance of the common-mode couplings in medium-voltage inductors is fitted by transfer functions, where the ground current is simulated in Matlab Simulink. According to the comparisons, the simulated ground current shows good agreement with the experimental measurements.

3.3 BEHAVIOR-BASED MODELING METHOD USING EQUIVALENT CIRCUIT

In this section, a multi-stage equivalent circuit for the common-mode couplings in medium-voltage inductors is proposed. The parameters of the multi-stage equivalent circuit are analytically calculated based on the measured impedance. The derived equivalent circuit is imported to LTSpice, where the ground current of the medium-voltage inductor is simulated using a digital twin of the double-pulse-test setup.

3.3.1 DERIVATION OF THE PROPOSED EQUIVALENT CIRCUIT

It is difficult to import and simulate the transfer functions into LTSpice, especially if the transfer functions have multiple poles and zeros. As a circuit simulator, LTSpice is convenient for simulating circuits. Thus, a method to extract the measured impedance into an equivalent circuit is significant.

The medium-voltage inductor used in this section is the same inductor introduced in Section 2.2, where the terminal A, B, and ground of the medium-voltage inductor is shown in Fig. 3-10. The measured impedance of the capacitive coupling between Terminal A and Ground in the medium-voltage inductor is shown in Fig. 3-11.

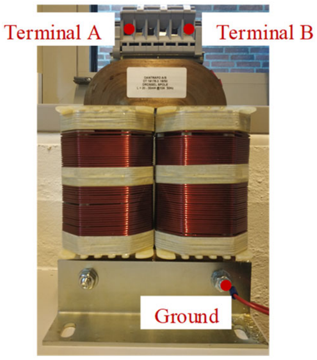


Fig. 3-10 The exampled medium-inductor with labeling terminals and ground

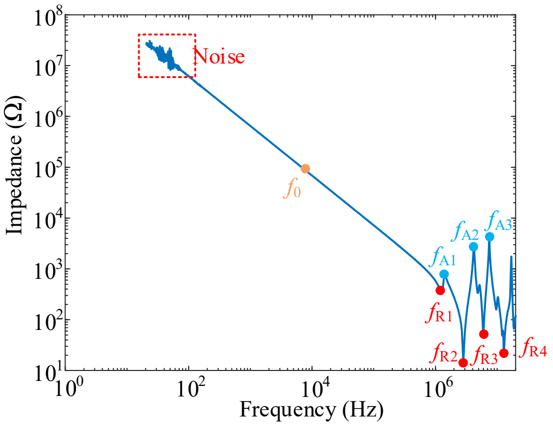


Fig. 3-11 Measured impedance of the capacitive coupling between Terminal A and Ground in the exampled medium-voltage inductor with selected frequencies.

In Fig. 3-11, f_0, f_{A1}-f_{A3}, and f_{R1}-f_{R4} are the selected frequencies, which will be used in the derivations later. f_0 is the frequency of an impedance point corresponding to a low frequency. f_{A1}-f_{A3} are the anti-resonant points, where f_{R1}-f_{R4} are the resonant points [J5].

In previous research [40], an RLC-based equivalent circuit, where the RLC components are in parallel first, and then the sub-circuits are in series, is introduced for characterizing the measured inductive impedance, where the magnitude of impedance keeps increasing at low frequency [J5]. Thus, the previous equivalent circuit cannot characterize the couplings with capacitive impedance before the first resonant frequency.

As shown in Fig. 3-12, an RLC-based equivalent circuit, whose components are in series first and then the sub-circuits are in parallel, is proposed for characterizing the capacitive impedance before the first resonant frequency. The proposed RLC-based equivalent circuit is dual to the equivalent circuit in previous research [J5].

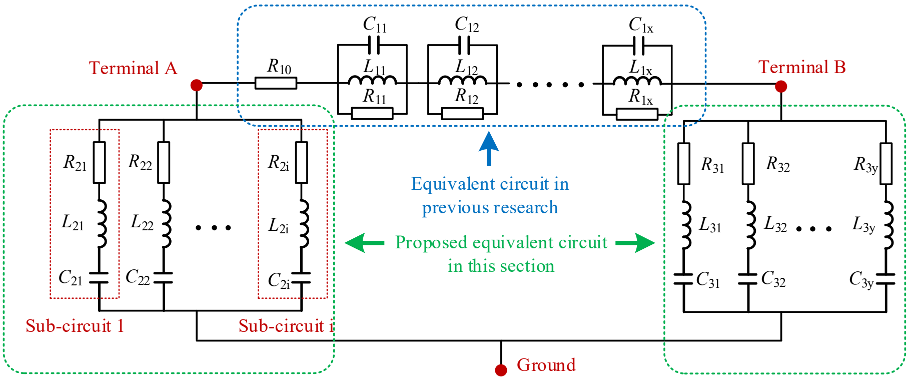

Terminal A
Terminal B
R_{10}
C_{11}
L_{11}
R_{11}
C_{12}
L_{12}
R_{12}
C_{1x}
L_{1x}
R_{1x}
R_{21}
L_{21}
C_{21}
R_{22}
L_{22}
C_{22}
R_{2i}
L_{2i}
C_{2i}
Sub-circuit 1
Sub-circuit i
Equivalent circuit in previous research
Proposed equivalent circuit in this section
R_{31}
L_{31}
C_{31}
R_{32}
L_{32}
C_{32}
R_{3y}
L_{3y}
C_{3y}
Ground

Fig. 3-12 High-frequency RLC-based equivalent circuit of a medium-voltage inductor

A few assumptions are made before analytically deriving the parameters of the proposed equivalent circuit [J5]:

- At low-frequency f_0, the impedance is fully contributed by the capacitance $C_{21} \sim C_{2i}$.
- The resonance at f_{Ri} is only caused by a single series $R_{2i}L_{2i}C_{2i}$ sub-circuit, where the impacts from other sub-circuits are neglected.
- The anti-resonance at f_{Ai} is only caused by the resonance of two sub-circuits $R_{2i}L_{2i}C_{2i}$ and $R_{2i+1}L_{2i+1}C_{2i+1}$, where the impacts from other sub-circuits are neglected.
- Some small resonant points are neglected for simplifying the equivalent circuit.

Clearly, such assumptions will finally lead to errors between the measured impedance and fitted equivalent circuit.

The stage of sub-circuits is equal to the number of resonant points. According to previous assumptions, the equation for the impedance at f_0 is derived.

$$\sum_{n=1}^{\mathrm{i}} C_{2n} = \frac{1}{2\pi f_0 \left|Z(f_0)\right|} \tag{3.3}$$

Then, the inductance of $L_{2\mathrm{i}}$ can be calculated due to the resonance.

$$L_{2\mathrm{i}} = \frac{1}{4\pi^2 f_{\mathrm{Ri}}^2 C_{2\mathrm{i}}} \tag{3.4}$$

$R_{2\mathrm{i}}$ is obtained based on the magnitude of $Z_{R2\mathrm{i}L2\mathrm{i}C2\mathrm{i}}$ on f_{Ri}.

$$R_{2\mathrm{i}} = \left|Z(f_{\mathrm{Ri}})\right| \tag{3.5}$$

According to the assumption, f_{Ai} is ruled by the two neighbor sub-circuits. Thus, f_{Ai} is calculated as (3.6).

$$f_{\mathrm{Ai}} = \frac{1}{2\pi\sqrt{\frac{C_{2\mathrm{i}}C_{2\mathrm{i}+1}}{C_{2\mathrm{i}}+C_{2\mathrm{i}+1}}(L_{2\mathrm{i}}+L_{2\mathrm{i}+1})}} \tag{3.6}$$

Finally, $C_{2\mathrm{i}}$ can be calculated as eq. (3.7) by simplifying eq. (3.6).

$$C_{2\mathrm{i}+1} = C_{2\mathrm{i}} \frac{1-\frac{f_{\mathrm{A1}}^2}{f_{\mathrm{Ri}+1}^2}}{\frac{f_{\mathrm{A1}}^2}{f_{\mathrm{Ri}}^2}-1} \tag{3.7}$$

Thus, using the derived equations eq. (3.3) – eq. (3.7), a four-stage equivalent circuit is calculated for the measured impedance shown in Fig. 3-11. Besides, for comparison, a single-stage equivalent circuit with only considering the resonances at f_{R2} is presented. The calculated parameters of the four-stage and single-stage equivalent circuit are shown in Table 3-II and 3-III.

Table 3-II Calculated parameters of the four-stage equivalent circuit

	i = 1	i = 2	i = 3	i = 4
R	347.2 Ω	15.8 Ω	51.7 Ω	19.9 Ω
L	382.6 μH	31.4 μH	16.7 μH	3.1 μH
C	42.4 pF	100.5 pF	42.9 pF	50.2 pF

Table 3-III Calculated parameters of the single-stage equivalent circuit

	R	*L*	*C*
i = 1	13.6 Ω	14.4 μH	223.1 pF

The impedance of the calculated four-stage and single-stage equivalent circuit is compared with the measured impedance in Fig. 3-13. The impedance of the four-stage equivalent circuit shows better agreement with the measured impedance, where the single-stage equivalent circuit can only fit the most dominant resonance.

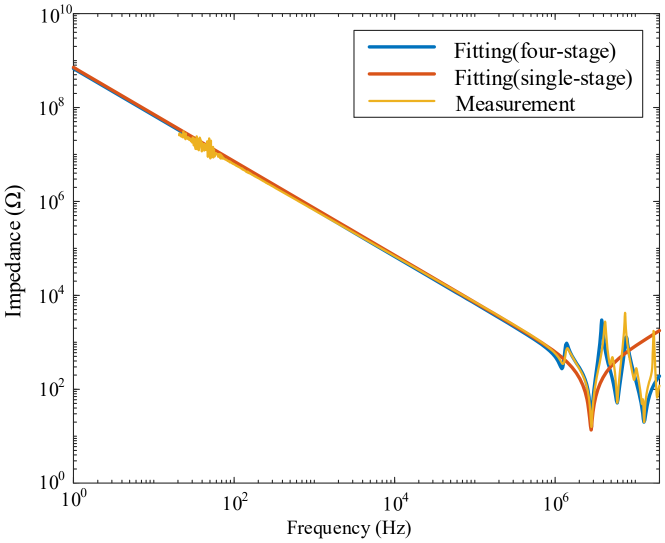


Fig. 3-13 A comparison between the fitted impedance by using the derived equivalent circuits and measurement

3.3.2 DIGITAL-TWIN SIMULATIONS AND EXPERIMENTAL VERIFICATIONS

The derived equivalent circuit of the capacitive couplings in inductors can be imported into LTSpice for system-level simulation. The behavior-based model of 10 kV/20 A behavior-based model of SiC MOSFET half-bridge module is developed in LTSpice [104]. Thus, by combining the behavior-based model of power modules and the developed behavior-based model of inductors, a digital twin of a double-pulse-test setup is built in LTSpice, considering a few extra parasitics introduced by other parasitic of hardware components within the circuit. The schematic of the double-pulse-test setup in LTSpice is shown in Fig. 3-14. Since terminal B of the inductor is clamped to the DC link, the impedance network between terminal B and ground is neglected. The actual coupling between terminal A and B is simplified since the main purpose is to simulate the ground current of medium-voltage inductors [J5].

The simulated ground currents using a four-stage and single-stage equivalent circuit are compared with the measured ground current in Fig. 3-15. The ground current of the inductor during the first turn-off transition is given in Fig. 3-15 (a), where the ground current during the second turn-on transition is shown in Fig. 3-15 (b).

In order to reduce the ground current, three methods are suggested as follows [J5]:

- Improving the geometrical structure of medium-voltage inductors. The ground current can be reduced if the capacitive couplings between the terminals and ground are weaker.
- Using a damping resistance. In Fig. 3-16, a 280 Ω damping resistor is used in series in the ground network of inductors. The digital twin simulation is compared with the experimental measurements, which show good agreements. By using a damping resistance, the ground current is reduced by 40%. However, the voltage potential on the core and frame is still high during the switching transition.
- Swapping the connections of inductors. It is found in previous sections that the coupling between the terminal at the outer layer and ground is smaller than the coupling between the terminal at the inner layer and ground in inductors with multi-layer structure. Therefore, connecting terminal B located at the outer layer of the medium-voltage inductor can result in 66% overshoot voltage reduction. The digital-twin simulation successfully predicts the experimental ground currents, as shown in Fig. 3-17.

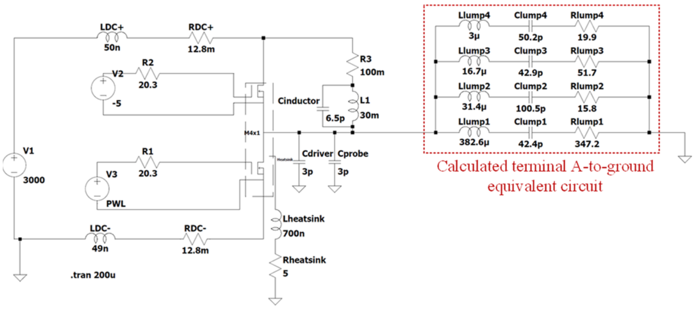
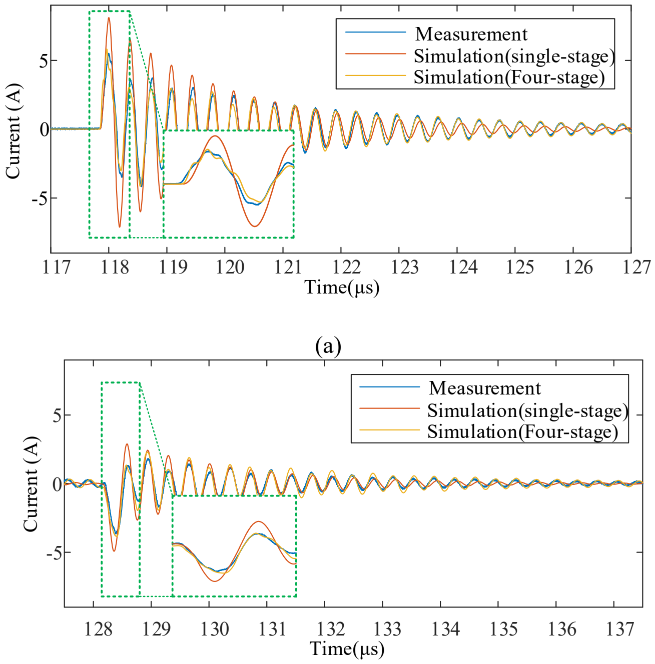

LDC+
50n
RDC+
12.8m
R2
V2
20.3
-5
R3
100m
Cinductor
6.5p
L1
30m
M4x1
V1
3000
R1
V3
20.3
PWL
Heatsink
Cdriver
3p
Cprobe
3p
LDC-
49n
RDC-
12.8m
Lheatsink
700n
Rheatsink
5
.tran 200u
Llump4
3μ
Clump4
50.2p
Rlump4
19.9
Llump3
16.7μ
Clump3
42.9p
Rlump3
51.7
Llump2
31.4μ
Clump2
100.5p
Rlump2
15.8
Llump1
382.6μ
Clump1
42.4p
Rlump1
347.2
Calculated terminal A-to-ground equivalent circuit

Fig. 3-14 Image of digital-twin of the double-pulse-test in LTSpice



(a)

(b)

Fig. 3-15 Measured and simulated ground current according to digital-twin simulation in LTSpice. a) during the first turn-off transition. b) during the second turn-on transition.

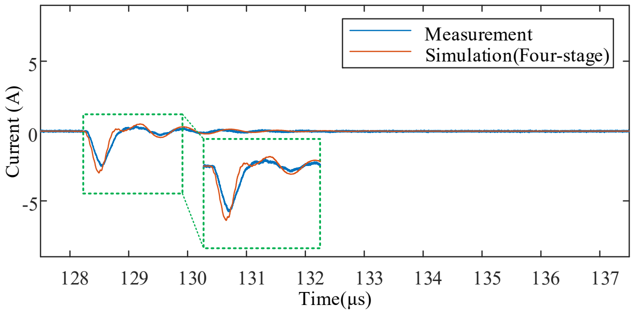


Fig. 3-16 Measured and simulated ground current from the digital-twin simulation in LTSpice using a damping resistance

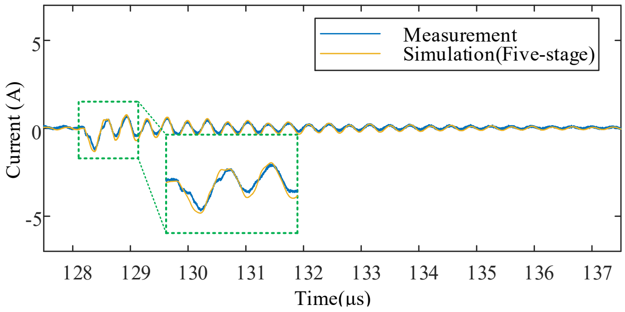


Fig. 3-17 Measured and simulated ground current from the digital-twin simulation in LTSpice swapping the connections of the medium-voltage inductor

3.3.3 SUMMARY

This section is supported by [J5]. A behavior-based modeling method for characterizing the capacitive impedance using a calculated multi-stage equivalent circuit is proposed. The ground current of an exampled medium-voltage inductor is simulated by the developed digital twin of a double-pulse test setup, which shows good agreement with the experimental results.

CHAPTER 4 REDUCING PARASITIC CAPACITANCE IN MV INDUCTORS

> *"The biggest room in the world is the room for improvement."*
> *— Helmut Schmidt*

This chapter introduces several methods for reducing the parasitic capacitance in round-cable-based medium-voltage inductors with multiple windings. Ten case studies of the medium-voltage inductors are presented, where the design-oriented guidelines are summarized.

4.1 CASE STUDIES

Two cases of the conventional design for medium-voltage inductors are illustrated first. Then, eight cases of the improved design for physically reducing the parasitic capacitance of medium-voltage inductors are given.

4.1.1 CONVENTIONAL DESIGN

Case 1 and 2 are the medium-voltage inductors with conventional design. Case 1 is the design where no spacers are applied between two adjacent layers in the inductors [71]. The schematic of the single winding in Case 1 is shown in Fig. 4-1.

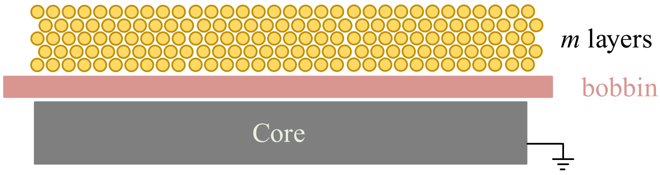


Fig. 4-1 Schematic of Case 1

Only half the schematic of the winding is presented in Fig. 4-1, and the complete structure of a medium-voltage inductor with two windings is shown in Fig. 4-2, where the single winding is symmetrical by the core. The two windings are electrically connected in parallel in conventional design. Two terminals of the inductors are labeled as Terminal 1 and 2, respectively. Case 1 is the most competitive design solution for achieving the highest power density of the windings. However, the strong capacitive couplings between two adjacent layers will contribute to a large parasitic capacitance. Therefore, in previous research [69], bobbins or spacers are inserted between two adjacent layers for reducing the capacitive couplings, as shown in Fig. 4-2 of Case 2.

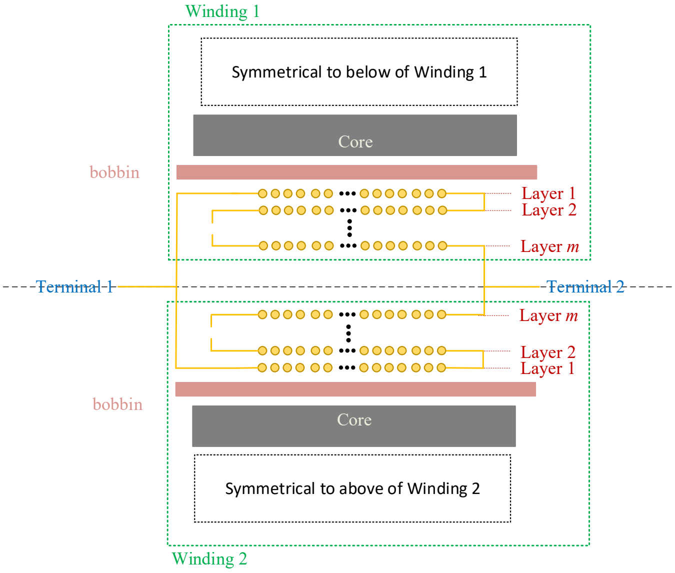

Winding 1
Symmetrical to below of Winding 1
Core
bobbin
Layer 1
Layer 2
Layer *m*
Terminal 1
Terminal 2
Layer *m*
Layer 2
Layer 1
bobbin
Core
Symmetrical to above of Winding 2
Winding 2

Fig. 4-2 Complete schematic of Case 1

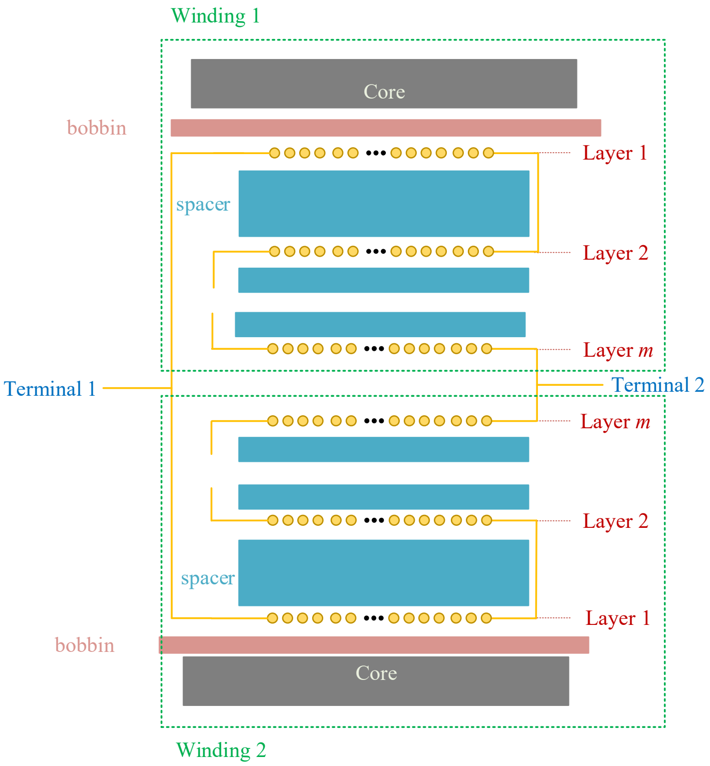

Winding 1
Core
bobbin
spacer
Layer 1
Layer 2
Layer m
Terminal 1
Terminal 2
Layer m
Layer 2
spacer
Layer 1
bobbin
Core
Winding 2

Fig. 4-3 Schematic of Case 2

In Case 2, the stored energy in the electrical field between two adjacent layers is reduced by sacrificing the power density. The thickness of the spacer is determined by the users. In both Case 1 and Case 2, two windings are connected in parallel, where a single winding is constructed by N turns with *m* layers.

4.1.2 IMPROVED DESIGN

In order to further reduce the parasitic capacitance, eight more cases of the inductor design are presented in this sub-section.

The schematic of Case 3 is shown in Fig. 4-4. The electrical connections of the two windings in Case 3 are in series. Thus, by constraining the same inductance and rated current as Case 1 and 2, the diameter of the conductor in Case 3 will become larger than Case 1 and 2. However, only N/2 turns are needed to construct a single winding due to the series connection of the two windings. In Case 3, the terminal at out layer of Winding 1 connects to the outer layer of Winding 2, where both Terminal 1 and 2 located at the inner layer.

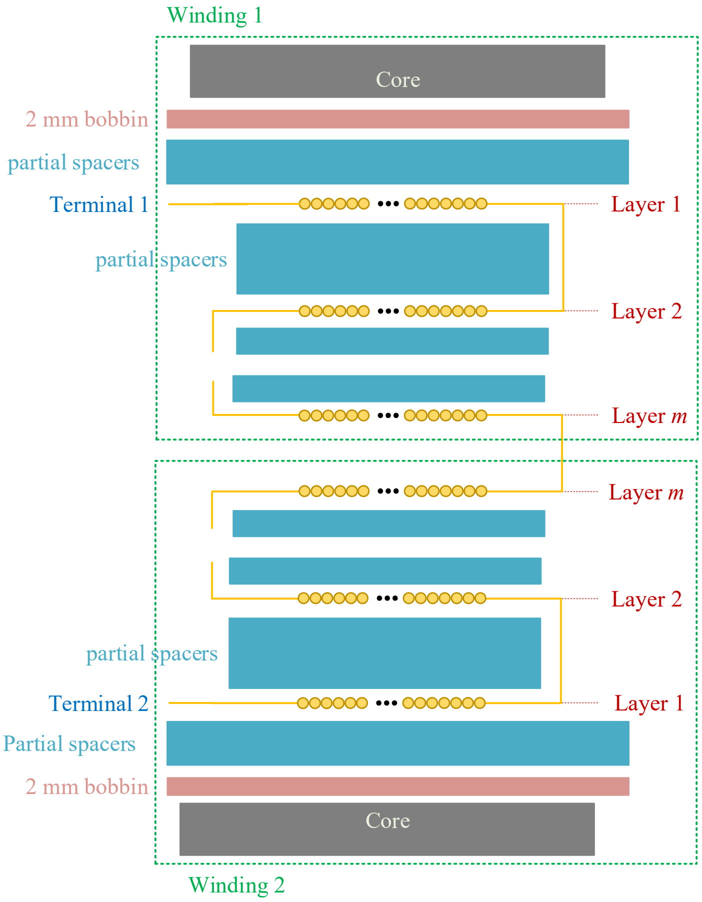

Winding 1
Core
2 mm bobbin
partial spacers
Terminal 1
Layer 1
partial spacers
Layer 2
Layer *m*
Layer *m*
Layer 2
partial spacers
Terminal 2
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-4 Schematic of Case 3

Based on Case 3, a small change is implemented in Case 4, where the schematic of Case 4 is shown in Fig. 4.5. The layout of Winding 1 in Case 4 is the same as Winding 1 in Case 3. However, Terminal 2 is located at the outer layer in Case 4, which is different from Case 3. The electrical field energy stored between the inner layer of winding 2 in Case 4 is smaller than that in Case 3, due to a smaller voltage potential difference between the inner layer and core.

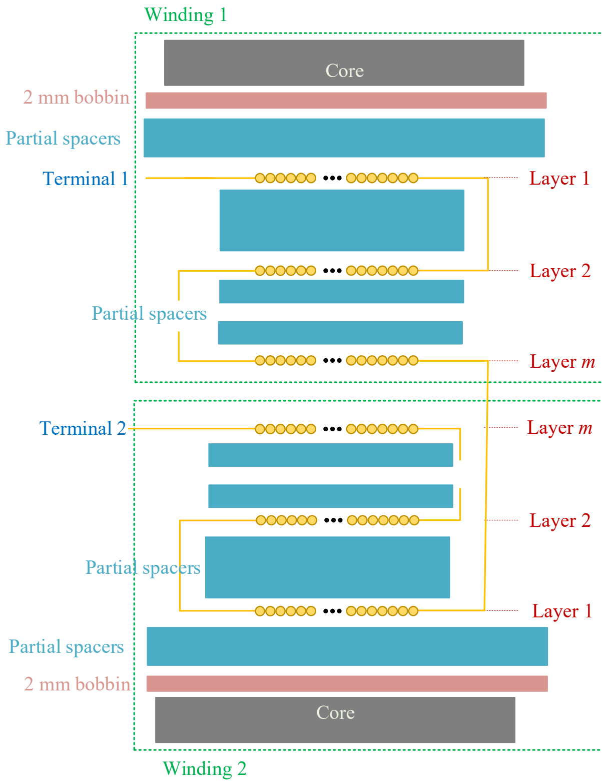

Winding 1
Core
2 mm bobbin
Partial spacers
Terminal 1
Layer 1
Layer 2
Partial spacers
Layer *m*
Terminal 2
Layer *m*
Layer 2
Partial spacers
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-5 Schematic of Case 4

The electrical field energy stored between two adjacent layers is also reduced. In Case 5, the connections between two adjacent layers are changed, as shown in Fig. 4-6. The parasitic capacitance is reduced by decreasing the voltage potential difference between two adjacent layers. The winding layout illustrated in Case 5 will add complexities during the manufacturing process.

Based on Case 5, Case 6 is proposed by splitting a single winding into two subsections, as shown in Fig. 4-7. Compared Case 6 with Case 5, the electrical field energy stored between two adjacent layers is further reduced due to the smaller voltage potential difference, where the dynamic capacitance contributed by adjacent layer is smaller. However, the power density will further decrease and the manufacturing complexity will further increase, with applying the design shown in Case 6.

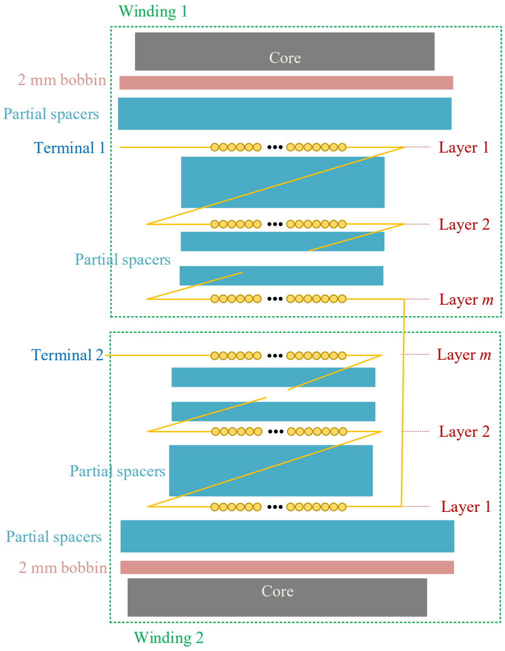

Winding 1
Core
2 mm bobbin
Partial spacers
Terminal 1
Layer 1
Layer 2
Partial spacers
Layer m
Terminal 2
Layer m
Layer 2
Partial spacers
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-6 Schematic of Case 5

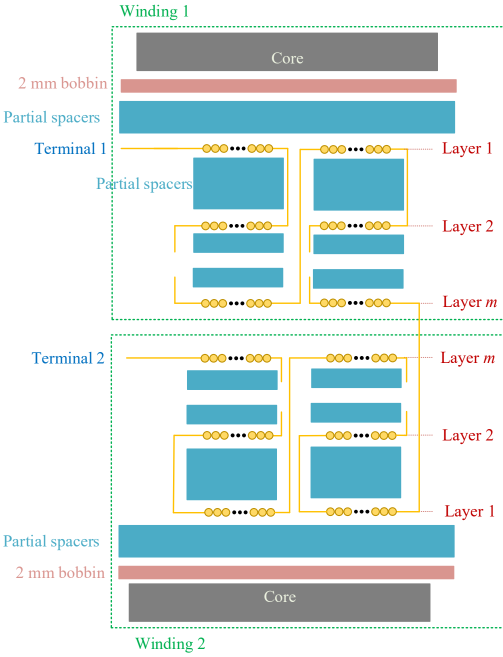

Winding 1
Core
2 mm bobbin
Partial spacers
Terminal 1
Layer 1
Partial spacers
Layer 2
Layer m
Terminal 2
Layer m
Layer 2
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-7 Schematic of Case 6

By combining Case 5 and Case 6, Case 7 is derived. The parasitic capacitance contributed by adjacent layers can be further reduced, however, the manufacturing complexity is further increased.

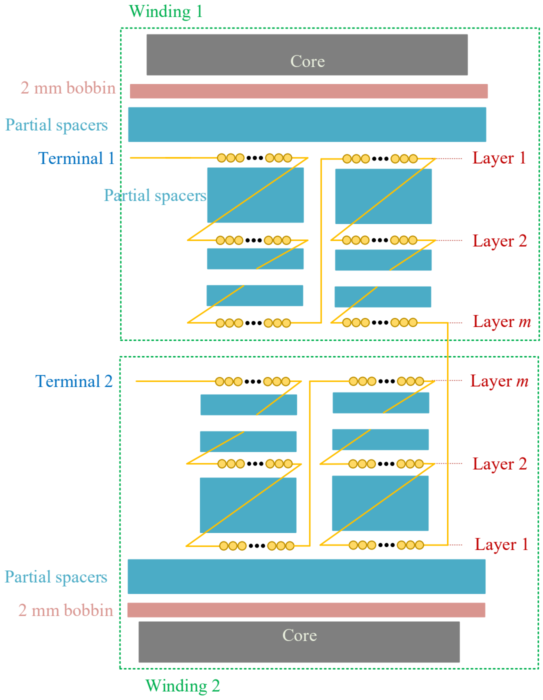

Winding 1
Core
2 mm bobbin
Partial spacers
Terminal 1
Layer 1
Partial spacers
Layer 2
Layer *m*
Terminal 2
Layer *m*
Layer 2
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-8 Schematic of Case 7

The winding can be spilt into more than two sub-sections. The schematic of Case 8 illustrates the winding layout of medium-voltage inductors with three sub-sections, as shown in Fig. 4-8. It is worth mentioning that the capacitive couplings between two subsections can also introduce significant capacitance if the distance between the two adjacent sub-sections is small.

Case 1 – Case 8 have similar geometrical structures in both windings. The geometrical structure of the two windings can also be designed with different parameters with an asymmetrical structure. An example is introduced as Case 9, and the schematic is shown in Fig. 4-10. Using a design like Case 9 can further reduce the equivalent capacitance between Terminal 2 and ground, which results in a smaller ground current when Terminal 2 connects to the output of the power module.

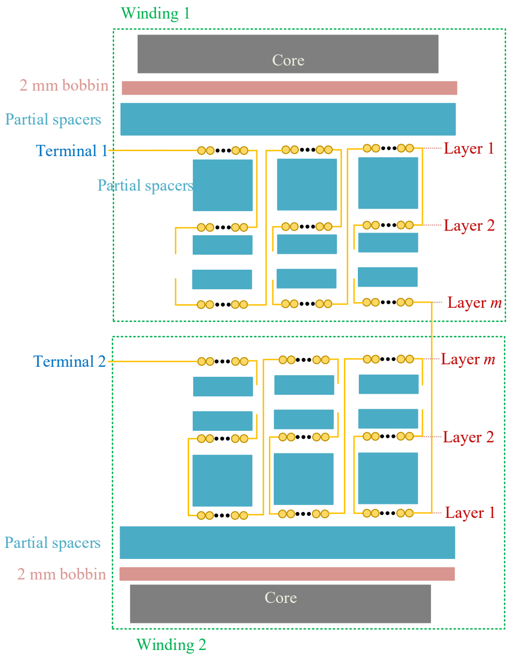

Winding 1
Core
2 mm bobbin
Partial spacers
Terminal 1
Layer 1
Partial spacers
Layer 2
Layer *m*
Terminal 2
Layer *m*
Layer 2
Layer 1
Partial spacers
2 mm bobbin
Core
Winding 2

Fig. 4-9 Schematic of Case 8

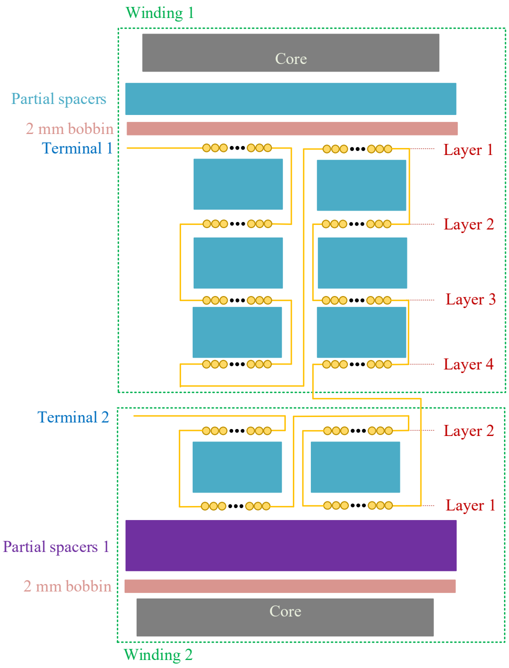

Winding 1
Core
Partial spacers
2 mm bobbin
Terminal 1
Layer 1
Layer 2
Layer 3
Layer 4
Terminal 2
Layer 2
Layer 1
Partial spacers 1
2 mm bobbin
Core
Winding 2

Fig. 4-10 Schematic of Case 9

Case 1-9 presented the design of medium-voltage inductors with two windings. The design of Case 1-9 can be extended to the medium-voltage inductors with more than two windings. As an example, Case 6 is extended to a medium-voltage inductor with three windings structure, and the schematic is shown as Case 10 in Fig. 4-11. The three winding are electrically connected in series [P1].

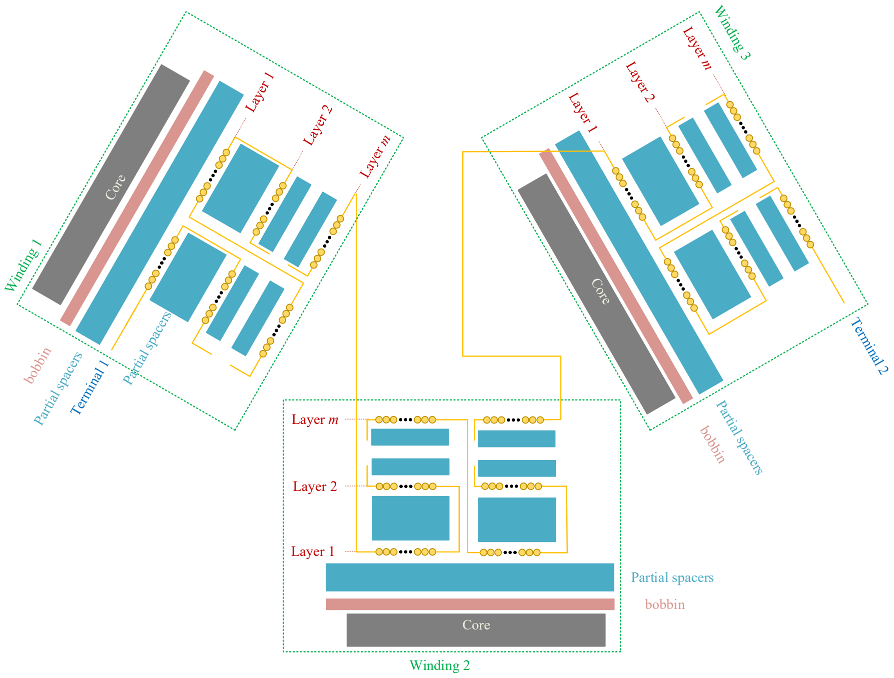

Core
Winding 1
bobbin
Partial spacers
Terminal 1
Partial spacers
Layer 1
Layer 2
Layer *m*
Winding 3
Layer *m*
Layer 2
Layer 1
Core
Terminal 2
Partial spacers
bobbin
Layer *m*
Layer 2
Layer 1
Partial spacers
bobbin
Core
Winding 2

Fig. 4-11 Schematic of Case 10

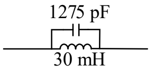
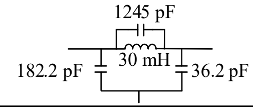
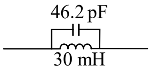
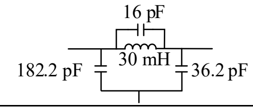
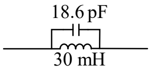
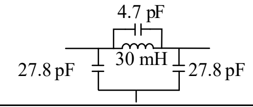
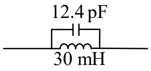
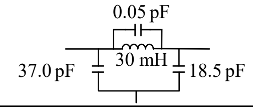
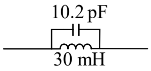
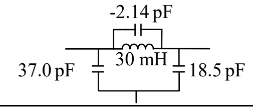
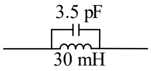
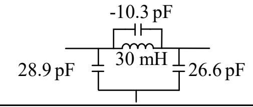
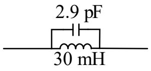
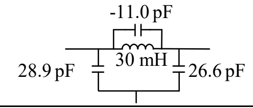
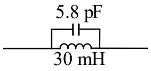
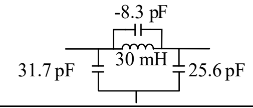
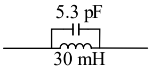
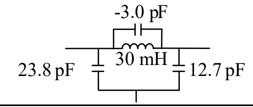
4.1.3 CALCULATIONS AND VERIFICATION

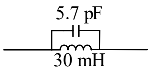
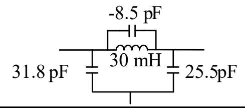
Using a few assumptions for simplifying the calculations, the parasitic capacitance of Case 1-10 is obtained whether the core/frame is grounded or floating.

- The parasitic capacitance contributed by the electrical fringe field is not considered.
- The parasitic capacitance contributed by the electrical field between two adjacent sub-sections is not considered, where the distance between the two sub-sections is assumed to be large enough.
- The parasitic capacitance contributed by the electrical field between two windings is not considered, where the distance between the two windings is assumed to be large enough.

There are no partial spacers applied in Case 1. The thickness of spacers between inner layer and core used in Case 2 and 4 is 6 mm, where the thickness of spacers between inner layer and core used in Case 3-10 is 12 mm. The diameter of the conductor of the round cable is 1.4 mm in Case 1 and 2. To ensure the same current rating in Case 3-10, the diameter of the cable is 2 mm. The medium-voltage inductor is designed with three layers and two windings. The key geometrical parameters used for calculating are the same as the parameters listed in Table 2-II. The calculations of Case 1-10 are summarized in Table 4-I.

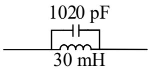
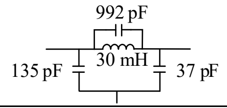
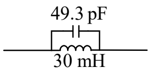
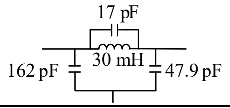
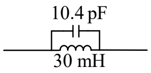
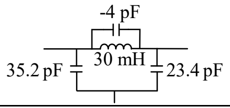
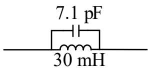
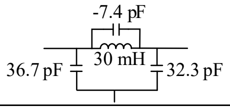
Table 4-I Calculations of Case 1-10 shown in this chapter

Case	Core/Frame floating	Core/Frame grounding
Case 1	 1275 pF 30 mH	 1245 pF 30 mH 182.2 pF 36.2 pF
Case 2		 16 pF 30 mH 182.2 pF 36.2 pF
Case 3		 4.7 pF 30 mH 27.8 pF 27.8 pF
Case 4		 0.05 pF 30 mH 37.0 pF 18.5 pF
Case 5		 -2.14 pF 30 mH 37.0 pF 18.5 pF
Case 6		 -10.3 pF 30 mH 28.9 pF 26.6 pF
Case 7		 -11.0 pF 30 mH 28.9 pF 26.6 pF
Case 8		 -8.3 pF 30 mH 31.7 pF 25.6 pF
Case 9		 -3.0 pF 30 mH 23.8 pF 12.7 pF

Case 10		 -8.5 pF 31.8 pF 30 mH 25.5pF

Four prototypes are manufactured according to the design of Case 1, Case 2, Case4, and Case 6. The parasitic capacitances of the four prototypes are measured with the impedance analyzer Keysight E4990A, which are listed in Table 4-II.

Table 4-II Measurements of four-cases shown in this chapter

Case in this patent	Core/Frame floating (Two-terminal circuit)	Core/Frame grounding (Three-terminal circuit)
Case 1	 1020 pF 30 mH	 992 pF 135 pF 30 mH 37 pF
Case 2		 17 pF 162 pF 30 mH 47.9 pF
Case 4		 -4 pF 35.2 pF 30 mH 23.4 pF
Case 6		 -7.4 pF 36.7 pF 30 mH 32.3 pF

According to Table 4-I and -II, the improved designs can significantly reduce the parasitic capacitances in medium-voltage inductors with grounding or floating core/fame, which is however, by sacrificing the power density and increasing the manufacturing complexity. It is still very difficult to judge which solution is the most cost-efficient. The main purpose of this sub-section is to show multiple possibilities for reducing the parasitic capacitance in medium-voltage inductors.

4.2 DESIGN-ORIENTED GUIDELINES

A few design-oriented guidelines are summarized in this subsection. Generally, three methods can be implemented for reducing the parasitic capacitance in medium-voltage inductors.

- Firstly, the parasitic capacitance in medium-voltage inductors can be reduced by improving the geometrical structure, e.g., adding a spacer with a larger thickness between two adjacent layers, which is simple and easy to implement for decreasing the capacitive couplings.
- Secondly, the material of spacers, bobbins, and insulation can be selected with lower permittivity, which can contribute to smaller stored electrical-field energy with the same geometrical structure of inductors.
- Thirdly, for medium-voltage inductors with multiple windings, it is recommended to electrically connect the windings in series, which can significantly reduce the parasitic capacitance but probably increase the AC and DC resistance.
- Fourthly, splitting the winding into multiple sub-sections is also helpful for reducing the parasitic capacitance of medium-voltage inductors. However, this may also lead to extra manufacturing complexities and reduced power density of the inductors.

4.3 SUMMARY

This chapter is supported by [P1]. Two cases of the conventional design for medium-voltage inductors are illustrated first. Then, eight cases of the improved design for physically reducing the parasitic capacitance of medium-voltage inductors are given in this sub-section. According to calculations and experimental measurements, the proposed improved design successfully reduces the parasitic capacitance. A few design-oriented guidelines are introduced in this sub-section.

CHAPTER 5. CONCLUSIONS AND PROSPECTS

"Yesterday is but today's memory, and tomorrow is today's dream.

— Khalil Gibran

5.1 CONCLUSIONS

This Ph.D. thesis has presented a comprehensive study on both physics-based and behavior-based modeling methods, as well as the approaches of reducing parasitic capacitance in medium-voltage filter inductors.

The major conclusions are summarized as follows.

For physics-based modeling method:

- The proper and improper assumptions applied in previous modeling methods are classified. It is found that the lumped-capacitor-network method fails to predict the equivalent parasitic capacitance at the first resonant frequency, and the energy-conservation-based modeling methods are encouraged to be used.
- The previous energy-conservation-based modeling method is applied in medium-voltage inductors with grounded core/frame, where the three individual equivalent capacitances at the first resonant frequency are analytically calculated. The measurement methods for experimentally characterizing the three parasitic capacitance in three-terminal medium-voltage inductors are also introduced.
- The physics-based modeling method of parasitic capacitance in copper-foiled medium-voltage inductors is proposed, considering the effects of the electrical fringe field, which is important for modeling the parasitic capacitances in copper-foiled medium-voltage inductors.
- The previous energy-conservation-based modeling method requires the knowledge of the floating core voltage potential prior to modeling. An improved modeling method, without knowing the floating core voltage

potential is proposed, which shows the scalabilities for applying in transformers, or other magnetic devices with multiple terminals.

For behavior-based modeling method:

- The behavior-based modeling methods to identify the couplings between terminals and core/frame of medium-voltage inductors are developed, either using transfer functions or multi-stage RLC circuits. The derived behavior-based model can be imported into LTSpice for system-level digital-twin simulations.

For reducing methods of parasitic capacitance in medium-voltage inductors:

- Multiple solutions are proposed as case studies for reducing the parasitic capacitance in medium-voltage inductors. Calculations and measurements of prototypes verified the effectiveness of the proposed solutions. Design-oriented guidelines are provided according to the case studies.

5.2 PROSPECTS

Based on the results of the Ph.D. project, some reminded challenges that are worthy of being investigated in the future are summarized as follows.

For physics-based modeling method:

- The current energy-conservation-based modeling method is only valid up to the first resonant frequency of inductors. The performance of the inductor after the first resonant frequency is not predictable due to the restrictions raised by the assumptions:
    1) The assumption about linear voltage potential distribution across the winding. Due to the self-resonance behaviors of the inductor, the voltage potential distribution will be non-linear after the first resonant frequency. Thus, it is a great challenge to analytically calculate the actual voltage potential distribution, as well as stored electrical-field energy after the first resonant frequency.
    2) The assumption about "perfect conductor" for the core. In this Ph.D. thesis, as well as previous research, the voltage potential on core is assumed to be of a constant value without any voltage drops. At higher frequency, the eddy-current or ground current may result in voltage drops on the core, where this assumption can introduce significant errors to the calculated results.
    3) The skin effects and proximity effects are not considered in this Ph.D. thesis. At higher frequency, these two effects can change the field

distribution, as well as the stored electrical field energy. In other words, these two effects will influence the calculated equivalent capacitance at high frequency.

Predicting the behaviors after the first resonant frequency of inductors might be extremely difficult. Therefore, it might be better first to investigate them in multi-physics FEM simulations, considering the material behaviors in terms of frequency.

- Only the equivalent parasitic capacitance at the first resonant frequency is considered in this thesis. However, damping resistance and main inductance will contribute to the magnitude and frequency at the first resonant point but not be physically modeled in this thesis. In future work, a more comprehensive system-level modeling is desired for characterizing the performance of inductors at or even beyond the first resonant frequency.
- This Ph.D. thesis is mainly focused on modeling the parasitic capacitances in three-terminal inductors, where the core/frames of the inductors are grounded. Theoretically, the proposed physics-based modeling method can be applied to transformers but not experimentally proven in this thesis.

For behavior-based modeling method:

- There is still some difference between the impedance of the calculated equivalent circuit and measurement, which will finally result in a mismatch in time-domain digital-twin simulations. The possible enhancement method for increasing the fitting accuracy of the multi-stage equivalent circuit, might be possible by applying fewer assumptions. The machine learning algorithms may also be applied to obtain the accurate parameters of the multi-stage RLC circuits.
- The behavior-based modeling method is still dependent on the measurement results, which requires the physical inductors to be manufactured first. In the future, the multi-physics FEM simulations can be applied for simulating the behaviors after the first resonant frequency, which can be the inputs for the proposed behavior-based modeling method. Thus, the behavior-based modeling method can be extended into a completely digitalized modeling method for inductors.

For the reducing approaches of parasitic capacitance in inductors:

- The proposed solutions are aimed at inductors, and the methods for reducing the parasitic capacitance in transformers are not presented.
- The introduced design-oriented guidelines are still relatively general and is primarily focused on reducing the parasitic capacitance without optimizing the magnetics. A more comprehensive design framework could be investigated by considering the complete inductor design, such as the

geometrical structures, material selections, winding layout, and thermal behaviors as well as cost.

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APPENDED PUBLICATIONS

[J1] Hongbo Zhao et al., “Proper and Improper Assumptions in Modeling Parasitic Capacitance of Inductors,” ***IEEE Transactions on Power Electronics***, submitted.

[J2] Hongbo Zhao et al., “Physics-based Modeling of Parasitic Capacitance in Medium-Voltage Filter Inductors,” ***IEEE Transactions on Power Electronics***, vol. 36, no. 1, pp. 829 – 843, Jan. 2021.

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