Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems

A Comparative Review

Khan, Noman; Forouzesh, Mojtaba; Siwakoti, Yam; Li, Li; Kerekes, Tamas; Blaabjerg, Frede

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***Abstract*—** In Photovoltaic (PV) applications, a transformer is often used to provide galvanic isolation and voltage ratio transformations between input and output. However, these conventional iron and copper-based transformers increase the weight/size and cost of the inverter whilst reducing the efficiency and power density. It is therefore desirable to avoid using transformers in the inverter. However, additional care must be taken to avoid safety hazards such as ground fault currents and leakage currents, e.g. via the parasitic capacitor between the PV panel and ground. Consequently, the grid connected transformerless PV inverters must comply with strict safety standards such as IEEE 1547.1, VDE0126-1-1, EN 50106, IEC61727, and AS/NZS 5033.

Various transformerless inverters have been proposed recently to eliminate the leakage current using different techniques such as decoupling the DC from AC side and/or clamping the common mode (CM) voltage during the freewheeling period, or using common ground configurations. The permutations and combinations of various decoupling techniques with integrated voltage buck-boost for maximum power point tracking (MPPT) allow numerous new topologies and configurations, which are often confusing and difficult to follow to select the right topology. Therefore, to present a clear picture on the development of transformerless inverters for the next generation grid-connected PV systems, this paper aims to comprehensively review and classify various transformerless inverters with detailed analytical comparisons. To reinforce the findings and comparisons as well as to give more insight on the CM characteristics and leakage current, computer simulations of major transformerless inverter topologies has been performed in PLECS software. Moreover, the cost and size are analysed properly and summarized in a table. Finally, efficiency and thermal analysis are provided with a general summary as well as technology roadmap.

***Index Terms*—** Photovoltaic (PV) system, transformerless inverter, grid-connected inverter, common-mode voltage (CMV), leakage current, AC-decoupling, DC-decoupling.

I. INTRODUCTION

Solar photovoltaic (PV) is one of the cleanest, readily and widely available energy sources among all renewable energies [1]. With the technological advancement in material and manufacturing techniques, the cost of PV system is continuously reduced, making it the cheapest energy source for future massive deployment. Many countries (USA, Germany, China, Japan, Australia, France, Italy, Spain, etc.) have already begun to reap the benefits through their increased adoption and integration to the utility grid. According to the annual report from International Energy Agency-Photovoltaic Power Systems Program (IEA-PVPS) [2], the global installed PV capacity reached 100 GW milestone in 2012, and 200 GW level in 2015. By the end of 2017, the total installed PV capacity is estimated to be roughly 410 GW, while 24 IEA-PVPS countries reached 264 GW [2]. Fig. 1 shows the cumulative installed PV capacity of the top IEA-PVPS countries from 2012 to 2017. From this figure, it

is evident that the PV industry is facing rapid growth, in which five leading countries are representing 90.1% of all PV installations in 2017. Among them, China, USA, and Japan experienced the largest PV installations increment in recent years.

Among all PV installations, the percentage of off-grid PV systems is very low [3]. The grid-connected PV systems need power inverters as an interface between the PV panel and the grid, which are generally categorized as the galvanic isolated inverter and non-isolated inverter. In the isolated type, usually a high-frequency DC side transformer or a low-frequency AC side transformer is used to achieve galvanic isolation, which enhances the system safety. Due to their lower cost, size/weight, and higher efficiency, transformerless inverters are of much interest for the low to medium power residential market [4-8].

Fig. 2 illustrates a general layout for a single-phase transformerless inverter for small-scale PV systems. As it can be seen, without a galvanic isolation, a direct ground-current path can be formed between the PV panel and the grid. Due to the presence of large stray capacitance (C_{PV}) between the PV and grid grounds, the varying voltage (also known as common-mode (CM) voltage) can excite resonant circuit formed by the parasitic capacitor and inverter filter inductor, which produces high CM ground current i_{cm}. This capacitive i_{cm} comprises line low-frequency and switching high-frequency components, which injects harmonics into the grid current, increases the system losses, impairs electromagnetic compatibility, and may also cause safety problems such as electric shock [9]-[15].

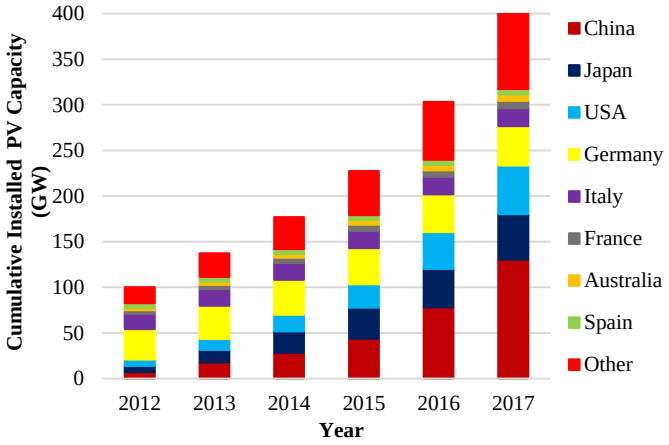


Fig. 1. Cumulative PV installations for the top IEA-PVPS countries from 2012 to 2017 [2].

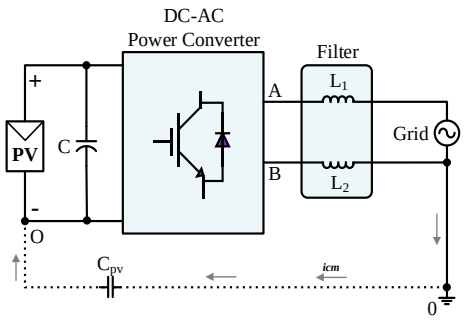


Fig. 2. The general layout of a single-phase transformerless inverter using an L-filter.

In order to understand the grid-connected PV systems to satisfy various grid codes and their safety standards, numerous inverter related issues have been thoroughly investigated [16]-[28]. So far, many transformerless inverter topologies have been

presented with the aim to eliminate the leakage current. To achieve that, various decoupling techniques have been adopted, such as, decoupling the DC from AC side [29]-[36] and/or clamping the common mode voltage (CMV) during the freewheeling period [9], [10], and [37]-[41], or using common ground configurations [5], [12], [16], and [42]-[45]. The combinations of these decoupling techniques with integrated MPPT circuits form an immense number of topologies and configurations, which are often confusing and difficult to follow. Therefore, to present a clear picture on the development of the transformerless inverter for the next generation grid-connected PV systems, this paper aims to review and classify various transformerless inverters. Further, it aims to provide an analytical overview and analysis of well-known single-phase transformerless inverter topologies as well as comparing the transformerless inverters based on the loss and efficiency analysis through detailed calculations. This categorisation and analysis can help researchers to understand the advantages and disadvantages of various transformerless inverter topologies in terms of their CMV and leakage current behaviour.

The rest of this paper is organized as follows. The main grid requirements and problems related to transformerless PV inverters are discussed in Section II. A broad classification of different single-phase transformerless inverter topologies is presented in Section III including simulation results of CM voltage and current using PLECS software. In Section IV, loss and efficiency calculations are presented for some of the major transformerless inverter topologies and the results are finally summarised and concluded in Section V.

II. REQUIREMENTS AND ISSUES OF TRANSFORMERLESS PV INVERTERS

Grid-connected PV systems need special attention in order to satisfy grid codes and standards. Hence, international agencies have regulated some broadly accepted standards for PV systems, which are required in end to avoid safety issues. The major culprit behind these safety issues and concerns is the presence of the ground capacitance C_{PV} between the PV cells/panel and the ground as illustrated in Fig. 3. PV panels are comprised of the combination of glass, Ethylene-Vinyl Acetate (EVA), back sheet (Tedlar), and aluminium frame, in which C_{PV} is created from the PV cell to the frame, to the rack, and the ground. Moreover, in the transformerless PV inverter, a CM resonant circuit can be created between the parasitic capacitor of PV module and output filter inductors at the grid side, which can cause severe problems such as high ground current i_{cm} and its subsequent problems [7], [46]. Furthermore, the output filter, which forms a resonant circuit with the power switching circuit, has a major role in ground leakage current. This is very important to understand the CM behaviour of the transformerless system. The following sub-sections provide a brief explanation on the CM behaviour of the circuit and its ground leakage current, followed by different grid codes as well as safety requirements.

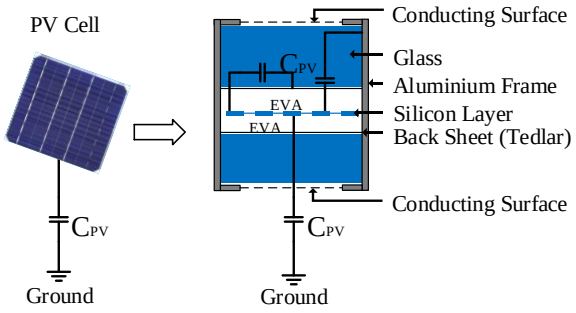


Fig. 3. Parasitic capacitance in PV panels [46].

A. Common-Mode Resonant Circuit and Leakage Current Issues

The amplitude and spectrum of leakage current depend mainly on the converter circuit topology, modulation strategy and the resonant circuit formed by the ground capacitor, the converter, the output AC filter and the grid. Fig. 4(a) shows the CM equivalent circuit of the inverter, which comprises the converter, filter inductors (L_1, L_2), and parasitic capacitor (C_{pv}). The power circuit in Fig. 4(a) can be replaced with phase voltages of the inverter V_{AO} and V_{BO}, which are equal to the potential of A and B points relative to the neural point O (see Fig. 4(b)) [29], and [47]-[48]. The CMV and differential-mode voltage (DMV) can be written based on the phase voltages as follows:

$$V_{cm} = \frac{V_{AO} + V_{BO}}{2} \tag{1}$$

$$V_{DM} = V_{AO} - V_{BO} \tag{2}$$

Moreover, the phase voltages can be expressed based on V_{cm} and V_{DM} as mentioned in (3) and (4).

$$V_{AO} = V_{cm} + \frac{V_{DM}}{2} \tag{3}$$

$$V_{BO} = V_{cm} - \frac{V_{DM}}{2} \tag{4}$$

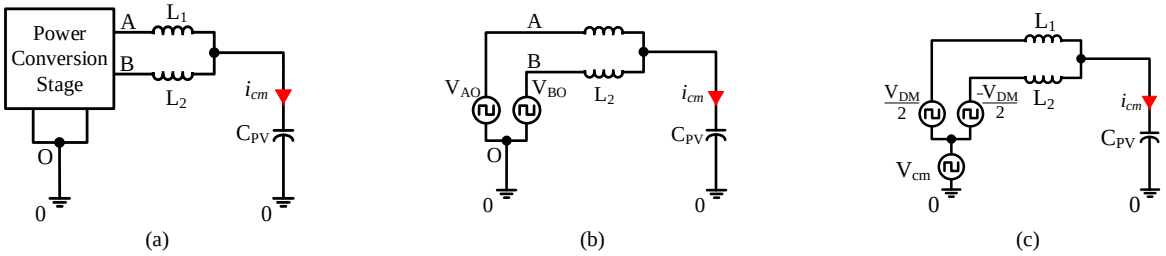


Fig. 4. CM model showing (a) the resonant circuit, and (b) the resonant circuit including V_{AO} and V_{BO}.

To better understand the CM behaviour, the equivalent circuit can be simplified into a single loop circuit as shown in Fig. 5(a). The equivalent CMV (V_{ECM}) shown in this figure can be obtained as

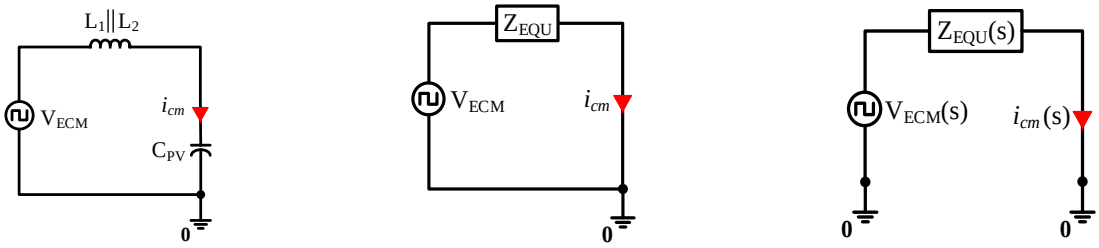
$$V_{ECM} = V_{cm} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2} \tag{5}$$

The magnitude of i_{cm} depends mainly on the amount of parasitic capacitance and the amplitude and frequency of the CMV, whose fluctuation can produce a large i_{cm}. To avoid the leakage current i_{cm}, (5) should be equal to zero, which is dependent on the circuit topology. Moreover, the equivalent CMV has to remain constant in each switching period in order to reduce i_{cm}. The effect of DMV can be eliminated in symmetrical topologies like H-bridge inverter by using two identical

inductor filter at the output (i.e., $L_1 = L_2$) [29], and [47]-[49]. The simplified equivalent CM circuit including the equivalent impedance (Z_{EQU}) is shown in Fig. 5(b). This circuit can be demonstrated in the *s*-domain to analyse the frequency and magnitude of the created resonant circuit (see Fig. 5(c)) [10]. Letting $L_1 = L_2$ in (5) for the topologies with a symmetrical structure (e.g. H-bridge), the equivalent CMV can be replaced with V_{cm}. The transfer function from i_{cm} to CMV created by the converter through the resonant circuit can be expressed as (7).

$$V_{ECM}(s) - \left(Ls + \frac{1}{sC_{PV}}\right) i_{cm}(s) = 0 \tag{6}$$

$$H(s) = \frac{i_{cm}(s)}{V_{ECM}(s)} = \frac{s}{Ls^2 + \frac{1}{C_{PV}}} \tag{7}$$



(a) (b) (c)

Fig. 5. Simplified single loop CM model, (a) considering the series connection of components, (b) the equivalent impedance circuit, and (c) the *s*-domain equivalent circuit.

In (6) and (7), $L = (L_1 L_2)/(L_1 + L_2)$. Fig. 6 illustrates the Bode plot of the transfer function in (7) considering $L_1 = L_2$ =3 mH and C_{PV} =75 nF.

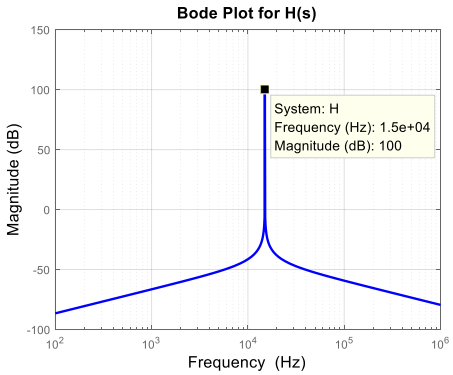


Fig. 6. Bode plot of the resonant circuit model in Fig. 5.

It is evident that the resonant frequency equals 15 kHz. Moreover, as the filter inductor and parasitic capacitor forms a typical LC resonant circuit, its resonant frequency can be calculated theoretically from (8). Both the simulation and analytical results show the same resonant frequency, with which a large CM current i_{cm} flows into the system.

$$f_r = \frac{1}{2\pi\sqrt{LC_{PV}}} = 15005 \text{ Hz} \tag{8}$$

Without a galvanic isolation, the potential between the PV array and the ground (V_{ECM}) fluctuates, which charges and discharges the parasitic capacitor (C_{pv}). This fluctuating CMV activates the resonant circuit as discussed above and may lead to higher ground leakage current. However, the resonant frequency is not fixed, as it depends on the parasitic capacitance

together with the DC lines that connects the PV array to the inverter. It also depends on the size of the PV array and the environmental conditions. All these conditions make the elimination of leakage current more difficult in practice [50].

B. Grid Requirements and Standards

Grid-connected PV systems should comply with different standards that are regulated internationally and by each country. In this subsection, a brief overview on different grid codes is given for grid-connected PV systems, while a more detailed study can be found in [51]. Table I illustrates important required grid codes regulated by major countries and associations.

TABLE I
GRID CONNECTED PV SYSTEM STANDARDS AND GRID CODES [17]-[24], [28], [52]-[54].

Standard No.	Publication Origin	THD	DC Current Injected	Grid Frequency (f_g) Range (Hz)	Power Factor
IEEE 1547 [17]	USA (IEEE)	Less than 5%	<0.5% of rated output current	57 ~ 60.5	0.9 to 0.97
IEEE 929-2000 [20]	USA (IEEE)	Less than 5%	<0.5% of rated output current	59.3 ~ 60.5	> 0.85
IEC 61727 [28]	Swiss (IEC)	Less than 5%	< 1% of rated output current	49 ~ 51	> 0.90
AS4777 [52]-[54]	Australia	Less than 5%	0.5% of rated output current per phase	48 ~ 52	0.8 to 0.95
EN 61000-3-2 [22]	England	Less than 5%	< 0.22A corresponding to a 50 W half-wave rectifier	47.5 ~ 50.2	NA
EREC G83 [21]	England	Less than 5%	0.25 % of AC current rating per phase	49 ~ 51	0.95
VDE 4105 [18]	Germany	Less than 5%	< 1 A; max. trip time 0.2 s	47.5 ~ 51.5	0.89 to 0.95
BDEW [23]	Germany	Less than 5%	NA	47.5 ~ 51.5 (-5% ~ +3%)	0.95
GB/T 19964-2012 [24]	China	Less than 5%	< 1% of rated output current	48-50.5	0.95
JEAC 9701-2012 [25]	Japan	Less than 5%	NA	47.5 ~ 51.5 (Eastern Japan) 57 ~ 61.8 (Western Japan)	0.9 to 0.95

When a PV panel is connected to the grid, different parameters need to be taken care of to have acceptable performance. The major ones are as follows: total harmonic distortion (THD), injected DC current, grid frequency (f_g) range, power factor and i_{cm} range. In most PV standards, the maximum allowable THD of the output current is limited to 5% which is the reason for having improved power quality at distribution feeders. On the other hand, the amounts of injected DC current to PV system is invariably limited to be within 0.22% - 1% of the rated output current. This current is difficult to measure precisely with the existing inverter circuits. The range of grid frequency is mentioned in Table I for different standards. However, the standard frequency range may fluctuate more for different abnormal conditions [17]-[25], [27].

TABLE II
LEAKAGE CURRENT WITH DISCONTINUITY TIME IN VDE 0126-1-1.

Leakage Current (mA)	Fault Discontinuity time (ms)
30	300
60	150
100	40

VDE 0126-1-1 specifies the acceptable range of i_{cm} that should not be more than 100 mA when the fault discontinuity time is not more than 40 ms [55]-[56] as shown in Table II. Grid-connected systems must follow active and passive anti-islanding requirements due to the fluctuating voltage and frequency range according to IEEE 929-2000, IEEE-1547, VDE-AR-N 4105, and IEC 61727 standards [17]-[19], and [27] and most of the standards follow a limit of voltage variations between 3% and 5% [19]-[21], [25]. On the other hand, voltage fluctuation must be kept within ±5% for standard IEEE 1547 [17].

III. CLASSIFICATION OF SINGLE-PHASE TRANSFORMERLESS INVERTER TOPOLOGIES

Voltage source inverters (VSIs) are favourable for PV applications due to cost, efficiency, and size over current source inverters (CSIs), and numerous voltage source single-phase transformerless topologies have been proposed and developed for

grid-connected PV systems to improve the performance and compatibility to grid codes [5], [7], [9], [12], [14], [15], [29], and [31]-[72]. Fig. 7 illustrates a classification of some of the important topologies in two major sub-groups based on the requirement for the DC-link voltage to achieve 240 Vac with 50 Hz grid frequency, i.e., DC link voltage ($2\times V_{PV}$) and DC link voltage (V_{PV}) based single-phase transformerless inverters. Moreover, the single-input group can be categorized into five subgroups, based on i_{cm} suppression, decoupling and voltage clamping, i.e., common ground, H-bridge, H6, and buck-boost type topologies.

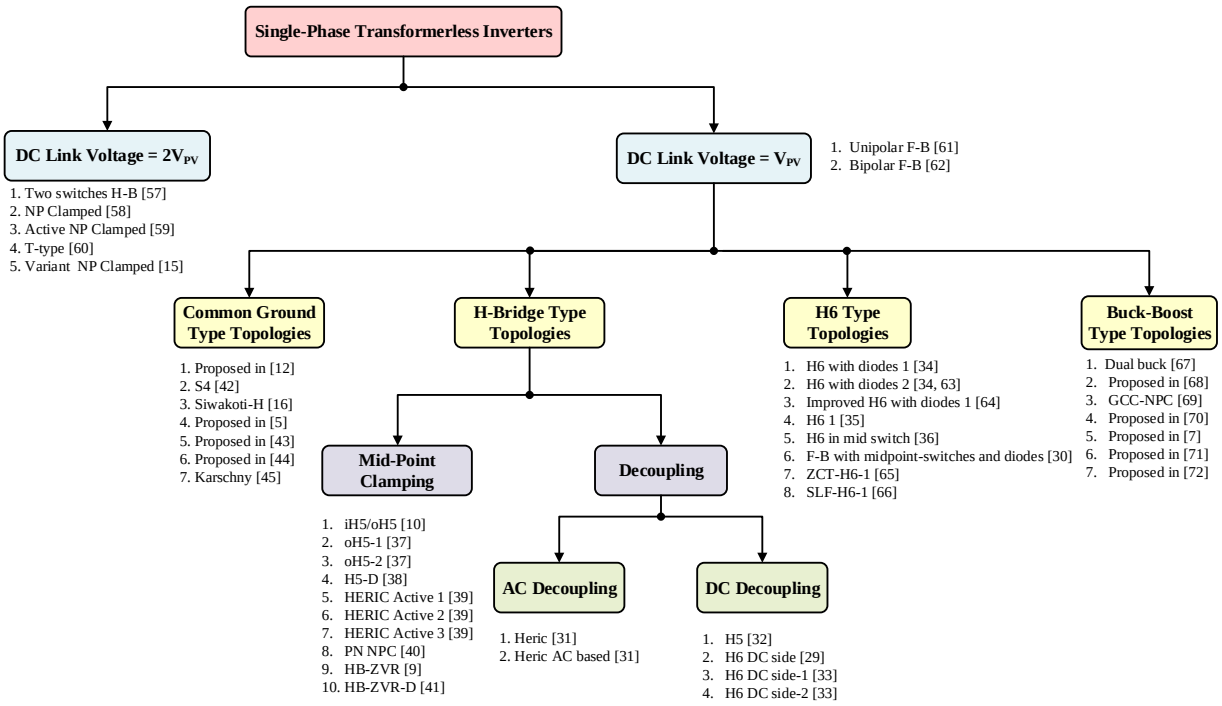


Fig. 7. Classification of single-phase transformerless inverter topologies used in PV systems according to DC-link voltage.

TABLE III
PARAMETERS USED FOR SIMULATIONS AND COMPARISONS.

Parameter	Value
Input Voltage (V_{pv})	400 V_{DC}
Output Load	32 Ω
Output Voltage (V_g)	240 V_{ac}
Line Frequency (f_g)	50 Hz
Output Current (i_o)	7.35 A
Modulation Index (M)	0.82
Rated Power	1800 kVA
Switching Frequency (f_{sw})	20 kHz
DC Bus Capacitor ($C = 2\times C_1$) & ($C_1 = C_2$)	1600 µF
Flying Capacitor (C_F)	470 µF
Flying Inductor (L_m)	0.3 mH
Filter Capacitor (C_o)	2.2 µF
Filter Inductor (L_1, L_2)	3 mH
Parasitic Capacitor (C_{pv1}, C_{pv2})	75 nF
Switches (IKW30N60DTP)	V_{CE} = 600 V, I_C = 30 A
Diodes (APT15D60B)	V_F = 600 V, I_F = 32 A

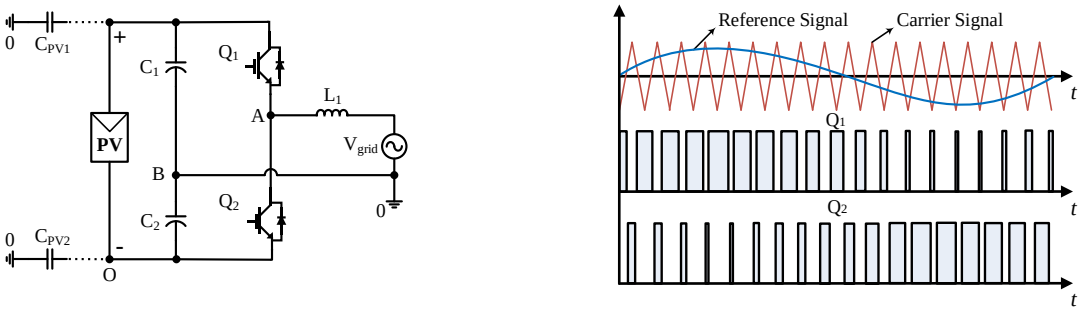
To shed more light on each topology considering the leakage current and CMV, the following sections provide analysis and simulation of some major topologies illustrating the key waveforms and CMV behaviour. Table III shows the parameters and values used for the simulations performed in this section and to benchmark the topologies. The voltage and current levels for the selected switches and diodes are 600 V and ~30 A, respectively. Moreover, all the components are chosen such that the

best performance can be achieved. The inverters are operated for 1.8 kVA where the input voltage is selected as 400 V_{DC} to obtain 230 V_{ac} and the output current is achieved as ~ 7.35 A (RMS) [9], [35], [39], and [41].

A. Double Input Voltage ($2V_{PV}$) Type Single-Phase Transformerless Inverter Topologies

In this section, five single-inductor based transformerless inverters are introduced, where either L_1 = 0 or L_2 = 0 and the parasitic capacitance is 75 nF. The operational modes of each topology is discussed, as well as switching pulses and the output current describing the CM effect.

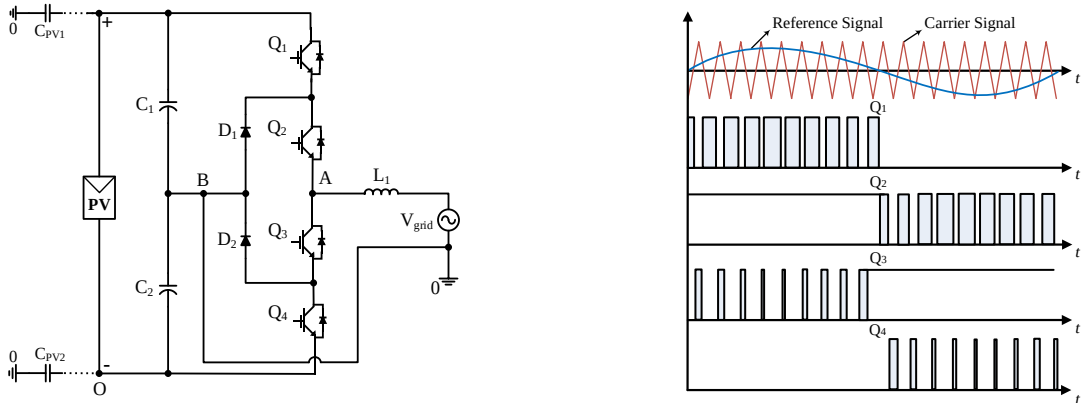
Two-switch based half-bridge (H-B) inverter works by alternatively switching pulses as shown in Fig. 8 (b), and the input voltage operates by charging and discharging the DC link capacitors (C_1 and C_2) (see Fig. 8 (a)) [73], which are shown to be more difficult to achieve the maximum power point of PV panel. Hence, the output current ripple is increased. To simplify the control system and improve the efficiency and current ripple, compared to two-switch based H-B [74], and [75], a new topology was introduced by A. Nabae, et al in 1981 [58] called the neutral point clamped (NPC), which is also well known for minimizing the cost and size of the filter. This topology operates with three voltage levels [76], and [77]. The zero voltage stage can be achieved by the clamping technique through the clamp diodes of the midpoint, which is shown by the schematic diagram (see Fig. 9 (a)), and the modulation pulses are illustrated in Fig. 9 (b). However, the main negative part of this topology is unbalanced conduction losses and a restricted DC link balance [78], which affects the whole system.



(a) (b)

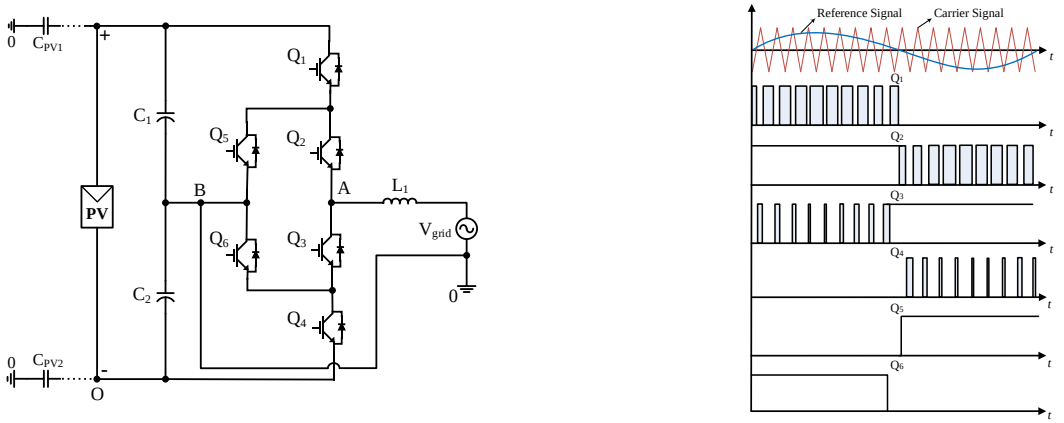
Fig. 8. Illustration of (a) two switches H-B inverter, and (b) its switching pulses.

The active NPC (ANPC) is illustrated in Fig. 10 (a) which is modified from the conventional NPC topologies [44], [79], and [80] and mitigates the limitation of NPC topology. In this topology, two switches Q_5 and Q_6 are used to replace D_1 and D_2 diodes of the NPC. The upper clamping occurs when tuning on the switches Q_2 and Q_5, whereas the lower clamped works when Q_3 and Q_6 are operated [77]. After replacing the diodes with switches, the conduction losses can be controlled [54]. Fig. 10 (b) demonstrates the six switching pulses.



(a) (b)

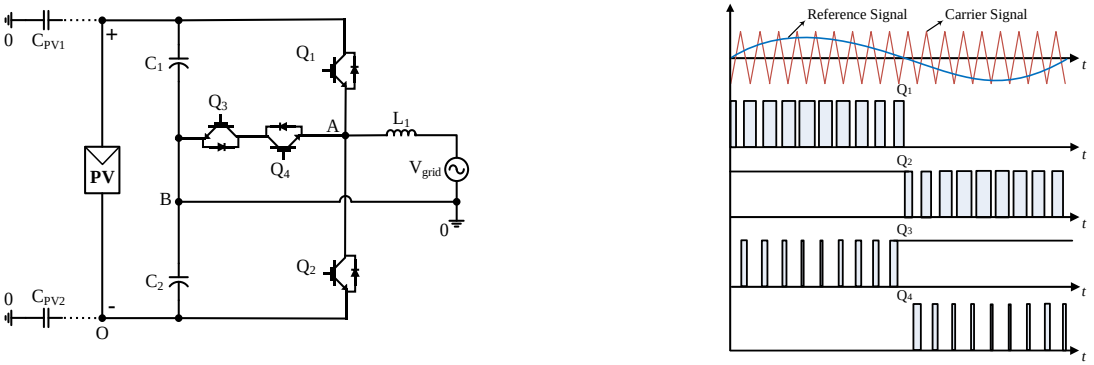
Fig. 9. Illustration of (a) NPC H-B inverter, and (b) its switching pulses.



(a) (b)

Fig. 10. Illustration of (a) ANPC H-B, and (b) its switching pulses.

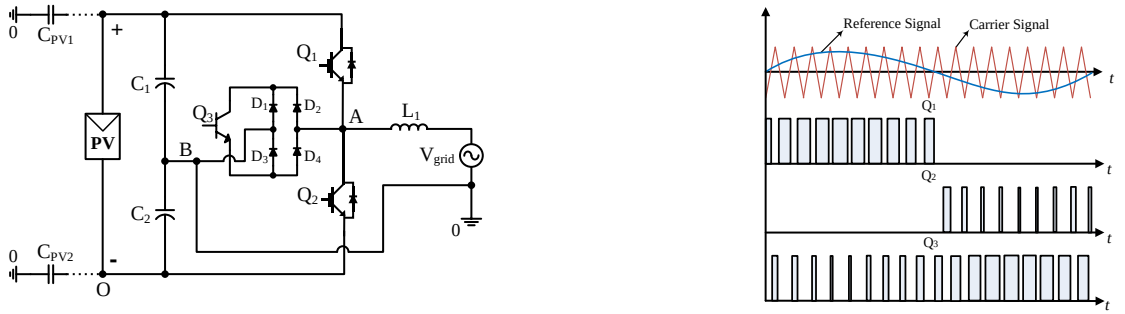
To reduce more conduction losses, the transistor (T)-type shown in Fig.11 (a) is a good solution with bidirectional switches which are inserted between the middle points of the DC-link capacitors and Q_1-Q_2 branch [78], [81], and [82]. The switching pulses are presented in Fig. 11 (b) showing that the switches Q_1 and Q_3 work in complement with switches Q_2 and Q_4 accordingly [83]. Moreover, the switching combination of the four switches are different where the midpoint clamping switches (Q_3 and Q_4) are selected for low switching losses and low forward voltage drops [78].



(a) (b)

Fig. 11. Illustration of (a) T-type H-B inverter, and (b) its switching pulses

The T-type, NPC and ANPC topologies are also well known in five-level inverters for improving the power quality and reducing the complexity in high power applications [84]-[87]. It can help to obtain a high conversion efficiency with low switching losses [87]- [89].



(a) (b)

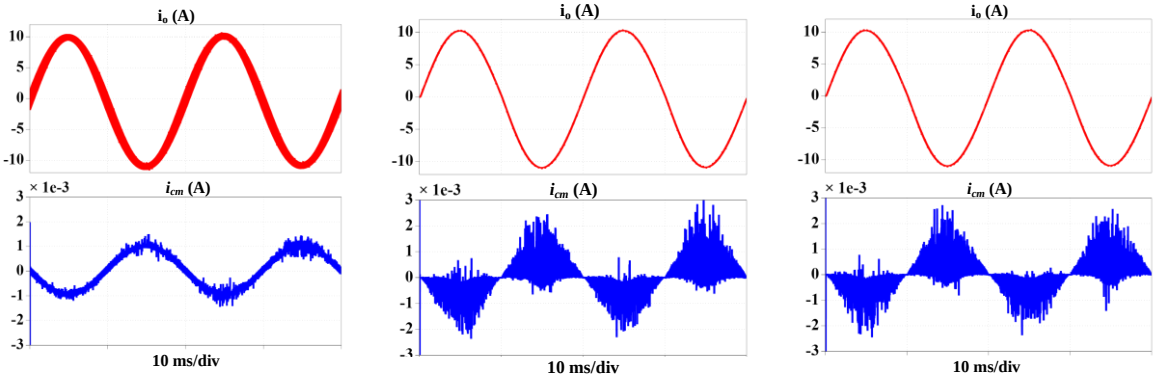
Fig. 12. Illustration of (a) three-switch H-B inverter, and (b) its switching pulses.

A variant of the NPC is introduced in Fig. 12(a) [15] to reduce the number of switches of NPC/ANPC topologies. This topology uses a diode bridge with a bidirectional switch Q_3. The diodes are used for providing a current path during the null states, and the concept of a bidirectional switch is taken from Conergy topology [83] by combining two bidirectional switches to one. The variant NPC topology operates in four operational modes. In the positive half cycle, only Q_1 is in ON condition, whereas in the negative half cycle, Q_2 is ON. In the freewheeling time of the positive half cycle, D_1 and D_4 are in forward bias mode with the switch Q_3; and in the negative cycle, the other two switches D_2 and D_3 are ON with the switch Q_3 [50]. Fig. 12(b) shows different switching pulses of the variant NPC.

TABLE IV
SUMMARY OF THE DOUBLE INPUT VOLTAGE TYPE TRANSFORMERLESS INVERTERS.

Topology name	Semiconductor Devices				i_{cm} (mA)	Passive Filter Component		Voltage Level
	IGBTs		Diodes					
	No.	Voltage	No.	Voltage		No. of Inductor (L)	No. of Capacitor (C)	
Two-Switches based	2	$1.5\times V_{pv}$	0	---	≤ 2	1	0	2
NPC	4	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 3.5	1	0	3
ANPC	6	$1.5\times V_{pv}$	0	---	≤ 2.5	1	0	3
T-type	4	$1.5\times V_{pv}$	0	---	≤ 4	1	0	3
Variant NPC	3	$1.5\times V_{pv}$	4	$1.5\times V_{pv}$	≤ 4.2	1	0	3

The simulation results of the above topologies are shown in Fig 13 (a) to Fig. 13(e) where the input voltage is selected as $2\times V_{PV}$, and L_1=3 mH. Table IV indicates the overall summary of the double-input voltage transformerless inverter topologies.



(a) (b) (c)

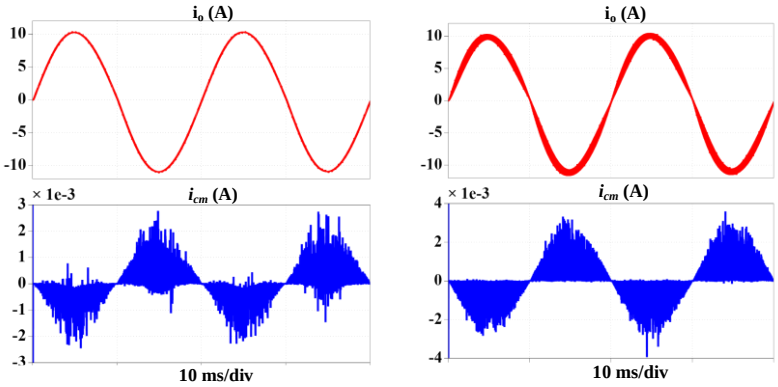
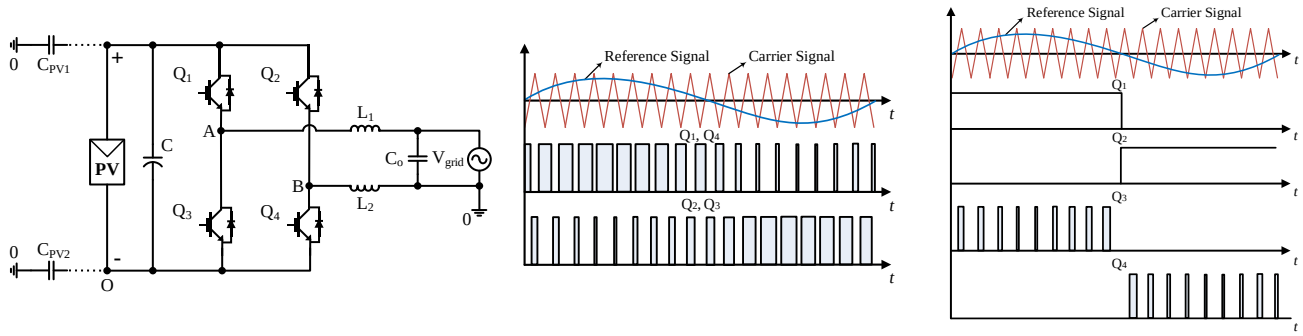


Fig. 13. Simulation results of (a) two-switch H-B inverter, (b) NPC inverter, (c) ANPC inverter, (d) T-type inverter and (e) variant NPC inverter.

B. Single-Input Voltage (V_{PV}) Type Single-Phase Transformerless Inverter Topologies

Full-bridge (FB) single-phase transformerless inverter topologies with both bipolar and unipolar switching pattern [61] are explained in this section. Conventional FB inverter with a bipolar configuration has been used for achieving constant CMV, and low i_{cm}. However, the loss increases which leads to a reduced system efficiency [90]. Hence, unipolar has been introduced for overcoming the efficiency issue [62]. In this section, bipolar and unipolar based FB inverters are shown in details and with the appropriate wave forms. Furthermore, the other single-input transformerless inverters are categorized in Fig. 7 and discussed with the simulated waveforms of i_{cm}, output voltage/current, CMV and the voltage of neutral (O) to points A and B. Table IV tabulates the parameter values used for the simulations.



(a) (b) (c)

Fig. 14. Illustration of (a) Full Bridge inverter, (b) its bipolar switching pulses, and (c) its unipolar switching pulses.

Fig.14 (a) illustrates the circuit configuration of the F-B transformerless inverter topology with the parasitic capacitors on both sides of the PV panel. Bipolar switching pattern is used as shown in Fig. 14 (b). Switches Q_1 and Q_4 are turned ON for the positive half cycle, and the output current flows through the antiparallel diode of Q_2 and Q_4 to the load. On the other hand, Fig. 14 (c) shows the switching modulation for unipolar operation. In this modulation scheme, Q_2 is complimentary to Q_1, and Q_3 complimentary to Q_4. For the positive half cycle, Q_1 and Q_4 are ON, and hence, the output voltage is equal to the input voltage. During the freewheeling period, the output current flows through Q_1 and antiparallel diode of Q_2 for the positive half cycle; and for the negative half cycle, the output current flows through Q_3 and antiparallel diode of Q_4.

The output voltage and current of the bipolar FB inverter are shown in Fig. 15 (a). The CM current is low and the CMV is constant. However, the output current ripple is high, which increase the size of the output filter. Moreover, the energy conversion efficiency is decreased significantly. On the other hand, the leakage current is very high when an FB inverter is

operated for unipolar switching pattern due to the occurrence of active and zero state in every pulse width modulation (PWM) cycle. Hence, the CMV varies from 200 V to 400 V with the switching frequency (see Fig. 15 (b)). However, the energy conversion efficiency is increased compared to the bipolar modulation due to the reduced output ripple and optimized freewheeling path of the unipolar PWM strategy.

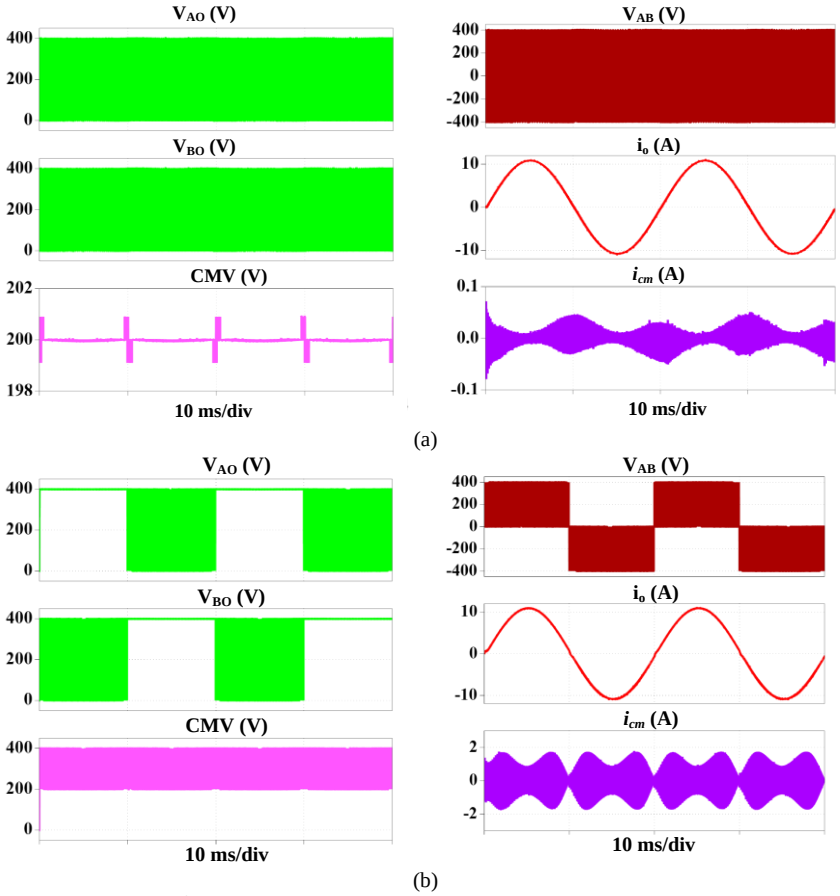


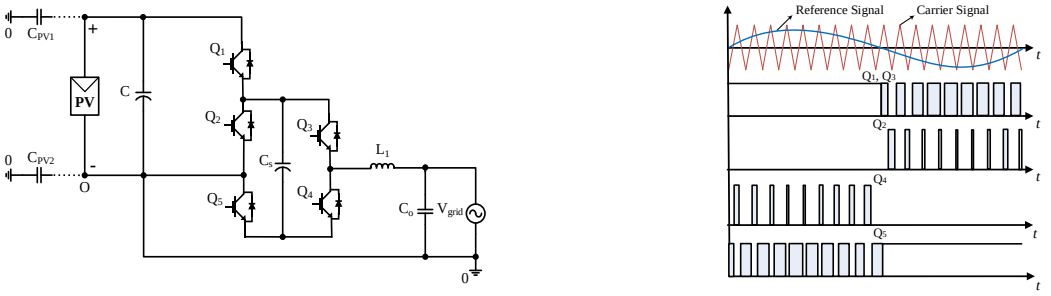
Fig. 15. Simulation results of F-B inverter with (a) bipolar switching pulses, and (b) unipolar switching pulses.

1) Common Ground Type Topologies

The topology where the negative polarity of the PV panel is directly connected with the grid is called common ground type topology, such as, S4 [42], Siwakoti-H [16], and those in [12], [5], [44]. The significant advantage of such kind of topologies is the constant CMV and the elimination of i_{cm}.

a) Inverter Topology in [12]

The topology presented in [12] is the concept of a virtual DC bus. The purpose of this technique is to generate the negative output voltage, which is necessary for the operation as an inverter. Hence, the grid neutral line (O) is directly connected with the negative pole of the PV panel, and therefore, the parasitic capacitors (C_{pv1} and C_{pv2}) are clamped to the zero potential of the neutral, theoretically resulting in zero i_{cm}. The circuit structure is given in Fig. 16 (a) with the modulating switching pulses in Fig. 16 (b). During the positive half cycle, the switches Q_1 and Q_3 are always ON, and Q_2 is always OFF. In the negative half cycle, Q_5 is always ON, and Q_4 is always OFF. The main challenging part of this topology is to control the virtual DC bus capacitor (C_s) along with the real bus in every switching frequency (f_{sw}).

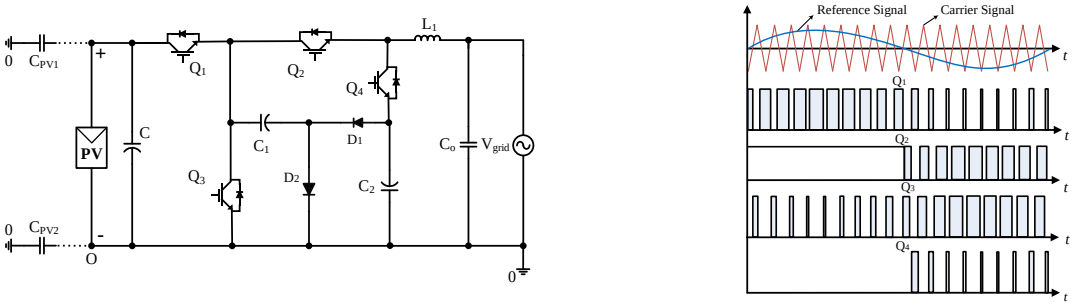


(a) (b)

Fig. 16. Illustration of (a) inverter topology in [11], and (b) its switching pulses.

b) S4 Topology

The S4 topology is demonstrated in [42], [91] as shown in Fig. 17 (a). To operate the inverter, sinusoidal PWM (SPWM) is used to minimize the switching losses and to reduce the filter requirement, as shown in Fig. 17 (b). During the positive half cycle, the switches Q_1 and Q_3 are ON with the switching frequency to produce positive and zero voltage, while Q_2 is OFF in the whole period. Hence, the output voltage of $+V_{DC}$ is achieved. In this period, the diode D_1 is OFF while the capacitor C_1 is charging with D_2. On the other hand, the voltage across the capacitor C_2 is constant as like the switched capacitor characteristic. To generate the negative voltage for the utility grid, the capacitor C_2 is charged by the capacitor C_1 with negative polarities up to $-V_{DC}$. However, the two-stage charge transfer process (V_{in} to C_1 and C_1 to C_2) increases the number of power components and also the losses in the system.

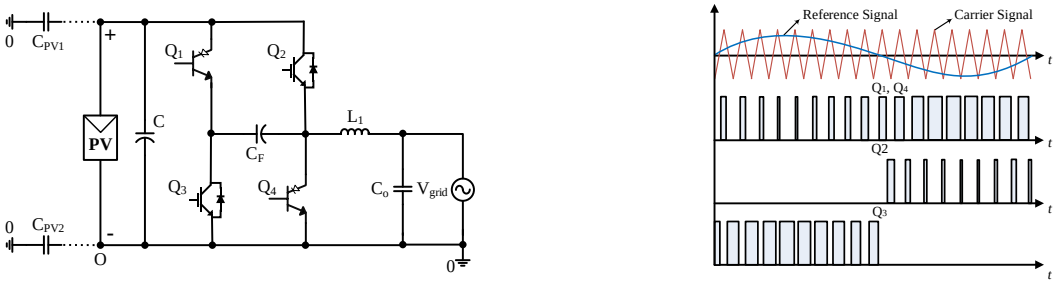


(a) (b)

Fig. 17. Illustration of (a) S4 inverter, and (b) its switching pulses [42].

c) Siwakoti-H

The number of semiconductor components is significantly reduced in the topology proposed in [16], where only four switches are used. Constructed like an H-bridge shown in Fig. 18 (a), the inverter uses a flying capacitor to create a negative bus voltage for the inverter during the negative cycle. Fig. 18 (b) illustrates the switching pulses. The switches (Q_1 and Q_4) experience bipolar voltage stress, which is equal to $\pm V_{DC}$. Thus, bipolar voltage blocking capability switches such as the



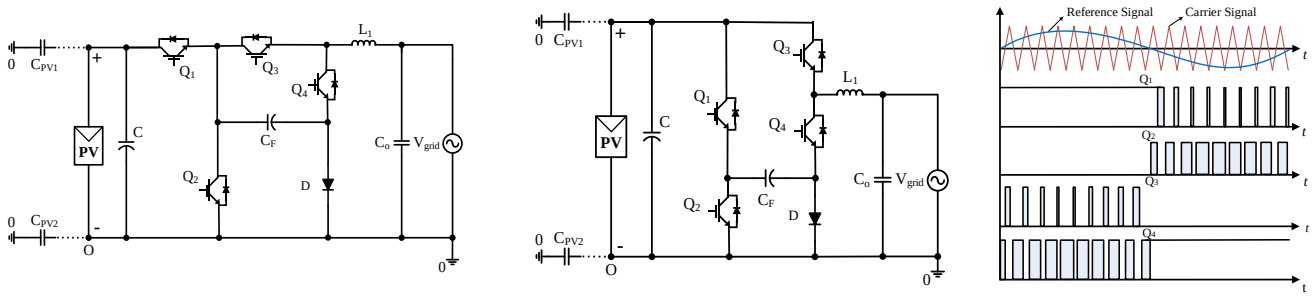
(a) (b)

Fig. 18. Illustration of (a) Siwakoti-H inverter, and (b) its switching pulses [16].

Reverse Blocking (RB) switches are needed (e.g. RB-IGBT). On the other hand, the other two switches (Q_2 and Q_3) are capable of producing the voltage stress of $2V_{DC}$. During the positive half cycle, only Q_2 is connected to produce the positive voltage, and Q_3 is ON for the negative half cycle to produce the negative voltage. The other two switches are used for zero states.

d) Flying Capacitor Topologies in [5], and [43]

Flying capacitor concept can be used in common ground transformerless inverter topologies as it is presented in [5], and [43]. The first one of these two new topologies is proposed by Siwakoti in [5], the seocnd one is propsoed by Chen in [43], which are shown in Fig. 19 (a) and Fig. 19 (b), respectively. Both topologies operate with the same modulation pulses (see Fig. 19 (c)). The same concept (negative polarity of PV panel is directly connected to the grid) is used to get zero i_{cm}. For instance, the switch Q_1 and diode charge the flying capacitor, and the discharging path is through switches Q_2 and Q_4, which creates the negative polarity. The flying capacitor (C_F) is charged from the input voltage, and the constant output voltage which is equal to the input voltage as like voltage converter integrated circuit, e.g., Maxim-ICL7660 and Texas Instrument-LMC7660. The circuit schematic in Fig. 19 (b) is quite similar to the one shown in [43], with only changing the device position. The switch Q_3 carries the load current during the positive active cycle and the negative half cycle; Q_2 and Q_4 carry the load current where Q_2 creates a negative power cycle by discharging the flying capacitor (C_F) through Q_4. All the switches work under the switching frequency (f_{sw}) with standard unipolar SPWM.

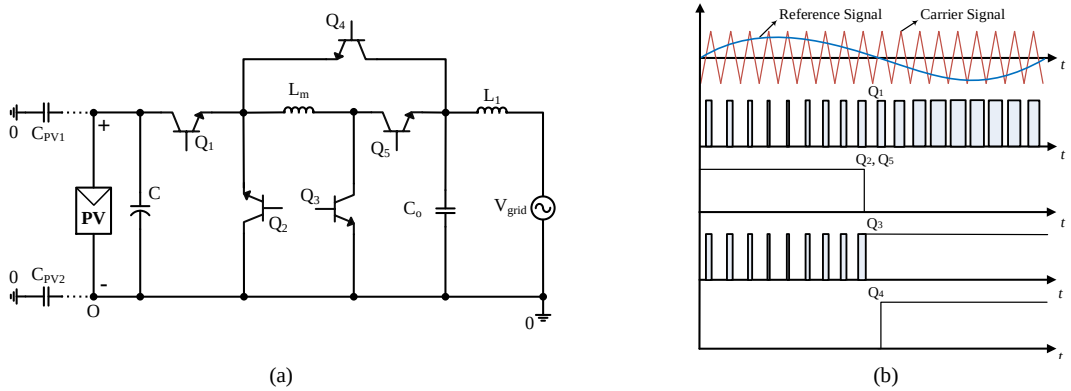


(a) (b) (c)

Fig. 19. Illustration of (a) inverter topology in [46], (b) inverter topology in [5], and (c) their switching pulses.

e) Flying-inductor inverter

The topology proposed in [44] is a five-switch based diode-less topology. Using a flying inductor (L_m) with low inductance helps to boost the input DC voltage with power injection from the PV panel to the grid [44]-[45].



(a) (b)

Fig. 20. Illustration of (a) inverter topology in [44], (b) its switching pulses.

L_m is charged by the simultaneous conducting of switches Q_1 and Q_3. However, the other three switches are used for discharging the flying inductor. The circuit structure of this topology is illustrated in Fig. 20 (a), and the gate pulses during operation are seen in Fig. 20 (b).

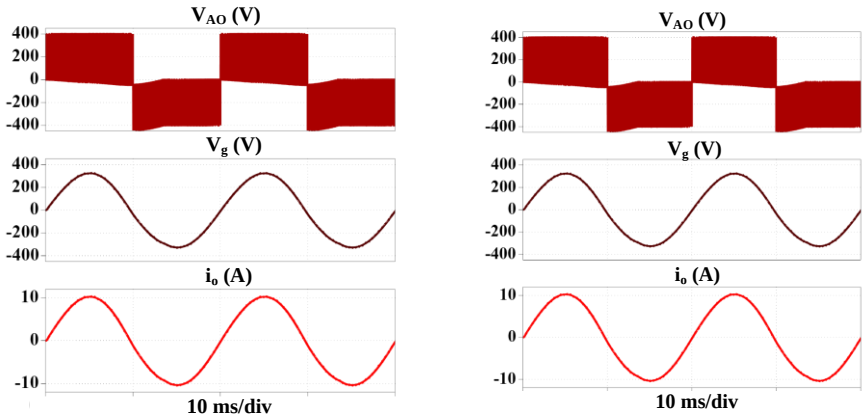


Fig. 21. Simulation results of common ground topologies, (a) inverter topology in [12], and (b) inverter topology in [5].

Fig. 21 displays the results of common ground topologies proposed in [5] and [12], where the flying capacitance (C_F) is chosen as 470 µF. Both figures (see Fig. 21 (a) and Fig. 21 (b)) show the inverter output, point A to ground (O) as well as the PV negative directly connected to ground through neutral and the output voltage (V_g) and current (i_o).

2) H-Bridge Type Topologies

i. Mid-point Clamped Type Topologies

The FB inverter can be extended through the semiconductor devices at either AC or DC side for clamping the voltage. Such kind of topologies are known as the midpoint clamping transformerless inverter topologies. The main advantages of midpoint clamping techniques are the reduced i_{cm} with lower ripple than other topologies where the CMV remains constant. The mid-point clamping topologies, such as iH5/oH5 [92], and [93], oH5-1 [37], oH5-2 [94], and [95], H5-D [38], HERIC Active 1 [39], HERIC Active 2 [39], and [96], HERIC Active 3 [39], PN-NPC [40], and [97], HB-ZVR [7], and HB-ZVR-D [41], are explained focusing on the operational and working principle. Further, simulated waveforms are presented.

a) iH5/oH5

This topology is presented in [9], and [37] where two switches (Q_5 and Q_6) are added at the DC side as revealed in Fig. 22 (a). The switching pulses are presented in Fig. 22 (b).

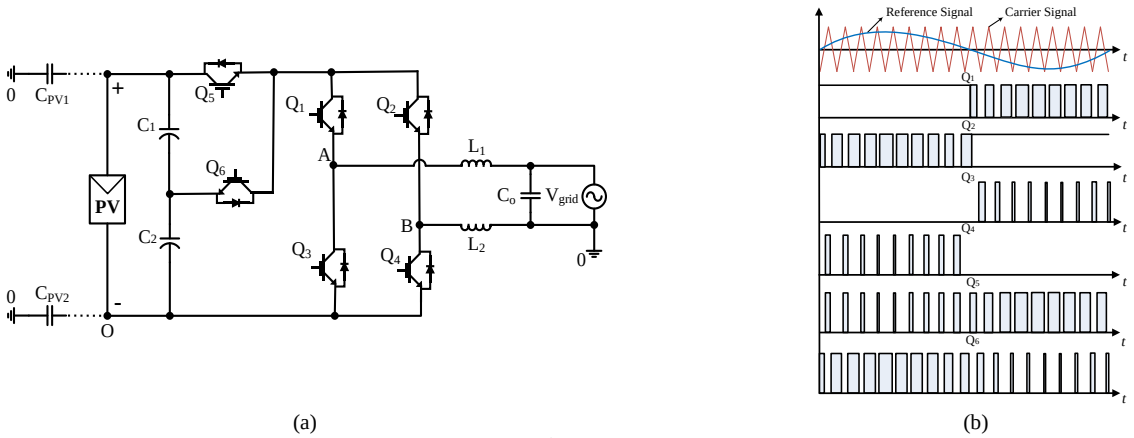


Fig. 22. Illustration of (a) oH5 inverter, and (b) its switching pulses.

The voltage clamping part of this topology is achieved in two ways. At potential up, the body diode of switch Q_6 is in the forwarding mode with the junction capacitor of switch Q_5 and DC link capacitor C_1 where the current flow path is Q_1 and the body diode of Q_2 through the grid.

On the other hand, at potential down, switch Q_6 is in active mode with the junction capacitors of switch Q_3, Q_4 and DC link capacitor C_2 where the current flow path is switched to Q_3 and the body diode of Q_4 through the grid. The main advantage of this topology is the achieved good differential mode characteristic, which is the same as unipolar SPWM FB grid-connected inverter, but with higher efficiency. Moreover, extra switches on DC side blocks the input voltage to be half; hence a constant CMV can be achieved.

b) oH5-1 and oH5-2

The oH5 topology (both 1 and 2) as shown in Fig. 23 is introduced in [44] to guarantee the clamping to half input voltage in the freewheeling period, thereby avoiding the high-frequency common-mode voltage. The two switches (Q_5 and Q_6) and diodes (D_1 and D_2) are used to clamp the voltage for constant CMV, which reduces the ground current. Switches Q_1 to Q_4 work like an FB inverter. Switches Q_5 and Q_6 are alternative to each other. Switches Q_1 and Q_2 work with the grid frequency (f_g), and the other four work at the switching frequency (f_{sw}).

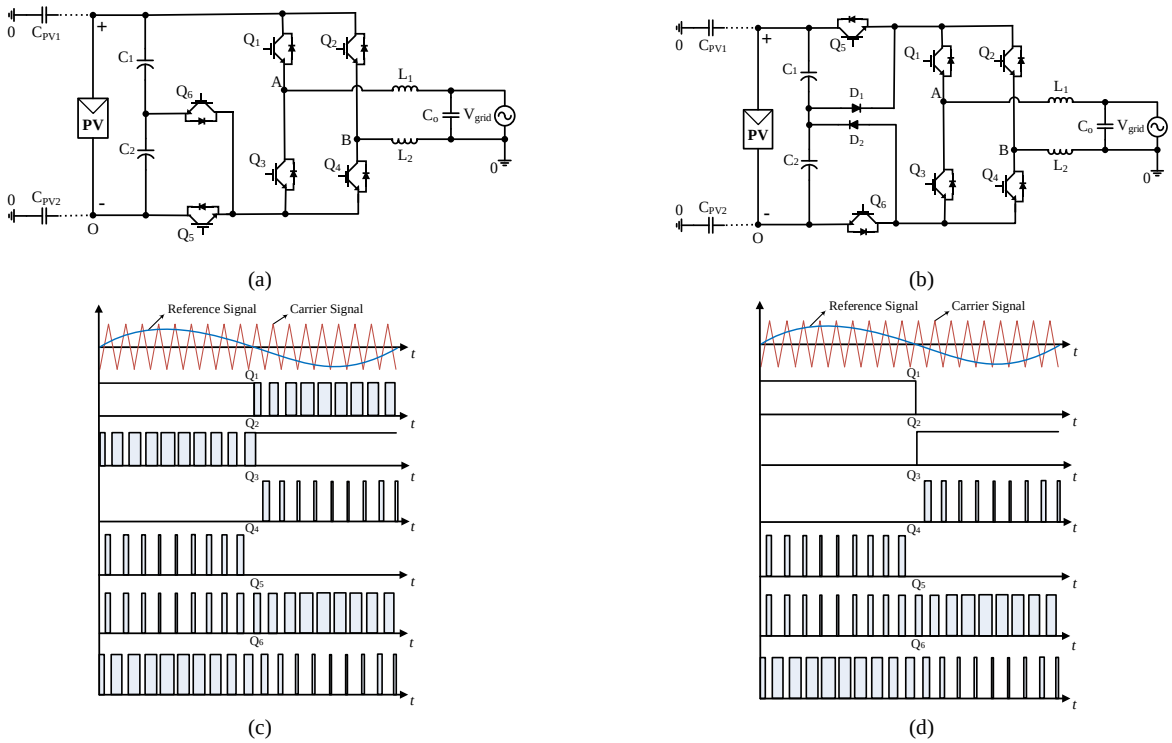
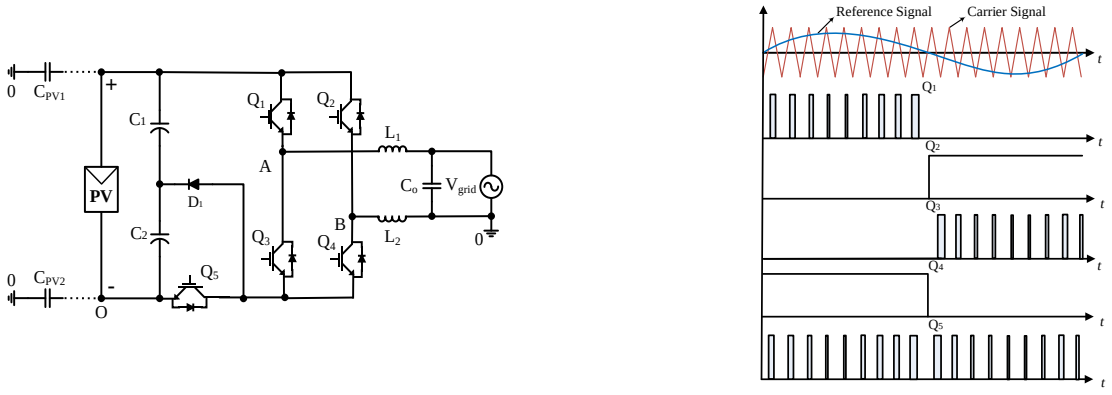


Fig. 23. Illustration of (a) oH5-1 inverter, (b) oH5-2 inverter, (c) switching pulses for oH5-1 inverter, and (d) switching pulses for oH5-2 inverter.

c) H5-D

The topology named as H5-D is presented in [38] where five switches are used together with a diode. This topology is an improved H5 topology, in which diode (D_1) and switch (Q_5) are used to clamp the input voltage in order to achieve a constant CMV. On the other hand, the improved modulation technique is set to keep the CM voltage constant. The CM current is only about one-third of that in H5 topology using the same electrical parameters and power switches. On the other hand, The THD

is quite high as H5 topology. The circuit diagram and the modulation strategy as shown in Fig. 24 reveal that the two switches operate at the grid frequency (f_g), and the remaining three switches operate at the switching frequency (f_{sw}).

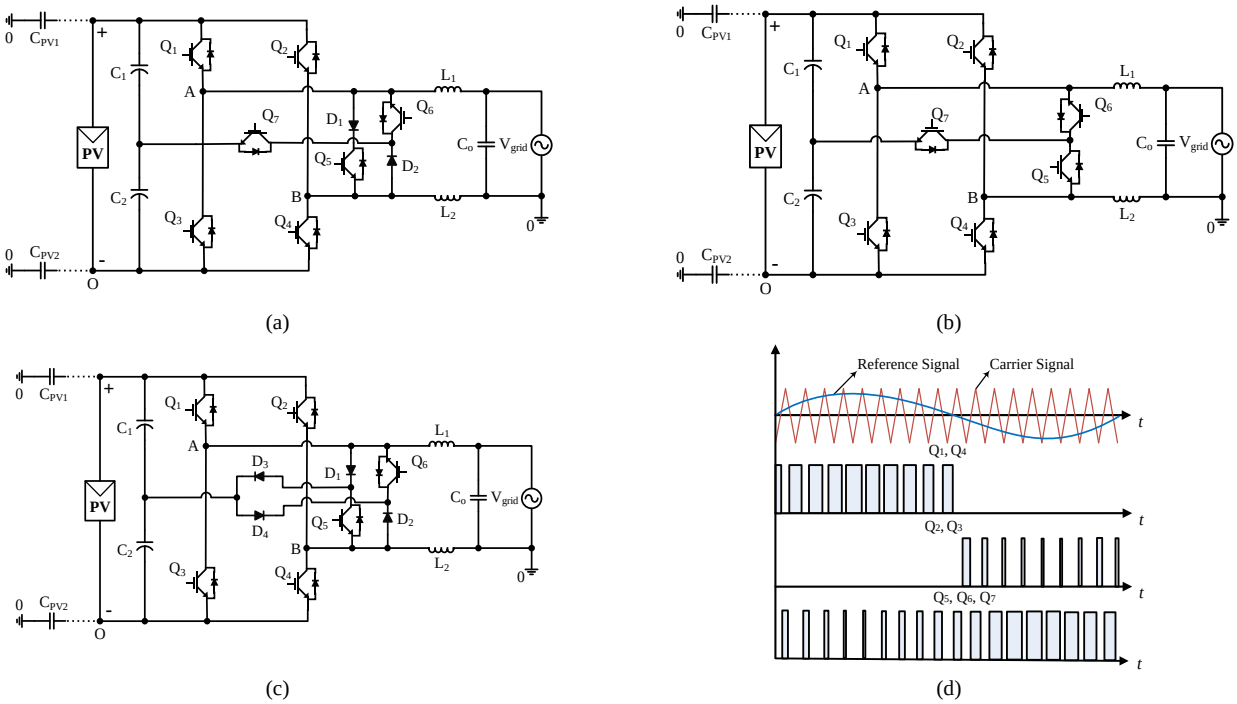


(a) (b)

Fig. 24. Illustration of (a) H5-D inverter, and (b) its switching pulses.

d) HERIC Active 1, HERIC Active 2 and HERIC Active 3

As discussed in the AC decoupling subsection, in the HERIC topology, it is shown that the leakage current is in the medium range and the CMV is not fully constant. Three major topologies are proposed by changing and adding the placement of semiconductor devices; see Fig. 25 (a) to Fig. 25 (c). Fig. 25 (d) shows the switching pulses to keep i_{cm} constant with low i_{cm} [37], [94]. The main disadvantage of these topologies is the shoot-through issue in the unidirectional controllable clamping path. Hence, a dead time should be introduced to avoid the short circuit issue [98].



(a) (b)

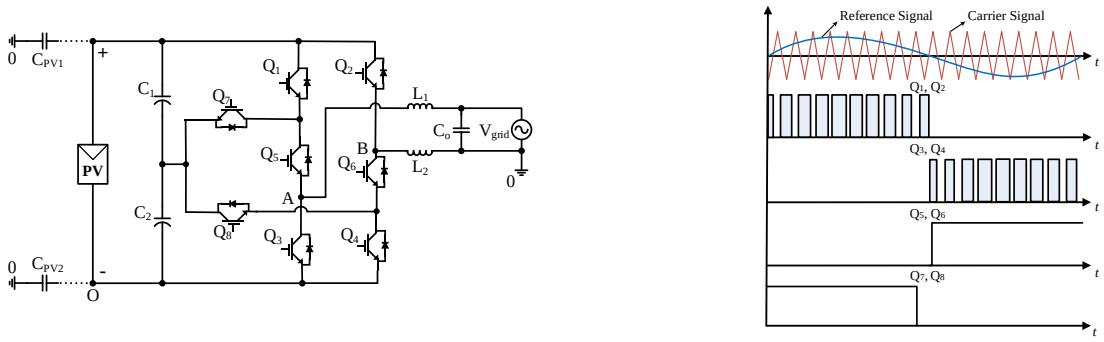
(c) (d)

Fig. 25. Modifications of HERIC inverter, (a) HERIC Active-1 inverter, (b) HERIC Active-2 inverter, (c) HERIC Active-3 inverter, and (d) their switching pulses.

e) PN-NPC

Positive negative NPC (PN-NPC) is proposed in [40] which combines the positive NPC (P-NPC) and negative NPC (N-NPC) switching cells. The circuit diagram of PN-NPC is illustrated in Fig. 26 (a) with the switching modulation in Fig. 26 (b). In this topology, four switches work at the grid frequency (f_g) while the other four work with the switching frequency (f_{sw}).

This topology can operate in four operational modes for each period of the utility grid. In the freewheeling period, four switches are ON so that the inductor current flows through all of those switches, which can cause high conduction losses.



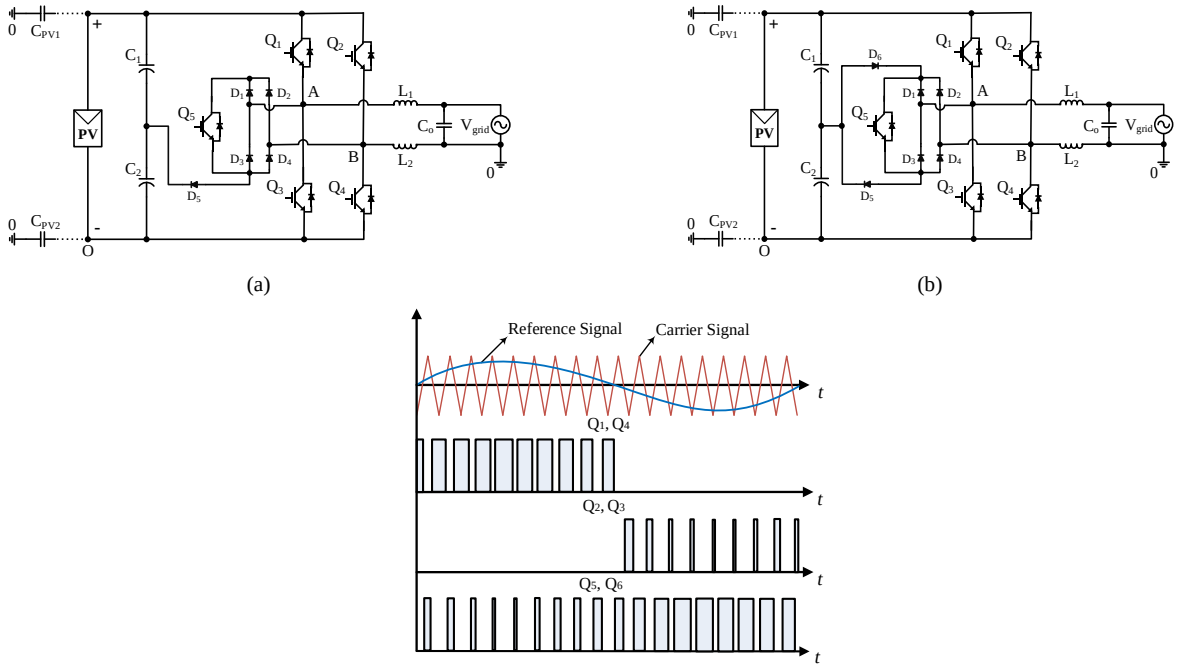
(a) (b)

Fig. 26. Illustration of (a) PN-NPC inverter, and (b) its switching pulses.

f) HB-ZVR, and HB-ZVR-D

H-Bridge Zero Voltage Rectifier (HB-ZVR) (see Fig. 27 (a)) topology is presented in [9] where four switches work like the FB inverter and the short-circuit voltage clamped to the midpoint of DC bus is done by four rectified diodes and bidirectional switch.

In the positive half cycle, Q_1 and Q_4 work to generate the active vector as shown in Fig. 27 (c). Similarly, in the negative half cycle, Q_2 and Q_3 are ON and work to generate the active vector. When Q_5 is ON, and the other switches are OFF. Thus, zero voltage states can be achieved.



(a) (b)

(c)

Fig. 27. HB-ZVR family inverters, (a) HB-ZVR inverter, (b) HB-ZVR-D inverter, and (c) their switching pulses.

The circuit structure of the H-Bridge Zero Voltage Rectifier-Diode (HB-ZVR-D) is revealed in Fig. 27 (b) with gate drive signals in Fig.27 (c) [41], which is very similar to HB-ZVR. The difference between these two topologies is a fast-recovery diode, which is used to achieve zero i_{cm} and constant CMV. The two diodes (D_5 and D_6) are used for clamping branches of the freewheeling path.

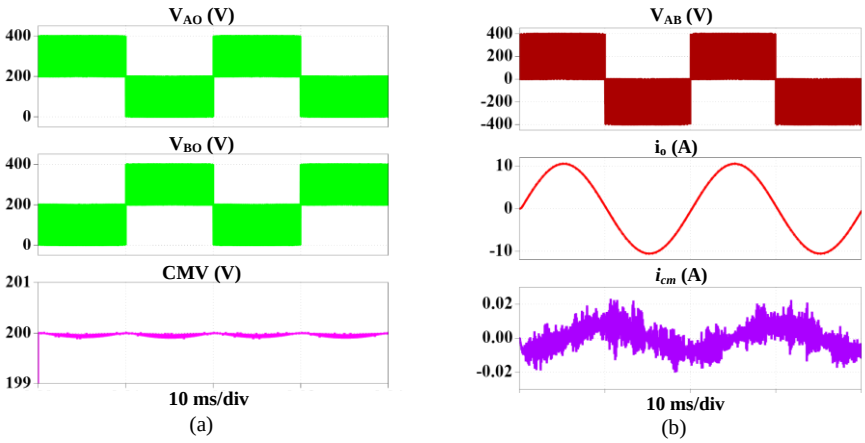


Fig. 28. Simulation results of iH5/oH5 inverter.

Fig. 28 (a) shows the voltage of the terminal A to neutral and terminal B to neutral where it is able to achieve a constant CMV. As it can be seen a low value of i_{cm} can be seen in Fig.28 (b) with low ripple on the output current. Fig. 29 shows the result for oH5-1 topology. It can be seen that the output current shows less ripple, the CMV is not sufficiently constant, and the common mode current is in the medium range.

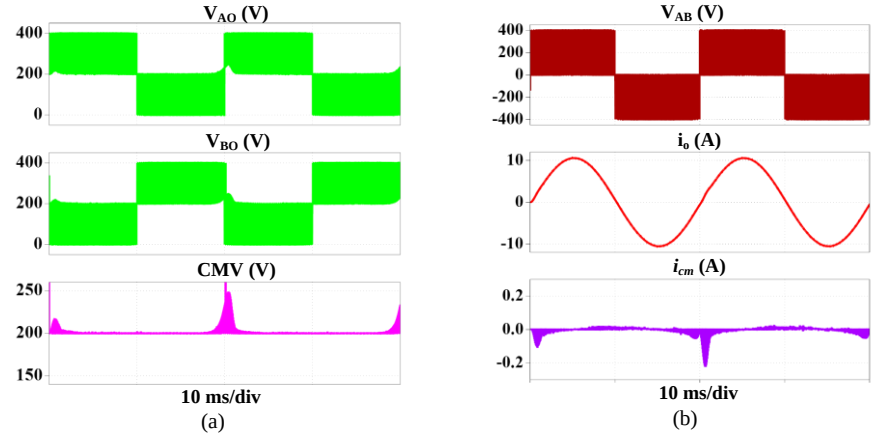


Fig. 29. Simulation results of oH5-1 inverter.

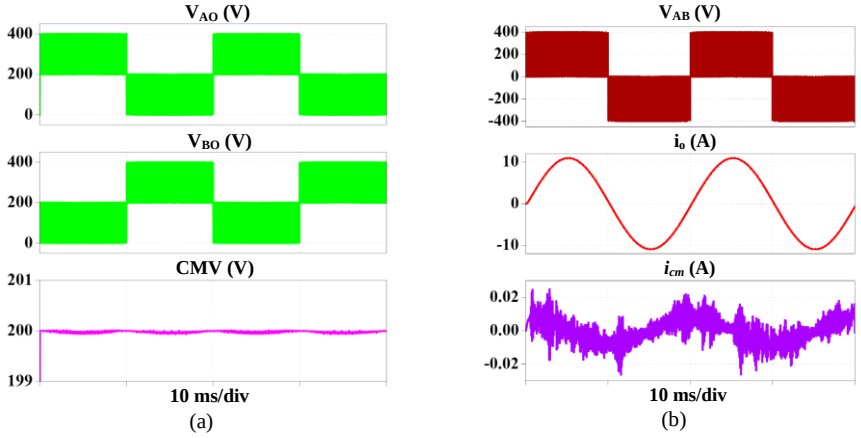


Fig. 30. Simulation results of HERIC Active-1 inverter.

With the additional placement of switches and diodes on the HERIC topology, as shown in Fig. 30, i_{cm} can be reduced more to have a constant CMV. The PN-NPC result is shown in Fig. 31 (a) and Fig. 31 (b) where a low i_{cm} with constant CMV is achieved.

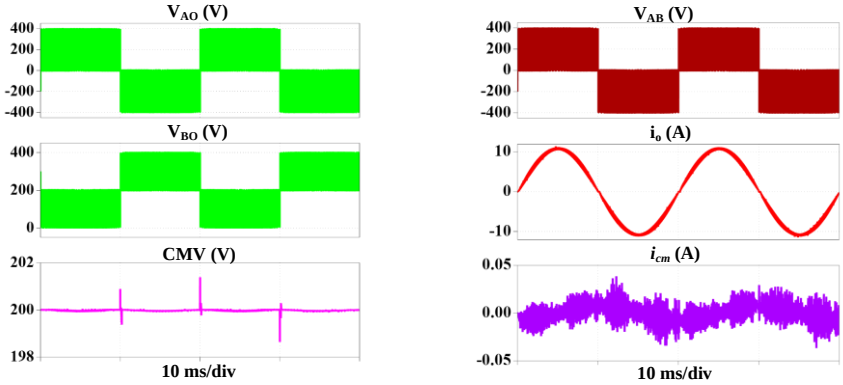


Fig. 31. Simulation results of PN-NPC inverter.

The resulting wave forms for HB-ZVR are shown in Fig. 32 (a), which achieves an almost constant CMV and medium range of i_{cm}. However, the HB-ZVR-D achieves low i_{cm} with an almost constant CMV as shown in Fig. 32 (b).

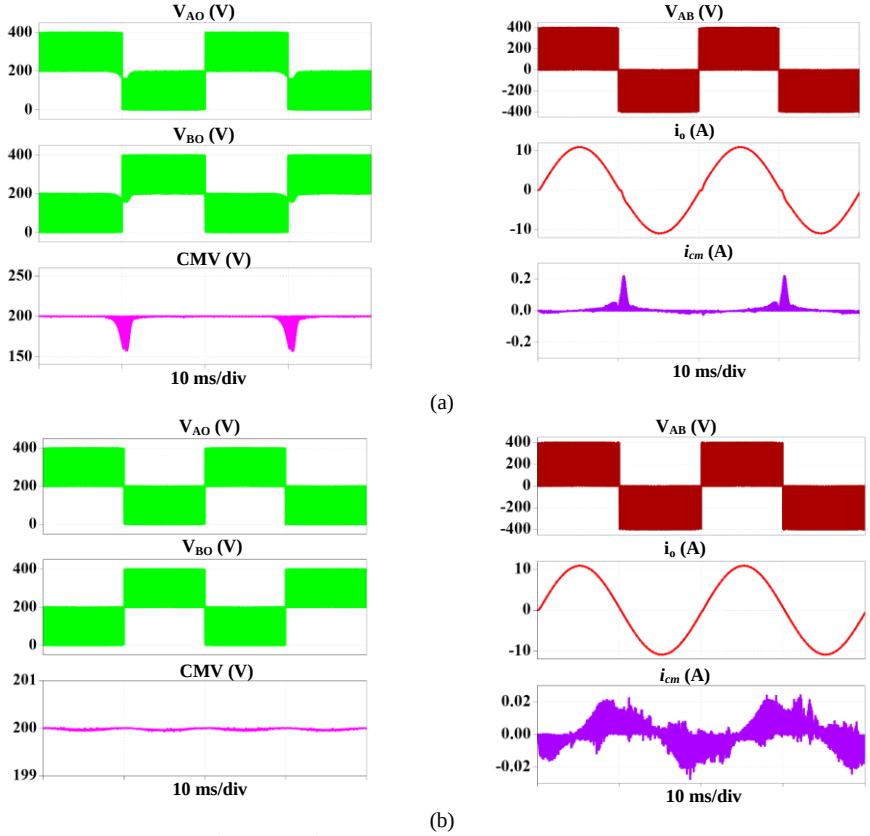


Fig. 32. Simulation results of HB-ZVR family inverters, (a) HB-ZVR inverter, (b) HB-ZVR-D inverter.

ii. Decoupling techniques

AC Decoupling

AC decoupling based transformerless inverter topologies are extended by adding switches and diodes at the AC side. These kinds of topologies are presented to achieve low THD based output voltage and current. Moreover, the leakage current is reduced with a balanced system and constant CMV. The AC decoupling topologies are HERIC and HERIC AC based topologies [9], [31], and [99].

The HERIC topology is well known in string inverters for achieving high efficiency, which is first invented in 2003 [80]. In addition, in the German manufactured Sunways NT solar inverter, it is highly recommended to use this topology. Moreover, 5 kW string inverters are investigated, which achieve 98% efficiency [100]. This topology employs Unipolar-SPWM to achieve

low current ripple and high efficiency because the load current is short-circuited through the switches Q_5 and Q_6 during the freewheeling period. On the other hand, the CM issue is present there as the PV module is decoupled from the grid and voltage is not clamped to the half of the supply voltage [101]. The HERIC AC based topology is similar to the HERIC topology, which uses two diodes with the switches Q_5 and Q_6 in series as proposed in [99], and [102]. These two diodes are used to conduct the output current at the freewheeling time. The operational mode of these topologies is the same as the FB inverter; the only difference is the output current flow path through the additionally used diodes and switches in the freewheeling period. The circuit diagrams of both topologies are given in Fig. 33 (a) and Fig. 33 (b) respectively and the gate drive signals in Fig. 33 (c).

The simulation results for HERIC topology are illustrated in Fig. 34. The obtained CMV is almost constant, and the i_{cm} is 160 mA. The main advantage of this topology is the obtained less ripple on the output. Hence the THD is very low.

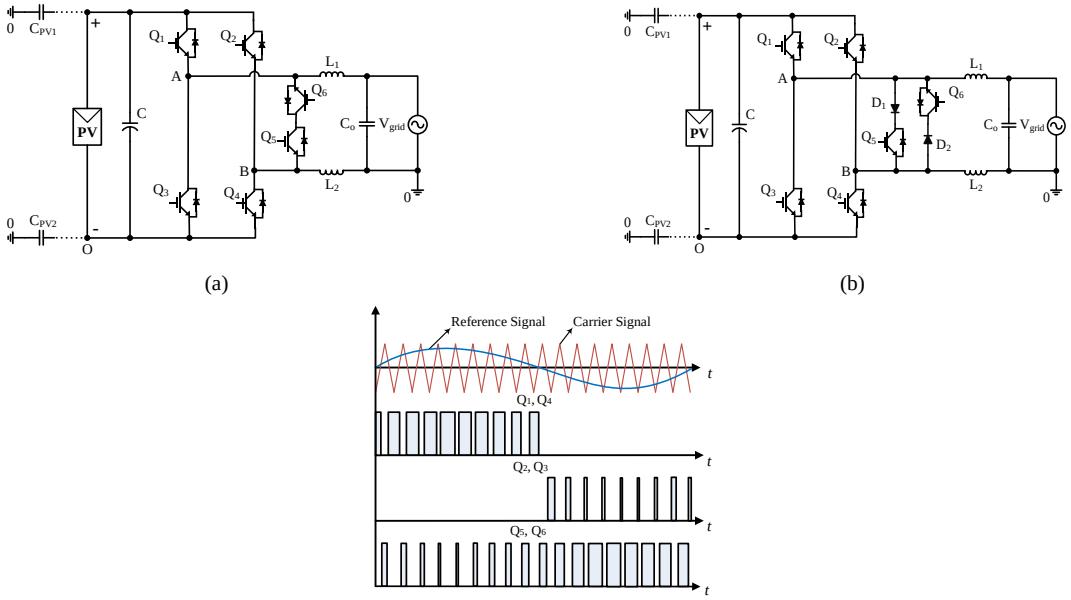


Fig. 33. (a) HERIC (b) HERIC ac based (c) Switching pulses.

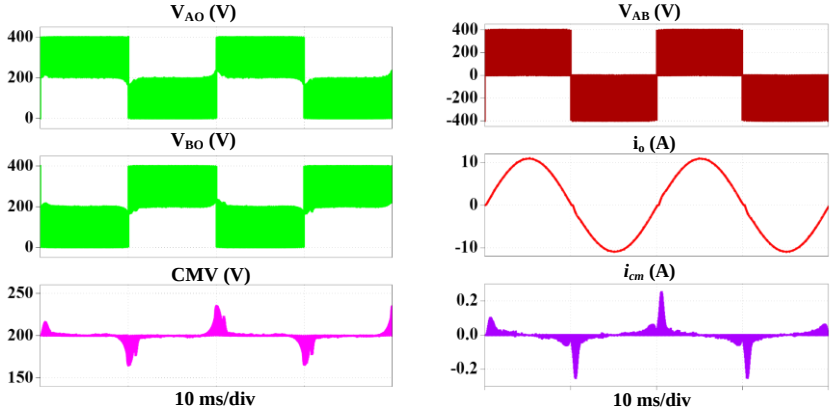


Fig. 34. Simulation results of HERIC inverter.

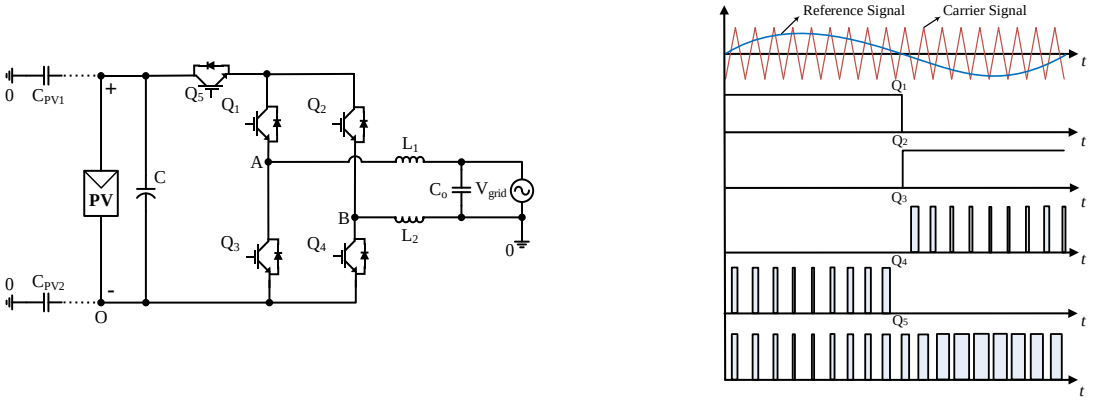
DC Decoupling Type Topologies

The extra switches and diodes on the DC side are added for inventing new topologies and such kind of topologies are known as DC decoupling based transformerless inverter topologies. These topologies are introduced for mitigating the common

mode current for balancing the system. A few topologies are explained below such as H5 [92], H6 DC side [54], H6 DC side -1 [33] and H6 DC side -2 [33] topologies.

a) H5

The H5 topology is a high efficiency based transformerless inverter topology and is first proposed in [32] which is patented by one of the best PV inverter producers, SMA solar technology. Its operational principle is almost same as the F-B. However, one switch is used on the DC side, which is called the DC decoupling switch. This switch is operated at the switching frequency (f_{sw}). The upper switches are operated with grid frequency (f_g), and the lower switches are operated with the switching frequency (f_{sw}). The PV panel is disconnected from the grid side during zero voltage states when the switch Q_5 is OFF; as a result, the current freewheeling period, there is no way to flow the output current at DC side which is an effective solution to reduce the i_{cm} [39], [103], and [104]. In the positive half cycle, switches Q_5 and Q_4 turn ON at the switching frequency (f_{sw}), and Q_1 at the grid frequency (f_g) whereas the other two switches are OFF.



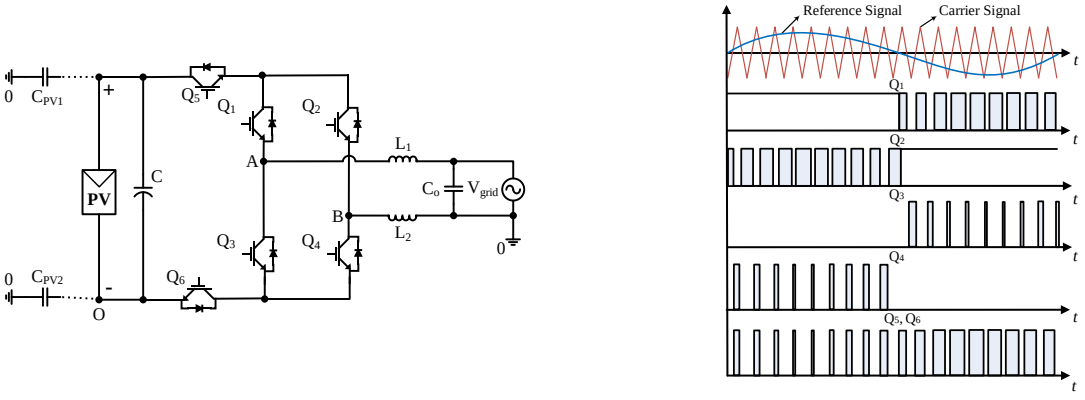
(a) (b)

Fig. 35. Illustration of (a) H5 inverter, and (b) its switching pulses [8].

On the contrary, Q_5 and Q_2 turn ON at the switching frequency (f_{sw}) and Q_3 at grid frequency (f_g) whereas the other two switches are OFF in the negative half cycle. At the freewheeling period, the output current flows through Q_1 and the body diode of Q_3 for the positive period, and through Q_3 and the body diode of Q_1 for the negative period. The main disadvantage of this topology is the higher conduction losses through the three associated series switches in the active phase [105]. The circuit structure and switching modulation of the H5 are shown in Fig. 35 (a) and Fig. 35 (b) respectively.

b) H6 DC side

The H6 DC side topology is displayed in Fig. 36 (a) with the gate drive signals in Fig. 36 (b). This topology is introduced in [48], which is operated in four stages. Moreover, the presence of junction capacitor in the H6 DC side topology as like as H5 topology is explained in [49] and [106], as well as the effect of the resonant circuit through the junction capacitor and thereby the leakage current issue. The switches Q_5, Q_1 and Q_6 conduct in the positive half cycle, while Q_3 and Q_2 are OFF. On the freewheeling period of positive and negative half cycle, the body diode of Q_3 is in the forward bias with conducting switch Q_1, and the body diode of Q_4 is in the forward bias with conducting switch Q_2 respectively. In this topology, extra low value capacitors are used to remove the CM effect which is the reason for increasing the losses [107].

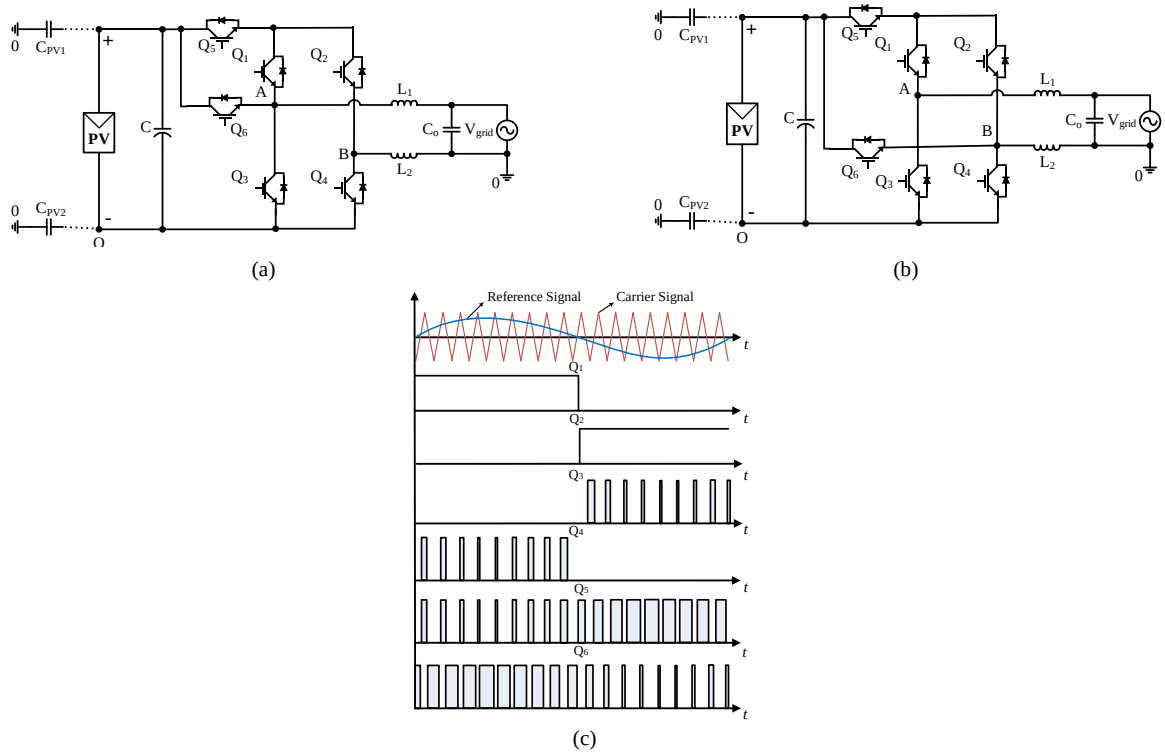


(a) (b)

Fig. 36. Illustration of (a) H6 DC side inverter, and (b) its switching pulses [29].

c) H6 DC side -1 and H6 DC side -2

These two topologies are presented in [33], and the concept is taken from the aforementioned topologies H5 [32] and H6 [48]. The positive terminal of the PV array and the terminal (A) are connected through a switch Q_6 to make a current path as seen in Fig. 37 (a), and further the terminal (A) is changed to terminal (B), which is shown in Fig. 37 (b). In both topologies, the gate drive signals are the same (see Fig 37 (c)). These topologies work in four operational modes. The switches Q_1 and Q_3 work at the grid frequency (f_g), and the other four switches work at the carrier frequency (f_{sw}). In the freewheeling period, switch Q_1 conducts with the body diode of Q_3 for the positive half cycle; the switch Q_3 and the body diode of Q_1 are ON for the negative half cycle. Both topologies have less power losses compared to H5. Fig. 38 illustrates the output waveforms of H5 where the inverter output voltage and the output current are shown. The i_{cm} is around 200 mA with an almost constant CMV.



(a) (b)

(c)

Fig. 37. Illustration of (a) H6 DC side-1 inverter, (b) H6 DC side-2 inverter, and (c) their switching pulses.

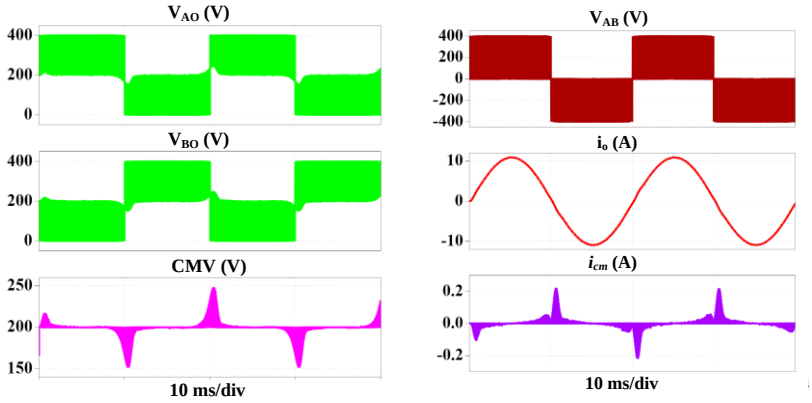


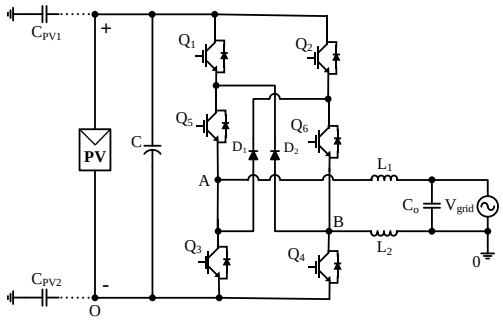
Fig. 38. Simulation results of H5 inverter.

3) H6 Type Topologies

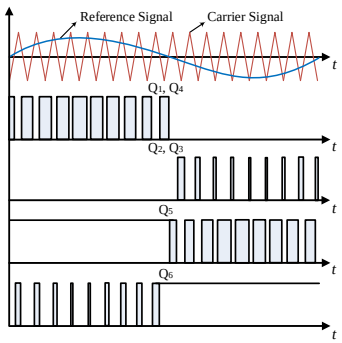
F-B topologies are extended with switches and diodes to reduce the leakage current with smoother output waveforms. In this sub-section, those kinds of topologies are presented like H6 with diodes-1 [34], H6 with diodes-2 [63], H6-1 [35], H6 in mid-switch [36], and midpoint switches with diodes [39], and [49]. Further, the circuits are simulated to see the output waveforms, i_{cm} and CMV.

a) H6 with diodes-1 and H6 with diodes-2

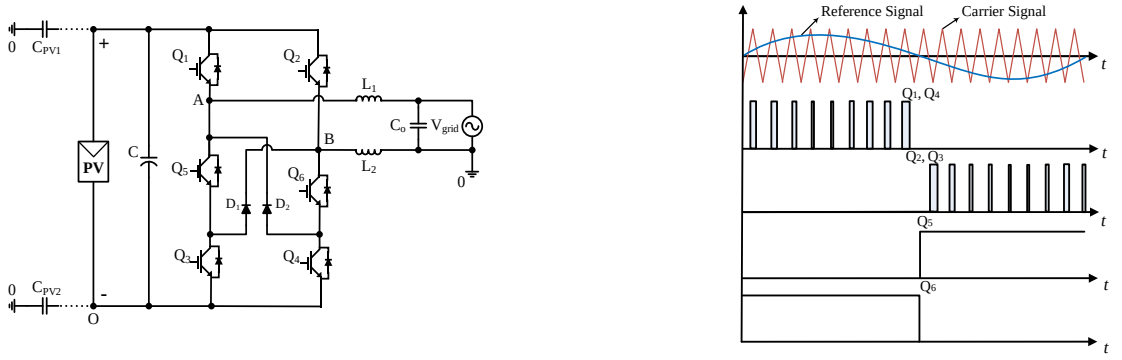
H6 with diodes-1 is presented in [34], which is structured by Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) switches. Four MOSFETs work as an F-B inverter as well as two extra switches and the diodes are used for freewheeling purposes. The same basic concept is used for H6 with diodes-2 topology. Fig. 39 (a) shows the circuit structure of H6 with diodes-1 and in Fig. 39 (c) is the circuit diagram of H6 with diodes -2. Meanwhile, Fig. 39 (b) and Fig. 39 (d) show the switching pulses for these two topologies. After simulating these two topologies, i_{cm} is obtained as around 200 mA for H6 with diodes-1 and 250 mA for H6 with diodes -2 topology. However, in both cases, the CMV is quite constant. To reduce the i_{cm} correctly, an accurate modulation technique is needed. Hence, in [108] a topology is proposed, which replaces the switches Q_5 and Q_6 by two IGBTs and uses a new modulation controller based on reactive power injection space vector PWM (SVPWM) technique as well as using proportion-integral-resonance (PIR) current controllers. The main demerit of these topologies is the higher conduction losses in the active mode as the output current is flowing through the three switches [107].



(a)



(b)

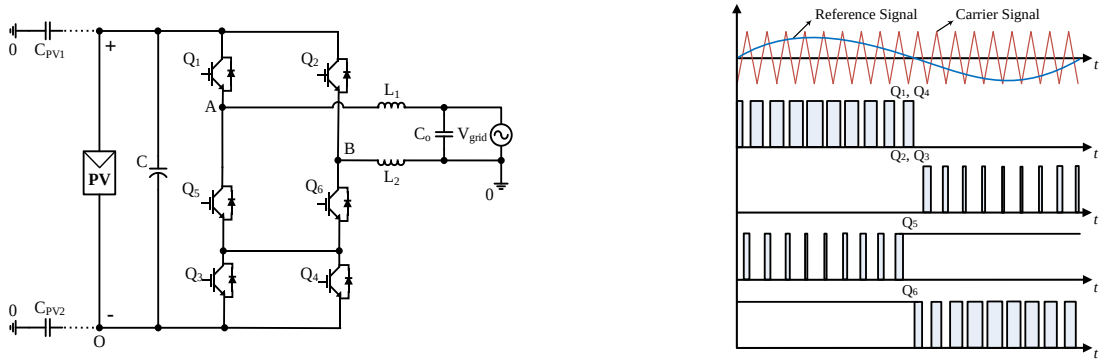


(c) (d)

Fig. 39. Illustration of (a) H6 with diodes-1 inverter, (b) its switching pulses, (c) H6 with diodes-2 inverter, and (d) its switching pulses. [57].

b) H6-1 topology

H6-1 topology is proposed in [35], and the idea is taken from the topologies including six switches with two diodes as discussed in [34], and [36]. However, the extra cross connected diodes are removed and MOSFET switches are replaced with IGBTs, as demonstrated in Fig. 40 (a) with the switching pulses in Fig. 40 (b). Hence, it is possible to handle the reactive power flow, which is not possible by MOSFET based topologies [109]. It works in six operational modes and makes a connection internally whereas creating a freewheeling path. Therefore, the circuit operates smoothly when it is connected to the grid. In the positive half cycle, Q_1, Q_6 and Q_4 are ON, and the current flows through the inductors, completing the cycle. Moreover, zero voltage state switch Q_6 and the antiparallel connected body diode of switch Q_5 are conducting, which are not connected with the input; and the current flows through the load. On the other hand, the remaining three switches Q_2, Q_5 and Q_3 conduct in the negative half cycle. A zero voltage state occurs in the negative half cycle, and the current flows between the switch Q_5 and the antiparallel connected body diode of switch Q_6.



(a) (b)

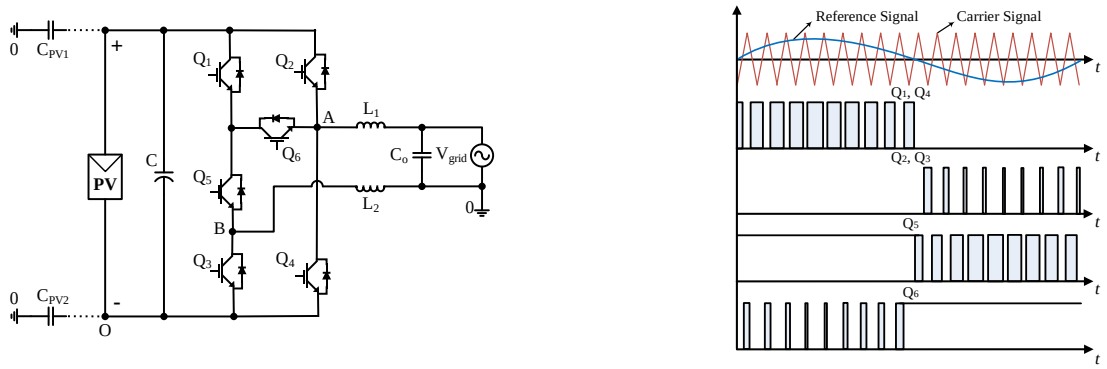
Fig. 40. Illustration of (a) H6-1 inverter, and (b) its switching pulses [58].

The topology H6-1 [35] can be modified after changing the position of point A to B and B to A, and this topology also works in six operating modes like H6-1 [35]. The modified one can be simulated after changing the switching pulse Q_5 of the H6-1 to Q_6 , and the other pulses remain the same. Indeed, the THD is reduced a little bit.

c) H6 in mid Switch

H6 in mid-switch topology is presented in [36] which has four operational modes. Fig. 41 (a) displays the schematic diagram of the midpoint switch based H6 topology, and the switching pulse is shown in Fig.41 (b). Moreover, the mid switch Q_6 is used to complete the circuit for the freewheeling period. In the positive half cycle, the freewheeling path works through

the switch Q_6 and the body diode of Q_5. On the other hand, for negative half cycle, the body diode of Q_6 is in active mode with the Q_5 switch. The main disadvantages of this topology are the high volume of the filter capacitor, and high ripple based output waveforms.

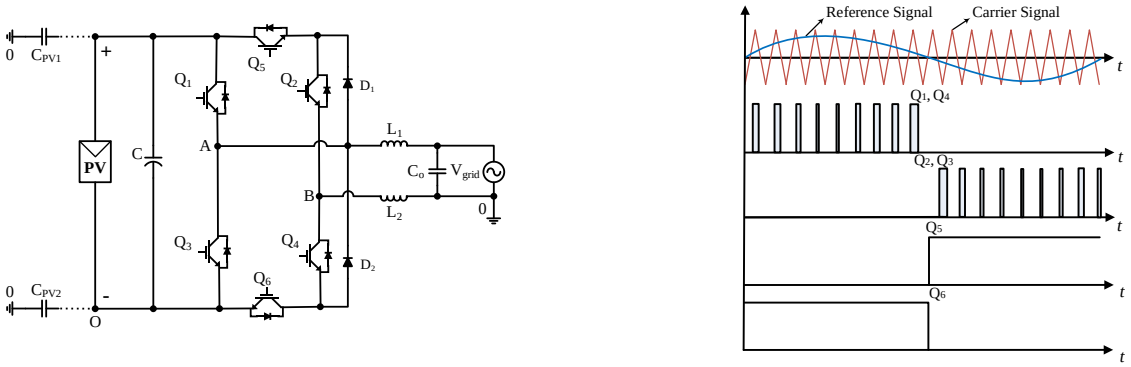


(a) (b)

Fig. 41. Illustration of (a) H6 with mid switch inverter, and (b) its switching pulses [60].

d) F-B with midpoint-switches and diodes

In [39], [49] and [110], a topology is discussed where the idea is taken from H5 topology. Two extra switches are added at the top and bottom of the middle of F-B topology, and the two diodes are used for creating a freewheeling path. This topology is also known as hybrid bridge topology [111]. Moreover, the topology consists of two modules such as H-B and NPC bridge. The circuit diagram is displayed in Fig. 42 (a). Switches Q_1 and Q_6 are conducting together when Q_4 is conducting. On the other hand, Q_5 works with the same switching pulses as Q_2 while Q_3 is continuously ON.



(a) (b)

Fig. 42. Illustration of (a) F-B inverter with midpoint-switches and diodes, and (b) its switching pulses [107].

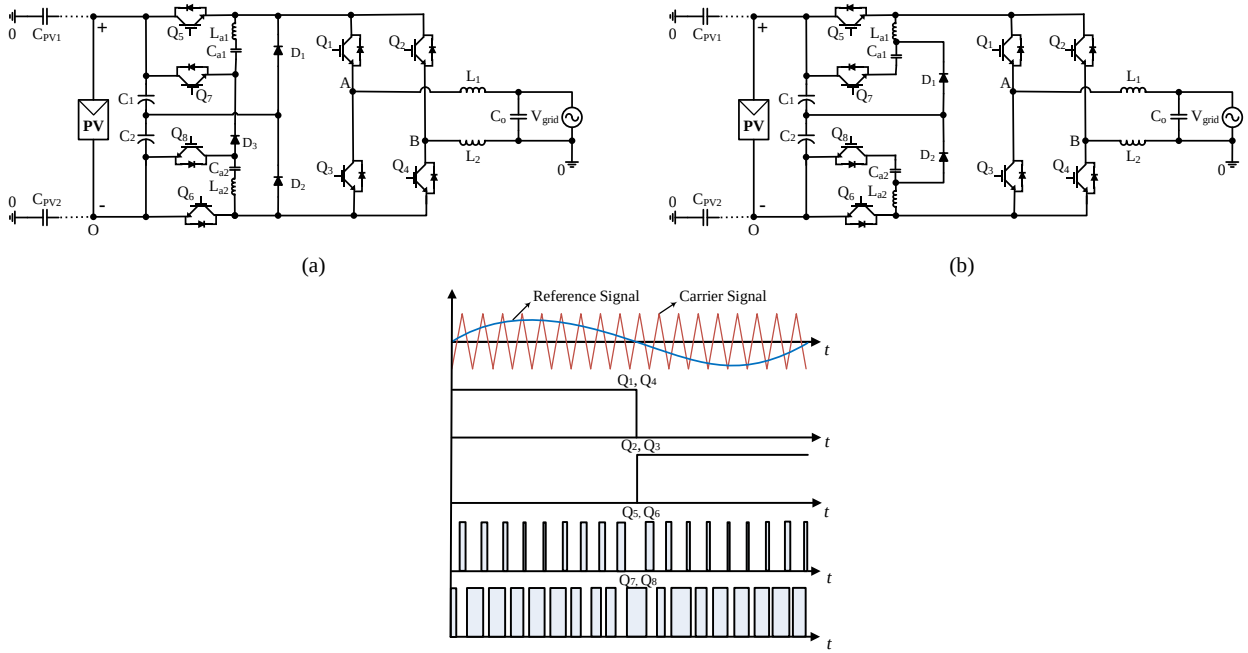
The switching strategy is shown in Fig. 42 (b). In the freewheeling period, during the positive half cycle, D_2 works in forwarding bias with the conducting switch Q_4, and the output current flows through the load. Alternatively, during the negative half cycle, D_1 is in forward bias with Q_2. In this topology, the most important is that the dead time is fixed because switches Q_1, Q_2, Q_4, Q_6, and diode D_1 might be turned ON once in the positive half cycle.

e) ZCT-H6-1 and SCF-H6-1

Using zero-current-transition (ZCT) technique, a new transformerless inverter is discussed in [65] as shown in Fig. 43 (a). In this topology, two auxiliary switches (Q_7, and Q_8) and two H6 switches (Q_5, and Q_6) are operated at high frequency, whereas the full-bridge inverter switches $Q_1 - Q_4$ operate at the line-frequency. In addition, few resonant components are also

used in this topology to realize ZCT operation. As a result of using many additional components, the overall efficiency is comparatively low.

Another improved soft-switching circuit called switching loss-fee (SLF) inverter is introduced in [66], where it is possible to reduce the number of auxiliary components (see Fig. 43 (b)). Compared to the s ZCT-H6-I topology, the connection points of two resonant tanks are moved from the midpoints of the auxiliary switch and resonant capacitor to the midpoints of the resonant capacitor and resonant inductor, respectively. With this arrangement, this new topology is able to obtain over 95% efficiency over a wide load range, which is roughly 1.5% higher than the ZCT-H6-1 topology. Moreover, SCF-H6-1 topology mitigates more leakage current than ZCT-H6-1 topology. Fig. 43 (c) shows the required gate signals for both topologies.

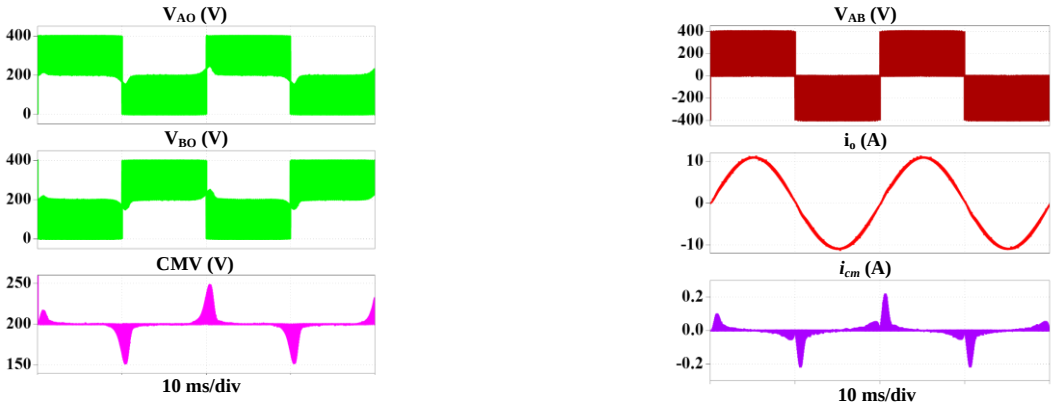


(a) (b)

(c)

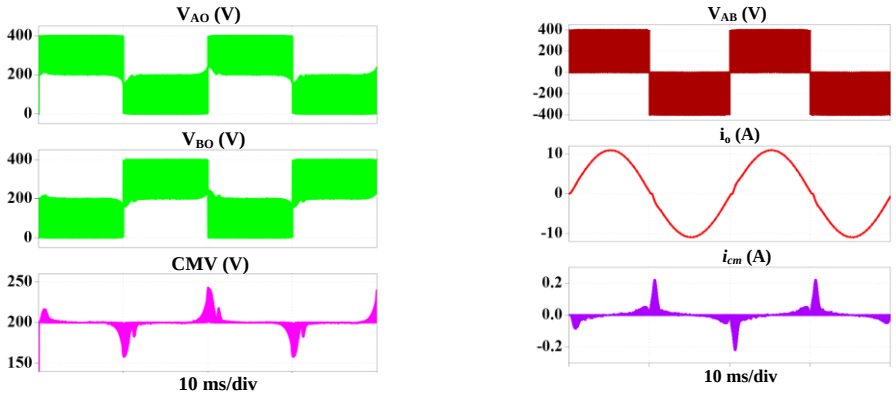
Fig. 43. Illustration of (a) ZCT-H6-1 [65], (b) SCF-H6-1 [66], and (b) its switching pulses.

Fig. 44 (a) displays the output voltage and current of the H6-1 topology with the i_cm. The RMS value of i_cm is around 180 mA, and the CMV remains almost constant. Fig. 43 (b) shows the output voltage and the current of hybrid bridge topology.



(a)

The CMV is almost constant like H6-1 topology. The extra switches based on the F-B transformerless inverter topologies are used with the almost same techniques, that is, just changing the location of the diodes and bidirectional switches. Hence, the obtained CMV and i_{cm} are practically identical.



(b)

Fig. 44. Simulation results (a) H6-1, (b) F-B inverter with midpoint-switches and diodes.

4) Buck-Boost Type Topologies

Buck-boost topologies are created by employing buck/boost and buck-boost topologies in the circuit to avoid complexity of single-phase transformerless inverters. As a result, the i_{cm} can be reduced dramatically for some buck-boost topologies [69-70]. In some topologies like [112], there is a direct connection between the ground of PV panel and load, and hence no leakage current will flow through the parasitic capacitor. However, their THD values might be high.

In [70], a boost converter is used at the front of the circuit that helps in reducing the minimum required input voltage level. In this topology, extra switches are used to clamp the mid-point voltage, and hence the CMV is remained constant with low level of i_{cm}. On the other hand, when the output voltage falls below the peak grid voltage, the DC-DC converter is energized in a way to charge the second DC-link capacitor such that the total DC-link voltage becomes more than the peak grid voltage. Thus, the topology is also used to increase the voltage level into five-level through the DC-link capacitors. Further, a high gain DC-DC converter based topology that is connected with doubly grounded voltage swing inverter is introduced in [72], which is able to reduce the components voltage requirement. However, such kind of topology utilize multiple stages and operates in high switching frequency, which results in a low conversion efficiency. Moreover, double PV panel is used with NPC and generation control circuit (GCC) to increase the DC-link voltage in [69]. This circuit construction allows the operation of each PV string at a different current-voltage point, which helps to avoid the partial shadowing problem. As a result, the maximum current of the most shaded PV module limits the current of the string. On the other hand, the output ground is directly connected to the mid-point of the DC-link capacitors, which is the main reason of getting low i_{cm}. The topology is implemented for 5 kW where the achieved efficiency is 96%. Moreover, the same technique is used in [68] and [7] obtaining a low i_{cm}. [72]

Table V summarizes the major single input type transformerless inverter topologies in terms of CMV, leakage current, voltage stress and number of components required which have been analysed previously.

TABLE V
SUMMARY OF SINGLE INPUT VOLTAGE TYPE TRANSFORMERLESS INVERTERS.

Topology Name	Semiconductor Devices		No. of C*	No. of L	Common Mode Current i_{cm} (mA)	Common Mode Voltage CMV (V)	Passive Filter		Output Voltage Level	Reported PF	Reported THD, (%)	Cost#	Reported Efficiency, η (%)
	No. of IGBTs	No. of Diodes					No. of C	No. of L					
Bipolar F-B [62]	4	0	1	0	≤ 55	199 to 201	1	2	2	Unity	N/A	+	95.2 @ 5 kVA
Unipolar F-B [61, 103]	4	0	1	0	≤ 1800	200 to 400	1	2	3	Unity	N/A	+	98.0@3 kVA
Inverter topology in [12]	5	0	2	0	≈ 0	constant	1	1	3	0.94	2.1	++	95.20 @ 0.5 kVA
S4 Topology [42]	4	2	3	0	≈ 0	constant	1	1	3	0.8	2.1	++	97.2 @ 0.5 kVA
Siwakoti-H [16]	4	1	2	0	≈ 0	constant	1	1	3	0.85	< 2.3	++	97.8 @ 1 kVA
Inverter topology in [5]	4	1	2	0	≈ 0	constant	1	1	3	0.85	< 2	++	99.25 @ 1 kVA
Inverter topology in [43]	4	1	2	0	≈ 0	constant	1	1	3	0.9	< 2.2	++	99.2 @ 1 kVA
Inverter topology in [44]	5	0	2	1	≈ 0	constant	1	1	3	Unity	N/A	++	95 @ 200 VA
Karschny [45]	5	2	2	1	≈ 0	constant	1	1	3	Unity	N/A	+++	N/A
iH5/oH5 [10]	6	0	2	0	≤ 20	199.89 to 200	1	2	3	Unity	N/A	++	96.9 @ 1 kVA
oH5-1 [37]	6	2	2	0	≤ 200	200 to 248	1	2	3	Unity	N/A	+++	N/A
oH5-2 [37]	6	0	2	0	≤ 200	198to 249	1	2	3	Unity	N/A	++	97.16 @ 5 kVA
H5-D [38]	5	1	2	0	≤ 50	185to 195	1	2	3	Unity	4.888	++	95@650 VA
HERIC Active 1 [39]	7	2	2	0	≤ 25	199.93 to 200	1	2	3	N/A	N/A	++++	N/A
HERIC Active 2 [39]	7	0	2	0	≤ 25	199.96 to 200	1	2	3	N/A	1.7	++++	97 @ 2 kVA
HERIC Active 3 [39]	6	4	2	0	≤ 25	199.91 to 200	1	2	3	Unity	N/A	++++	N/A
PN-NPC [40]	8	0	2	0	≤ 35	199.3 to 201.1	1	2	3	Unity	N/A	++++	97.2 @ 1 kVA
HB-ZVR [9]	5	5	2	0	≤ 200	163 to 200	1	2	3	Unity	N/A	+++	94.88 @ 2.8 kVA
HB-ZVR-D [41]	5	6	2	0	≤ 40	199.89 to 200	1	2	3	Unity	1.9	+++	95.03 @ 1 kVA
HERIC [31]	6	0	1	0	≤ 200	165 to 235	1	2	3	Unity	N/A	++	97.1 @ 2 kVA
HERIC AC based [31]	6	2	1	0	≤ 200	165 to 236	1	2	3	Unity	N/A	+++	N/A
H5 [32]	5	0	1	0	≤ 200	159 to 235	1	2	3	Unity	N/A	++	98.50 @ 0.5 kVA
CH5 [113]	5	5	1	2	≤ 50	N/A	1	2	3	Unity	2.69		N/A
H6 DC side [29]	6	0	2	0	≤ 200	151 to 249	1	2	3	Unity	1.585	++	95.9 @ 1kVA
H6 DC side improved-1 [33]	6	0	1	0	≤ 1000	200 to 400	1	2	3	Unity	N/A	++	N/A
H6 DC side improved-2 [33]	6	0	1	0	≤ 1000	200 to 400	1	2	3	Unity	N/A	++	N/A
H6 in mid diodes-1 [34]	6	2	1	0	≤ 200	159 to 240	1	2	3	0.9937	1.86	++	97.33 @ 1 kVA
H6 with diodes-2 [34]	6	2	1	0	≤ 200	150 to 249	1	2	3	Unity	N/A	+++	97.31 @ 1 kVA
Improved H6 in mid diodes-1 [64]	6	2	1	0	≤ 20	190 to 200	1	2	3	0.9	N/A	+++	96.5 @ 4 KVA
H6 -1 [35]	6	0	1	0	≤ 200	151 to 258	1	2	3	Unity	1.7	++	97.22 @ 1 kVA
H6 in mid switch [36]	6	0	1	0	≤ 200	159 to 240	1	2	3	Unity	N/A	++	N/A
Hybrid bridge [30]	6	2	1	0	≤ 250	158 to 241	1	2	3	Unity	N/A	+++	94.75 @ 1 kVA
ZCT-H6-1 [65]	8	3	4	2	≤ 250	N/A	1	2	3	Unity	N/A	++++	95.6 @ 1 kVA
SCF-H6-1 [66]	8	2	4	2	≤ 150	N/A	1	2	3	Unity	N/A	++++	96.25@ 1 kVA
Inverter topology in [67]	4	2	1	0	≤ 150	N/A	1	6	3	0.9	3.6	++++	98.2 @ 2 kVA
Inverter topology in [68]	6	0	2	0	≤ 250	N/A	1	3	3	Unity	< 4.5	+++	94.8 @ 1.5 kVA
GCC-NPC [69]	6	2	2	1	≤ 20	N/A	1	1	3	Unity	4.08	++++	95.7 @ 2 kVA
Inverter topology in [70]	8	1	2	1	≤ 20	N/A	1	2	3	Unity	4.2	++++	96.11@ 220 VA
Inverter topology in [7]	8	0	2	0	≤ 20	N/A	2	2	3	Unity	4.35	++++	96@ 1 kVA
Inverter topology in [71]	6	2	1	1	≤ 150	N/A	1	2	3	Unity	N/A	+++	97.5@ 2 kVA
Inverter topology in [114]	8	4	4	2	≤ 100	N/A	1	3	3	Unity	< 4.61	++++	97.02@ 1.5 kVA
Inverter topology in [72]	7	3	4	4	≤ 100	N/A	1	1	3	0.7	N/A	++++	94.09@ 300 VA
Inverter topology in [115]	4	0	2	1	≤ 200	N/A	1	1	3	0.7	2.1	+++	95.8@ 100 VA
Inverter topology in [50]	6	0	3	0	≤ 20	N/A	1	3	3	0.95	N/A	+++	N/A
Inverter topology in [116]	5	2	4	2	≤ 40	N/A	0	1	3	Unity	N/A	++++	N/A

* including the input capacitor

The more "+" represents the higher cost, + ≡ low, ++ ≡ medium, +++ ≡ high, and ++++ ≡ extremely high.

In the above table, "C" represents capacitor, "L" represents inductor, "PF" power factor, "THD "total harmonic distortion

IV. THERMAL ANALYSIS AND LOSS CALCULATION FOR EFFICIENCY EVALUATION

Inverters are operated in a wide range of temperature and their operating temperature affects the overall system cost and efficiency. Therefore, the thermal analysis is an important aspect for the technical analysis of a power electronics system, which affects the required heat sink size, cooling system and thermal protection of the switches [117]-[125]. The temperature needs to be considered for each semiconductor devices from junction temperature (T_j) to case temperature (T_c). Fig. 45 shows the thermal impedance model which is related to the temperature.

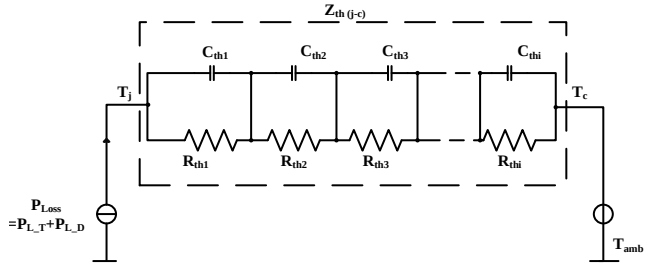


Fig. 45. Thermal impedance Foster- model used in circuit design.

The junction temperature depends on thermal capacities C_{th} and thermal resistances R_{th} through the following equations.

$$R_{th} = \frac{T_j}{\rho} = \frac{T_j}{Q/_t} \tag{9}$$

where ρ is the heat flow, Q is the flowing heat, and t is the time,

$$\frac{1}{C_{th}} = \frac{T_j}{Q} \tag{10}$$

The total impedance is

$$Z_{thi}(t) = \frac{\Delta T}{P} = \sum_{i=1}^{n} R_{thi}(1 - e^{-\frac{t}{\tau_{thi}}}) \tag{11}$$

where ΔT is the temperature between different nodes in the system, n is the number of exponential terms to fit $Z_{th}(t)$ to the transient thermal impedance curve, P is the power dissipation, and

$$\tau_{thi} = R_{thi}.C_{thi} \tag{12}$$

On the other hand, the power losses (IGBT (P_{L_T}) + diode (P_{L_D})) are dependent on the junction temperature and case temperature as shown in (13).

The junction temperature can be expressed as follows

$$T_j = \mathrm{P_{Loss}}.Z_{th(j-c)} + T_c \tag{13}$$

The junction temperature of the IGBT can be calculated by the following equation

$$T_{j-IGBT} = T_H + \mathrm{P_{avg.IGBT\ Loss}}(\mathrm{R_{th-IGBT}} + \mathrm{R_{th(ch-IGBT)}}) \tag{14}$$

The junction temperature of the diode can be calculated by the following equation

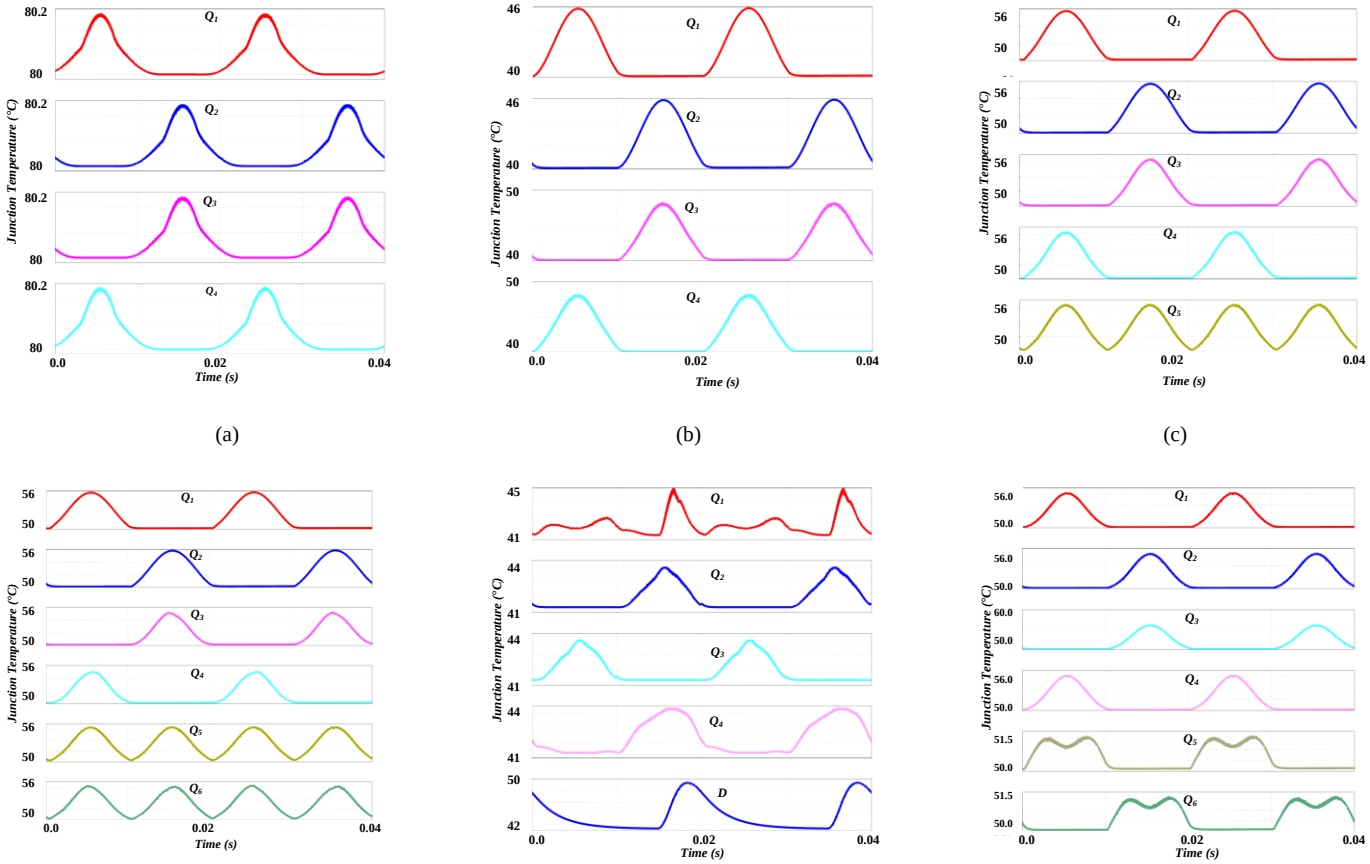
$$T_{j-diode} = T_H + \mathrm{P_{avg.Diode\ Loss}}(\mathrm{R_{th-diode}} + \mathrm{R_{th(ch-diode)}}) \tag{15}$$

The heatsink temperature can be found as given in (16).

$$T_H = T_{amb} + \mathrm{R_{th-H}}(\mathrm{P_{avg.IGBT\ Loss}} + \mathrm{P_{avg.Diode\ Loss}}) \quad (16)$$

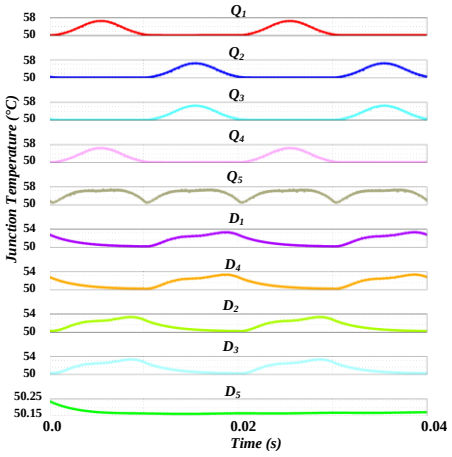
where T_{amb} represents the ambient temperature, and $\mathrm{R_{th-H}}$ stands for the thermal resistance between the heat sink and the environment.

Fig. 45 illustrates the junction temperature curves of the semiconductors in turn-ON and turn-OFF conditions. The maximum junction temperature is related to the bipolar F-B inverter [62], and hence the maximum losses occur through the switches, which are almost identical for all switches (see Fig 46 (a)). The junction temperature is dramatically reduced for all switches in the unipolar F-B inverter, where two switches (Q_1 and Q_2) are operated at a slightly lower temperature than the other two switches (Q_3 and Q_4); see Fig. 46 (b). Fig. 46 (c) and Fig 46 (d) illustrate the junction temperature curves for H5 and H6 DC side semiconductor devices. In these topologies, the additional switches (Q_5 and Q_6) represent an increase in the junction temperature in both turn-ON and turn-OFF conditions according to the switching pulses. The topology presented in [5] demonstrates the lowest junction temperature and loss among the evaluated topologies (see Fig. 46(e)). Moreover, the junction temperature curves for semiconductor switches in HERIC and HB-ZVR topologies are illustrated in Fig 46 (f) and Fig. 46 (g), respectively.



(a) (b) (c)

(d) (e) (f)



(g)

Fig. 46. Semiconductor devices junction temperature curves in switching intervals, (a) Bipolar F-B topology, (b). Unipolar F-B topology, (c) H5 topology, (d) H6 DC side topology, (e) Topology in [5], (f). HERIC topology, and (g) HB-ZVR topology.

The loss analysis is verified through simulations for seven major topologies using the parameters listed in Table IV. The values of the individual devices are taken from the datasheets [120]-[121]. The power losses of the semiconductor switches are comprised of conduction losses and switching losses. Similarly, for diodes, the power losses comprise conduction and reverse recovery. The mathematical expressions of the losses of IGBT (conduction loss and switch turn-ON/OFF loss) and the diode (conduction loss and reverse recovery loss) are adopted from [110-116]. As discussed, the conduction losses of the semiconductor devices depend on the ON-state voltage $V_{ON}(t)$, and the instantaneous current *i(t)* [126]-[130].

The conduction losses or the ON-state losses are disclosed in (17) where the inverter fundamental period is T, and ON-state voltage is V_{ON} with the instantaneous current I_{ce} which is the IGBT collector emitter-current.

$$P_{\text{conduction loss}} = \frac{1}{T}\int_0^T (V_{ON}(t) \times I_{ce}(t))dt \tag{17}$$

The ON-state voltage (18) is the voltage across the collector and emitter; this voltage depends on the internal series resistance (r_T). In the time of conduction losses through the antiparallel diode of the switches, the diode current (I_D) flows through the internal diode resistance as shown in (19).

$$V_{ON}(t) = V_T(t) + r_T\, I_{ce}(t) \tag{18}$$

$$V_{ON}(t) = V_D(t) + r_D\, I_D(t) \tag{19}$$

On the other hand, the conduction losses of the diode occur at the active state through the forward voltage V_F and freewheeling current I_F as shown in (20) [35].

$$P_{\text{conduction loss}} = \frac{1}{T}\int_0^T \big(V_F(t) \times I_F(t)\big)dt \tag{20}$$

The turn-ON energy losses can be calculated by (21),

$$E_{ON} = E_{ON.T} + E_{ON.FD} \tag{21}$$

where $E_{ON.T}$ is the switch turn-ON energy without reverse recovery process, and $E_{ON.FD}$ is the switch turn-ON energy by considering the reverse recovery process. The peak reverse recovery current (I_{PRR}) is given in (22),

$$I_{PRR} = \frac{2 * Q_{RR}}{T_{RR}} \tag{22}$$

where T_{RR} is the reverse recovery time. Now, the diode reverse recovery losses are dependent on the reverse recovery energy $E_{ON.D}$ and diode voltage at the time of reverse recovery $V_{RR.D}$.

$$E_{ON.D} = \frac{1}{4} \times Q_{RR} \times V_{RR.D} \tag{23}$$

For the turn-OFF energy, the reverse recovery effect is negligible. From (18) and (21), the total turn-ON and OFF losses of the switches are obtained by (24).

$$E_T = E_{ON} + E_{ON.FD} + E_{OFF} \tag{24}$$

The total switching losses for the IGBT ($P_{IGBT.T}$) are

$$P_{IGBT.T} = \frac{I}{T} \sum_{n=1}^{\frac{f_{sw}}{f}} (E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) \tag{25}$$

where f_{sw} is the switching frequency. The reverse recovery losses for diode is

$$P_{D.T} = \frac{I}{T} \sum_{n=1}^{\frac{f_{sw}}{f}} (E_{ON}.D(n)) \tag{26}$$

The total IGBT losses are expressed in (27) for IGBT and (28) for the diode from (20), (23), (25), and (26)

$$\begin{aligned} P_{avg.IGBT\ Loss} &= P_{turn\ ON\ loss} + P_{turn\ OFF\ loss} + P_{conduction\ loss} \\ &= \frac{I}{T} \sum_{n=1}^{\frac{f_{sw}}{f}} (E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) + \frac{1}{T} \int_0^T (V_{ON}(t) \times I_{ce}(t)) dt \end{aligned} \tag{27}$$

$$\begin{aligned} P_{avg.Diode\ Loss} &= P_{reverse\ recovery} + + P_{conduction\ loss} \\ &= P_{D.T} = \frac{I}{T} \sum_{n=1}^{\frac{f_{sw}}{f}} (E_{ON}.D(n)) + \frac{1}{T} \int_0^T \big(V_F(t) \times I_F(t)\big) dt \end{aligned} \tag{28}$$

From (14) and (27), the total temperature for IGBT losses can be expressed as given in (29), and from (15) and (28), the total temperature for diode losses can be expressed in (30).

$$\begin{aligned} T_{j-IGBT} &= T_H + \Big(\frac{I}{T} \sum_{n=1}^{\frac{f_{sw}}{f}} (E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) \\ &+ \frac{1}{T} \int_0^T (V_{ON}(t) \times I_{ce}(t)) dt\Big)(R_{th-IGBT} + R_{th(ch-IGBT)}) \end{aligned} \tag{29}$$

$$T_{j-diode} = T_H + P_{D.T} = \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}.D(n)) + \frac{1}{T}\int_0^T \left(V_F(t) \times I_F(t)\right)dt)(R_{th-diode} + R_{th(ch-diode)}) \quad (30)$$

The power losses of each semiconductor device of the major transformerless topologies ([5], H5, H6 DC side, HERIC, and HB-ZVR) are shown graphically in Fig. 47. It is clear that the maximum power losses are associated with the FB bipolar topology. On the other hand, the lowest power losses in the semiconductor devices are achieved by the topology in [5] and the HERIC topology.

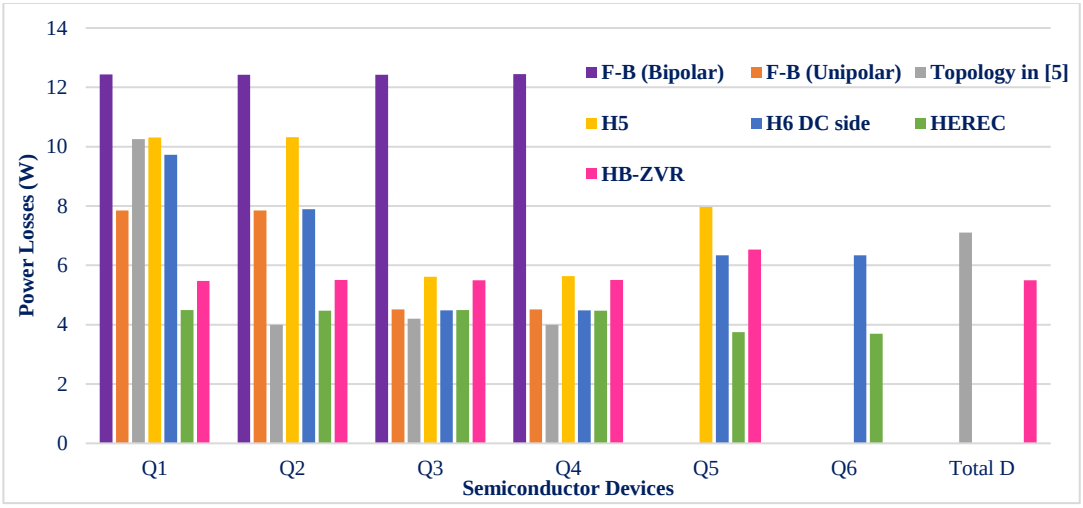


Fig. 47. Comparison of power losses for some of the transformerless inverter topologies for 1.8 kW rated power.

The losses are found for seven selected topologies where only the semiconductor device losses are revealed. Table VII displays the efficiency for different percentages of the output power. To find out the total efficiency, the filter losses have to be considered too.

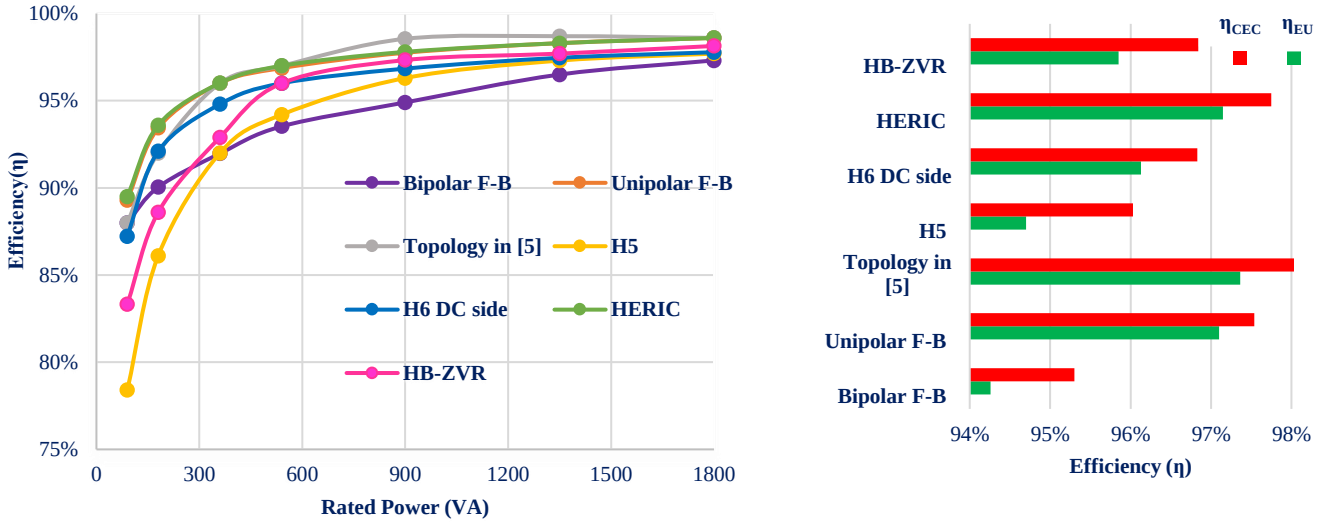


Fig. 48. Efficiency evaluations for major transformerless inverter topologies, (a) efficiency curves vs. output power, and (b) CEC and EU efficiencies.

The maximum efficiency is achieved by the topology in [5] (see Fig. 19 (b)) which is 98.06 % efficiency when selecting California Energy Commission (CEC) weighted efficiencies for calculation formula, and 97.36 % when selecting the European

(EU) weighted efficiencies. The formula for calculating the overall efficiencies are given in (31) and (32) for EU and CEC weighted efficiencies respectively. Fig. 48 illustrates the efficiency curve for different ranges of the output power as well as the overall efficiency.

$$\eta_{EU} = 0.03.\ \eta_{5\%} + 0.06.\ \eta_{10\%} + 0.13.\ \eta_{20\%} + 0.10.\ \eta_{30\%} + 0.48.\ \eta_{50\%} + 0.20.\ \eta_{100\%} \quad (31)$$

$$\eta_{CEC} = 0.04.\ \eta_{10\%} + 0.05.\ \eta_{20\%} + 0.12.\ \eta_{30\%} + 0.21.\ \eta_{50\%} + 0.53.\ \eta_{75\%} + 0.05.\ \eta_{100\%} \quad (32)$$

V. CONCLUSION

Single-Phase transformerless PV inverters have gained widespread attention due to the low cost/weight and high efficiency compared to single-phase inverters with galvanic isolation. In this paper, CM and i_{cm} analysis, and output filter design based on ripple factor are presented for single-phase transformerless inverters. Moreover, various single-phase transformerless inverter topologies are reviewed systematically based on their common mode and leakage current behaviour. The main principles of operation and required switching pulses for each topology are presented and compared for each category. Moreover, simulation results for each topology are also presented to give new insight into the understanding of CM and i_{cm} for safer operation of grid-connected PV system.

Finally, a theoretical power loss modeling and efficiency calculation are provided for major topologies, and an efficiency performance of different topologies is compared numerically. As a summary to this review, Table VI provides a comparative study of main single-phase transformerless inverter categories concerning their major characteristics (i.e., common-mode behaviour, leakage current, efficiency, reactive power transfer capability, component count, and complexity). Overall, the authors hope that this comprehensive review can be a useful resource to help both academic and industry readers comprehend transformerless inverter topologies and identify their respective pros and cons.

TABLE VI
QUALITATIVE SUMMARY OF THE MAJOR SINGLE-PHASE TRANSFORMERLESS INVERTER TOPOLOGIES.

Transformerless Inverter Topologies	Advantages	Disadvantages	Reactive Power Capability	Size of the Inverter	Efficiency	Recommended Topology
Common Ground Type Topologies	▪ No CM effect. ▪ Less semiconductor devices are used. ▪ Small filter required.	▪ Flying capacitor or switched capacitor or flying inductor controlling is difficult.	Yes	Small	Very high	Inverter topology in [5]
Mid-Point Clampling	▪ Constant CMV and low i_{cm}.	▪ Increased complexity. ▪ More semiconductor devices.	Yes	Large	Medium	HERIC Active 2 [39]
AC-Decoupling	▪ Low Conduction losses. ▪ Output current is not flowing through the antiparallel diodes of F-B. ▪ Lower THD.	▪ Additional switches required. ▪ Residual line frequency leakage current.	Yes	Medium	High	HERIC [31]
DC-Decoupling	▪ DC bypass switch helps to disconnect PV from grid during leakage current.	▪ High conduction losses. ▪ Additional devices required. ▪ Unbalanced switching.	Yes	Medium	Medium	H5 [32]
H6 Type Topologies	▪ Low output current ripple.	▪ Complex control ▪ More semiconductor devices. ▪ CMV is fluctuated.	Yes (except H6 with diodes-1 and H6 with diodes-2)	Large	Medium	H6-1 [35]
Buck-Boost Type Topologies	▪ Low i_{cm}	▪ High THD	Yes	Large	Medium	Inverter topology in [71]

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