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DC Fault Current Analyzing, Limiting, and Clearing in DC Microgrid Clusters

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Abstract: A new DC fault current limiter (FCL)-based circuit breaker (CB) for DC microgrid (MG) clusters is proposed in this paper. The analytical expressions of the DC fault current of a bidirectional interlink DC/DC converter in the interconnection line of two nearby DC MGs are analyzed in detail. Meanwhile, a DC fault clearing solution (based on using a DC FCL in series with a DC circuit breaker) is proposed. This structure offers low complexity, cost, and power losses. To assess the performance of the proposed method, time-domain simulation studies are carried out on a test DC MG cluster in a MATLAB/Simulink environment. The results of the proposed analytical expressions are compared with simulation results. The obtained results verify the analytical expression of the fault current and prove the effectiveness of the proposed DC fault current limiting and clearing strategy.

Keywords: DC microgrid; fault; cluster; DC/DC converter; fault current limiter (FCL)

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1. Introduction

DC microgrids (MGs) have attracted wide attentions over the last years in both industry and academia. At the point of practical applications, DC MGs make sense to be used because important types of distributed energy resources (DERs), such as fuel cells (FCs), photovoltaic (PV) arrays, wind turbines (WTs), and battery energy storage systems (BESSs), and also many types of electronics loads are DC [1]. The DC MGs have demonstrated superiority over the alternating current (AC) MGs from the viewpoints of reliability, efficiency, control complexity, penetration of renewable energy resources, and connection of DC loads [2–4]. Despite these significant advantages, designing and implementing a suitable protection scheme for DC MGs remains an important challenge [5]. The protection challenges in the rapid rise of DC fault current and the absence of a naturally occurring zero crossing point potentially lead to sustained arcs. To address the DC MG protection challenges, proper grounding architectures, fast fault current limiting methods, efficient fault detection/location strategies, and well-designed DC circuit breakers are required [6].

As a solution for better power support, the DC MG clusters are designed with the help of bidirectional interlink DC/DC converters [7]. One or several DC MGs can be connected to the AC grid by bidirectional interlink AC/DC converters. Due to the bidirectional current in the interconnected link between DC MGs, a bidirectional DC/DC converter should be implemented in these lines. In [8], a bidirectional DC/DC converter has been presented for connecting two adjacent DC MGs. This converter has two functions: operating as a

boost converter during the power flow from the low voltage (LV) to the high voltage (HV) side, and as a buck converter during the power flow from HV to the LV side. DC MGs can be connected to the main utility grid via a modular multilevel converter (MMC) [9–11]. Due to the modular structure of MMCs, it is not necessary to connect the power electronic devices in series, and so the difficulties of manufacturing are reduced [12]. The MMC system provides a suitable output for modulated current and voltage. Therefore, these systems are widely used in AC/DC converter applications [13].

Up to now, most of the reported studies on the DC MG clusters have been focused on the control [14–17], switching network topology [18], power scheduling mechanism [19], management [20], and resiliency [21] of these systems. When the DC MG clusters consist of several DC systems and the connection to the utility grid, the DC fault characteristics and corresponding fault clearing solutions should be analyzed in depth. In Table 1, the focus of the reported studies on DC MG clusters is summarized to highlight the lack of enough investigations on the protection of these systems. In [22], an LV DC circuit breaker (CB) has been suggested for the protection of autonomous DC MG clusters. However, the interlink converter between individual DC MGs was not discussed in the paper. Moreover, the system under study has only been operated in islanded mode. In [23], the performance of a multiport DC/DC converter in a DC network has been analyzed to find solutions for protecting a DC network equipped with multiport converters and avoid the long clearing time of traditional DC CBs. A hybrid MMC (HMMC) with integrated BESS has been proposed in [24], and its performance during AC and DC grid faults has been analyzed. In [25], the fault analysis method has been presented for a simple AC/DC voltage source converter for a DC MG application.

Table 1. Comparison of the reported studies on DC MG clusters.

Reported Study	Focusing Area	Operation Mode
[14]	Communication-based control	Grid-connected
[15]	Coordinated control	Islanded and grid-connected
[16]	Power flow control	Islanded
[17]	Modeling and control	Islanded
[18]	Switching network topology	Islanded
[19]	Power scheduling mechanism	Islanded
[20]	Power exchange management	Islanded
[21]	Resiliency	Grid-connected

DC fault isolation and limitation are the most essential technical obstacles during the fault in interconnection lines of DC MG clusters. Generally, there have been four solutions for solving these problems:

- Implementing AC CB at the AC side of the AC/DC converter for faults at the interconnection line between the AC grid and DC MG cluster: Several AC CB strategies have been investigated for LV AC MGs protection systems [26,27]. However, the slow response time of the AC CBs makes them unsuitable for implementation in the clustered DC MGs.
- Integrating FCL functionality into the converter of interconnection lines: FCL is deactivated during the normal operation of the system; however, during the fault, it adds a high resistance to the fault path to limit the value of the fault current [28]. In the literature, both AC FCL [29] and DC FCL [30] have been proposed for converter-based LV systems. However, the implementation of conventional FCLs in DC MG clusters suffers from high response time, cost, size, and installation complexity [31].
- Implementing DC CB in series to the DC/DC converter for faults at the interconnection line between the two adjacent DC MGs: In [32], a hybrid DC CB has been presented to break the DC fault current up to 9 kA within 5 ms. However, existing DC CBs have some disadvantages, such as low technology maturity and high manufacturing cost.
- Implementing fault limiting capability in the converter control: Some of the reported strategies have suggested active FCL strategies for the AC/DC converters to limit the

fault current and enhance the fault-ride-through (FRT) capability of MGs [33,34]. Converter limits the fault current to two times the nominal value to prevent overheating. Therefore, for adopting this option in the converters, more powerful electronic devices are required, and the power losses and the cost of the system increase [35].

By reviewing the previous literature, it has been found that there is a lack of study on the fault analysis of the bidirectional DC/DC converter as the interlink of DC MG clusters. This paper proposes an analytical expression of the current of a DC MG cluster under fault conditions. First, the analytical model of the fault current of the AC/DC converter between the grid and DC MG is presented. Second, the analytical model of a bidirectional interlink DC/DC converter of the interconnection line between two adjacent DC microgrids in a clustered DC MG is derived in detail. Then, a DC fault clearing strategy is proposed based on using a DC FCL in series with a DC circuit breaker. Finally, the performance of the proposed method is evaluated based on time-domain simulation studies on a test DC MG cluster in MATLAB/Simulink environment. The simulation results are also compared with the results of the proposed analytical model. The obtained results verify the analytical expression of the fault current and prove the effectiveness of the proposed DC fault current limiting and clearing strategy. The main salient features of this presented study are as follows:

i. A detailed analysis of converters during short circuit faults is investigated, which allows the better design of converters during faults. It can also model the converter behavior during different stages of fault by transient equations.
ii. An accurate transient analysis of DC MG clusters during fault by considering the characteristic of converters is presented. Therefore, the importance of the current limiting of interconnected lines between converters is highlighted and investigated.
iii. A DC FCL is proposed for interconnected DC MG clusters, which has a higher speed, lower coordination problems, and power losses make it different from existing FCL strategies. Moreover, the proposed method is designed and specified for DC MG clusters, which have a few studies on the protection of these systems.

The rest of the paper is organized as follows: The structure of the DC MG cluster is discussed in Section 2. The analytical expression of the AC/DC converter is presented in Section 3. Section 4 proposes the detailed analytical expression of the bidirectional DC/DC converters in the DC MG cluster. In Section 5, a strategy is presented for limiting and clearing the DC fault in the DC MG cluster. Section 6 is dedicated to the simulation results and discussion to verify the performance and demonstrate the accuracy of the presented analytical equations. Finally, conclusions are stated in Section 7.

2. DC MG Cluster

The structure of a sample DC MG cluster consisting of two DC MGs is depicted in Figure 1, and the parameters are presented in Table 2. Neighboring DC MGs can be connected by a bidirectional DC/DC converter. Because a DC MG cluster can operate in grid-connected mode, one or several DC MGs are connected to the upstream AC utility grid by AC/DC converters. Both DC MGs in this cluster are connected to the AC grid by AC/DC MMCs. Increasing the number of connections increases the probability and the current level of a fault. Therefore, detailed fault analysis is an important task in these systems. In this paper, only the faults in the interconnected lines between one of the DC MGs to the AC/DC MMC are investigated, as mentioned by *F1* and *F2* in Figure 1. For example, *F1* is a candidate scenario for a fault at the interconnected link between grid and DC microgrids. The highest possible fault current usually belongs to the interconnected lines because typically, these lines have the highest power transfer capability and connect two main buses. Figure 2a,b illustrate the structure of an AC/DC MMC. Each sub-module (SM), as shown in Figure 2c, consists of two IGBTs, two freewheeling diodes, and a cell capacitor [36]. The modulation strategy of this scheme is different from the two-level voltage source converters (VSCs), which makes high-quality waveforms and low switching losses. Section 3 discusses the fault characteristics of this type of converter in a DC MG cluster.

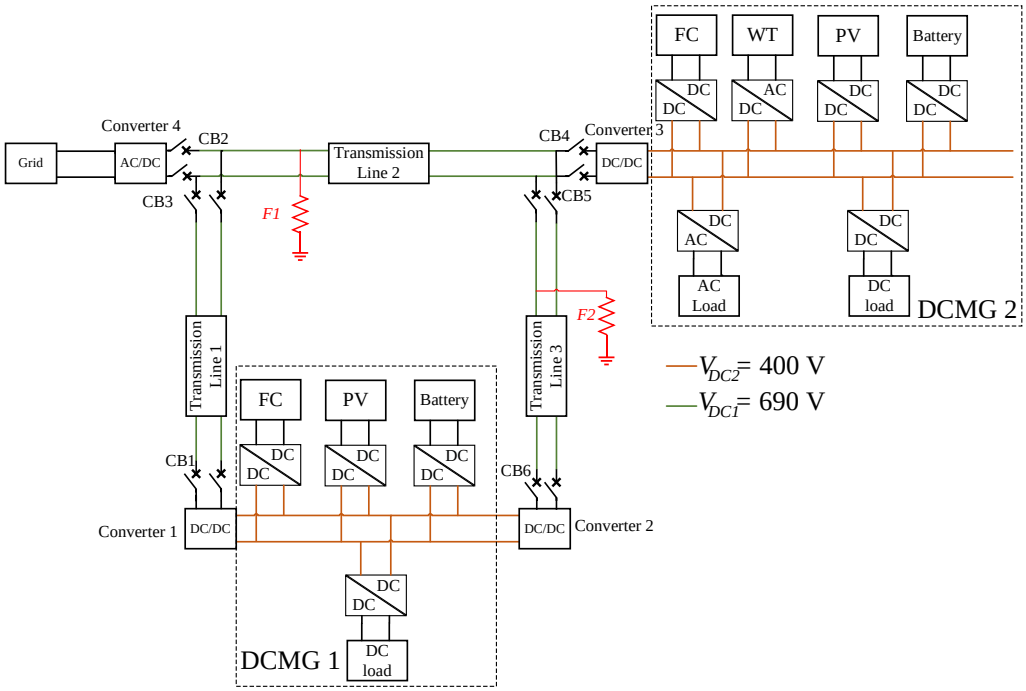

Figure 1. Structure of a DC MG cluster.

Table 2. Main parameters of the case study.

Component	Rated Value
Inductor of DC/DC converter	5 mH
Capacitor of DC/DC converter, C1	500 μF
Capacitor of DC/DC converter, C2	5000 μF
Resistance of DC/DC converter	1.358 mΩ
Capacitor of AC/DC converter	600 μF
Inductance of AC/DC converter	76 mH
Resistance of DC/DC converter	1.5 mΩ
Nominal voltage of VDC1	690 V
Nominal voltage of VDC2	400 V
Line resistance	1.6 mΩ/m
Line inductance	0.1 mH/m

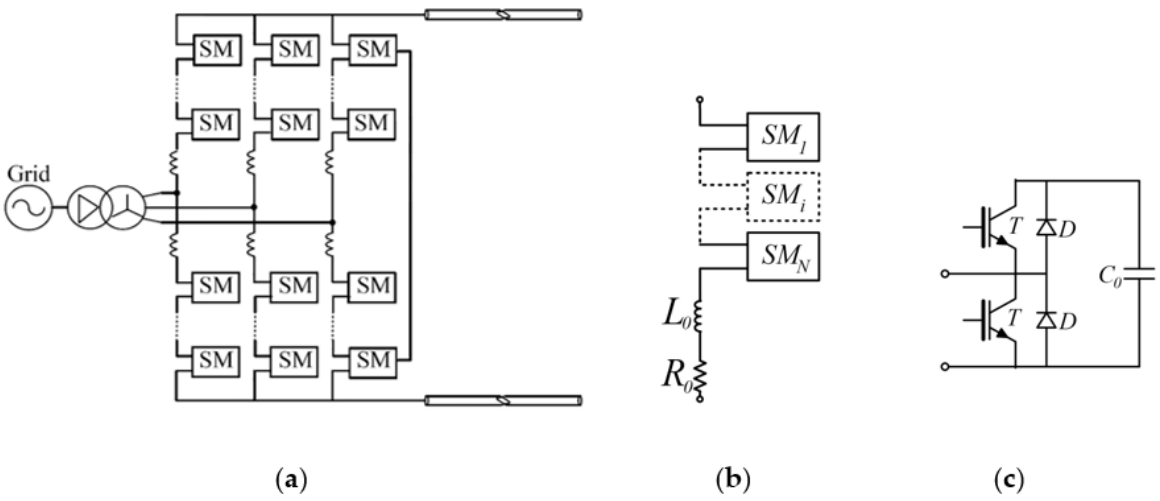

Figure 2. (**a**) Structure of an AC/DC MMC, (**b**) structure of each arm, (**c**) equivalent model of SM.

In Figure 3, a bidirectional DC/DC converter for use in the interconnection line between two adjacent DC MGs is represented, as shown in Figure 1 for converters one to three. This type of converter for managing the bidirectional power flow between two DC MGs has been introduced in [9]. This converter is a boost converter when power flow is from the LV (V_{DC2}) side to the HV (V_{DC1}) side, and a buck converter for power flow from the HV to the LV. Therefore, during the normal operation mode, this converter meets an appropriate bidirectional power sharing and voltage regulation among the DC MGs. The detailed fault analysis of this converter in the DC MG cluster is discussed in Section 4.

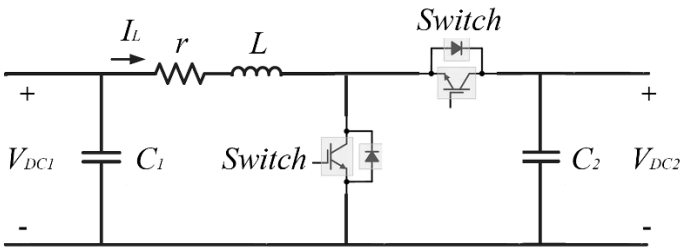

Figure 3. Structure of a bidirectional DC/DC converter.

3. DC Fault Analysis of AC/DC Converter

The previous literature has presented the two stages of a fault in the converters, namely capacitor-discharge and freewheeling diode operation. With the onset of a fault, the capacitors are discharged into the cable, and a high-rise current flows through it. Then, after a few milliseconds, the voltage of the terminal of the converter gets reversed, and the diodes start conducting. It should be noted that due to the surge energy in converters during the capacitor discharge stage, caused by high *di/dt*, the main damages to power electronic converters happen during the capacitor discharge stage [37].

The fault current starts with the capacitor discharge state, which has the highest magnitude of the current. Each SM of the interface AC/DC converter between the grid and the DC MGs includes a capacitor, inductance, and resistance, as shown in Figure 2b. The values of R_0, C_0, and L_0 are assumed to be the equivalent resistance, capacitor, and inductance of all SMs in each arm, respectively. According to [38], the value of the fault current of the DC side, F_1 fault in Figure 1, during the capacitor discharge state is given by

$$I_{DC}(s) = \frac{1}{s^2(\frac{2}{3}L_0 + L_{DC}) + s(\frac{2}{3}R_0 + R_{DC}) + \frac{N}{6C_0}} \tag{1}$$

by using inverse Laplace transform of Equation (1), the time domain equation of fault current is obtained as:

$$i_{DC}(t) = -\frac{1}{sin\theta} Ae^{-\frac{t}{\sigma}} sin(\omega_{DC}t - \theta) + Be^{-\frac{t}{\sigma}} sin(\omega_{DC}t) \tag{2}$$

where, L_{DC} and R_{DC} are the inductance and resistance of the DC line, respectively. N shows the number of SMs in each arm. The values of A and B are calculated by the initial values of the current and voltage of the AC/DC converter and

$$\theta = arctan(\sigma\omega_{DC}) \tag{3}$$

$$\sigma = \frac{4L_0 + 6L_{DC}}{2R_0 + 3R_{DC}} \tag{4}$$

$$\omega_{DC} = \sqrt{\frac{2N(2L_0 + 3L_{DC}) - C_0(2R_0 + 3R_{DC})^2}{4C_0(2L_0 + 3L_{DC})^2}} \tag{5}$$

After the DC line's voltage reaches zero, the voltage of the terminal gets reversed, and diodes start to conduct. Therefore, each SM could be modeled by a resistance, an

inductance, and a capacitor. According to [39], the lower and upper arm currents of MMC could be calculated by

$$\begin{cases} i_{pa}(t) = A_0 + \sum\limits_{n=1}^{\infty} A_n sin(n\omega t + \varphi_n) \\ i_{na}(t) = A_0 + \sum\limits_{n=1}^{\infty} (-1)^n A_n sin(n\omega t + \varphi_n) \\ i_a = i_{pa}(t) - i_{na}(t) = \sum\limits_{n=2k-1}^{\infty} 2A_n sin(n\omega t + \varphi_n) \end{cases} \quad (6)$$

where, i_{pa} and i_{na} are upper and lower arm currents, respectively. i_a is the current from the AC side, A_0 and A_n are the DC component and nth harmonic of the current of the arm, and k is a positive integer. The harmonic orders in i_{pa} higher than A_0 and A_1 are assumed to be zero, and by applying Kirchhoff's voltage law to Figure 2, the following equation can be obtained

$$\begin{cases} u_{AC} = L_{ac}\frac{di_a}{dt} + L_0\frac{di_{pa}}{dt} \\ u_{AC} = Usin(\omega t + \beta) \end{cases} \quad (7)$$

where, u_{ac} is the voltage of the AC side, and U is the magnitude of this voltage, L_{ac} is the inductance of the AC line, and β is the angular displacement of the harmonics in the upper and lower arm currents. Therefore, by comparing Equations (6) and (7), the $A_n = 0$ for n = 2, 3, 4. Consequently, the value of the DC fault current during the freewheeling stage is obtained as

$$i_{pa}(t) = \frac{U}{2\omega L_{ac} + \omega L_0}(1 - cos(\omega t + \beta)) \quad (8)$$

It should be noted that Equation (8) represents the steady-state performance of the converter after the blocking stage. It takes some time for DC current to vary from the blocking moment to the steady state. This process can generally be modelled by a first-order inertia behavior. Therefore, the complete expression of DC current can be shown by

$$i_{dc}(t) = I_{dc\infty} + (I_{dcBlock} - I_{dc\infty})e^{-\frac{t}{\tau_{dcBlock}}} \quad (9)$$

where, $I_{dc\infty}$ is the peak of (8), $I_{dcBlock}$ is the initial DC current after MMC blocking, and $\tau_{dcBlock}$ is the first-order inertia time constant. For practical systems, $\tau_{dcBlock}$ is between 10 ms to 200 ms [39].

4. DC Fault Analysis of DC/DC Converter

A DC fault in the interlink DC/DC converter between two adjacent DC MGs (F_2 fault in Figure 1) is a severe condition for near to fault converters. During a fault, the fault analysis should be done in two states. The first state is the response of the RLC equivalent circuit due to the DC link capacitor discharge of the bidirectional DC/DC converter. The second stage starts after the current magnitude reaches the maximum value and consequently, the voltage of the capacitor reaches zero.

4.1. Analysis of Capacitor Discharge

After a fault, at the first step, capacitors start discharging through the cable impedance and the equivalent circuit of the bidirectional DC/DC converter in a DC MG cluster, as shown in Figure 4. R_L and L_L are the resistance and inductance of the cable, respectively, and R_f is the fault resistance.

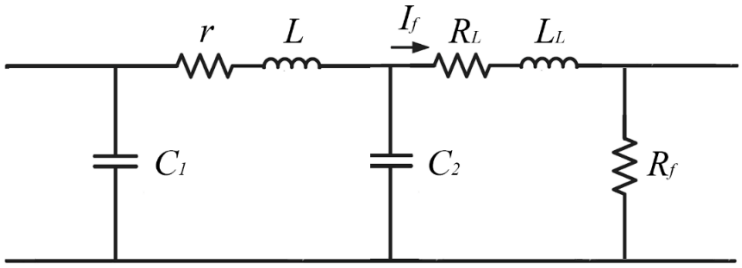

Figure 4. Equivalent circuit of DC/DC converter during capacitor discharge.

The RLC circuit response in the frequency domain can be obtained by Equation (11).

$$I_f(s) = \frac{LL_LC_2is^3 + s^2(C_2u_2L + L_LrC_2i) + s(Li + L_Li + C_2u_2r + \frac{C_2}{C_1}L_Li) + u_1 + \frac{C_2}{C_1}u_2}{LL_LC_2s^4 + s^3(RC_2L + rL_LC_2) + s^2(RrC_2 + L + L_L(1 + \frac{C_2}{C_1})) + s(r + \frac{RC_2}{C_1} + R) + \frac{1}{C_1}} \tag{10}$$

where, u_1 and u_2 are the initial voltages of the C_1 and C_2, respectively, and i is the initial value of the current of the converter. r and L are the internal resistance and inductance of the DC/DC converter, respectively, and $R = R_f + R_L$. The fault current in the time domain can be calculated by solving the differential Equation of (11).

$$LL_LC_2\frac{d^4I_f}{dt^4} + (RC_2L + rL_LC_2)\frac{d^3I_f}{dt^3} + (RrC_2 + L_L + L + L_L\frac{C_2}{C_1})\frac{d^2I_f}{dt^2} + (r + R + R\frac{C_2}{C_1})\frac{dI_f}{dt} + \frac{1}{C_1}I_f = 0 \tag{11}$$

Due to the low length of the cable between two adjacent DC MGs, the value of line inductance is very small. Therefore, assuming $L_L = 0$, Equation (11) is simplified as Equation (12)

$$(RC_2L)\frac{d^3I_f}{dt^3} + (RrC_2 + L)\frac{d^2I_f}{dt^2} + (r + R + R\frac{C_2}{C_1})\frac{dI_f}{dt} + \frac{1}{C_1}I_f = 0 \tag{12}$$

And the fault current is calculated as

$$I_f(t) = Ae^{-\alpha t} + Be^{-\lambda t}cos(\mu t) + De^{-\lambda t}sin(\mu t) \tag{13}$$

where, the value of A, B, and D are calculated by the initial values of capacitors voltages. α, μ, and λ are obtained by the Equations (14)–(16)

$$\Delta_0 = R^2r^2C_2^2 + L^2 - LRrC_2 - 3R^2C_2L \tag{14}$$

$$\Delta_1 = 2R^3r^3C_2^3 - 3R^2r^2C_2^2L - 3RC_2rL^2 + 2L^3 - 9R^3rC_2^2L - 9R^2C_2L^2 + \frac{27R^2C_2^2L^2}{C_1} \tag{15}$$

$$\zeta = \sqrt[3]{\frac{\Delta_1 \pm \sqrt{\Delta_1^2 - 4\Delta_0^3}}{2}} \tag{16}$$

Then, Equation (16) has three different roots, one of them is a real number, and two of them are complex. The real value is α, the real part of the complex values is λ, and the imaginary parts are $\pm\mu$.

$$\tau = \frac{1}{3RC_2L}(\mathrm{R}rC_2 + L + \delta^k\zeta + \frac{\Delta_0}{\delta^k\zeta}) \tag{17}$$

where δ is

$$\delta = -\frac{1}{2} \pm \frac{\sqrt{3}}{2}j \tag{18}$$

where, j is the imaginary unit, δ defines the three roots of Equation (16), and k is 0, 1, and 2.

4.2. Freewheeling Diode Operation

The second step of the fault current analysis is the freewheeling diode stage. This stage starts after DC-link capacitors' (C_1 and C_2 in the equivalent circuit of Figure 5) voltages reach zero. Then, the converter terminal voltage is reversed and makes a diode-capacitor equivalent circuit, as depicted in Figure 5.

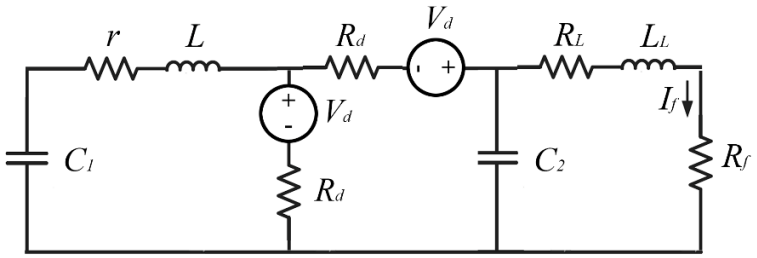

Figure 5. Equivalent circuit of DC/DC converter during the freewheeling diode operation.

The differential equation of the fault current during the freewheeling diode stage for calculating the fault current in the time domain is shown in Equation (19).

$$\begin{aligned}(2R_dRC_2L)\frac{d^3I_f}{dt^3} + \left((R+2R_d)L + 2R_dRC_2r + R_d^2RC_2\right)\frac{d^2I_f}{dt^2} \\ +(Rr + (R+2r)R_d + \frac{2R_dRC_2}{C_1} + R_d^2)\frac{dI_f}{dt} + (\frac{R+2R_d}{C_1})I_f = 0\end{aligned} \tag{19}$$

R_d is the diode resistance, and consequently, the fault current in the time domain is obtained by

$$I_f(t) = \frac{2V_d}{2R_d + R} + Ee^{-vt} + Fe^{-\eta t}cos(\Psi t) + Ge^{-\eta t}sin(\Psi t) \tag{20}$$

where, V_d is the voltage of the diode, and E, F, and G are defined by using initial values of the freewheeling diode stage. η and Ψ are the real and imaginary parts of Equation (23), respectively, and v is the real value of Equation (23).

$$\begin{cases} a_1 = 2R_dRC_2L \\ a_2 = RL + 2R_dRC_2r + R_d^2RC_2 + 2R_dL \\ a_3 = Rr + RR_d + \frac{2R_dRC_2}{C_1} + 2rR_d + R_d^2 \\ a_4 = \frac{R+2R_d}{C_1} \end{cases} \tag{21}$$

$$\begin{cases} b_1 = {a_2}^2 - 3a_1a_3 \\ b_2 = 2a_2^3 - 9a_1a_2a_3 + 27a_1^2a_4 \\ b_3 = \sqrt[3]{\frac{b_2 \pm \sqrt{b_2^2 - 4b_1^3}}{2}} \end{cases} \tag{22}$$

$$\Gamma = \frac{1}{6R_dRC_2L}(a_2 + \delta^k b_3 + \frac{b_1}{\delta^k b}) \tag{23}$$

5. DC Fault Clearing and Limiting Solution

In this section, a novel DC FCL-based CB configuration is presented as a solution for installing a lower-rate CB and limiting the fault current. Figure 6 depicts the schematic connection of the proposed DC FCL-based CB including a rectifier bridge, a resistor, an inductance, a capacitor, and also a DC CB which is connected in series with the DC/DC converter of Figure 1 in the interconnected line. Herein, the FCL is installed before the converter, which is used to achieve the energy transmission and conversion between DC MGs. Note that the proposed FCL can operate in both the normal and fault operation mode of the system. The basic concept of the proposed DC FCL-based CB operation uses a novel FCL in series with DC CB to reduce the fault current before clearing the fault by CB. It offers a soft current clearing and a lower fault current.

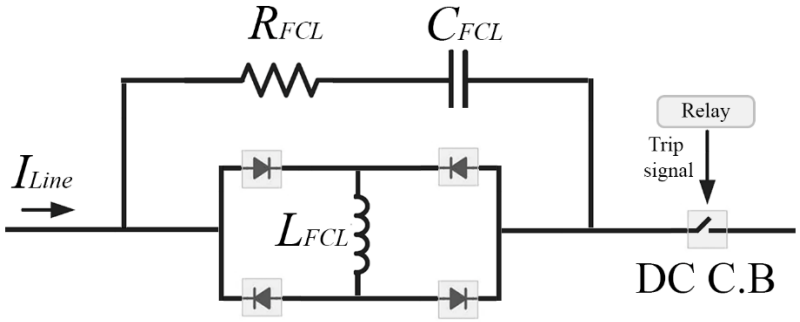

Figure 6. Proposed DC FCL configuration.

It should be noted that in Figure 6, it is necessary to use a diode bridge in the DC link; otherwise, the ripple of current generates a voltage drop, which will have an impact on the performance of the normal operation of connected converters. The DC FCL is composed of three main parts:

i. A diode rectifier bridge;
ii. A series inductor;
iii. A shunt RC branch for fault current reduction.

Furthermore, in the proposed DC FCL, the diode bridge composed of four diodes is utilized to enable the bidirectional current-flowing function, replacing the anti-parallel structure of the half and full-controlled switches. It also improves the economic considerations, due to lower price of diodes than the half and full-controlled switches. However, the forward voltage of diodes altogether causes a small voltage drop, but, in comparison to the total voltage drop in line, this voltage drop is negligible and has an insignificant impact on the normal operation [40].

The DC FCL-based CB operation is divided into two modes, namely normal and fault operation mode. During the normal operation mode, as shown in Figure 7a, the line current only flows through the inductor, and since the normal current of the system is DC, the overall power losses of inductance are relatively low, and they depend on the reactor copper loss. As shown in Figure 7b, during the fault, depending on the frequency components of the fault current, the capacitor branch absorbs some part of the fault current, and the inductance makes an impedance path for this current. The equivalent impedance of the DC FCL-based CB during the fault is obtained as

$$Z_{FCL} = \frac{s(LRCs + L)}{LCs^2 + RCs + 1} \tag{24}$$

where, L, R, and C are the inductance, resistance, and capacitance of the DC FCL-based CB, respectively. In the frequency domain, the size of the impedance of FCL for the fault current limiting stage is calculated as

$$|Z_{FCL}| = \frac{(L\Psi)(\sqrt{R^2C^2\Psi^2 + 1})(\sqrt{(1 - LC\Psi^2) + R^2C^2\Psi^2})}{(1 - LC\Psi^2)^2 + R^2C^2\Psi^2} \tag{25}$$

where, Ψ is the frequency of the current during the freewheeling diode operation mode, and then during the capacitor discharge stage, it will be replaced by μ, as explained in Equation (16). Based on Equation (25), the fault current magnitude is reduced by the coefficient of $1/|Z_{FCL}|$, as the total impedance of FCL during fault conditions. Therefore, the value of Z_{FCL} should be selected as higher than 1 Ω, to operate as a fault current reducing component. To determine the parameters of FCL, the thermal resistance of the

equipment should be considered [3] to find the reduction value. Therefore, the objective value of Z_{FCL} can be determined by:

$$\begin{aligned} &\frac{I_{obj}}{I_{peak}} = \frac{1}{|Z_{FCL}|} \\ &\text{Subject to :} \\ &L_{\min} \le L \le L_{\max} \\ &R_{\min} \le R \le R_{\max} \\ &C_{\min} \le C \le C_{\max} \end{aligned} \tag{26}$$

where, I_{obj} is the final value of fault current after reduction, and I_{peak} is the peak of fault current before reduction. The values of R, C, and L should be in the range of minimum and maximum values of existed components. Therefore, the proposed DC FCL parameters can have different values based on cost and existing components, which causes a better availability of the design of this FCL.

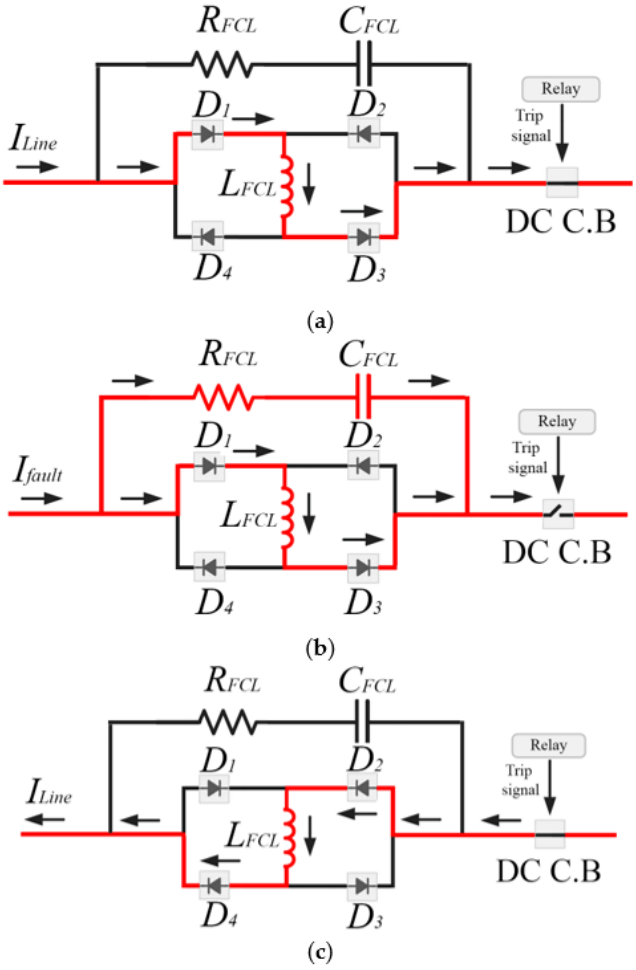

Figure 7. DC FCL-based CB and current flow (**a**) normal, (**b**) fault, (**c**) bidirectional condition.

During normal operation, as long as the DC current direction is positive, as shown in Figure 7a, the diodes D_1-D_3 are in conducting state. On the other hand, during the negative DC current direction, as shown in Figure 7c, the diodes D_2-D_4 are in conducting state. In this situation, the DC reactor L_{FCL} is bypassed from the DC line, thus, having no impact on the DC grid during normal operations. After a fault, the DC fault current rises rapidly to a high magnitude. As shown in Figure 7b, due to the high frequency of the DC fault current, the RC circuit will be paralleled with inductance to limit the fault current to the desired value. Moreover, this bridge-type FCL can deal with the bidirectional fault current limitation in the DC systems.

The modeling of the DC FCL-based CB has been based on the consideration of the transient impedance during the fault, since they are effective parameters in the study of the behaviors of the fault current. From Figure 1, an AC-DC converter is utilized to convert the AC grid power to the DC MG cluster power. Due to the existence of the power electronic components and controllers, the transient impedance of the proposed method is obtained by (25), which is different from the normal operation mode. The access of DC FCL-based CB helps to increase the impedance of the system and the damping factor, for decreasing the fault current from the two aspects. Meanwhile, this current reduction will help relays to keep their settings during variations of fault resistances.

In order to avoid the negative impacts of the directly installed DC reactors, the bridge-type FCLs are implemented in the DC grids. The implemented bridge-type FCL in a DC system consists of an H-bridge composed of four series diodes, and a branch composed of the series-connected DC reactor. Therefore, it can avoid the negative impact of the DC reactor on a system in normal operation. However, during normal operation, the rated current will flow through diodes in the bridge-type FCL, thus leading to a small power loss [30].

During normal operation, the current of the DC inductor is an almost ripple-free DC current with a magnitude equal to the peak of the DC-link current. Therefore, the ripple current in the DC inductor of FCL is approximately zero, and then, the average current in FCL in normal operation is equal to the peak value of DC-link current in steady-state. Consequently, the total power losses of DC FCL (P_{Loss}) is the sum of power losses of DC inductor ($P_{Inductor}$) and diode-bridge (P_{Bridge}), and can be determined as follows [28]

$$\begin{cases} P_{Bridge} = 2V_d I_{Line} \\ P_{Inductor} = r_d I_{\max}^2 \\ P_{Loss} = I_{Line}(r_d I_{Line} + 2V_d) \end{cases} \quad (27)$$

where, I_{line} is normal current, V_d is the voltage drop of diodes, I_{max} is the peak value of DC-link current in steady-state, r_d is the resistance of the inductor. On the other hand, in a DC system without FCL, the normal flowing power can be defined by P_{DC}. Thus, the ratio of power losses to active flowing power is defined by K, and can be calculated by:

$$K = \frac{P_{Loss}}{P_{DC}} = \frac{I_{Line}(r_d I_{Line} + 2V_d)}{P_{DC}} \quad (28)$$

For example, consider the under-study system by V_{DC} = 690 V, r_d = 0.005 Ω, V_d = 2 V, I_{line} = 20 A. For this case, the value of K = 0.5%. This shows that in the presence of the proposed DC FCL, the total power loss has a very small percentage of the overall rated power of the system, and it will be acceptable in most practical applications. Furthermore, by using a superconductor inductor in DC FCL, the power loss of the inductor will be cancelled out, however, it increases the cost and weight of the system. Obviously, it is also possible to use a switch parallel with DC FCL to bypass it during steady-state conditions and avoid any power losses, however, it will increase the overall operation time of the proposed DC FCL.

6. Simulation and Real-Time Validation Results

In this section, the simulation results and discussion are presented for the case study system of Figure 1 with the parameters provided in Table 2. To validate the proposed fault analysis method, two cases are considered to obtain the fault current behavior for both AC/DC and DC/DC converters in the interconnected lines. In addition, the effectiveness of the proposed DC FCL-based CB is evaluated by using time-domain simulation studies in MATLAB/Simulink software environment and verified by comparing the proposed DC FCL with other reported FCL techniques.

6.1. Behavior of AC/DC Converter during the Fault

In the first part, the presented fault analysis of the AC/DC converter between the grid and the DC MG cluster, as represented in Section 3, is compared with the simulation results. Figure 8 shows the behavior of the fault current for a fault with a resistance of 0.1 Ω for both analytical results and simulation results. The results of Figure 8 show a small error between the analytical model and simulation results.

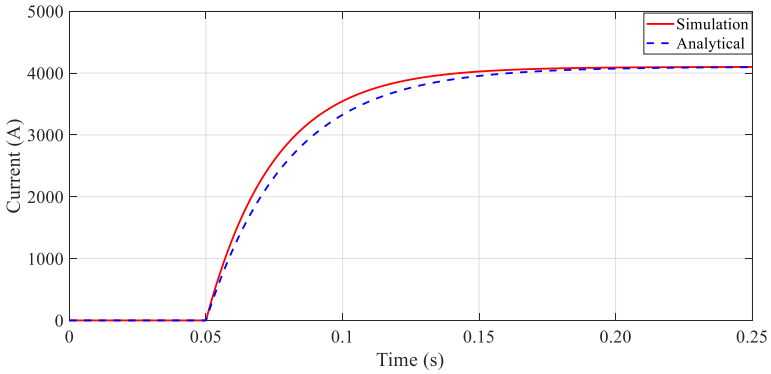

Figure 8. DC current of MMC during the fault.

6.2. Behavior of DC/DC Converter during the Fault

In Figure 9, the behavior of the DC/DC converter during a fault with a fault resistance of 0.1 Ω is presented for both analytical and simulation cases. During the capacitor discharge, the fault current reaches 6485 A in less than 0.03775 ms. One of the main parameters used for detecting the fault, as a threshold of the switching and relay settings, is the slope of the fault current. Therefore, this threshold is 171,788 kA/s and 158,616 kA/s by calculation using Equation (13) and simulation, respectively, which shows a small error of 7%. Thus, selecting the threshold by the proposed analytical equations is suitable for adjusting the setting of the relay. The parameters of Equations (13) and (20) for this case study are shown in Table 3.

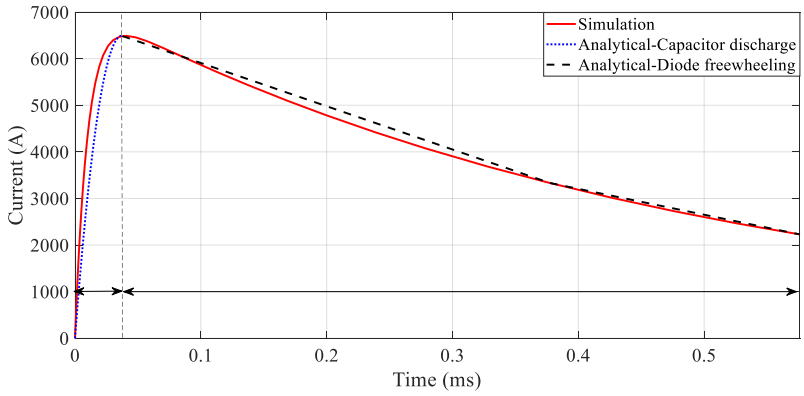

Figure 9. Comparison between analytical and simulation results.

Table 3. Parameters of the analytical model.

	Parameter	Value (s^{-1})
Capacitor discharge	α	2153
	λ	76
	μ	604
Freewheeling diode	υ	102×10^3
	η	2.157
	Ψ	88.5

6.3. Characteristics of DC FCL-Based CB during the Fault

By installing a DC FCL-based CB in series with a bidirectional DC/DC converter in the interconnected line between two DC MGs in a DC MG cluster, the desired maximum fault current magnitude is controlled by selecting a suitable value for resistance, inductance, and capacitance parameters of the DC FCL-based CB. According to the thermal resistance of the converter diodes [3], the maximum magnitude of the fault current is selected as 1100 A, and the equivalent impedance of FCL is calculated by Equation (25). The values of R_{FCL}, L_{FCL}, C_{FCL} are selected as 0.5 Ω, 0.1 H, and 2 mF, respectively. The fault current characteristic of the system equipped with DC FCL-based CB is shown in Figure 10. In Figure 11, the impact of the fault resistance on the performance of the proposed FCL is evaluated. The fault current peak of DC MGs reduces by increasing the fault resistance, and therefore, by using the proposed DC FCL scheme, fault current magnitude remains approximately constant. Furthermore, for low fault resistances, a considerable reduction in fault current is caused by using the proposed DC FCL scheme.

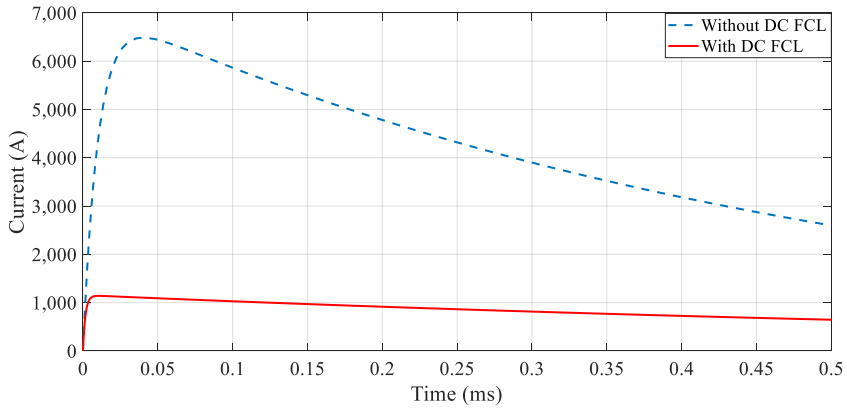

Figure 10. Impact of the DC FCL on the fault current.

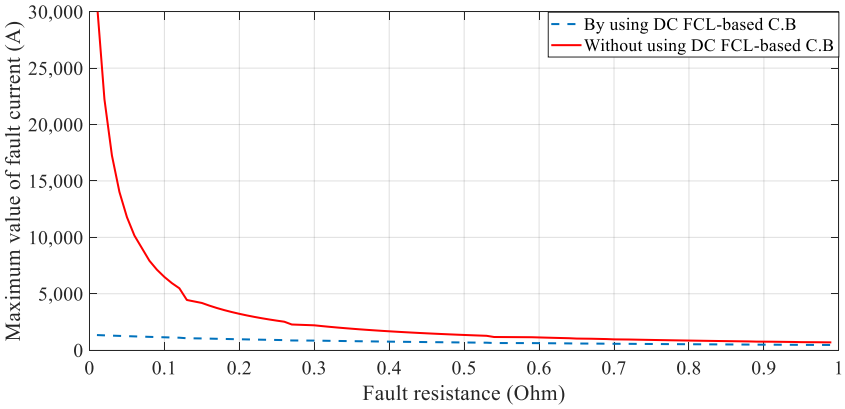

Figure 11. Performance of proposed DC FCL-based CB on the fault current.

In DC MG clusters, the fault current is injected from different sources. For example, in Figure 1, a fault at F1 with a fault resistance of 0.15 Ω causes a high-rise current from the DC MG and grid, as shown in Figure 12. Consequently, due to the converters' capacitor discharge, the fault current injected into the faulty point also has a high-rise peak, as represented in Figure 13. This high-rise current can damage the converters; therefore, installing the proposed DC FCL reduces the fault current to a lower level, as presented in Figure 13.

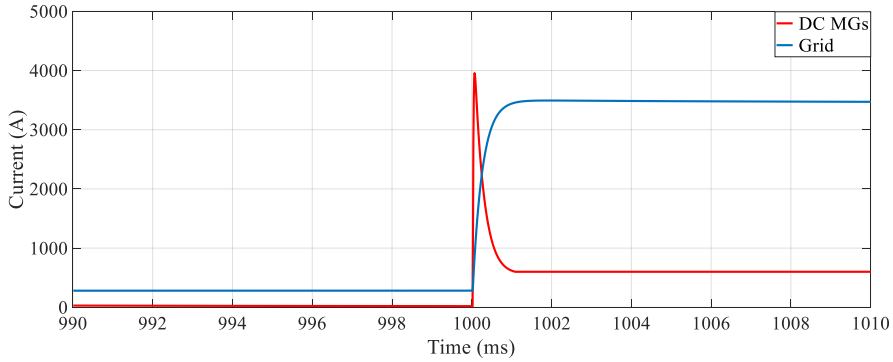

Figure 12. Fault current contributions without FCL, from grid and DC MGs.

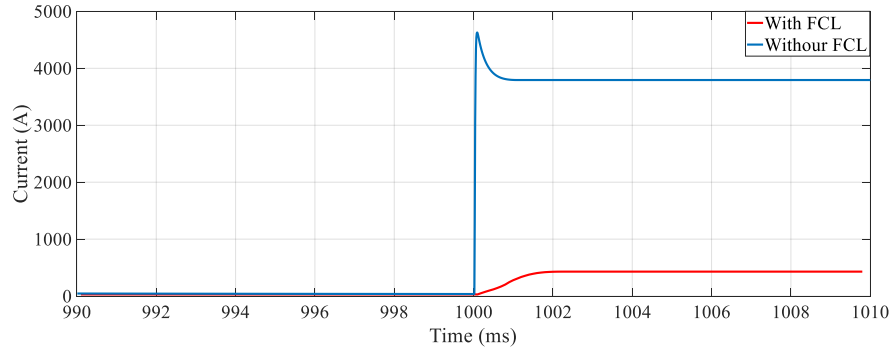

Figure 13. Fault current with and without FCL.

6.4. Real-Time Validation

The proposed DC FCL scheme has been modeled using an OPAL-RT simulator for validating the performance of the proposed method using real-time simulation. The experimental setup with oscilloscope, personal computer (PC), and OPAL-RT simulator is shown in Figure 14. Figure 15a,b presents the per-unit fault current waveforms for a fault in MG at F1, which occurred at t = 1 s with fault resistances of 0.45 Ω and 1.5 Ω, respectively. This verification using OPAL-RT assures the operation and effectiveness of the proposed scheme during different fault conditions.

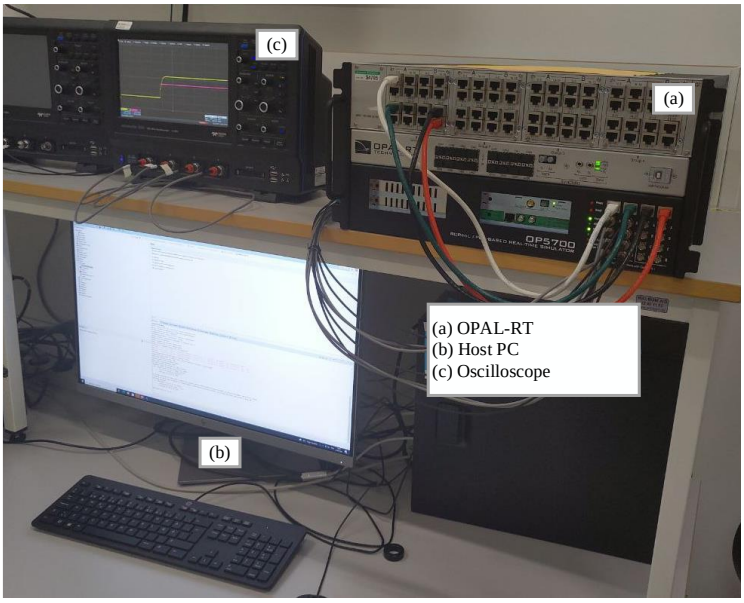

Figure 14. Real-time setup.

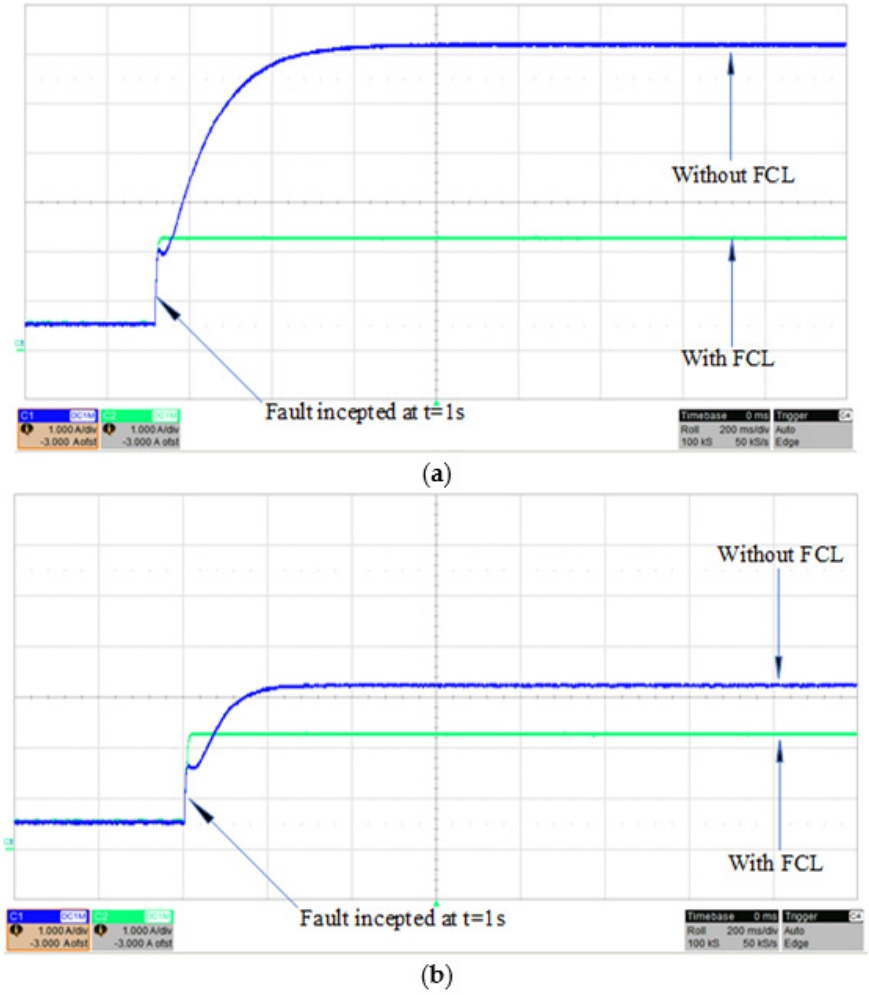

Figure 15. Fault current waveform with and without FCL for (**a**) 0.45 Ω and (**b**) 1.5 Ω faults.

6.5. Comparison between the Proposed DC FCL and Existing FCL Strategies

Finally, the proposed DC FCL-based CB is compared with other methods from several points of view, including cost, size, bidirectional operation, speed, complexity, and impact on the coordination of overcurrent relays. These comparison points are summarized in Table 4. Moreover, to better clarify the comparison of the existing methods and proposed scheme, detailed installed components for each DC FCLs, and the range of implemented voltage are summarized in Table 5.

Table 4. Comparison of the proposed DC FCL with other existing methods.

Type	Cost	Size	Speed	Complexity	Coordination Problem	Power Losses
[32]	High	Large	High	High	Medium	Low
[41]	High	Large	Low	High	Low	Low
[42]	High	Large	Medium	High	Miscoordination	Medium
[43]	High	Large	Medium	High	Miscoordination	Medium
[44]	Low	Large	Medium	High	Miscoordination	High
[45]	Low	Large	Low	Low	Medium	Low
[46]	Low	Small	High	High	Medium	High
proposed method	Moderate	Small	High	Low	Low	Low

Table 5. Comparison of the proposed DC FCL with the existing methods.

Type	Fault Current Limiting Component	Installed Power System
[32]	Arrester bank	High voltage
[41]	Ultrafast switch, diode bridge, a resistor with a high positive temperature	Medium Voltage
[42]	Switch, diode bridge, inductor capacitor branch	Low Voltage
[43]	Superconductor resistance bank	Medium Voltage
[44]	Diode bridge, two parallel RC thyristors, two series inductor diodes	Medium Voltage
[45]	Resistor, two IGBTs, switch	Low Voltage
[46]	Metal oxide varistor, diode bridge, IGBT, parallel RC	Medium Voltage
proposed method	Diode bridge, parallel RC, inductor	Low and Medium Voltage

***Cost*:** The overall cost of an FCL strategy is estimated based on utilizing semiconductor and mechanical components and auxiliary circuits, such as communication and cooling systems. In order to investigate the overall cost, it is supposed that the mechanical switches are from the same type in the considered structures, and the cost of the semiconductor elements (including MOSFETs, silicon-controlled rectifiers, and diodes) are determined for a certain current and voltage rating. Among the existing FCL schemes, due to the implementation of arrester or superconductor resistance banks, the methods presented in [32,41–43] have the highest cost, and the strategies proposed in [44–46] have the lowest cost, due to the utilization of only a few elements.

***Size*:** The size of an FCL is determined by several required control and power elements. The methods proposed in [45,46] have a small size, however, its size increases by increasing the rating of the FCL. On the other hand, the semiconductor and mechanical branches in [32,41,44] result in the large size of their suggested FCLs. Implementing the capacitor charging circuit and superconductor with a cooling system in [42,43], respectively, resulted in bulky FCLs. The installed components in each method are also shown in Table 5.

***Speed*:** The speed of an FCL is determined by the breaking and operating time of mechanical switches. In [41,45], the multistage current limiting and positive temperature coefficient resulted in a low-speed operation for these structures, and these methods limited the current by approximately 2 ms. Implementing one stage FCL using PWM in [46] caused a fast FCL operation. The methods of [42–44], with an operation time of approximately 1 ms, due to the switching in zero current and the fact that they require charging time, are categorized as medium-speed FCLs.

***Complexity*:** Control, power circuits and the capability of bidirectional conducting are three parameters that determine the complexity of an FCL scheme. Therefore, [39–45] have the lowest complexity, while [32,41–43,46] have the highest complexity. In references [32,41–43,46], the systems are relatively complicated because of employing several operating sequences, PWM function, complicated power circuitry including the considerable number of mechanical switches and semiconductor devices, active circuitry to charge their commutation capacitors, and super-conductor elements.

***Impact on the Coordination with Other Protection Devices*:** Most protection devices are coordinated based on the magnitude of the fault current of the system. The method suggested in [41] can only be used in the upstream network, which causes better coordination for overcurrent relay only in the upstream. Furthermore, due to the transient behavior in [42–44], these schemes are not appropriate for the coordination of fast protection devices. On the other hand, due to the expected value of the fault current and suitability of suggested FCLs in [45,46], these FCL strategies help to coordinate the protection devices.

***Power Losses*:** The overall power losses of an FCL are evaluated during the normal condition. The method in [41] uses a fast-tripping switch with zero resistance during normal conditions, however, it was unusable for MV DC systems. In [42,43], FCL included two diodes series with a capacitor. Therefore, the power losses include the losses of the internal resistance of diodes and the ESR of the capacitor. The FCL of [44–46] has three

diodes in a normal operation mode that cause a power loss. In [32,45], during the normal condition, only one IGBT is conducting, and the power losses of IGBTs are normally less than diodes.

The proposed DC FCL-based CB does not require a communication system, capacitor charging circuit, and has a low number of elements, but the rating of inductance and diode, and the high value of current tolerance of diodes increase the cost. Then, this method is categorized as a moderate-cost DC FCL strategy. Moreover, there is no need for a capacitor discharge circuit or any controlling circuit for DC FCL; thus, the size of this structure is low. In the proposed scheme, due to the passive structure of FCL and its connection in series with the DC/DC converter, the speed of fault current limiting of the proposed structure is high. On the other hand, in terms of the coordination problem, as the proposed FCL provides an approximately constant fault current in the protected line by changing the fault resistance, the value of fault current will be constant. Therefore, the overcurrent relays do not require new settings, and it can be a reliable and secure coordination of current-based protection devices. The proposed method uses two diodes in the current path during normal conditions. Therefore, the total power losses are only the sum of power losses of these diodes.

The qualitative performance evaluation of each method based on six performance parameters is depicted as spider diagrams in Figure 16. The axes in the spider charts present qualitative performance parameters in the range of low to high, starting from the center point. For example, in the category of cost, the low-cost and high-cost are marked with 1 and 3, respectively.

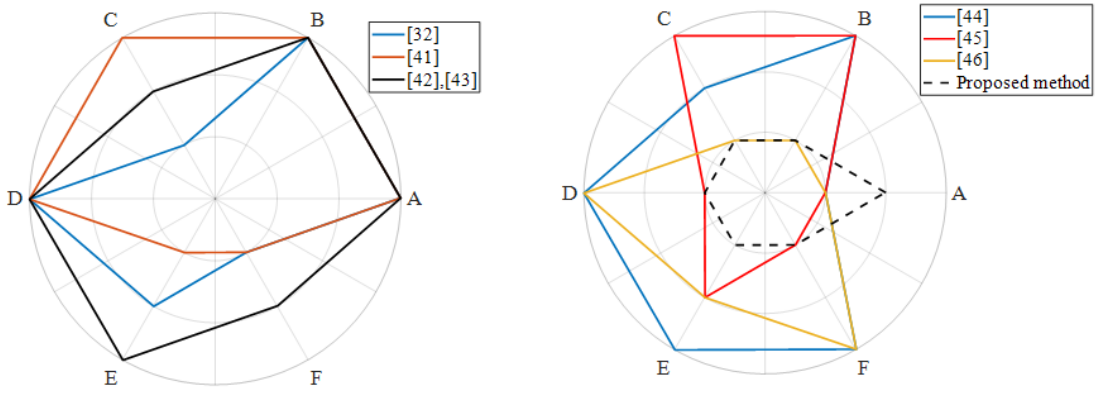

Figure 16. Comparative evaluation of existed and proposed scheme, (A) cost, (B) size, (C) operation time, (D) complexity, (E) coordination problem, (F) power losses.

7. Conclusions

In this paper, the DC fault currents of a DC MG cluster were analyzed. The analytical DC fault current expressions of a bidirectional DC/DC converter and AC/DC MMC converter were presented. After the fault occurrence, the capacitor discharge of the converters causes a high-rise fault current within several milliseconds, and the main damage is caused by the *di/dt* level in the power electronic devices. Then, the freewheeling stage starts, and the fault current reduces to the steady-state value. Consequently, a new DC FCL-based CB was proposed to limit the fault current and provide a soft clearing for CB. The proposed DC FCL scheme causes an approximately constant maximum fault current in a lower level of fault current before installation of FCL in the protected line, and it makes the setting adjustment of other protection devices more convenient and reduces the required current rating of the CBs. The simulation results and the comparison with several previously reported FCL strategies proved the accuracy of the analytical expressions and the proper operation of the proposed DC FCL-based CB during the fault condition.

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