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# Design and Implementation of 31-Level Asymmetrical Inverter With Reduced Components

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**ABSTRACT** This paper presents a novel topology for the single-phase 31-level asymmetrical multilevel inverter accomplished with reduced components count. The proposed topology generates maximum 31-level output voltage with asymmetric DC sources with an H-bridge. The fundamental 13-level multilevel inverter (MLI) topology is realized, and further, the topology is developed for 31-level can be used for renewable energy applications. This reduces the overall components count, cost and size of the system. Rather than the many advantages of MLIs, reliability issues play a significant role due to higher components count to reduce THD. This is a vital challenge for the researchers to increase the reliability with less THD. Several parameters are analyzed for both fundamental 13-level and developed 31-level MLIs such as total standing voltage (TSV), cost function (CF) and power loss. The inverter is tested experimentally with various combinational loads and under dynamic load variations with sudden load disturbances. Total standing voltage with the cost function for the proposed MLI is compared with various topologies published recently and is cost-effective. A detailed comparison of several parameters with graphical representation is made. Less TSV and components requirement is observed for the proposed MLI. The obtained total harmonic distortion (THD) is under IEEE standards. The topology is simulated in MATLAB/Simulink and verified experimentally with a hardware prototype under various conditions.

**INDEX TERMS** Multilevel inverter, TSV calculation, cost function (CF), total harmonic distortion (THD).

## I. INTRODUCTION

In the recent past, multilevel inverters gain attention due to their high power operation capability and several benefits like lower harmonics, high power quality, and lower switching losses with improved electromagnetic interference [1], [2]. These MLIs provide a stepped voltage waveform at its output using various DC sources with a power electronic circuitry comprising different power semiconductor switches [3]. Further, the waveform quality can be improved by the expanding of the level. However, the reliability and efficiency performance of MLI is a challenging task due to the more components in the circuit results in high cost [4].

In general, there exist three structures of MLIs, such as diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) [5]. The CHB inverter comprises several single-phase H-bridge topologies and classified into symmetric and asymmetric type based on the DC voltage magnitudes [6]. In the symmetric variety of MLIs, all DC voltage sources' magnitude is equal, whereas in case of an asymmetrical type, the magnitudes are not equal. In the conventional CHB type inverter, each unit comprises three

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output levels, such as positive, negative, and zero voltage levels. The evaluation of CHB type inverter's output is simple as the sum of the output voltages at each unit [7], [8]. CHB type inverters are used in high and medium voltage level, whereas in the case of FC and NPC type inverters, voltage balancing is a complex task in high voltage level [9].

In the recent past, several topologies are proposed for cascaded multilevel inverters among various control techniques [4], [10]–[13]. Multiple topologies of symmetric cascaded multilevel inverters are presented in [3], [14]–[20]. These topologies' significant benefits are low DC voltage sources, which play a major role in determining an inverter's cost. In contrast to this, several topologies used more bidirectional switches where the large number of IGBTs are needed, which is the main drawback of these topologies. In [21], the topology presented is an asymmetric type inverter where the number of bidirectional power switches results in more IGBTs, which increases the cost of the inverter. A novel topology with a reduced number of switches presented with various algorithms in [18] but many voltage sources exist, which is a drawback of this topology. The optimal utilization of semiconductor devices reduces these complexities. The reduced switch count can be achieved by using unequal dc voltage magnitude of sources [3]. Several units are designed with an increased voltage level with reduced power switches are presented in [22], [23]. The output of these units is a DC step and is converted to AC step using a full-bridge converter. Hence the applications are limited to the high voltages as the full-bridge converter blocks the higher voltages. Many novel topologies are presented to reduce the components count for both single-phase and three-phase system. The three-phase system with three single phases is presented in [24].

Some topologies presented the subunit MLIs: fewer switches and DC sources produce the multilevel output [25]. Bidirectional switches connected in antiparallel are used in the topologies which conducts current in both directions with reduced switches are presented in [26]–[29]. The sub-units are cascaded to decrease the blocking voltage at the switches which resemble a modular structure. In these topologies, the switch count increases with the increase of output level, which is a drawback. Hence there is a demand for novel MLI structures to get several levels with fewer components and blocking voltage. This, in turn, reduces the cost of the inverter. A packed H-bridge MLI topology is proposed in the recent past, which comprises the basic units connected on both sides of the full-bridge [30], [31]. In contrast to this, the topologies are designed with the absence of H-bridge and aimed to decrease the voltage stress on the circuit's switches. Many of these topologies require several components.

The analysis of cascaded MLI topologies with the combination of symmetric and asymmetric configurations is presented in [32], [33]. A novel MLI type with symmetric structure having less switch count as shown in [34], [35]. There exists a possibility to expand this type to more level. A novel topology with a control scheme tested for resistive and even in motor loads uses a genetic algorithm proposed in [35], where a stable voltage is maintained at the output under various load disturbances. The characteristics of the cascaded MLI are improved in [36]. The topology presented in [36], [37], the output level of the MLI are doubled for the same components of the circuit. A transistor clamped H-bridge MLI topology is presented in [38] provides several output levels, where the higher voltage and power ratings are achieved without expanding the components' rating. However, this type has the benefits of less switching losses with under high switching frequencies with high efficiency [39]–[44] controlled by a carrier-based PWM technique. The analysis of MLI topologies with an open extreme wind configuration is done in [45].

In general, high power loss occurs in high power applications for high switching frequency [6], [45]–[47]. Several such topologies use more component count, which causes the bulky circuit with high control complexity and produces higher THD with less efficiency. These issues are conquered in the topologies presented in [48], [49]. An asymmetrical MLI topology is shown in [50] in which the DC links are consecutively connected with opposite polarities using semiconductor switches. A 13-level asymmetric MLI topology is presented in [51] uses ten switches and four DC sources in each module. Several MLI configurations are presented based on the fundamental switch ladder and stacked back-to-back MLI in[52], [53].

In this paper, a novel 31-level MLI topology is developed from a 13- level MLI topology. However, both 13-level and 31-level MLIs are realized, and their respective outcomes are beneficial compared with several existing topologies. The proposed topology's main benefit is the output level is increased with reduced components count such as power switches, gate driver circuits, and DC sources. The total standing voltage (TSV) represents the maximum blocking voltage across the switches is calculated. Further, a cost function is realized concerning the TSV. Power loss and efficiency calculations are made, and the individual results are compared with the various existing topologies. The proposed MLI topology is found to be cost-effective with less TSV and high efficiency. THD value obtained is less and is under IEEE standards. The proposed topology is well-suited for the high and medium power applications such as FACTS, UPS, active filters and renewable energy sources. The developed 31-level MLI is tested for various loads such as resistive, motor and the combination of resistive and motor loads. The testing is done even under sudden and dynamic load variations.

The paper's organization is as follows: proposed 13-level and 31-level reduced switch H-bridge MLIs are realized in section-II; the simulation and experimental results are represented in section-III. Section IV explains the calculations such as power loss, efficiency, TSV, cost function and several comparisons with the various topologies. Finally, the conclusion followed by future work is presented in section V.

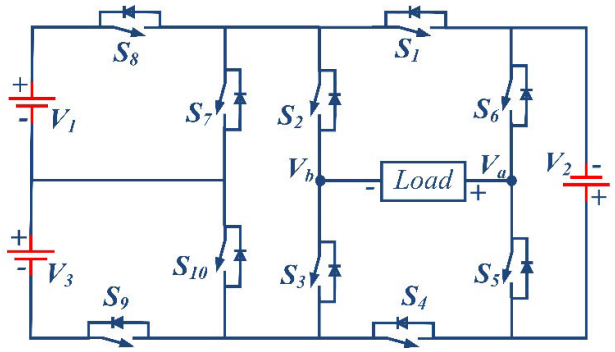


**FIGURE 1.** Structure of the asymmetrical 13-level MLI topolog.

## II. PROPOSED REDUCED SWITCH H-BRIDGE MLI

### A. 13 LEVEL MLI TOPOLOGY

Thirteen level MLI topology comprises ten unidirectional switches $S_1$ to $S_{10}$ and three asymmetric DC sources $V_1$, $V_2$, and $V_3$. A module of switches $S_2$, $S_3$, $S_5$, and $S_6$ forms the H Bridge and the load is connected between $V_a$ and $V_b$ points is shown in Fig. 1. The desired 13 level output voltage is obtained by 1:2:3 ratio of an asymmetrical configuration of three DC sources hence the magnitude of three DC sources are $V_{dc} = V_1 = 66.6V$, $V_2 = 133.3V$, and $V_3 = 200V$ respectively.

The 13-level MLI operation can be easily understood from the pulses generated by switch's corresponding operation. In proposed MLI staircase modulation scheme is used for switching pulses and the state of switches can be activated with '↑' and the switch is turn ON; otherwise the switch resembles to turn OFF. Table 1 represent the modes of operation of 13-level MLI and the path of load current $I_o$ and conducting devices and Table 2 represent the corresponding switching table of 13-level MLI. Fig. 2 depicts the expected output voltage waveform of the proposed 13-level MLI. The various modes of the proposed 13-level MLI are represented in Fig. 3.

Let 'p' is the number of basic units

$$\text{Total switch count } N_{SW} \text{ is evaluated as : } N_{sw} = 10p \tag{1}$$

$$\text{Total DC source count } N_{DCS} \text{ is evaluated as : } N_{DCS} = 3p \tag{2}$$

$$\text{The number of levels } N_{LEL} \text{ is evaluated as : } N_{LEL} = 2(7^p) - 1. \tag{3}$$

The proposed MLI comprises only one unit; therefore, $p = 1$, total switch count $N_{SW}$ is 10, total DC source count $N_{DCS}$ is 3, and the total number of levels is $N_{LEL}$ is 13.

In mode I: switches $S_1$, $S_3$, $S_5$, $S_8$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_1$-$S_8$-$S_1$-$V_2$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$, all three sources $V_1$, $V_2$, and $V_3$ supplies the circuit produce $+6V_{dc}$ output level. In mode II: switches $S_1$, $S_3$, $S_5$, $S_7$, and $S_9$ are in conduction stage, hence the path

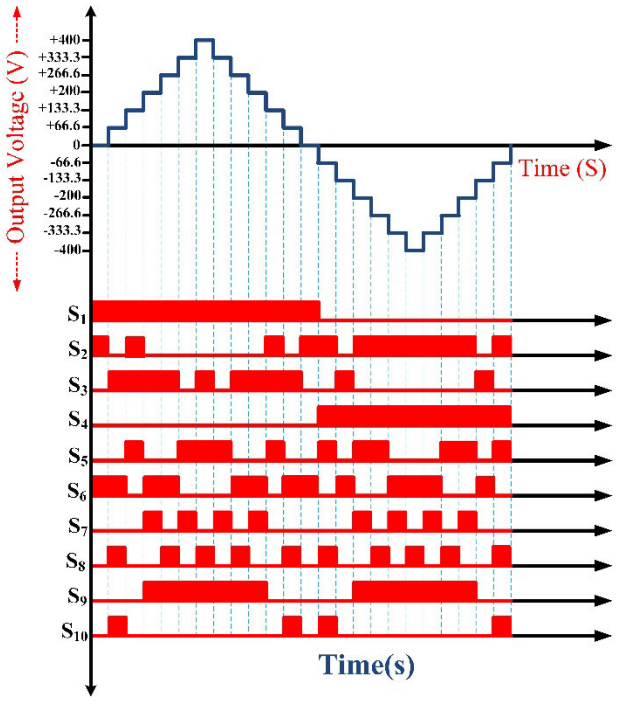


**FIGURE 2.** The expected output voltage waveform of 13-level MLI.

**TABLE 1.** Operating modes of 13-level inverter.

| *Modes* | *Load Current Path* | *Active sources* | *$V_0$ (volt)* |
|---|---|---|---|
| $M_1$ | $V_1$-$S_8$-$S_1$-$V_2$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_2$+$V_3$ | 400 |
| $M_2$ | $V_2$-$S_5$-L-$S_3$-$S_9$-$V_3$-$S_7$-$S_1$-$V_2$ | $V_2$+$V_3$ | 333.3 |
| $M_3$ | $V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_3$ | 266.6 |
| $M_4$ | $V_3$-$S_7$-$S_1$-$S_6$-L-$S_3$-$S_9$-$V_3$ | $V_3$ | 200 |
| $M_5$ | $V_2$-$S_5$-L-$S_2$-$S_1$-$V_2$ | $V_2$ | 133.3 |
| $M_6$ | $V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_{10}$-$V_1$ | $V_1$ | 66.6 |
| $M_7$ | L-$S_2$-$S_1$-$S_6$-L | - | 0 |
| $M_8$ | $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_{10}$-$V_1$ | -$V_1$ | -66.6 |
| $M_9$ | $V_2$-$S_4$-$S_3$-L-$S_6$-$V_2$ | -$V_2$ | -133.3 |
| $M_{10}$ | $V_3$-$S_7$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$ | -$V_3$ | -200 |
| $M_{11}$ | $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$-$V_1$ | -($V_1$+$V_3$) | -266.6 |
| $M_{12}$ | $V_2$-$S_4$-$S_9$-$V_3$-$S_7$-$S_2$-L-$S_6$-$V_2$ | -($V_2$+$V_3$) | -333.3 |
| $M_{13}$ | $V_3$-$V_1$-$S_8$-$S_2$-L-$S_6$-$V_2$-$S_4$-$S_9$-$V_3$ | -($V_1$+$V_2$+$V_3$) | -400 |

of load current $I_o$ through $V_2$-$S_5$-L-$S_3$-$S_9$-$V_3$-$S_7$-$S_1$-$V_2$ and the sources $V_2$, and $V_3$ supplies the circuit produce $+5V_{dc}$ output level. In mode III: switches $S_1$, $S_3$, $S_6$, $S_8$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_9$-$V_3$-$V_1$ and the sources $V_1$, and $V_3$ supplies the circuit produce $+4V_{dc}$ output level. In mode IV: switches $S_1$, $S_3$, $S_6$, $S_7$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_3$-$S_7$-$S_1$-$S_6$-L-$S_3$-$S_9$-$V_3$ and the source $V_3$ supplies the circuit produce $+3V_{dc}$ output level. In mode V: switches $S_1$, $S_2$, and $S_5$, are in conduction stage, hence the path of load current $I_o$ through $V_2$-$S_5$-L-$S_2$-$S_1$-$V_2$ and the source $V_2$ supplies the circuit produce $+2V_{dc}$ output level. In mode VI: switches $S_1$, $S_3$, $S_6$, $S_8$, and $S_{10}$ are in conduction stage, hence the path of load current $I_o$ through

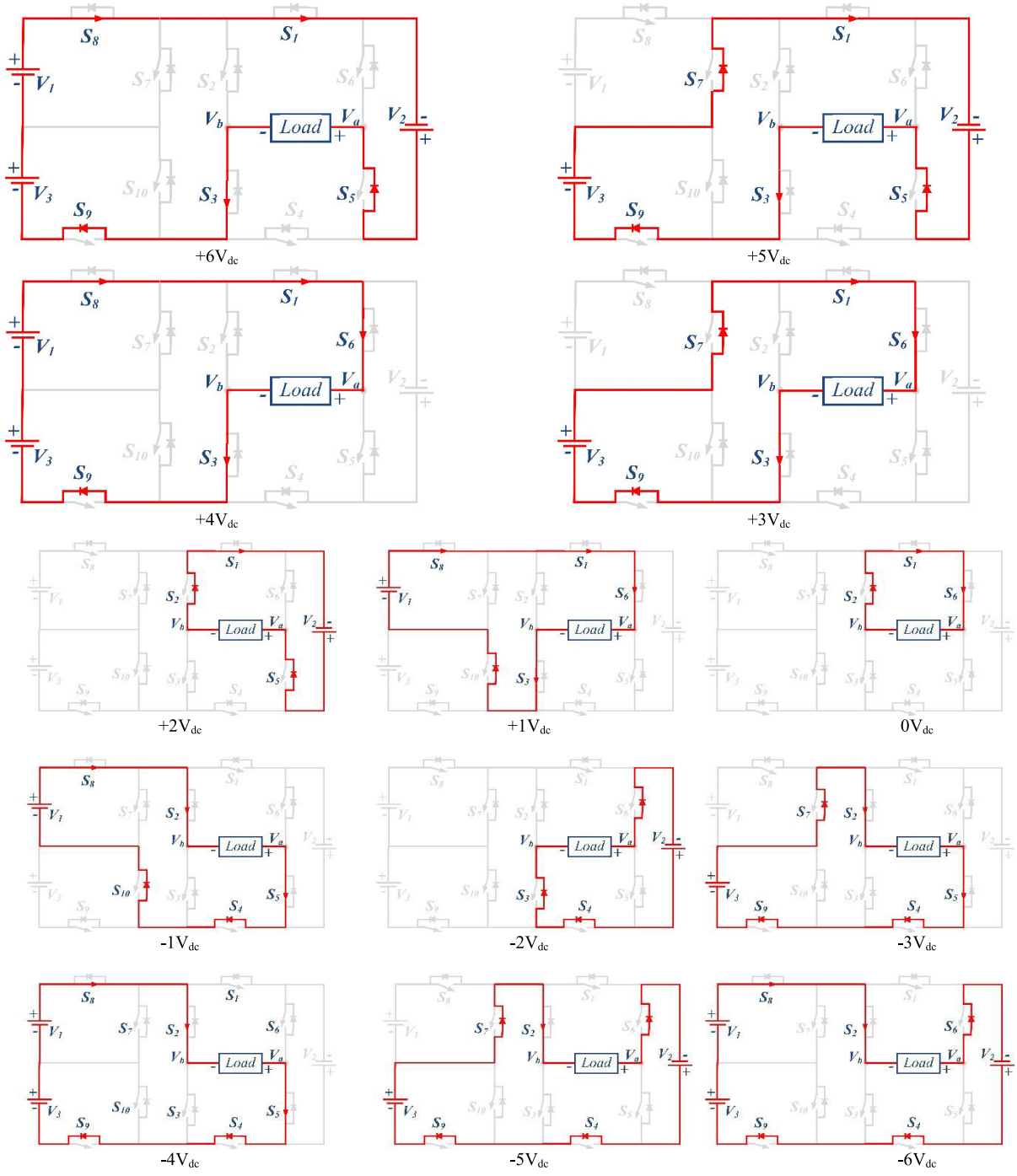


**FIGURE 3.** Operating modes of thirteen levels MLI topology.

$V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_{10}$-$V_1$ and the source $V_1$ supplies the circuit produce $+1V_{dc}$ output level. In mode VII: switches $S_1$, $S_2$, and $S_3$ are in conduction stage; hence the path of load current $I_o$ through L-$S_2$-$S_1$-$S_6$-L and no sources are connected to the circuit produce $+0V_{dc}$ output level. In mode VIII: switches $S_2$, $S_4$, $S_5$, $S_8$, and $S_{10}$ are in conduction stage, hence the path of load current $I_o$ through $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_{10}$-$V_1$ and the source $V_1$ supplies the circuit produce $-1V_{dc}$ output level. In mode IX: switches $S_2$, $S_3$, and $S_6$ are in conduction stage, hence the path of load current $I_o$ through $V_2$-$S_4$-$S_3$-L-$S_6$-$V_2$ and the source $V_2$ supplies the circuit produce $-2V_{dc}$ output level. In mode X: switches $S_2$, $S_4$, $S_5$, $S_7$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_3$-$S_7$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$, and the source $V_3$ supplies the circuit produce $-3V_{dc}$ output level. In mode XI: switches $S_2$, $S_4$, $S_5$, $S_8$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$-$V_1$ and the sources $V_1$, and $V_3$ supplies the

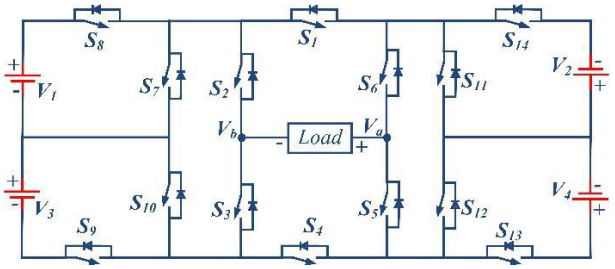


**FIGURE 4.** Proposed asymmetrical 31-level MLI topology.

circuit produce $-4V_{dc}$ output level. In mode XII: switches $S_2$, $S_4$, $S_6$, $S_7$, and $S_9$ are in conduction stage, hence the path of load current $I_o$ through $V_2$-$S_4$-$S_9$-$V_3$-$S_7$-$S_2$-L-$S_6$-$V_2$ and the sources $V_2$, and $V_3$ supplies the circuit produce $-5V_{dc}$ output level. In mode XIII: switches $S_2$, $S_4$, $S_6$, $S_8$, and $S_9$ are in ON state, hence the path of load current $I_o$ through $V_3$-$V_1$-$S_8$-$S_2$-L-$S_6$-$V_2$-$S_4$-$S_9$-$V_3$ and the sources $V_1$, $V_2$, and $V_3$ supplies the circuit produce $-6V_{dc}$ output level.

13-level MLI is perfectly adapted for improving power quality issues like THD, a smaller number of switches, minimized dv/dt stress these qualities further improved by increasing the number of level with fever switch count, this can be achieved by using proposed 31-level MLI with reduced switch count.

### B. PROPOSED 31-LEVEL MLI TOPOLOGY

The proposed 31-level MLI extends thirteen level inverter topology it can be achieved by adding one additional DC source and four extra switches. The proposed 31-level MLI comprises fourteen unidirectional switches $S_1$ to $S_{14}$ and four DC voltage sources $V_1$, $V_2$, $V_3$, and $V_4$ shown in Fig.4. The voltage magnitude of all four sources is chosen with different values; hence, the proposed topology configuration is asymmetrical. For 31-level the value of DC sources are selected as 1:2:4:8 ratio, the input voltages of the circuit are $V_{dc} = V_1 = 26.6V$, $V_2 = 53.3V$, $V_3 = 106.6V$, and $V_4 = 213.3V$ respectively.

Let 'p' is the number of necessary units

$$\text{Total switch count } N_{SW} \text{ is evaluated as} N_{sw} = 14p \quad (4)$$

$$\text{Total DC source count } N_{DCS} \text{is evaluated as} N_{DCS} = 3p \quad (5)$$

$$\text{The number of levels } N_{LEL} \text{is evaluated as : } N_{LEL} = 2\left(16^{p}\right) - 1. \quad (6)$$

The proposed MLI comprises only one unit therefore p = 1, total switch count $N_{SW}$ is 14, total DC source count $N_{DCS}$ is 4, and the total number of levels is $N_{LEL}$ is 31. The 31-level MLI operation can be easily understood from the switching pulses generated by the switch's corresponding operation. In proposed MLI staircase modulation technique is used for switching pulses and the state of switches can be activated with '↑' and the switch is turn ON; otherwise the switch resembles to turn OFF. Table 3 represents the corresponding switching table of 31-level MLI, and Table 4 represents the modes of operation of 31-level MLI and the path of load current $I_o$ and conducting devices. A positive peak voltage level switches $S_1$, $S_3$, $S_5$, $S_8$, $S_9$, and $S_{13}$ are in conduction stage, hence the path of load current $I_o$ through $V_1$-$S_8$-$S_1$-$S_{14}$-$V_2$-$V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$, all four sources $V_1$, $V_2$, $V_3$, and $V_4$ supplies the circuit produce $+15V_{dc}$ output level.

Similarly, the remaining positive level is achieved by controlling the switches and DC sources. We get zero voltage level at switches $S_1$, $S_2$, and $S_6$ are in conduction stage, hence the path of load current $I_o$ through L-$S_2$-$S_1$-$S_6$-L, no voltage sources supplies the circuit. The negative peak voltage level is occurring at switches $S_2$, $S_4$, $S_6$, $S_8$, $S_9$, $S_{13}$, and $S_{14}$ are in conduction stage; hence the path of load current $I_o$ through $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$V_4$-$S_{13}$-$S_4$-$S_9$-$V_3$-$V_1$, all four sources $V_1$, $V_2$, $V_3$, and $V_4$ supplies the circuit produce $-15V_{dc}$ output level, likewise remaining negative level are achieved by controlling the switches and DC sources. Some modes of operation of the proposed 31-level MLI is shown in Fig. 5.

## III. RESULTS AND DISCUSSIONS

### A. SIMULATION AND EXPERIMENTAL RESULTS OF 13-LEVEL MLI

Presented 13-level MLI topology is simulated in MATLAB/Simulink, switching pulses are generated at 2 kHz switching frequency compared with 50Hz reference frequency, the topology is tested for 100Ω resistive load, maximum peak voltage 400V is attained by giving input DC sources $V_{dc} = V_1 = 66.6V$, $V_2 = 133.3V$, and $V_3 = 200V$ respectively. Fig. 6(a) and Fig. 6(b) represents the Simulation results of outputs such as Voltage and Current waveforms output Voltage, of presented 13-level MLI, respectively. From Fig. 6(a) and Fig. 6(b) the maximum voltage is 400V and the load current is 4A, the output is refined with THD of 5.65% shown in Fig. 7.

The presented asymmetrical configuration of 13-level MLI topology is validated experimentally by accomplishing a laboratory setup shown in Fig. 8. The inverter prototype setup assembled using ten CM75DU-12H IGBT's which are provoked by MCT2E optocouplers, three unequal DC supplies with voltage magnitude of $V_1 = 66.6V$, $V_2 = 133.3V$, and $V_3 = 200V$, 100Ω R-load, 98mH L-load, and switching pulse are get from dSPACE RTI1104. The waveforms are observed in digital storage oscilloscope (DSO), experimental prototype results with R-Load under steady-state output voltage $V_0 = 400V$ equal to 282.84 $V_{rms}$, load current $I_0 = 4A$ equal to 2.82A $I_{rms}$ are represented in Fig. 9(a) & (b) respectively. Total voltage harmonic spectrum 5.77% is measured with power analyzer, the voltage THD spectrum is illustrated in Fig. 10.

### B. SIMULATION AND EXPERIMENTAL RESULTS OF 31-LEVEL MLI

The developed 31-level MLI topology is simulated in MATLAB/Simulink, switching pulses are generated at 2 kHz

**TABLE 2.** Switching table of 13-levels inverter.

| *Switching Levels* | *Direction of conducting Switches* | | | | | | | | | | *DC Sources* | | | *$V_0$ (volts)* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $V_1$ | $V_2$ | $V_3$ | |
| $L_1$ | → | | ↓ | | ↑ | | | → | ← | | √ | √ | √ | $+6V_{dc}$ |
| $L_2$ | → | | ↓ | | ↑ | | ↑ | | ← | | | √ | √ | $+5V_{dc}$ |
| $L_3$ | → | | ↓ | | | ↓ | | → | ← | | √ | | √ | $+4V_{dc}$ |
| $L_4$ | → | | ↓ | | | ↓ | ↑ | | ← | | | | √ | $+3V_{dc}$ |
| $L_5$ | → | ↑ | | | ↑ | | | | | | | √ | | $+2V_{dc}$ |
| $L_6$ | → | | ↓ | | | ↓ | | → | | ↑ | √ | | | $+1V_{dc}$ |
| $L_7$ | → | ↑ | | | | ↓ | | | | | | | | $0V_{dc}$ |
| $L_8$ | | ↓ | | ← | ↓ | | | → | | ↑ | √ | | | $-1V_{dc}$ |
| $L_9$ | | | ↑ | ← | | ↑ | | | | | | √ | | $-2V_{dc}$ |
| $L_{10}$ | | ↓ | | ← | ↓ | | ↑ | | ← | | | | √ | $-3V_{dc}$ |
| $L_{11}$ | | ↓ | | ← | ↓ | | | → | ← | | √ | | √ | $-4V_{dc}$ |
| $L_{12}$ | | ↓ | | ← | | ↑ | ↑ | | ← | | | √ | √ | $-5V_{dc}$ |
| $L_{13}$ | | ↓ | | ← | | ↑ | | → | ← | | √ | √ | √ | $-6V_{dc}$ |

*'↑' indicates the direction of the conducting switch*

**TABLE 3.** Switching table of 31-levels inverter.

| Switching Levels | Direction of conducting Switches | | | | | | | | | | | | | | Sources | | | | $V_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $V_1$ | $V_2$ | $V_3$ | $V_4$ | |
| $L_1$ | → | | ↓ | | ↑ | | | → | ← | | | | ← | → | √ | √ | √ | √ | $+15V_{dc}$ |
| $L_2$ | → | | ↓ | | ↑ | | ↑ | | ← | | | | ← | → | | √ | √ | √ | $+14V_{dc}$ |
| $L_3$ | → | | ↓ | | ↑ | | | → | ← | | ↓ | | ← | | √ | | √ | √ | $+13V_{dc}$ |
| $L_4$ | → | | ↓ | | ↑ | | ↑ | | ← | | ↓ | | ← | | | | √ | √ | $+12V_{dc}$ |
| $L_5$ | → | | ↓ | | ↑ | | | → | | ↑ | | | ← | → | √ | √ | | √ | $+11V_{dc}$ |
| $L_6$ | → | ↑ | | | ↑ | | | | | | | | ← | → | | √ | | √ | $+10V_{dc}$ |
| $L_7$ | → | | ↓ | | ↑ | | | → | | ↓ | ↓ | | ← | | √ | | | √ | $+9V_{dc}$ |
| $L_8$ | → | ↑ | | | ↑ | | | | | | ↓ | | ← | | | | | √ | $+8V_{dc}$ |
| $L_9$ | → | | ↓ | | ↑ | | | → | ← | | | ↓ | | → | √ | √ | √ | | $+7V_{dc}$ |
| $L_{10}$ | → | | ↓ | | ↑ | | ↑ | | ← | | | ↓ | | → | | √ | √ | | $+6V_{dc}$ |
| $L_{11}$ | → | | ↓ | | | ↓ | | → | ← | | | | | | √ | | √ | | $+5V_{dc}$ |
| $L_{12}$ | → | | ↓ | | | ↓ | ↑ | | ← | | | | | | | | √ | | $+4V_{dc}$ |
| $L_{13}$ | → | | ↓ | | ↑ | | | → | | ↑ | | ↓ | | → | √ | √ | | | $+3V_{dc}$ |
| $L_{14}$ | → | ↑ | | | ↑ | | | | | | | ↓ | | → | | √ | | | $+2V_{dc}$ |
| $L_{15}$ | → | | ↓ | | | ↓ | | → | | ↑ | | | | | √ | | | | $+1V_{dc}$ |
| $L_{16}$ | → | ↑ | | | | ↓ | | | | | | | | | | | | | $0V_{dc}$ |
| $L_{17}$ | | ↓ | | ← | ↓ | | | → | | ↑ | | | | | √ | | | | $-1V_{dc}$ |
| $L_{18}$ | | | ↑ | ← | | ↑ | | | | | | ↓ | | → | | √ | | | $-2V_{dc}$ |
| $L_{19}$ | | ↓ | | ← | | ↑ | | → | | ↑ | | ↓ | | → | √ | √ | | | $-3V_{dc}$ |
| $L_{20}$ | | ↓ | | ← | ↓ | | ↑ | | ← | | | | | | | | √ | | $-4V_{dc}$ |
| $L_{21}$ | | ↓ | | ← | ↓ | | | → | ← | | | | | | √ | | √ | | $-5V_{dc}$ |
| $L_{22}$ | | ↓ | | ← | | ↑ | ↑ | | ← | | | ↓ | | → | | √ | √ | | $-6V_{dc}$ |
| $L_{23}$ | | ↓ | | ← | | ↑ | | → | ← | | | ↓ | | → | √ | √ | √ | | $-7V_{dc}$ |
| $L_{24}$ | | | ↑ | ← | | ↑ | | | | | ↓ | | ← | | | | | √ | $-8V_{dc}$ |
| $L_{25}$ | | ↓ | | ← | | ↑ | | → | | ↑ | ↓ | | ← | | √ | | | √ | $-9V_{dc}$ |
| $L_{26}$ | | | ↑ | ← | | ↑ | | | | | | | ← | → | | √ | | √ | $-10V_{dc}$ |
| $L_{27}$ | | ↓ | | ← | | ↑ | | → | | ↑ | | | ← | → | √ | √ | | √ | $-11V_{dc}$ |
| $L_{28}$ | | ↓ | | ← | | ↑ | ↑ | | ← | | ↓ | | ← | | | | √ | √ | $-12V_{dc}$ |
| $L_{29}$ | | ↓ | | ← | | ↑ | | → | ← | | ↓ | | ← | | √ | | √ | √ | $-13V_{dc}$ |
| $L_{30}$ | | ↓ | | ← | | ↑ | ↑ | | ← | | | | ← | → | | √ | √ | √ | $-14V_{dc}$ |
| $L_{31}$ | | ↓ | | ← | | ↑ | | → | ← | | | | ← | → | √ | √ | √ | √ | $-15V_{dc}$ |

*'↑' indicates the direction of the conducting switch*

**TABLE 4.** Operating modes of 31-levels MLI.

| *Modes* | *Load Current Path* | *Output voltage $V_0$ (volts)* | | |
|---|---|---|---|---|
| | | *Active sources* | *Magnitude of $V_0$* | |
| $M_1$ | $V_1$-$S_8$-$S_1$-$S_{14}$-$V_2$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_2$+$V_3$+$V_4$ | +15$V_{dc}$ | 400 |
| $M_2$ | $V_2$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$S_7$-$S_1$- $S_{14}$-$V_2$ | $V_2$+$V_3$+$V_4$ | +14$V_{dc}$ | 373.3 |
| $M_3$ | $V_1$-$S_8$-$S_1$-$S_{11}$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_3$+$V_4$ | +13$V_{dc}$ | 346.6 |
| $M_4$ | $V_3$-$S_7$-$S_1$- $S_{11}$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_9$-$V_3$ | $V_3$+$V_4$ | +12$V_{dc}$ | 320 |
| $M_5$ | $V_1$-$S_8$-$S_1$-$S_{14}$-$V_2$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_{10}$-$V_1$ | $V_1$+$V_2$+$V_4$ | +11$V_{dc}$ | 293.3 |
| $M_6$ | $V_2$- $V_4$-$S_{13}$-$S_5$-L-$S_2$-$S_1$-$S_6$-$S_{14}$-$V_2$ | $V_2$+$V_4$ | +10$V_{dc}$ | 266.6 |
| $M_7$ | $V_1$-$S_8$-$S_1$-$S_{11}$- $V_4$-$S_{13}$-$S_5$-L-$S_3$-$S_{10}$-$V_1$ | $V_1$+$V_4$ | +9$V_{dc}$ | 240 |
| $M_8$ | $V_4$-$S_{13}$-$S_5$-L-$S_2$- $S_1$-$S_{11}$- $V_4$ | $V_4$ | +8$V_{dc}$ | 213.3 |
| $M_9$ | $V_1$-$S_8$-$S_1$-$S_{14}$-$V_2$-$S_{12}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_2$+$V_3$ | +7$V_{dc}$ | 186.6 |
| $M_{10}$ | $V_2$-$S_{12}$-$S_5$-L-$S_3$-$S_9$-$V_3$-$S_7$-$S_1$-$S_{14}$-$V_2$ | $V_2$+$V_3$ | +6$V_{dc}$ | 160 |
| $M_{11}$ | $V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_9$-$V_3$-$V_1$ | $V_1$+$V_3$ | +5$V_{dc}$ | 133.3 |
| $M_{12}$ | $V_3$-$S_7$-$S_1$- $S_6$-L-$S_3$-$S_9$-$V_3$ | $V_3$ | +4$V_{dc}$ | 106 |
| $M_{13}$ | $V_1$-$S_8$-$S_1$-$S_{14}$-$V_2$-$S_{12}$-$S_5$- L-$S_3$-$S_{10}$-$V_1$ | $V_1$+$V_2$ | +3$V_{dc}$ | 80 |
| $M_{14}$ | $V_2$-$S_{12}$-$S_5$-L-$S_2$-$S_1$-$S_{14}$-$V_2$ | $V_2$ | +2$V_{dc}$ | 53.3 |
| $M_{15}$ | $V_1$-$S_8$-$S_1$-$S_6$-L-$S_3$-$S_{10}$-$V_1$ | $V_1$ | +1$V_{dc}$ | 26.6 |
| $M_{16}$ | L-$S_2$-$S_1$-$S_6$-L | - | 0$V_{dc}$ | 0 |
| $M_{17}$ | $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_{10}$-$V_1$ | -$V_1$ | -1$V_{dc}$ | -26.6 |
| $M_{18}$ | $V_2$-$S_{12}$-$S_4$-$S_3$-L-$S_6$-$S_{14}$-$V_2$ | -$V_2$ | -2$V_{dc}$ | -53.3 |
| $M_{19}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$S_{12}$-$S_4$-$S_{10}$-$V_1$ | -($V_1$+$V_2$) | -3$V_{dc}$ | -80 |
| $M_{20}$ | $V_3$-$S_7$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$ | -$V_3$ | -4$V_{dc}$ | -106 |
| $M_{21}$ | $V_1$-$S_8$-$S_2$-L-$S_5$-$S_4$-$S_9$-$V_3$-$V_1$ | -($V_1$+$V_3$) | -5$V_{dc}$ | -133.3 |
| $M_{22}$ | $V_2$-$S_{12}$-$S_4$-$S_9$-$V_3$-$S_7$-$S_2$-L-$S_6$-$S_{14}$-$V_2$ | -($V_2$+$V_3$) | -6$V_{dc}$ | -160 |
| $M_{23}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$S_{12}$-$S_4$-$S_9$-$V_3$-$V_1$ | -($V_1$+$V_2$+$V_3$) | -7$V_{dc}$ | -186.6 |
| $M_{24}$ | $V_4$-$S_{13}$-$S_4$-$S_3$-L-$S_6$-$S_{11}$-$V_4$ | -$V_4$ | -8$V_{dc}$ | -213.3 |
| $M_{25}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{11}$-$V_4$-$S_{13}$-$S_4$-$S_{10}$-$V_1$ | -($V_1$+$V_4$) | -9$V_{dc}$ | -240 |
| $M_{26}$ | $V_2$-$V_4$-$S_{13}$-$S_4$-$S_3$-L-$S_6$-$S_{14}$-$V_2$ | -($V_2$+$V_4$) | -10$V_{dc}$ | -266.6 |
| $M_{27}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$V_4$-$S_{13}$-$S_4$-$S_{10}$-$V_1$ | -($V_1$+$V_2$+$V_4$) | -11$V_{dc}$ | -293.3 |
| $M_{28}$ | $V_3$-$S_7$-$S_2$-L-$S_6$-$S_{11}$-$V_4$-$S_{13}$-$S_4$-$S_9$-$V_3$ | -($V_3$+$V_4$) | -12$V_{dc}$ | -320 |
| $M_{29}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{11}$-$V_4$-$S_{13}$-$S_4$-$S_9$-$V_3$-$V_1$ | -($V_1$+$V_3$+$V_4$) | -13$V_{dc}$ | -346.6 |
| $M_{30}$ | $V_3$-$S_7$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$V_4$-$S_{13}$-$S_4$-$S_9$-$V_3$ | -($V_2$+$V_3$+$V_4$) | -14$V_{dc}$ | -373.3 |
| $M_{31}$ | $V_1$-$S_8$-$S_2$-L-$S_6$-$S_{14}$-$V_2$-$V_4$-$S_{13}$-$S_4$-$S_9$-$V_3$-$V_1$ | -($V_1$+$V_2$+$V_3$+$V_4$) | -15$V_{dc}$ | -400 |

switching frequency compared with 50Hz reference frequency, the topology is tested for 100Ω resistive load, maximum peak voltage 400V is attained by supplying input DC sources $V_{dc} = V_1 = 26.6V$, $V_2 = 53.3V$, $V_3 = 106.6V$, and $V_4 = 213.3V$ respectively. Fig. 11(a) and Fig. 11(b) show the Simulation results of output Voltage, output Voltage and Current waveforms of presented 31-levels MLI, respectively. From Fig. 11(a) and Fig. 11(b) the maximum voltage is 400V, and the load current is 4A, the output waveform is refined with a THD of 3.32 % represented in Fig. 12.

The proposed asymmetrical configuration of 31-level MLI topology is validated experimentally in a laboratory by accomplished a prototype setup of inverter assembled using fourteen CM75DU-12H IGBT's which are provoked by MCT2E optocouplers, four unequal DC supplies with voltage magnitude of $V_1 = 26.6V$, $V_2 = 53.3V$, $V_3 = 106.6V$, and $V_4 = 213.3V$ respectively, 100Ω R-load, 98mH L-load, and switching pulse are getting from dSPACE RTI1104. The waveforms are observed in digital storage oscilloscope (DSO), experimental prototype results with R-Load under steady-state output voltage $V_0 = 400V$ equal to 282.84 $V_{rms}$, load current $I_0 = 4A$ similar to 2.82A $I_{rms}$ are represented in Fig. 13(a) & (b) respectively. Fig. 14 illustrates the output voltage $V_0 = 400V$ equal to 282.84 $V_{rms}$, load current $I_0 = 6.8A$ similar to 4.8A $I_{rms}$ of the 31-level MLI with L-Load. The proposed MLI's dynamic response is obtained by introducing an Inductive load parallel to R-Load, or R-Load is added in parallel to L-Load represented in Fig.15 and Fig.16. Total voltage harmonic spectrum 3.32% is measured with power analyzer; the voltage THD spectrum is illustrated in Fig. 17.

## IV. CALCULATIONS AND COMPARATIVE STUDIES

### A. LOSS AND EFFICIENCY

Two significant losses in power electronic devices are switching and conduction losses. In an IGBT, the transistor voltage, ON-state voltage, and resistance are termed $V_T$, $V_{Ton}$ and $R_T$

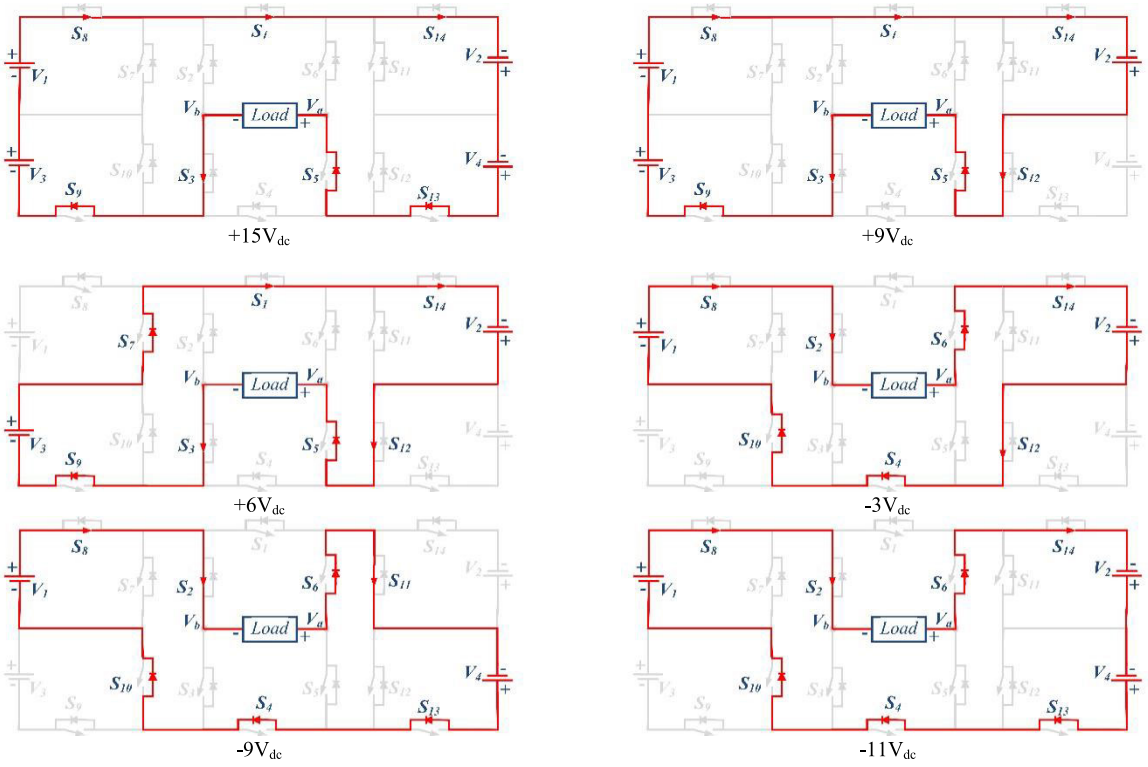


**FIGURE 5.** Operating modes of proposed asymmetrical 31-levels MLI topology.

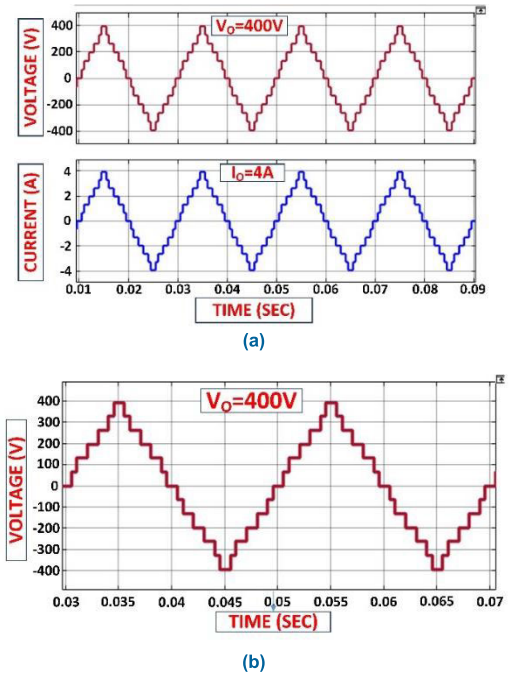


**FIGURE 6.** (a) Simulation result of Voltage wave and current waveform (b) Simulation result of Voltage waveform of 13-level MLI.

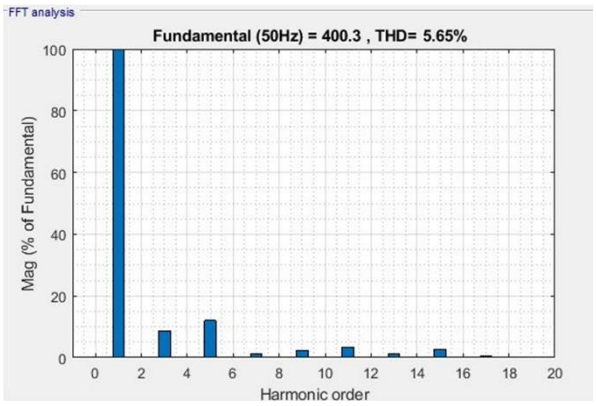


**FIGURE 7.** Simulation result of Voltage Harmonic spectrum of 13-level MLI.

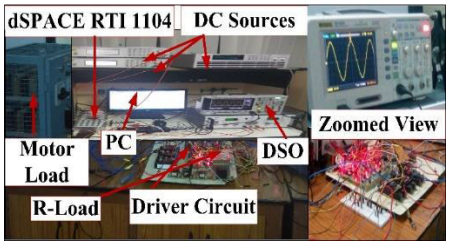


**FIGURE 8.** Experimental setup for the proposed topology.

respectively. Whereas for diode voltage, ON-state voltage, resistance is termed as $V_D$, $V_{Don}$ is and $R_D$ respectively. Then conduction losses of transistor $P_{SC}$ and diode $P_{DC}$ are evaluated as

$$P_{DC}(t) = V_D(t)\, i(t) + R_D i^2(t) \tag{7}$$

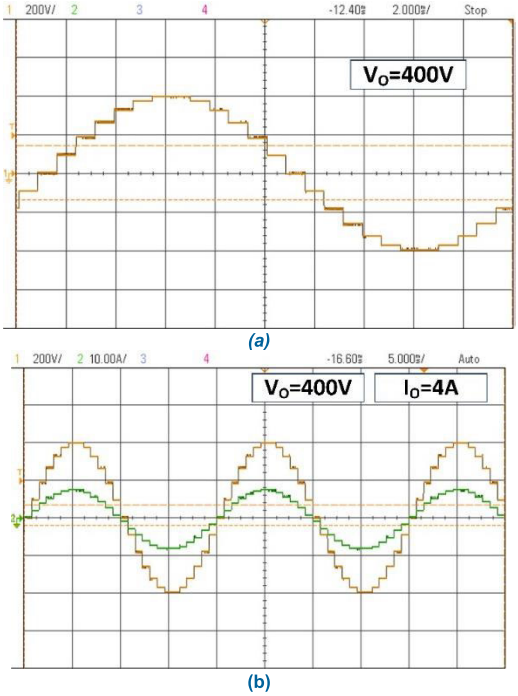


**FIGURE 9.** (a) Experimental results showing voltage waveform (b) Experimental results of voltage and current waveforms of 13-level MLI topology with R-Load.

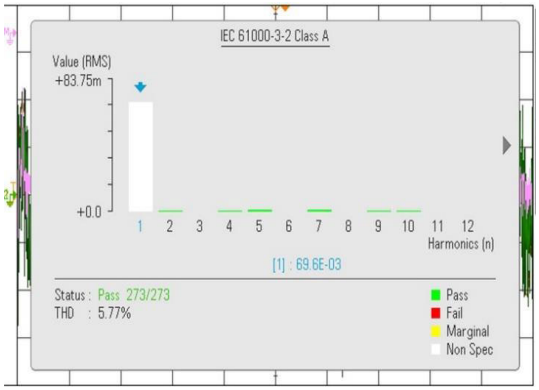


**FIGURE 10.** Experimental results of Voltage Harmonic spectrum of 13-level MLI topology.

**TABLE 5.** Power and efficiency of proposed 13 and 31 level MLI.

| *Parameters* | *13-level MLI* | *31-level MLI* | |
|---|---|---|---|
| | R-Load | R-Load | L-Load |
| $V_{rms}$ *(v)* | 282.84 | 282.84 | 282.84 |
| $I_{rms}$ *(A)* | 2.82 | 2.82 | 4.8 |
| *Conduction losses (W)* | 48.72 | 68.22 | 169.34 |
| *Switching losses (W)* | 0.168 | 0.3405 | 0.984 |
| *Total losses (W)* | 48.88 | 68.56 | 170.32 |
| *Output power (W)* | 791.95 | 791.95 | 1357.6 |
| *Efficiency (%)* | 94.18 % | 92.32 % | 88.85% |

$$P_{TC}(t) = [V_T + R_T i^{\beta}(t)]i(t) \quad (8)$$

Constant $\beta$ is derived from characteristics of a switch. There is no Bi-directional switch in proposed topology, let

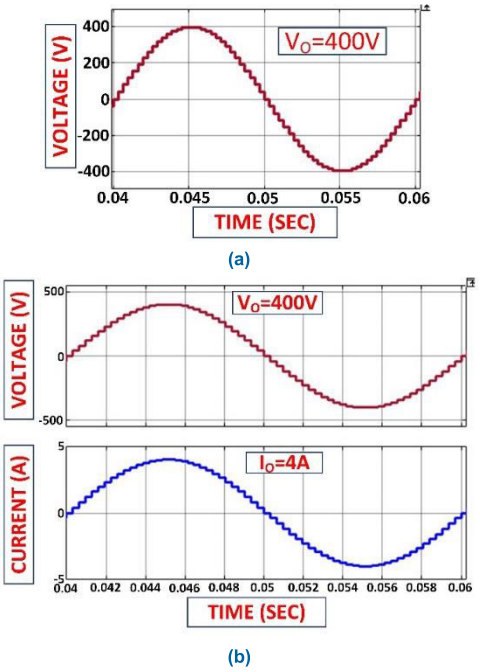


**FIGURE 11.** (a) Simulation result of Voltage waveform (b) Simulation result of Voltage wave and current waveform of 31-level MLI.

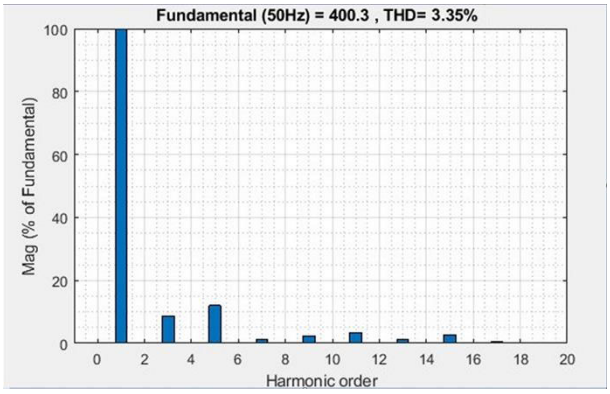


**FIGURE 12.** Simulation result of Voltage Harmonic spectrum of 31-level MLI.

ON-state transistor and diodes are conduction at instant 't', hence the conduction losses are

$$P_C = \frac{1}{\pi}\int_0^{\pi} [N_{Ton}(t)\,P_{TC}(t) + N_{Don}(t)\,P_{DC}(t)]\,dt \quad (9)$$

Switching losses $P_{SW}$ depends on the energy loss at the state of the switch on both ON-state ($P_{Son}$) and OFF-state ($P_{Soff}$), the switching period (T) is the addition of ON-state time ($T_{On}$) and OFF-state time ($T_{off}$) is linearly varied between voltage and current. Switch peak voltage is termed as $V_{SP}$, let the energy state of the switch be related as

$$P_{Son} = \frac{1}{T}\int_0^{T_{On}} [v(t)\,i(t)]dt$$

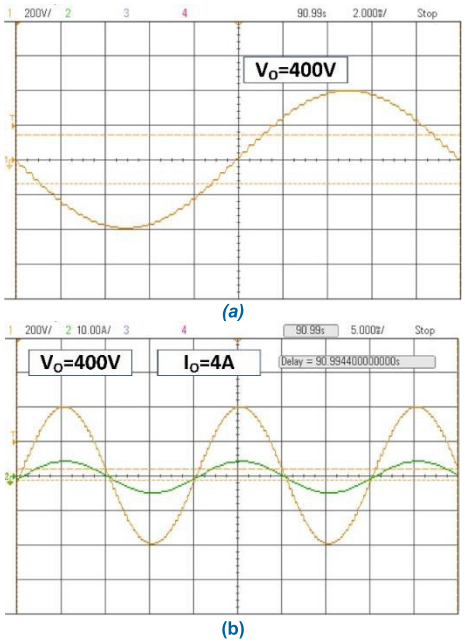


**FIGURE 13.** (a) Experimental results of voltage waveform (b) Experimental effects of voltage and current waveforms of 31-level MLI topology with R-Load.

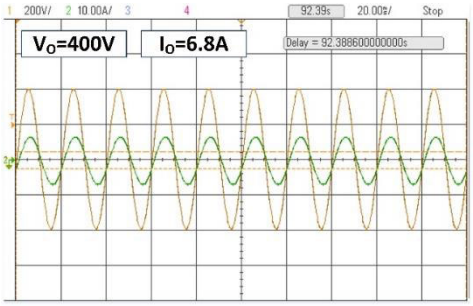


**FIGURE 14.** Experimental results of voltage and current waveforms of 31-level MLI topology with L-Load.

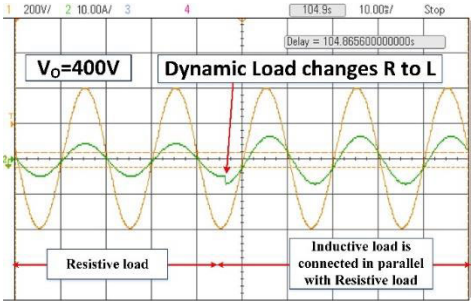


**FIGURE 15.** Experimental results of voltage and current waveforms of 31-level MLI topology with Dynamic load (R//L-Load).

$$P_{Son} = \frac{1}{6T}[V_{SP}IT_{On}] \tag{10}$$

$$P_{Soff} = \frac{1}{T}\int_{0}^{T_{Off}} [v(t)\, i(t)]dt$$

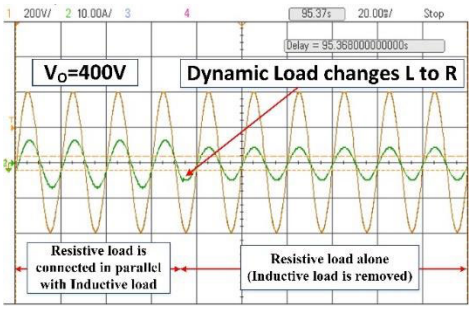


**FIGURE 16.** Experimental results of voltage and current waveforms of 31-level MLI topology with Dynamic load (L//R-Load).

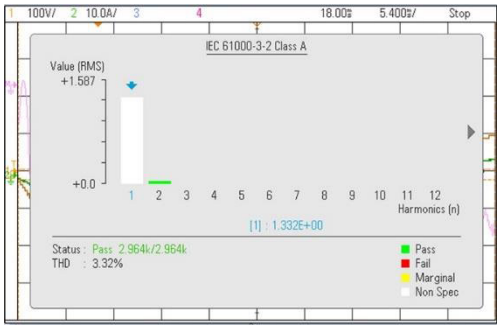


**FIGURE 17.** Experimental results of voltage harmonic spectrum of 31-level MLI topology.

$$P_{Soff} = \frac{1}{6T}[V_{SP}IT_{Off}] \tag{11}$$

$$P_{SW} = P_{Son} + P_{Soff} \tag{12}$$

Therefore the total losses

$$P_L = P_{SW} + P_C \tag{13}$$

Further, the efficiency $\eta$ can evaluate as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_L} \tag{14}$$

The output power can be got as follows;

$$P_{out} = V_{rms} * I_{rms} \tag{15}$$

As per IGBT CM75DU-12H datasheet $R_T = 0.4\Omega$, turn ON delay and rising times are 100nS and 250nS respectively. Similarly, the turn-OFF delay and rising times are 200nS 300nS, respectively, and $V_{SP}$ is 0.6V. The proposed 13-level MLI is made of 10 switches and 25 steps in one full cycle, whereas 31-level MLI is made of 14 switches and 61 steps in one entire cycle. Efficiency and power loss of proposed MLIs are tabulated in TABLE 5.

### *B. TOTAL STANDING VOLTAGE (TSV)*

The total standing voltage (TSV) is an essential factor for the choice of switches. This is the sum of peak blocking voltage across the individual power semiconductor device. The voltage stress of both types of switches i.e., bi-directional and unidirectional switches is given by: $V_{Sbi} = V_i$ and $V_{Suni} =$

**TABLE 6.** Comparison of 13-level with similar MLI topologies.

| *Topologies* | *Year* | $N_{LEL}$ | $N_{SW}$ | $N_{DK}$ | $N_D$ | $N_C$ | $N_{SDC}$ | $N_{MCD}$ | *CC/L* | $TSV_{PU}$ | *CC/L* | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | α = 0.5 | α = 1.5 |
| [55] | 2018 | 13 | 23 | 23 | - | 6 | 1 | 6 | 4.07 | 6.67 | 4.25 | 4.77 |
| [56] | 2019 | 11 | 8 | 7 | - | - | 3 | 3 | 1.63 | 4.2 | 1.82 | 2.2 |
| [57] | 2019 | 13 | 8 | 8 | - | - | 3 | 4 | 1.46 | 4 | 1.61 | 1.92 |
| [58] | 2019 | 13 | 14 | 14 | 9 | 2 | 2 | 5 | 3.15 | 5.33 | 6.41 | 7.23 |
| [59] | 2020 | 13 | 12 | 12 | 2 | 2 | 2 | 5 | 2.30 | 7 | 4.84 | 5.9 |
| [60] | 2020 | 13 | 10 | 10 | 1 | 1 | 2 | 4 | 1.84 | 6.3 | 3.86 | 4.83 |
| [61] | 2020 | 13 | 13 | 13 | 2 | 3 | 1 | 5 | 2.46 | 5.33 | 2.58 | 2.99 |
| [62] | 2020 | 13 | 10 | 10 | 4 | 4 | 1 | 5 | 2.22 | 5.5 | 2.36 | 2.78 |
| [63] | 2020 | 13 | 15 | 15 | - | 3 | 2 | 6 | 2.69 | - | - | - |
| [64] | 2020 | 13 | 12 | 11 | - | 2 | 1 | 4 | 2 | 6 | 2.15 | 2.61 |
| [65] | 2021 | 13 | 14 | 14 | 1 | 3 | 1 | 7 | 2.53 | 5.5 | 2.67 | 3.25 |
| **Proposed** | - | 13 | 10 | 10 | - | - | 3 | 5 | 1.76 | 2.66 | 1.83 | 1.95 |

**TABLE 7.** Comparison of 31-level with similar MLI topologies.

| **Topologies** | **Year** | $N_{SW}$ | $N_{DK}$ | $N_D$ | $N_C$ | $N_{SDC}$ | $N_{MCD}$ | **CC/L** | $TSV_{PU}$ | **CC/L** | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | α = 0.5 | α = 1.5 |
| [66] | 2020 | 18 | 18 | - | 4 | 2 | 8 | 1.35 | 5.66 | 1.44 | 1.62 |
| [67] | 2020 | 12 | 10 | - | 4 | 3 | 4 | 0.93 | 5.87 | 2.80 | 3.37 |
| [68] | 2019 | 16 | 16 | 2 | 4 | 2 | 8 | 1.29 | 5.67 | 2.63 | 3.0 |
| [69] | 2019 | 10 | 10 | - | - | 4 | 5 | 0.93 | - | - | - |
| **Proposed** | - | 14 | 14 | - | - | 4 | 7 | 1.03 | 2.4 | 1.07 | 1.15 |

$2V_i$ respectively, where i = 1,2……n and n are the number of complementary switches.

The maximum output voltage ($V_{O,max}$) of the developed topology is:

$$V_{O,max} = 400V$$

In the developed MLI topology, the respective voltages are the same for the switches' complimentary state, and all the switches are unidirectional. Hence the TSV can be obtained by using the following relations: For 13-level MLI.

$$\begin{aligned} TSV &= 2(V_{S1} + V_{S3} + V_{S5} + V_{S7} + V_{S9}) \\ &= 2(8V_{dc}) \\ &= 16V_{dc} \end{aligned}$$

For 31-level MLI.

$$\begin{aligned} TSV &= 2(V_{S1} + V_{S3} + V_{S5} + V_{S7} + V_{S9} + V_{S11} + V_{S13}) \\ &= 2(18V_{dc}) \\ &= 36V_{dc} \end{aligned}$$

### C. COST FUNCTION

The cost factor (CF) for the developed 13, and 31-level MLI can be obtained with several specifications like switch count $N_{SW}$, source count $N_{DCS}$, diode count $N_D$, capacitor count $N_{C,}$ total standing voltage TSV, driver circuits number $N_{DK}$ and number of sources $N_{SDC}$. The cost factor is estimated by using the formula represented in equation (8)[54].

$$CF = (N_{SW} + N_{SDC} + N_{DK} + N_D + N_C + \alpha TSV_{PU}) \quad (16)$$

$TSV_{pu}$ is given by

$$TSV_{PU} = \frac{V_{TSV}}{V_{OMAX}} \quad (17)$$

'$\alpha$' is the weight coefficient which is combined along with the multiplication of TSVpu. For the developed asymmetrical 31-level MLI topology, due to the absence of the diodes and capacitors, they are neglected, and the respective cost function is calculated using the following relation.

$$CF = (N_{SW} + N_{SDC} + N_{DK} + \alpha TSV_{PU}) \quad (18)$$

In general, the value of $\alpha$ is to be considered as the value should be greater and less than unity, respectively. In the developed MLI, the respective value of $\alpha$ is realized as 0.5 (<1) and 1.5 (>1) for the optimal evaluation of the cost function. The MLI is cost-effective based on the component level count (CF/L).

$$\begin{aligned} \text{For 13-level} \quad \text{CF/level} &= 1.83 \text{ if } \alpha = 0.5 \\ &= 1.95 \text{if} \alpha = 1.5 \end{aligned}$$

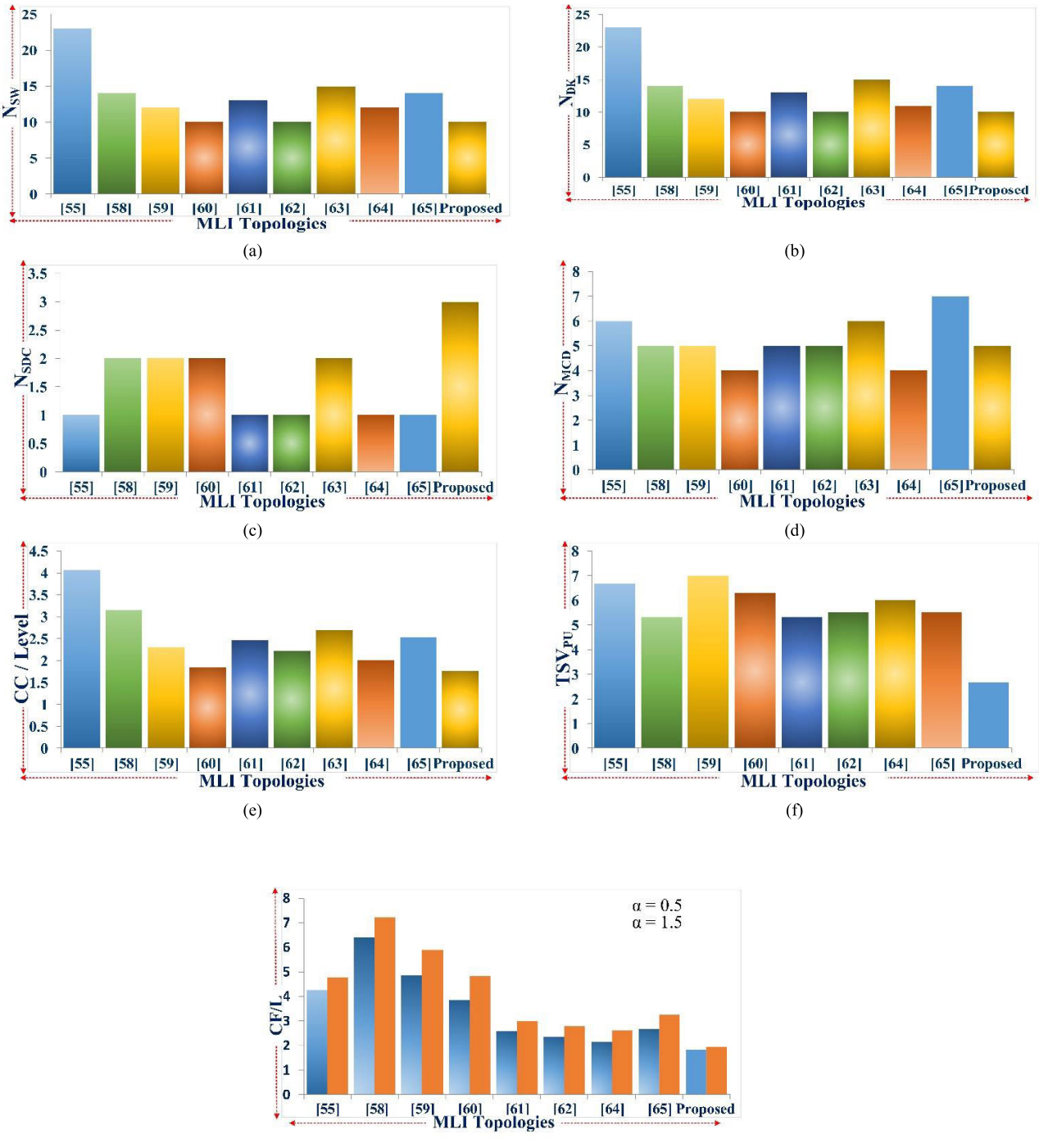


**FIGURE 18.** Comparison of (a) $N_{SW}$ (b) $N_{DK}$ (c) $N_{SDC}$(d) $N_{MCD}$(e) CC/L (f)$TSV_{PU}$ (g) CF/L with similar 13 level MLI topologies.

$$\text{For 31-level} \quad \text{CF/level} = 1.07 \text{ if } \alpha = 0.5$$
$$= 1.15 \text{if} \alpha = 1.5$$

The component level factor is calculated from equation 19.

$$F_{ccl} = \frac{N_s + N_d + N_{cap} + N_{dk} + n}{N_{Lev}} \tag{19}$$

### D. COMPARATIVE STUDIES

In this section a comprehensive comparison is made on switch count $N_{SW}$, number of driver circuits $N_{DK}$, diode count $N_D$, number of capacitors $N_C$, number of voltage sources $N_{SDC}$, total standing voltage per unit $TSV_{PU}$, the maximum number of conduction devices $N_{MCD}$, components count per level CC/L and cost factor per level CF/L. Comparison

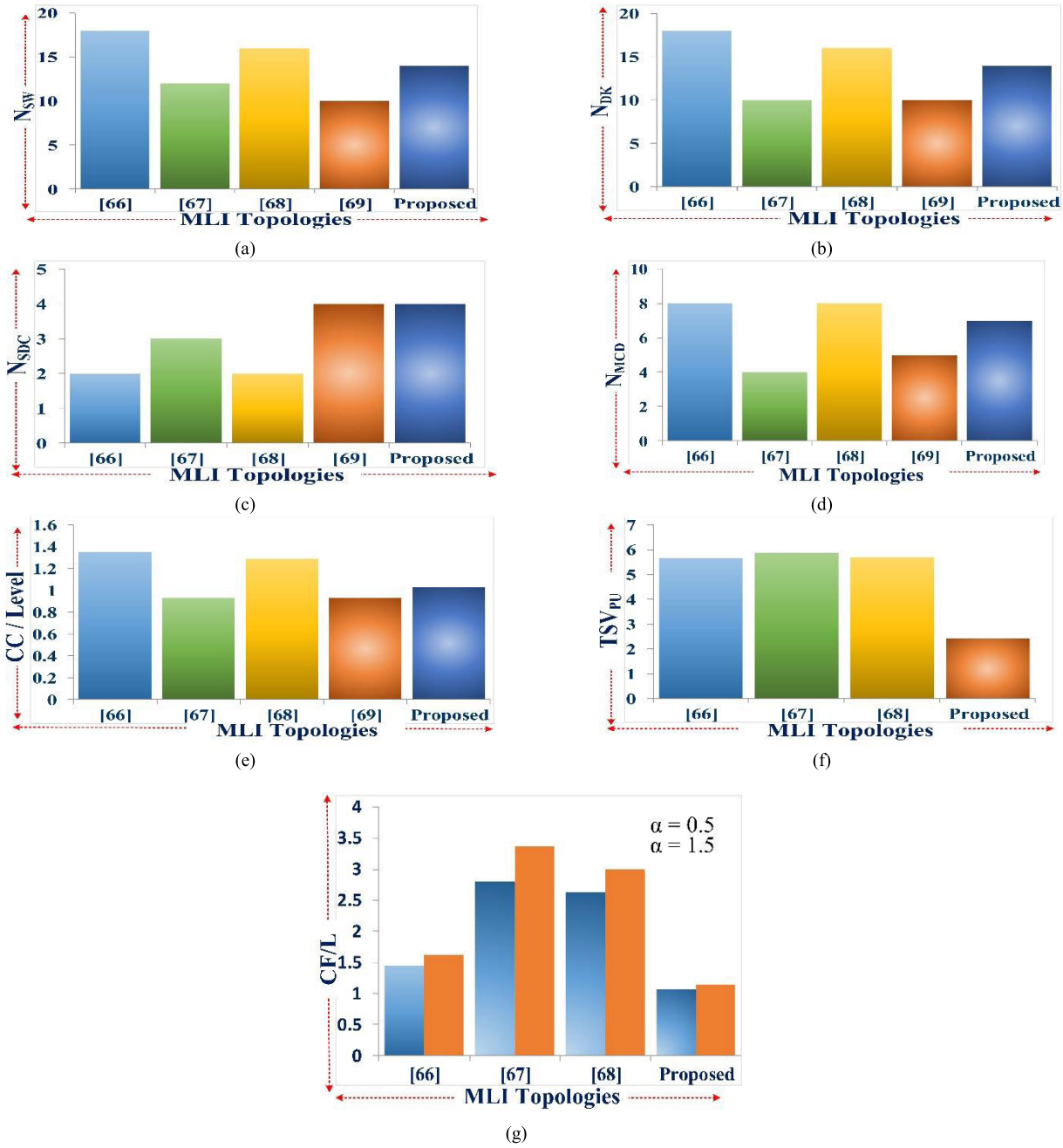


**FIGURE 19.** Comparison of (a) $N_{SW}$ (b) $N_{DK}$ (c) $N_{SDC}$(d) $N_{MCD}$(e) CC/L (f)$TSV_{PU}$ (g) CF/L with similar 31 level MLI topologies.

of 13-level MLI with similar recent topologies are done and tabulated in TABLE 6 similarly comparison of 31-level MLI with similar current topologies are done and tabulated in TABLE 7.

Number of switches $N_{SW}$, driver circuit count $N_{DK,}$ number of DC sources $N_{SDC}$, maximum conducting devices per level $N_{MCD}$, components count per level CC/L, total standing voltage per unit $TSV_{PU}$, cost factor per level CF/L are compared with similar 13 level MLI topologies and shown in Fig.17. Similarly, the comparison of 31 level MLI with similar topologies are represented in Fig.18, and the Impressive peculiarities of the developed topology are illustrated in Fig.19.

## V. CONCLUSION

A novel asymmetrical 31-level MLI topology is designed and implemented in this paper. The proposed 31-level MLI is developed from a fundamental 13-level MLI topology and is realized. The proposed MLI comprises fewer semiconductor devices which reduce the cost and also the size of the inverter. Moreover, the efficiency and reliability of the MLI get improved. The proposed MLI require fewer components

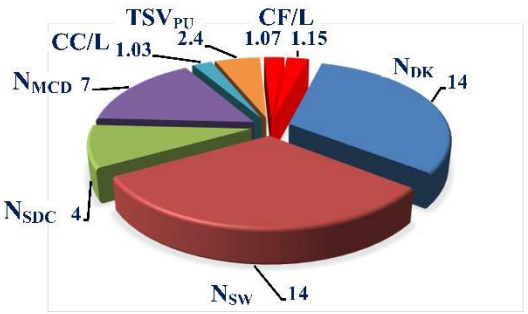


**FIGURE 20.** **Remarkable peculiarities of the proposed 31-level MLI Topology.**

to generate the desired output voltage level with a low THD. TSV and cost function is calculated, and all such parameters are compared with various existing topologies. The comparisons show the proposed MLI is highly efficient with fewer power losses. It is precisely noticed that simulation and experimental THD values are 3.35% and 3.32% respectively. $TSV_{pu}$ is 2.4; efficiency is 92.32%, CF/L value for both values of $\alpha$ is 1.07 and 1.15 respectively, which shows that the cost is significantly less compared with various topologies. The developed MLI is tested with multiple dynamic load variations. Based on the several tests carried out, the developed MLI is well suited for renewable energy applications.

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