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ORIGINAL RESEARCH PAPER

Novel high voltage gain dc–dc converter with dynamic analysis

Mohammad Ghaffarpour[1] | **Reza Ebrahimi**[1] | **Hossein Madadi Kojabadi**[1] | **Liuchen Chang**[2] | **Josep M. Guerrero**[3]

[1] Renewable Energy Research Centre, Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran

[2] Department of Electrical and Computer Engineering, University of New Brunswick, Fredericton, Canada

[3] Department of Electrical Engineering, Aalborg University, Aalborg, Denmark

Correspondence
Reza Ebrahimi, Renewable Energy Research Centre, Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran.
Email: r.ebrahimi@sut.ac.ir

Abstract

This study proposes a non-isolated dc–dc converter based on a coupled inductor and switch-capacitor–boosting techniques. The goal of the proposed topology is to increase the voltage gain with low-duty cycle, so voltage stresses are decreased across power switches and diodes. The power switches are controlled by pulse width modulation. The common ground of input and output of the proposed converter makes it suitable for many applications such as photovoltaic systems. The proposed converter topology is discussed in continuous and discontinuous operation modes. A dynamic analysis of the proposed converter is also provided. Simulation and experimental verifications are presented to prove the effectiveness of the proposed topology.

1 | INTRODUCTION

Since traditional energy sources like fossil fuels are not clean and renewable, they will be gradually eliminated in the near future. On the other hand, the energy observed from renewable sources is extremely low and a boost converter is typically used to increase the output voltage of these kinds of energy sources like photovoltaic (PV) systems which are widely used in industry and home applications. Heating water and lightening by PV systems are the most common usage of these renewable energies. Step-up dc–dc converters have been widely used for many industrial applications such as uninterruptable power supplies (UPS) and dc-link stages of renewable energy sources. Therefore, there is a consistent demand for reliable, efficient, small sized, and lightweight step-up dc–dc converters that are commonly used in a large number of power conversion applications [1]; the literature has reported on various voltage-boosting techniques, in which fundamental energy-storing elements in conjunction with switches and diodes are utilised in the circuit. A new family of dc–dc converters based on three-state switching cell and voltage multiplier with high voltage gain that can be applied in uninterruptible power supplies and fuel cell systems is presented in [2]. This new topology is also suitable in the case where dc voltage step-up is demanded, such as audio amplifiers and many other applications. The conventional non-isolated boost converter is the most popular topology that has high-dc voltage gain, but it suffers from limited conversion efficiency at high-duty cycle values. In order to overcome such limitations and improve the conversion ratio, derived topologies can be found in numerous publications. Some of the most important non-isolated boost-based dc–dc converters are classified and reviewed in [3].

A novel high step-up dc–dc converter with coupled inductors has been proposed in [4] which includes coupled inductors, diodes, capacitors, and metal-oxide semiconductor field-effect transistors (MOSFETs). The duty cycle of the power switches can vary in a wider range and the voltage gain is higher in comparison to most of the other coupled-inductor-based converters. In addition, a regenerative snubber is used to absorb the energy of stray inductance. A high step-up converter and a voltage doubler are proposed in [5], the integration of the quadratic boost converter makes the system easier to lift up its voltage gain through slightly increasing the duty ratio of the single switch. Besides, the voltage doubler further increases the voltage gain of the system as the turns ratio rises. To achieve an extremely large voltage conversion ratio with an appropriate duty cycle and reduction of voltage stress on power devices, a converter is proposed in [6], which extended voltage doubler cell, and diode-capacitor techniques are used in this converter. Moreover, the energy stored in the leakage

inductance of coupled inductor efficiently recycled to the output.

A new high step-up dc–dc converter especially for regulating the dc interface between various microsources and a dc-ac inverter to electricity grid is proposed in [7]. The figuration of the converter is a quadratic boost converter with the coupled inductor, the operating principles and steady-state analyses of continuous-conduction and boundary-conduction modes are discussed in detail. As mentioned above, the output voltage of renewable energy sources such as PV systems are typically much lower than the voltage required by the dc bus, and the output voltage drops significantly as the output current increases. In order to match the output voltage of renewable sources to dc-bus voltage, a new dc–dc boost converter with a wide input range and high voltage gain is proposed to act as the required power interface, which reduces voltage stress across the power devices and operates with an acceptable conversion efficiency [8]. Thus, a dc–dc boost converter with high voltage gain is required to increase the low dc output voltages. Many different topologies have been introduced and implemented with high voltage gain for this purpose.

To simplify these topologies and their applications, they are divided into two groups, (i) isolated and (ii) non-isolated. Isolated topologies are used in medical and military purposes; and the cost and losses of non-isolated converters are low. There are so many techniques to boost voltage in high step-up dc–dc converters. The switch-capacitor (charge pump) which meets the input voltage and power level needs of the majority of modern PV panels while still being suitable for connection with a high-voltage dc bus is proposed in [9]. The voltage multiplier switched inductor, and voltage-lift techniques [10] are other topologies for boosting applications that have been reported so far that utilises transformer with low turns ratio. Analysis and design of a single-switch high step-up coupled inductor boost converter are presented in [11]. With the aid of coupled inductor, the proposed converter can achieve high voltage gain without an extreme duty cycle. Moreover, the converter features continuous input current, which is desirable and friendly to the battery, fuel cell, and PV applications.

Multistage (multilevel) converters are thoroughly reviewed in [12] to establish the current state-of-the-art technology and trends, and provide readers with a comprehensive review of where multilevel converter technology stands and is heading. A non-isolated high step-up dc–dc converter with dual-coupled inductors suitable for distributed generation applications is proposed in [13]. By implementing an input parallel connection, this structure inherits shared input current with low ripple, which also requires small capacitive filter at its input. Moreover, this topology can reach high voltage gain by using dual-coupled inductors in series connection at the output stage. This converter uses active clamp circuits with a shared clamp capacitor for the main switches. In addition to the active clamp circuit, the leakage energy is recycled to the output by using an integrated regenerative snubber. pulse width modulation (PWM) boost converters are more prevalent and suitable for various applications. The main advantages of these converters are their simplicity and reduced element counts. Although the PWM method is more preferable in most applications, it has the reverse-recovery problem of output diodes and the objection of hard switching [14]. A quasi-active switched-inductor structure as a high step-up dc–dc converter for renewable energy systems is presented in [15] that is composed of two coupled inductors which can be integrated into one magnetic core. Usage of coupled inductor is more common in dc–dc boost converters, which achieve a high step-up gain without utilising either a large duty cycle or a high turns ratio [16]. An interleaved converter which benefits the coupled inductor and built-in transformer voltage multiplier cell (VMC) is proposed in [17]. Compared with the other converters with only built-in transformer or only coupled inductors, the combination of these techniques gives an extra degree of freedom to increase the voltage gain. The VMC is composed of the windings of the built-in transformer and coupled inductors, capacitors, and diodes. The voltage stress of MOSFETs are clamped at low values and can be controlled via the turns ratio of the built-in transformer and coupled inductor that increases the design flexibility. A model is proposed and used to derive the small-signal control-to-output transfer function of the converter incorporating coupled inductors, with which the effect of coupling on the dynamic behaviours of the converter power stage can be easily evaluated [18]. The recently developed symmetrical-coupled inductor model is first extended to include the inductor-winding dc resistance (DCR). The extended model is then used to analyse the influence of the coupling on the DCR-based current-sensing schemes popularly used in multiphase-switching regulators. It is found that the time-constant matching condition in coupled inductor converters needs to be modified to include the coupling coefficient. Even though these methods have some disadvantages, using coupled inductor causes core and conduction losses of windings [19] and leakage inductances also cannot be ignored mostly. Using a coupled power inductor in a multistage dc–dc power converter instead of using multiple single-phase power inductors reduces the inductor size and achieve better steady-state and transient performances [20]. To reduce voltage stress on the main power switch in high step-up dc–dc converters, a passive clamp circuit is applied in [21], which leads to utilising a power switch with lower on-state resistance, which decreases conduction losses. To alleviate the power losses caused by the fluctuation of the output current of the PV array, a dc–dc converter with a high voltage gain is proposed for PV generation systems in [22]. The input current ripples of the converter can be greatly reduced by the application of coupled inductors. Then the electrolytic capacitor on the input side could be replaced by a polypropylene capacitor with a smaller capacity. A new non-isolated high step-up dc–dc converter using one switch and low voltage stress on semiconductors is presented for PV applications in [23]. The proposed converter consists of one switch in the input side (S), voltage multiplier units (D-C-L), one diode in the output side (Do) and one capacitor (Co). In order to achieve high voltage gain and power level, the proposed converter can be extended to n stages of voltage multiplier units. Hence, the output voltage level will be reasonably increased and the nominal value of power devices will be decreased. A new non-isolated dc–dc cuk–boost converter structure with high-voltage gain is proposed in [24] which

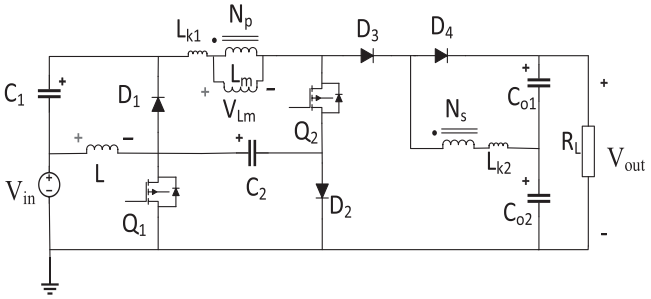


FIGURE 1 The topology of the proposed converter

is composed of boost and cuk converters and has low output voltage ripple and high voltage gain in comparison with the traditional boost and cuk converter. The operation of diodes and switches of this converter under zero voltage and zero current switchings can play an important role in reducing circuit losses.

This study presents a high-gain dc–dc converter, which is shown in Figure 1 along with the analyses of dynamic characteristics. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analysed. The major contributions of the proposed dc–dc converter are:

1. Providing high voltage gain in medium-duty cycles.
2. The low voltage stress on semiconductors.
3. The output is not floating and has common ground with the input side.
4. The number of elements per voltage gain is low.
5. Dynamic analysis has been included.
6. Leakage energy of coupled inductor is recycled through the diode to the output of the converter.

Because of the converter's high voltage gain and continuous input current, the proposed topology is desirable and friendly to the battery, fuel cell, UPS, and PV applications.

2 | OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

2.1 | Configuration of the proposed converter

The novel dc–dc converter uses two power switches (Q_1 and Q_2), four diodes (D_1–D_4), four capacitors (C_1, C_2, C_{o1}, C_{o2}), an inductor (L) and a coupled inductor, which is consist of a magnetising inductor L_m, a primary leakage inductor L_{k1} and a secondary leakage inductor L_{k2} to boost input voltage. Inductor L and input source V_{in} operate as energy resources to charge capacitors C_1 and C_2. A coupled inductor is another energy storage component which not only helps to boost input voltage but also reduces the use of another inductor [25]. Diodes D_3 and D_4 are implemented to recycle leakage energy of coupled inductor and elimination of voltage spikes across power switches, respectively.

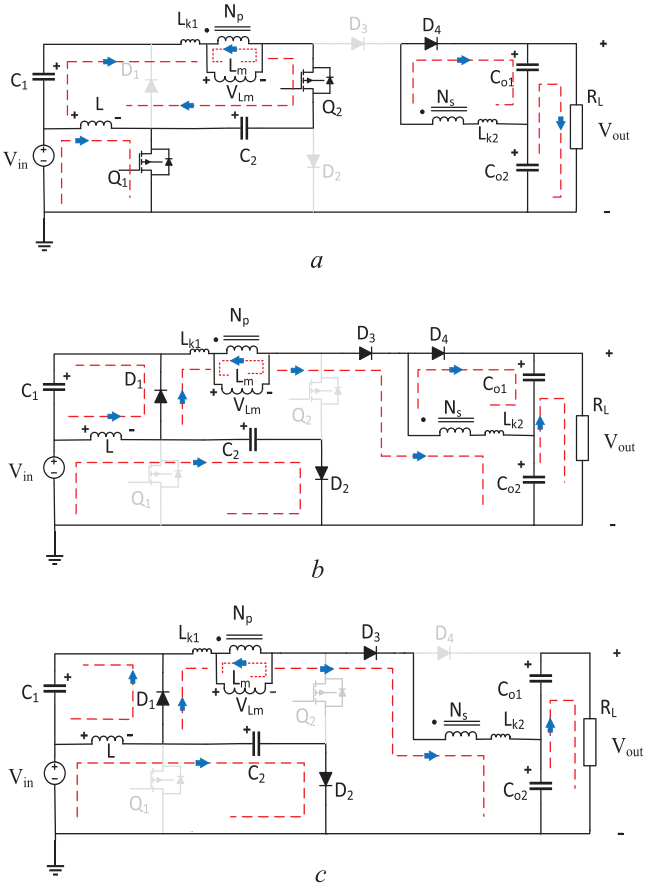


FIGURE 2 Switching modes of proposed converter in continuous conduction mode (CCM) operation, (a) mode 1, (b) mode 2, (c) mode 3

The secondary side of coupled inductor helps to further increase of voltage gain on the high-voltage side. The turns ratio of coupled inductor is n which is equal to N_s / N_p, where N_p is the number of primary windings turns, and N_s is the number of secondary windings turns. Figure 1 depicts the configuration of the proposed dc–dc converter.

2.2 | Operating principles of the proposed converter

Mode 1 (t_0–t_1): As shown in Figure 2(*a*), Q_1, and Q_2 are turned on simultaneously, inductor L is charged by input dc power supply and the voltage across the input inductor L is V_{in}. Due to the reverse bias of D_1, D_2, and D_3, they will be off. Capacitors C_1 and C_2 deliver their energy to the magnetising inductor L_m and the primary leakage inductor L_{k1}. The primary-side current of the coupled inductor (i_{Lk1}) increases linearly and C_1 and C_2 are discharged by the primary-side current of the coupled inductor. Thus, currents i_{Lm}, i_{Lk1}, and i_L are increased. Meanwhile, due to the forward bias of D_4, the diode will conduct and current flows from the secondary side of the coupled inductor to capacitor C_{o1} and secondary-side current of the coupled inductor (i_{Lk2}) is increased. The magnetising inductor Lm also transfers the

magnetising energy through the coupled inductor to secondary leakage inductor L_{lk2} to charge capacitor C_{o1}. The output load has been disconnected from the converter through the diode D_3, also, the energy stored in C_{o1}, and C_{o2} are discharged to the load R.

Mode 2 (t_1–t_2): During this short interval, both powers switches Q_1, and Q_2 are turned off simultaneously as indicated in Figure 2(b). According to the forward bias of D_1 and D_2, diodes are conducted. Thus, inductor L releases its energy to charge C_1 and C_2. Meanwhile, due to the forward bias of D_3 and D_4, diodes will conduct and the magnetising inductor L_m transfers its magnetising energy through coupled inductor and diode D_3 to the secondary leakage inductor L_{lk2} that causes to charge capacitor C_{o2}. In addition, the energy stored in the leakage inductance L_{lk1} is recycled and transferred via D_1 and D_3 to C_{o2}. Therefore, current flows from the converter to load (the output capacitor C_{o2}). Thus, the primary-side currents of the coupled inductor (i_{Llk1}) and current i_L will be decreased. Besides, capacitor C_{o1} is charged through D_4 and secondary side of the coupled inductor. Thus, the secondary-side current of the coupled inductor (i_{Llk2}) is decreased. The energy stored in C_{o1} and C_{o2} is discharged to the load R.

Mode 3 (t_2–t_3): As shown in Figure 2(c), Q_1, and Q_2 remain off. Due to the negative voltage difference across D_4, the diode is not conduced. Diodes D_1, D_2, and D_3 are on and they are still conducted. Capacitor C_1 is charged by the energy of inductor L. At the same time, capacitor C_2 is charged by input DC power supply and inductor L in series. Magnetising inductor L_m, like mode 2, transfers its magnetising energy through coupled inductor and diode D_3 to the secondary leakage inductor L_{lk2} that cause to charge capacitor C_{o2}. The output voltage V_{out} is equal to the sum of the voltage across C_{o1} and C_{o2}.

3 | STEADY-STATE ANALYSIS OF VOLTAGE GAIN

3.1 | Continuous conduction mode

Suppose that the switching period is T and D is the duty cycle of the power switches, for this analysis, it is assumed that inductor current and capacitor voltages are constant during each switching period. Since the time interval of mode 2 is short, only modes 1 and 3 are considered at CCM operation for the steady-state analysis, and the coupling coefficient k of the coupled inductor in the proposed converter is considered as $L_m / (L_m + L_{lk1})$.

In addition, the forward-voltage drop of diodes and on-state resistance of power semiconductors are neglected to ease mathematical calculations.

By utilisation of kirchhoffs voltage law (KVL) in mode 1 (Figure 2(a)), the following equations can be written as

$$V_L = V_{in} \tag{1}$$

$$V_{Lm} + V_{lk1} = V_{C1} + V_{C2} + V_L \tag{2}$$

$$V_{Lm} = k\,(V_{C1} + V_{C2} + V_L) \tag{3}$$

$$V_{lk1} = (1-k)\,(V_{C1} + V_{C2} + V_L) \tag{4}$$

$$V_{Co1} = nV_{Lm} + V_{lk2} \tag{5}$$

where n corresponds to the turns ratio of the coupled inductor.

Also in mode 3, we have

$$V_{in} = V_L + V_{C2} \tag{6}$$

$$V_L = -V_{C1} \tag{7}$$

$$V_{in} = V_L + V_{Lm} + V_{lk1} + nV_{Lm} + V_{lk2} + V_{Co2} \tag{8}$$

The following equations can be derived according to the volt-second balance principle for the inductor L:

$$\int_0^{DT} V_{in}\,dt + \int_0^{(1-D)T} (V_{in} - V_{C2})\,dt = 0 \tag{9}$$

$$\int_0^{DT} V_{in}\,dt + \int_0^{(1-D)T} (-V_{C1})\,dt = 0 \tag{10}$$

$$V_{C1} = \frac{DV_{in}}{1-D} \tag{11}$$

$$V_{C2} = \frac{V_{in}}{1-D} \tag{12}$$

The voltage across magnetising inductor L_m by the volt-second balance principle is shown as

$$\int_0^{DT} k\,(V_{C1} + V_{C2} + V_{in})\,dt + \tag{13}$$

$$\int_0^{(1-D)T} \left(\frac{V_{C2}}{n+1} - V_{lk1} - \frac{V_{Co2}}{n+1}\right) dt = 0$$

$$\int_0^{DT} \left(\frac{V_{Co1}}{n} - V_{lk1}\right) dt +$$

$$\int_0^{(1-D)T} \left(\frac{V_{C2}}{n+1} - V_{lk1} - \frac{V_{Co2}}{n+1}\right) dt = 0 \tag{14}$$

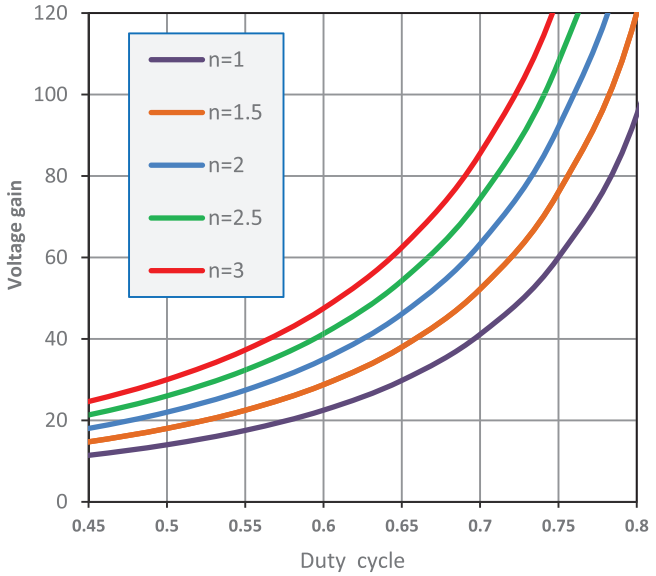


FIGURE 3 Voltage gain comparison of proposed converter for different turns ratios

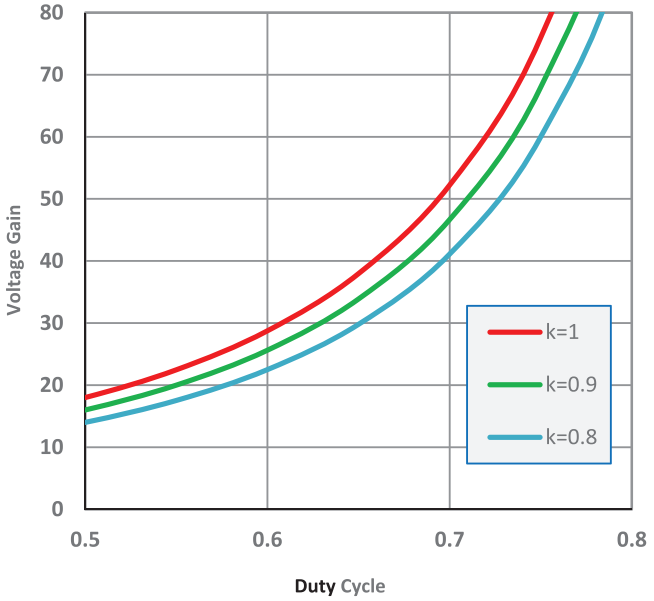


FIGURE 4 The relationship between voltage gain, duty cycle, and coupling coefficient

By substituting Equations (11) and (12) into (13) and (14), and assuming that L_{k2} is equal to n_{Lk1}, the average voltage of capacitors C_{o1} and C_{o2} are determined as follows:

$$V_{Co1} = \frac{2nV_{in}}{1-D} \tag{15}$$

$$V_{Co2} = \frac{2\,(n+1)\,(k+D-1)+(1-D)}{(1-D)^2}\,V_{in} \tag{16}$$

The output voltage V_o can be express as

$$V_o = V_{Co1} + V_{Co2} \tag{17}$$

By substituting Equations (15) and (16) into (17), we can obtain the voltage gain M_{CCM}:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2k\,(n+1)+(D-1)}{(1-D)^2} \tag{18}$$

As shown in Figure 3, the comparison of voltage gains versus the duty cycle is presented for different turns ratios. This figure illustrates that higher voltages are obtained while the turns ratio (n) is increased.

The effect of the coupling coefficient (leakage inductance) on the voltage gain is shown in Figure 4, where the turns ratio is set to 1.5. It is clear that by higher values of duty cycle, voltage gain is affected strongly. Also, higher leakage inductance (lower k) will lead to lower voltage gain.

Figure 5 shows the key waveforms of the proposed converter. It can be obtained that capacitors C_{o1} and C_{o2} have the same charging and discharging states. While current of the inductor, L is increasing linearly (when Q_1 and Q_2 are turned on), the primary-side current of (I_{Lk1}) and secondary-side current (I_{Lk2}) of coupled inductor increases. It is important to mention that the magnetising current of inductor L_m is increasing and decreasing linearly. Diodes D_1 and D_2, are not conducting in mode 1, so their currents are zero, and diode D_3 is conducting in modes 2 and 3. Also, D_4 is forward-biased in modes 1 and 2, which is shown in Figure 5.

3.2 | Discontinuous conduction mode

By increasing the output load (R), decreasing inductance (L), or switching frequency (f), the converter will enter to DCM, which causes the inductor (L) and coupled inductor (L_m) currents to be zero for a short period. The primary leakage inductance is neglected during the following analysis. Modes 1 and 2 of DCM mode are similar to CCM mode and mode 3 is shown in Figure 6.

The operating modes are described as

Mode 1 (t_0–t_1): During this interval (Figure 2(a)), switches Q_1 and Q_2 are turned on simultaneously, the current of inductor L is increasing linearly and storing energy, capacitor C_1 and C_2 are discharging which cause an increase in the magnetising and leakage inductance current of the coupled inductor (I_{Lm}, I_{Lk1}). On the high-voltage side, the secondary side of coupled inductor charges the capacitor C_{o1} through diode D_4. This mode is terminated when the current I_{Lm} reaches its peak value at $t = t_1$.

Mode 2 (t_1–t_2): As shown in Figure 2(b), switches Q_1 and Q_2 are turned off simultaneously. Due to the forward-bias of diodes D_1, D_2, D_3, and D_4, they are conducted. Thus, inductor L releases its energy to charge C_1 and C_2, and the current of inductor L decreases linearly. On the high-voltage side, the primary and secondary sides of the coupled inductor will boost

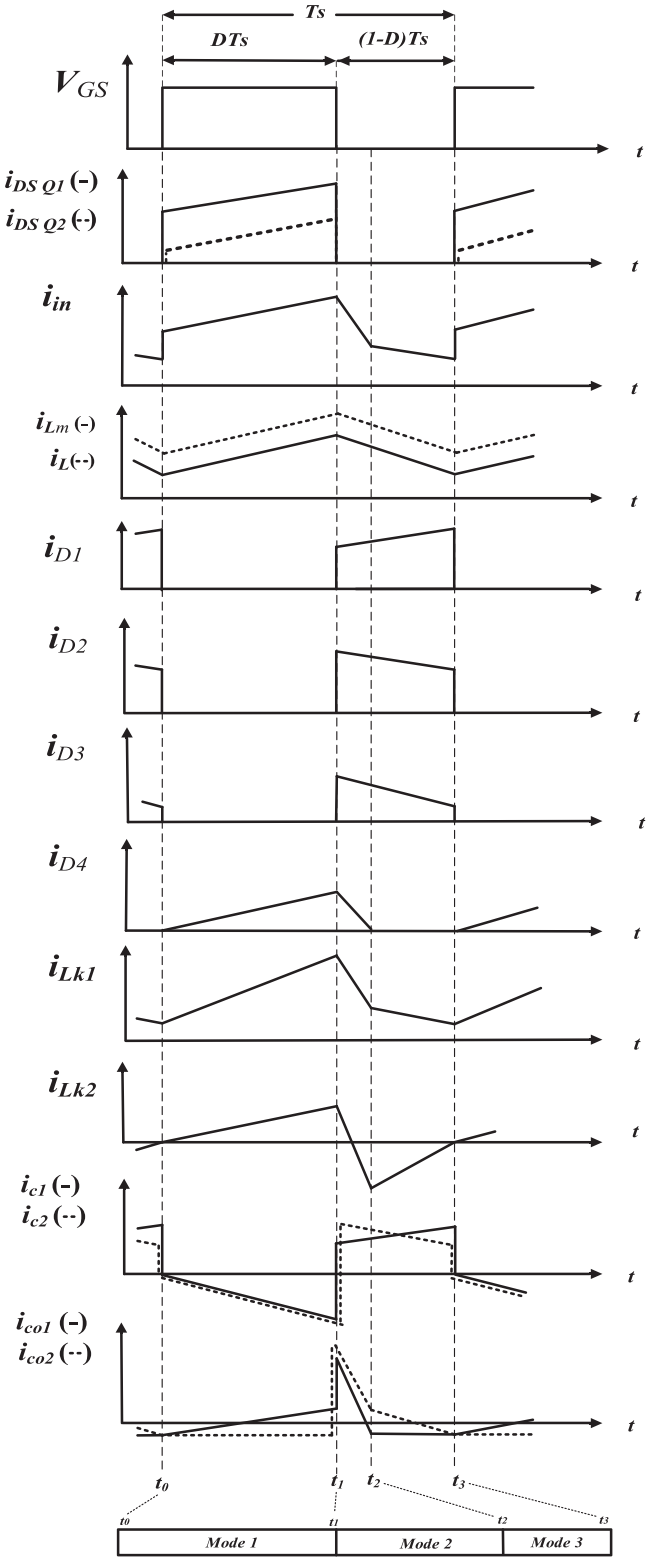


FIGURE 5 Key operation waveforms of the proposed converter in CCM operation

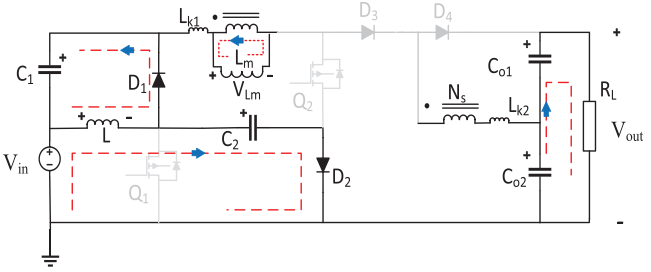


FIGURE 6 Mode 3 of the proposed converter in discontinuous conduction mode (DCM) operation

the voltage level of capacitor C_{o2}. This mode will be ended by reaching the current of diode D_3 to zero at $t = t_2$.

Mode 3 (t_2–t_3): Diodes D_1 and D_2 are conducting as depicted in Figure 2(c) and switches Q_1 and Q_2 are still turned off. This interval causes the current of the primary side of the coupled inductor to be zero and creates the DCM operation because there is no path in which current i_{lk1} can flow. This mode terminates when the current of inductor L starts to increase from zero at $t = t_3$.

By using the assumptions of the CCM, Figure 7 shows the key waveforms in DCM operation and the following equations can be derived in mode 1:

$$V_{in} = V_L \tag{19}$$

$$V_{Lm} = V_{in} + V_{C1} + V_{C2} \tag{20}$$

$$n\,V_{Lm} = V_{Co1} \tag{21}$$

$$V_o = V_{Co1} + V_{Co2} \tag{22}$$

By applying KVL in mode 2, the following equations can be obtained:

$$V_L = V_{in} - V_{C2} \tag{23}$$

$$V_L = -V_{C1} \tag{24}$$

$$V_{Lm} = \frac{V_{C2} - V_{Co2}}{n+1} \tag{25}$$

Finally, the equations of mode 3 in DCM operation can be derived according to Figure 6.

$$V_L = -V_{C1} \tag{26}$$

$$V_L = V_{in} - V_{C2} \tag{27}$$

By considering that the average voltage of inductors is zero during a period (volt-second balance for inductor L and L_m in

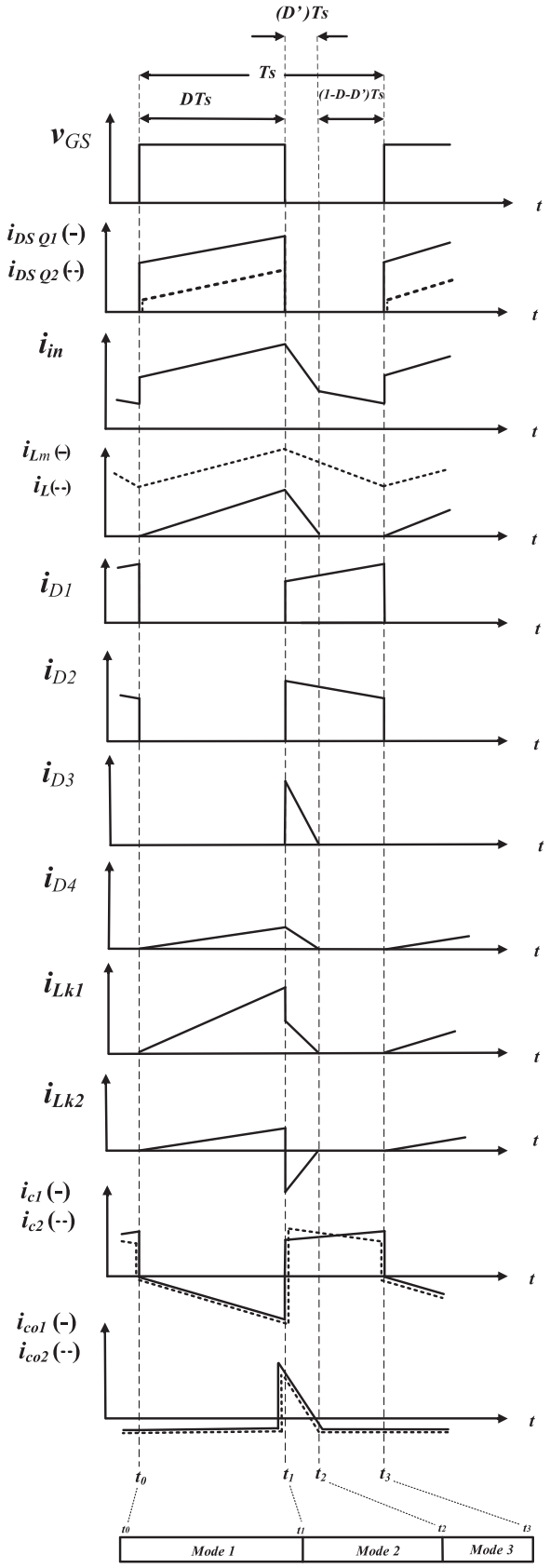


FIGURE 7 Key operation waveforms of the proposed converter in DCM operation

DCM operation) the following equations can be obtained:

$$\int_0^{DT} V_{in}dt + \int_0^{D'T} (V_{in} - V_{C2})\,dt + \int_0^{(1-D-D')T} (V_{in} - V_{C2})\,dt = 0 \tag{28}$$

$$\int_0^{DT} V_{in}dt + \int_0^{D'T} (-V_{C1})\,dt + \int_0^{(1-D-D')T} (-V_{C1})\,dt = 0 \tag{29}$$

$$\int_0^{DT} (V_{in} + V_{C1} + V_{C2})dt + \int_0^{D'T} \left(\frac{V_{C2} - V_{Co2}}{n+1}\right) dt + \int_0^{(1-D-D')T} (0)\;dt = 0 \tag{30}$$

$$\int_0^{DT} \left(\frac{V_{Co1}}{n}\right) dt + \int_0^{D'T} \left(\frac{V_{C2} - V_{Co2}}{n+1}\right) dt + \int_0^{(1-D-D')T} (0)\;dt = 0 \tag{31}$$

By simplifying Equations (28) to (31), we can get:

$$V_{C1} = \frac{DV_{in}}{1-D} \tag{32}$$

$$V_{C2} = \frac{V_{in}}{1-D} \tag{33}$$

$$V_{Co1} = \frac{2nV_{in}}{1-D} \tag{34}$$

$$V_{Co2} = \frac{V_{in}\left(2n + 2D + D'\right)}{(1-D)\,D'} \tag{35}$$

The output voltage V_o can be calculated by the sum of voltages across capacitor C_{o1} and C_{o2} that is simplified as

$$V_o = V_{Co1} + V_{Co2} = \frac{V_{in}\left(2Dn + 2D'n + 2D + D'\right)}{(1-D)\,D'} \tag{36}$$

According to Equation (36) the relationship between D and D' is calculated as Equation (37):

$$D' = \frac{2D(n+1)}{\frac{V_o}{V_{in}}(1-D) - (2n+1)} \tag{37}$$

As shown in Figure 6, the output current (I_o) is expressed by

$$I_o = I_{D4} + I_{Co1} \tag{38}$$

Because the average current value of C_{o1} is equal to zero, so we have:

$$I_o - I_{D4} = 0 \rightarrow I_o = \frac{I_{Lmp}D'}{2n} \tag{39}$$

The peak value of magnetising current (I_{Lmp}) is equal to:

$$I_{Lmp} = \frac{V_{C1} + V_{C2} + V_{in}}{L_m} DT = \frac{2}{1-D}\frac{V_{in}}{L_m}DT \tag{40}$$

By substitution Equations (40) into (39), the following equation can be derived:

$$I_o = \frac{DD'T}{n(1-D)L_m} V_{in} \tag{41}$$

By utilising Equations (37) and (41), we can obtain the following relationship:

$$I_o = \frac{V_o}{R} = \frac{DT}{n(1-D)L_m} \times \frac{2D(n+1)}{\frac{V_o}{V_{in}}(1-D) - (2n+1)} V_{in} \tag{42}$$

The normalised magnetising time constant of the coupled inductor (τ_{Lm}) is defined as

$$\tau_{Lm} = \frac{L_m}{RT} = \frac{L_m f}{R} \tag{43}$$

By substituting Equations (43) into (42), the equation of M_{DCM} can be obtained.

$$M_{DCM} = \frac{(2n+1) + \sqrt{(2n+1)^2 - \frac{8D^2(n+1)}{\tau_{Lm}n}}}{2(1-D)} \tau_{Lm} \tag{44}$$

The voltage gain of DCM is obtained as Equation (44) which can be used to design components of converters. Besides, the conversion ratio is independent of the load during CCM but when it enters in DCM, it depends on the load. To avoid this problem, the voltage gain of continuous and discontinuous modes are used to determine the boundary condition, which helps to design components properly.

3.3 | Boundary conduction mode (BCM)

To design the elements of the proposed converter the complete analysis of BCM operation is presented as follows:

The normalised inductor time constant for L_m is calculated as Equation (43), and for calculating the normalised inductor time constant of inductor L, the following relationship can be written as

$$I_{in} = \frac{P_o}{V_{in}} = \frac{V_o^2}{RV_{in}} \tag{45}$$

$$I_{L(Boundary)} = \Delta i_L = \frac{i_{Lpeak}}{2} = \frac{DTV_{in}}{2L} = \frac{V_o^2}{RV_{in}} \tag{46}$$

$$\tau_L = \frac{L}{RT} = \frac{L_{(Boundary)}f}{R} \tag{47}$$

$$\tau_{LB} = \tau_{L(Boundary)} = \frac{D}{2}\left[\frac{(1-D)^4}{(2n+D+1)^2}\right] \tag{48}$$

In BCM, the CCM and DCM voltage gains are equal, so the normalised magnetising inductor time constant is calculated as

$$M_{CCM} = M_{DCM} \tag{49}$$

$$\tau_{LmB} = \tau_{Lm(Boundary)} = \frac{D(1-D)^2}{n(2n+D+1)} \tag{50}$$

By Equations (48) and (50), Figures 8(a) and (b) can be depicted.

The relationship between the normalised boundary time constant, duty cycle, and the turns ratio for inductors L and L_m are plotted in Figures 8(a) and (b), respectively. The inductor L and L_m will be operated in CCM, once the L and L_m are higher than L_{mB} and L_B, respectively.

3.4 | Current analysis

Assumed that the output power is equal to input power. Using Equation (18), input and output currents relationship is obtained as

$$I_{in} = \frac{2k(n+1) + (D-1)}{(1-D)^2} I_o \tag{51}$$

By applying kirchhoffs current law (KCL) in modes 1 and 3 and Equation (51), the currents of capacitors in each mode can be obtained as

Mode 1: Q_1 and Q_2 are on.

$$i_{c1} = i_L - i_{in} \tag{52}$$

$$i_{c2} = -i_{Lk1} \tag{53}$$

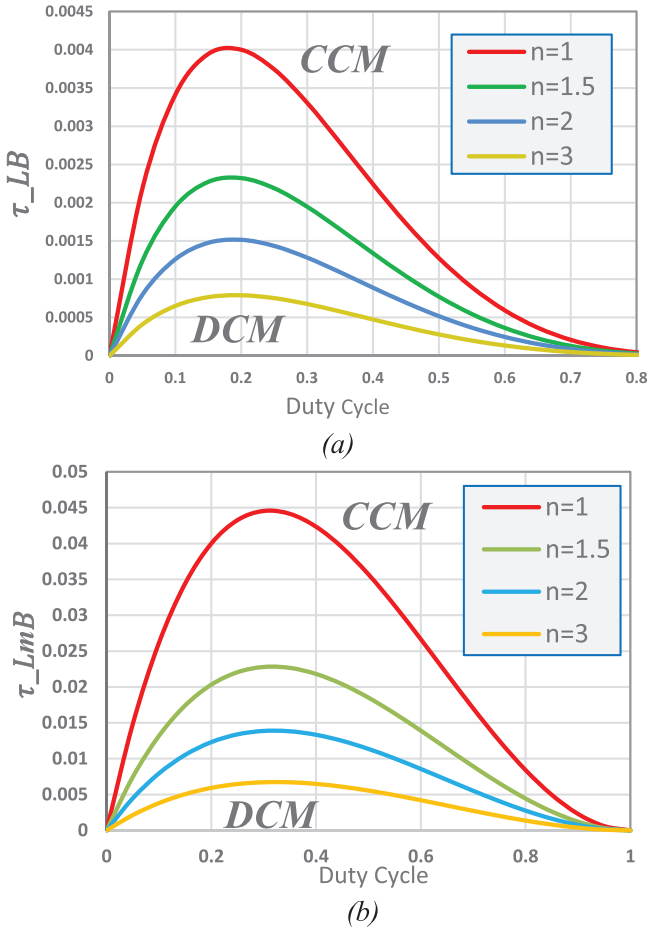


FIGURE 8 The normalised boundary time constant of the inductors (a) L, (b) L_m for different turns ratio

$$i_{co1} = -i_o - i_{Lk2} \tag{54}$$

$$i_{co2} = -i_o \tag{55}$$

Mode 3: Q_1 and Q_2 are off.

$$i_{c1} = i_L - i_{in} \tag{56}$$

$$i_{c2} = i_{in} - i_{Lk1} \tag{57}$$

$$i_{co1} = -i_o \tag{58}$$

$$i_{co2} = i_{Lk1} - i_o \tag{59}$$

By using ampere-second balance principle, for Equations (52) to (59), the average currents of inductance L and magnetising inductance L_m can be obtained:

$$I_{in} = I_L = \frac{2k(n+1)+(D-1)}{(1-D)^2} I_o \tag{60}$$

TABLE 1 Voltage stresses across power devices

Component	Voltage stress
Q_1	$\frac{1-D}{2k(n+1)+(D-1)} V_o$
Q_2	$\frac{2k+D-1}{2k(n+1)+(D-1)} V_o$
D_1	$\frac{1-D}{2k(n+1)+(D-1)} V_o$
D_2	$\frac{1-D}{2k(n+1)+(D-1)} V_o$
D_3	V_o
D_4	$\frac{2nk}{2k(n+1)+(D-1)} V_o$

$$I_{Lk1} = \frac{(2k(n+1)+(D-1)) \cdot D}{1-D} I_o \tag{61}$$

So, the average currents of the switches and diodes can be expressed as

$$I_{Q1} = \frac{2k(n+1)+(D-1)}{(1-D)^2} D.(2-D) I_o \tag{62}$$

$$I_{Q2} = \frac{2k(n+1)+(D-1)}{1-D} D^2 I_o \tag{63}$$

$$I_{D1} = I_{D2} = \frac{2k(n+1)+(D-1)}{1-D} D I_o \tag{64}$$

$$I_{D3} = I_{D4} = I_o \tag{65}$$

4 | ANALYSIS OF COMPONENTS VOLTAGE STRESS

According to the steady-state analysis in the previous sections, voltage stresses of power devices (MOSFETs and diodes) can be calculated as shown in Table 1. It can be seen that the voltage stress across the power switches (Q_1 and Q_2) is less than half of output voltage V_o, and also from Table 1 the lower voltage stresses can be obtained by the use of higher values of turns ration (n).

5 | DYNAMIC MODELLING

In this section, the average and the small-signal models are obtained while all components are analysed under ideal conditions. By using the state-space averaging method, the parameters and state variables discussed in this part are as follows:

The inductances are expressed as L, L_m, L_{k1}, and L_{k2} and R is resistive load. To simplify the analyses, all capacitors (C_1, C_2, C_{o1}, and C_{o2}) are set to C. $V_{in}(t)$, $V_o(t)$ and d are inputs, output, and control input variables, respectively. $i_L(t)$, $i_{Lm}(t)$, $i_{Lk1}(t)$, $i_{Lk2}(t)$, $V_{c1}(t)$, $V_{c2}(t)$, $V_{co1}(t)$ and $V_{co2}(t)$ are state variables.

By defining all variables, state-space average models are obtained in each switching state. The parameter k is defined as

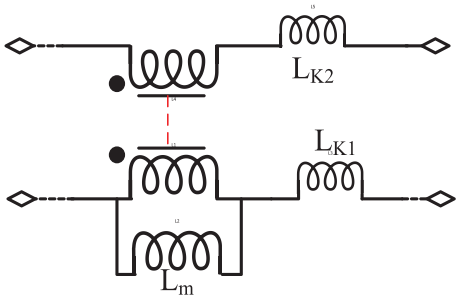


FIGURE 9 Equivalent circuit and three state variables related to the coupled inductor

the coupling coefficient ($K = L_m/(L_m + L_{k1})$), so it is necessary to consider L_{k1} as one of the state variables. According to the fact that coupled inductors are mostly used in forward and flyback applications, so the L_m and L_{k1} are not enough to describe the coupled inductor state-space average model. So, the current through secondary winding would be considered as another state variable. The state variables related to coupled inductors are shown in Figure 9.

The on-state period is (dT) when Q_1 and Q_2 are turned on simultaneously, so the state-space matrixes are defined as Equation (66):

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{di_{Lm}(t)}{dt} \\ \frac{di_{Lk1}k(t)}{dt} \\ \frac{di_{Lk2}(t)}{dt} \\ \frac{du_{c1}(t)}{dt} \\ \frac{du_{c2}(t)}{dt} \\ \frac{du_{co1}(t)}{dt} \\ \frac{du_{co2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{k}{L_m} & \frac{k}{L_m} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-k}{L_{k1}} & \frac{1-k}{L_{k1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_{k2}} & 0 \\ 0 & 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C} & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{k}{L_m} \\ \frac{1-k}{L_{k1}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t)$$

$$u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix} \quad (66)$$

The off-state period is $(1-d)T$ when Q_1 and Q_2 are turned off simultaneously, so the state-space matrixes are defined as Equation (67):

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{di_{Lm}(t)}{dt} \\ \frac{di_{Lk1}k(t)}{dt} \\ \frac{di_{Lk2}(t)}{dt} \\ \frac{du_{c1}(t)}{dt} \\ \frac{du_{c2}(t)}{dt} \\ \frac{du_{co1}(t)}{dt} \\ \frac{du_{co2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{-1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{k}{(n+1)L_m} & 0 & \frac{-k}{(n+1)L_m} \\ 0 & 0 & 0 & 0 & 0 & \frac{1-k}{(n+1)L_{k1}} & 0 & \frac{k-1}{(n+1)L_{k1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{(1+1/n)L_{k2}} & 0 & \frac{-1}{(1+1/n)L_{k2}} \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \\ 0 & 0 & \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{k}{L_m} \\ \frac{1-k}{L_{k1}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t)$$

$$u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix} \quad (67)$$

The combination of Equations (66) and (67) can obtain the average model of the converter as Equation (68) (see the Appendix).

Figure 10 shows the bode diagram of the proposed converter. Also, Figure 11 shows the bode diagram of the converter while it is closed loop.

According to Figure 12 closed-loop circuit is presented to achieve stable operation by designing the proportional, integral controller (PI controller).

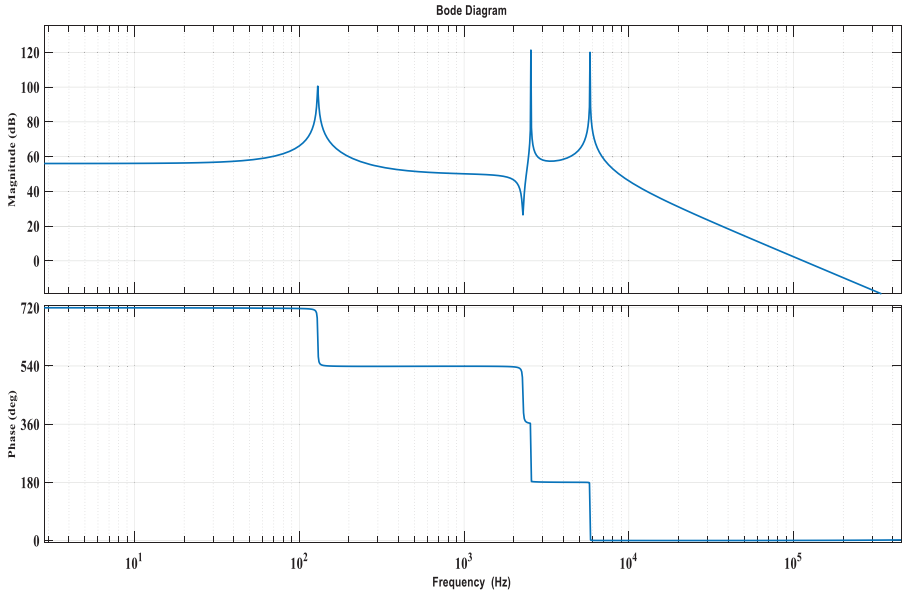


FIGURE 10 Bode diagram of the proposed open-loop converter

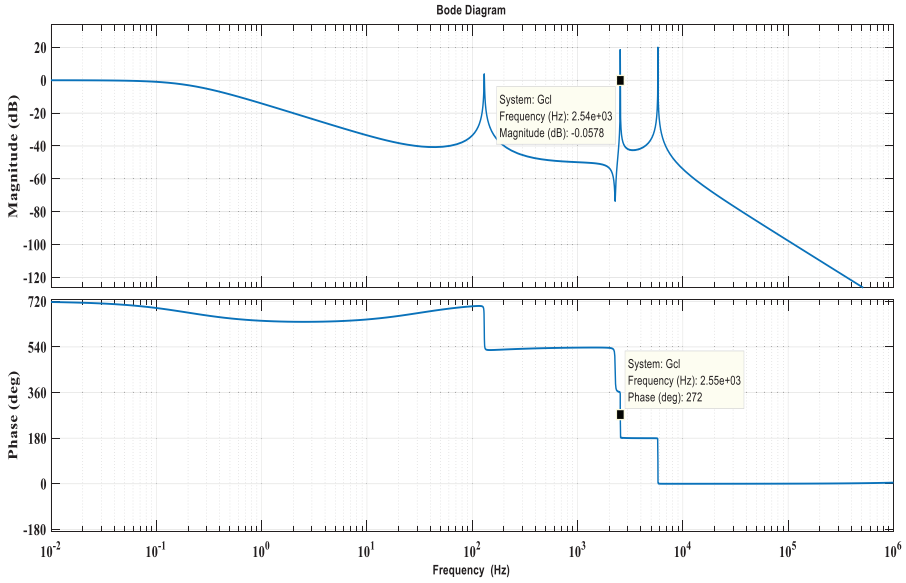


FIGURE 11 Bode diagram of the closed-loop proposed converter

The small-signal disturbance of all variables can be defined as Equation (69):

$$\begin{aligned}
i_L(t) &= I_L + \hat{i}_L(t)\\
i_{Lm}(t) &= I_{Lm} + \hat{i}_{Lm}(t)\\
i_{Lk1}(t) &= I_{Lk1} + \hat{i}_{Lk1}(t)\\
i_{Lk2}(t) &= I_{Lk2} + \hat{i}_{Lk2}(t)\\
u_{C1}(t) &= U_{C1} + \hat{u}_{C1}(t)\\
u_{C2}(t) &= U_{C2} + \hat{u}_{C2}(t)\\
u_{Co1}(t) &= U_{Co1} + \hat{u}_{Co1}(t)\\
u_{Co2}(t) &= U_{Co2} + \hat{u}_{Co2}(t)\\
u_{in}(t) &= U_{in} + \hat{u}_{in}(t)\\
u_o(t) &= U_o + \hat{u}_o(t)\\
d &= D + \hat{d}
\end{aligned} \tag{69}$$

where I_{L1}, I_{Lm}, I_{Lk1}, I_{Lk2}, U_{C1}, U_{C2}, U_{Co1}, U_{Co2}, D, U_{in} and U_o are steady-state variables.

Also $\hat{i}_L(t)$, $\hat{i}_{Lm}(t)$, $\hat{i}_{Lk1}(t)$, $\hat{i}_{Lk2}(t)$, $\hat{u}_{C1}(t)$, $\hat{u}_{C2}(t)$, $\hat{u}_{Co1}(t)$, $\hat{u}_{Co2}(t)$, $\hat{d}$, $\hat{u}_{in}(t)$ and $\hat{u}_o(t)$ are the small-signal disturbance variables. By using Equations (68) and (69), the small-signal model for the proposed converter can be expressed as Equation (70) (see the Appendix).

The transfer function $G_c(s)$ is supposed to be the PI controller. According to the dynamic of the proposed converter, proper values for PI controller is designed as follows:

$$G_c(s) = K_p + K_i\left(\frac{1}{s}\right) \xrightarrow{\textit{proper design}} \tag{71}$$

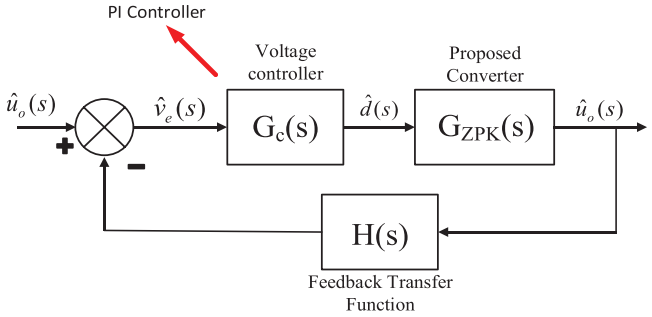


FIGURE 12 Diagram of proposed converter voltage control loop

$$K_p = 0.0004, K_i = 0.001$$

According to the bode diagram of closed loop, it can be seen that the phase margin is greater than zero (272 – 180 = 92 degrees) when the amplitude (gain) is zero. So this guarantees stable operation in the closed-loop circuit for the proposed converter.

6 | KEY PARAMETER DESIGN GUIDANCE

6.1 | Coupled inductor

In the proposed converter, the coupled inductor stores energy like a typical inductor, so it should be designed like a flyback transformer. According to Equations (47), (48) and (50), the minimum values for input inductance L and magnetising inductance L_m can be calculated. In order to operate in CCM mode, the values of input inductance and magnetising inductance must be greater than boundary inductances L_B and L_{mB}, respectively. Since the turns ratio of the coupled inductor (n) determines the voltage stresses of the switches and the operational duty cycle of the converter, it is the key parameter in the circuit parameter design. So, cut design steps of the coupled inductor are mentioned below:

1. A proper turns ratio can be obtained once the duty cycle is designed (typically lower than 0.7), which is given by

$$n = \frac{M_{CCM}\,(1-D)^2 + (1-D)}{2k} - 1 \tag{72}$$

Considering the requirements of the proposed converter, input and output voltages are 12 and 430 V, respectively, so ($M_{CCM} \approx 36$) and $D = 0.65$ are defined. Therefore, n is obtained by 1.5.

1. For $D = 0.65$, $n = 1.5$, $R = 800\ \Omega$ and $f = 20\ kHz$ and according to Equations (47), (48) and (50), the value of 120 μH for L and 400 μH for L_m would be sufficient to guarantee the CCM operation.

2. The initial determination of core size can be based on the area product (A_P) formula [26]. The maximum flux density B_{max} is determined based on saturation limited or allowable core loss. A conservative saturation limit is defined as 3000 Gauss (0.3 Tesla) for ferrite:

$$A_p = \left(\frac{LI_{SCpk}}{B_{max}} \cdot \frac{I_{FL}}{K}\right)^4 / 3cm^4 \tag{73}$$

where
L = inductance, Henrys
I_{SCpk} = max peak short circuit current, A
B_{max} = saturation limited flux density, T
I_{FL} = root mean square (RMS) current, full load (primary), A
K = primary copper area / window area.
Ferrite is used for core material due to its properties of high magnetic permeability coupled with low electrical conductivity with the maximum flux density of 0.25 T, which helps prevent eddy current.

1. By defining parameters related to A_P formula and simulation of the proposed converter, values are calculated as

$I_{SCpk} = 60$ A, $B_{max} = 0.25$ T, $I_{FL} = 0.7$ A and $K = 0.014$ (for forward converter), So A_P is almost equaled to $8cm^4$. Referring to the core catalog, $EE70$ ferrite core with area product of nine is chosen.

1. Since flux density is more likely to be limited by core saturation, B_{max}, corresponding maximum peak current of the primary side of coupled inductor L_m ($i_{Lm\,(peak)}$) and maximum peak current of inductor L ($i_{L(peak)}$) are used in Equations (74) and (75) to calculate the minimum number of primary turns capable of achieving the required inductance value and push core operation to its flux density limit. In the most step-up dc–dc converters, the coupling coefficient (k) needs to be more than 0.9 in order to have better energy transfer. The coupling coefficient in the proposed converter is set to 0.95. Therefore, L_k is defined as $L_k = (1 - k)L_m / k$ and calculated as $L_k = 20\ \mu$H [18].

The toroid (L) and $EE70$ (L_m) ferrite cores are selected for this purpose which primary and secondary turn numbers are calculated as follows:
For inductor L:

$$N_L = \frac{LI_{M(max)}}{B_{max}A_c}\ 1\ 0^4 = \frac{120\ ^{-}\text{H} \times 20\ \text{A}}{0.25\ \text{T} \times 2.18\ \text{cm}^2}\ 10^4 = \tag{74}$$

$$44.03 \rightarrow N_L = 44$$

For coupled inductor L_m:

$$N_p = \frac{L_m I_{M(max)}}{B_{max}A_c}\ 1\ 0^4 = \frac{400\ ^{-}\text{H} \times 9.8\ \text{A}}{0.25\ \text{T} \times 3.24\ \text{cm}^2}\ 10^4 = \tag{75}$$

TABLE 2 Performance comparison between the proposed converter and other topologies

Ref	Number of elements		Voltage gain ($n = N = 1.5$, $D = 0.65$)		Switch max. stress	Diode max. stress	The stored energy of coupled inductor per cycle
	Diode - cap – switch – coupled inductor – Inductor	Total	Formula	Value			LI^2 (mJ)
Proposed	4 – 4 – 2 – 1 – 1	12	$\frac{2n+D+1}{(1-D)^2}$	38	$\frac{(1+D)V_o}{2n+D+1}$	V_o	4.9
[5]	5 – 4 – 1 – 1 – 1	12	$\frac{1+n}{(1-D)^2}$	20.4	$\frac{V_o}{n+1}$	$\frac{nV_o}{n+1}$	0.76
[6]	5 – 4 – 1 – 1 – 1	12	$\frac{2+n}{(1-D)^2}$	28.6	$\frac{V_o}{n+2}$	$\frac{(n+1)V_o}{n+2}$	3.2
[8]	5 – 5 – 2 – 0 – 2	14	$\frac{3+D}{(1-D)^2}$	30	$\frac{(1+D)V_o}{3+D}$	$\frac{2V_o}{3+D}$	—
[11]	2 – 3 – 1 – 1 – 1	8	$\frac{1+(n+1)D}{1-D}$	7.5	$\frac{V_o}{1+(n+1)D}$	$\frac{V_o}{1+(n+1)D}$	0.46
[17]	6 – 5 – 2 – 2 – 0	15	$\frac{2(N+1)+n}{1-D}$	18.6	$\frac{V_o}{2(N+1)+n}$	$\frac{(2N+1+n)V_o}{2(N+1)+n}$	62.7
[21]	6 – 7 – 1 – 1 – 0	15	$\frac{3+2n+nD}{1-D}$	20	$\frac{V_o}{3+2n+nD}$	$\frac{(n+1)V_o}{3+2n+nD}$	6.4

$$48.39 \rightarrow N_p = 50$$

$$N_s = 1.5\ N_p = 1.5 \times 50 \rightarrow N_s = 75 \tag{76}$$

where $I_{M(max)}$ is the maximum current of inductance, B_{max} and A_c are the maximum flux density of ferrite and cross-sectional area of the magnetic core, respectively.

According to American wire gauge (AWG) table formula [27], conductor diameter of the primary and secondary windings of the coupled inductor are calculated as

$$D_x = \frac{2.54}{\pi} \times 10^{-AWG/20}\text{cm} \tag{77}$$

The RMS value of primary and secondary currents of coupled inductor windings are equal to 4.5 and 1.3 A, respectively. Using the AWG table, the value of AWG is obtained for primary and secondary windings as 17 and 23, respectively. Using Equation (77), conductor diameters are calculated as $D_x = 1.14$ mm for primary and $D_x = 0.57$ mm for secondary. To avoid the effect of eddy current due to high switching frequency (50 kHz), the diameter of primary and secondary windings are selected as $D_x = 2$ mm and $D_x = 1$ mm, which consists of four twisted wires by the diameter of 0.5 and 0.25 mm, respectively.

6.2 | Consideration of the capacitor design

By using the prominent equation of capacitor current, ($i_C = C\frac{dv_C}{dt}$), and output power, (P_{max}), the minimum value of capacitors is calculated which can tolerate the 2% voltage ripple for C_1, C_2, and C_{o1} and 0.1% voltage ripple for C_{o2}.

$$i_C = C\frac{\Delta v_c}{\Delta t} \rightarrow C = i_c\frac{\Delta t}{\Delta v_c} \rightarrow \tag{78}$$

$$i_c\frac{\Delta t}{r_v\%\ v_c};\ \Delta t = dT = d/f$$

$$C \geq \frac{DV_o}{Rf_s r_v\% v_C} \tag{79}$$

where $r_v\%$ is the percentage of voltage ripple related to capacitors. In addition to Equation (79), for designing C_{o2}, the value of C_{o2} should tolerate any changes of load R to provide suitable and regulated output dc voltage.

7 | COMPARISON

A comprehensive summary of the proposed converter and the recent studies are presented in Table 2, including voltage gain, number of elements, maximum voltage stress of diodes, and power switches. As shown in this table, considering the voltage gain, the number of elements of the proposed converter is equal to the converters presented in [5, 6] and lower than [11] and [21], however, the voltage conversion ratio of the proposed converter is higher than the other references. The comparisons of voltage gain versus the duty cycle are shown in Figure 13(a). It can be seen that the voltage gain of the proposed converter is higher than other topologies. In addition, the number of elements per voltage gain versus the duty cycle is shown in Figure 13(b), which demonstrates lower elements usage in the proposed converter. The maximum voltage stress of the power switches and diodes are shown in Table 2. In addition, Figures 13(c) and (d) compare the normalised voltage stresses of power switches and diodes, respectively. It can be concluded that the normalised maximum voltage stress of power switches in the proposed converter by the duty cycle around 0.65, is lower than that presented in [5, 8, 11]. Also, the normalised maximum voltage stress of diodes in the proposed converter is higher than all other topologies. Usually, the inductors and coupled inductors are the bulkiest components in the dc–dc converter's layouts. By increasing the output power of converters, the required

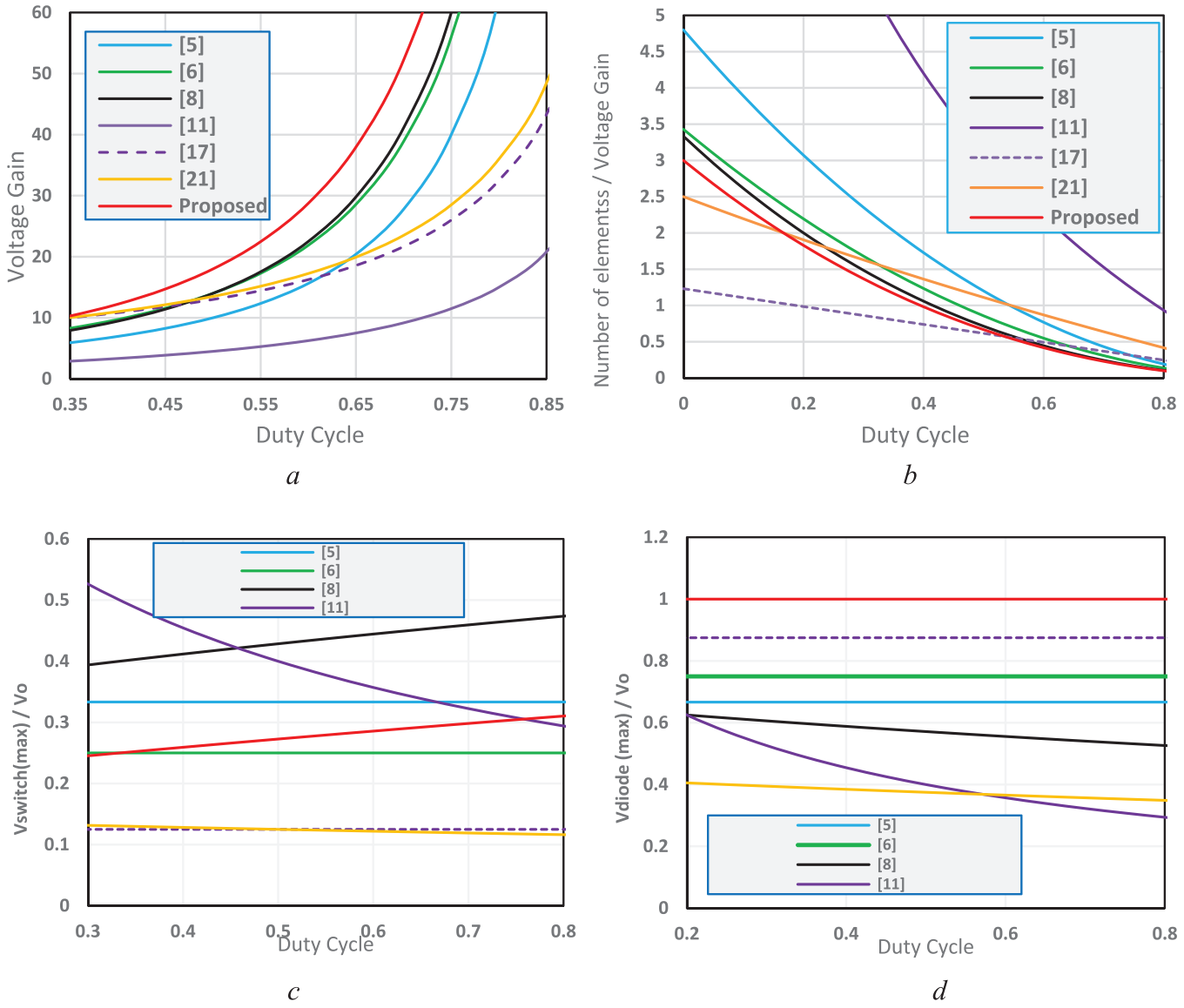


FIGURE 13 Comparison results of the proposed converter with other references. (a) Voltage gain versus duty cycle when $n = 1.5$ for all references. (b) The number of elements per CCM voltage gain versus duty cycle when $n = 1.5$ for all references. (c) Normalised maximum voltage stresses of power switches versus the duty cycle. (d) Normalised maximum voltage stresses of diodes versus duty cycle

energy transferred by the coupled inductor will increase and this one will lead to larger inductor size (inductor size will be increased by required energy transferred by the inductors) and larger size of the converter. The area product of ferrite cores (size) will increase by energy transferred by the inductors. (Ap will increase by LI^2, see Keith Billings' [28] handbook that consists of several sections such as power converters, switch mode power supply design, flyback and forward-transformer design, and inductor design.)

The stored energy of coupled inductors is compared for each reference on the last column of Table 2 which is the main factor for the size of the coupled inductor. In this column, L indicates the magnetic inductance and I is the average current that flows from inductor L.

8 | EXPERIMENTAL VALIDATION

A prototype of a 230 W dc–dc boost converter is developed and implemented to verify the performance of the proposed converter, which is implemented and shown in Figure 14. The dc input voltage varies from 12 to 24 V and the output voltage is regulated to be 391 V. Table 3 shows the complete information about the components used in this prototype.

As mentioned in Table 3, the ATmega8A microcontroller is utilised for pulsating power switches. Also, IRFP260N, SFAF2004G, and MUR840 are selected for power switches, diodes D_1, D_2, and diodes D_3, D_4, respectively. Figure 15 depicts the input and output voltages and currents of the proposed converter plus gate pulses of power switches. As shown

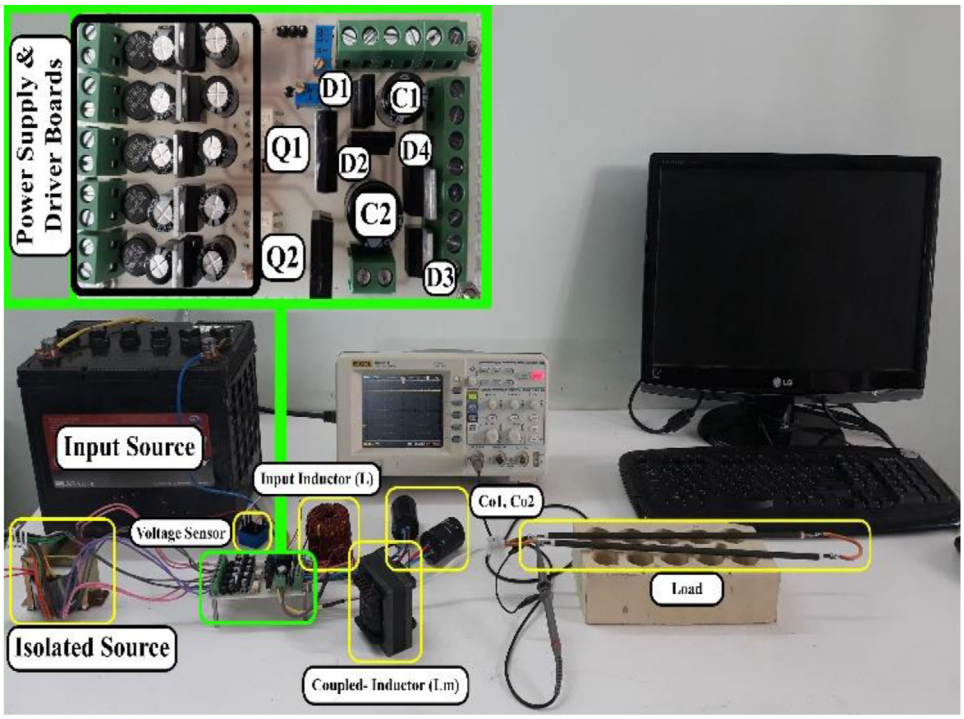
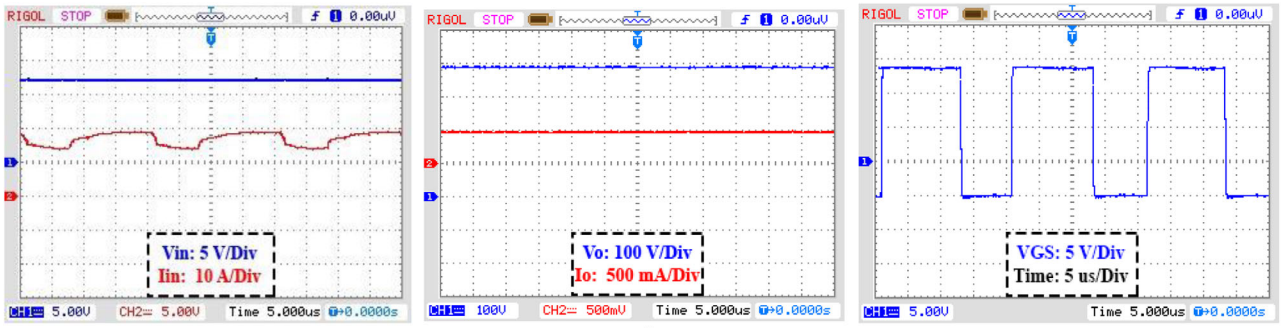


FIGURE 14 Experimental prototype of the proposed converter



a *b* *c*

FIGURE 15 Experimental input and output voltages and currents of the proposed converter. (a) Measured input voltage and current, (b) measured output voltage and current, (c) experimental gate pulses for power switches

in Figure 15(a), the measured input current ripple is 23.5% in practice. By adding the 15 μH inductance in series with input voltage source the current ripple will reduce to 11.4% and the current ripple calculated theoretically would be 10%. The voltage gain is 32.5 (= 391/12). This gain is slightly less than the theoretical value of 36 that can be obtained from Equation (18). This is due to the fact that the parasitic elements are ignored in theoretical analysis. The continuous behaviour of input current is obvious in this figure, which leads the input source to become more durable.

The drain-source voltages and currents across power switches are shown in Figure 16. The maximum voltage of switches is less than 140 V, which comply with the theoretical analysis and is much less than the output voltage.

Experimental results of diode voltage and current are shown in Figure 17, which demonstrates that voltages of D_1 and D_2 are the same, and their voltage stresses are 30 V which is typically low. Also, the voltage stress across diodes D_3 and D_4 are 390 and 251 V, respectively. Figure 18 shows experimental inductor currents including current of inductor L and L_{k1}. The average current value of inductor L and input currents are the same (17 A) that is in accordance with the calculation from Equation (60).

The experimental voltages waveforms of capacitors are shown in Figure 19. It is clear that voltage across capacitors C_1, C_2, C_{o1}, and C_{o2} are around 20, 30, 85, and 305 V, respectively, which are in accordance with the calculations from Equations (11), (12), (15) and (16). In order to evaluate the

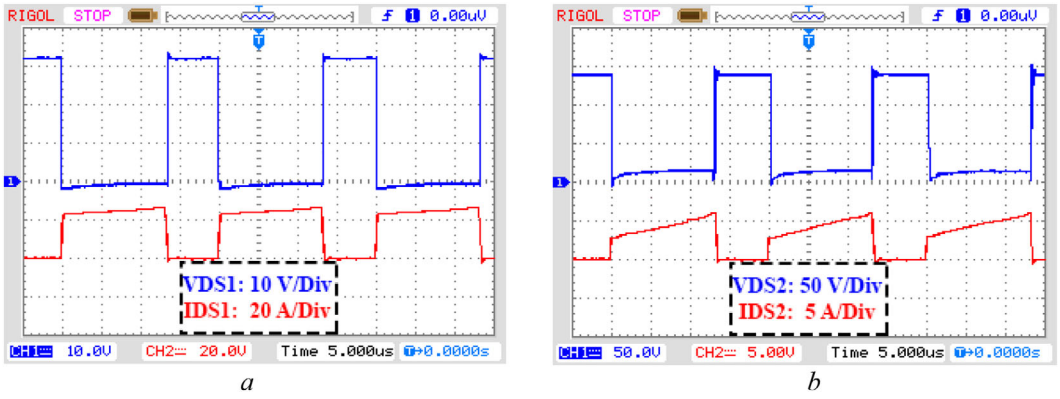


FIGURE 16 Experimental power switch voltages and currents of the proposed converter. (a) Measured voltage and current of power switch Q_1, (b) measured voltage and current of power switch Q_2

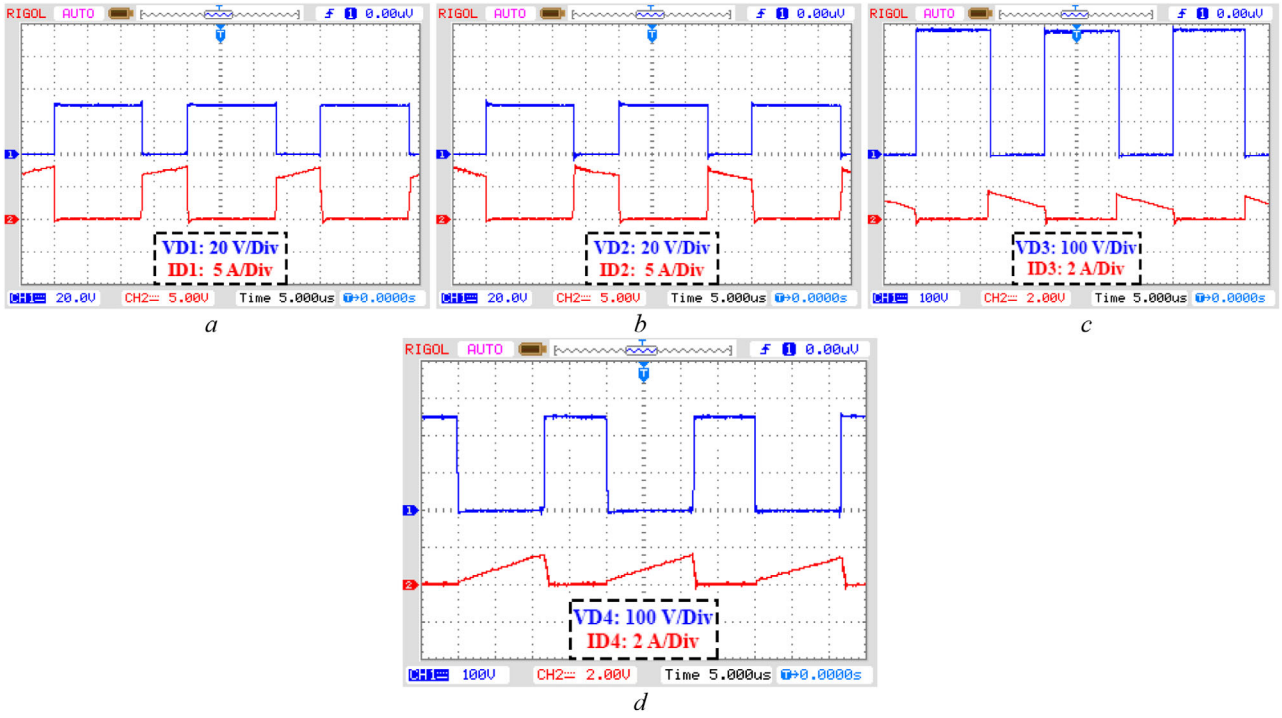


FIGURE 17 Experimental diode voltages and currents of the proposed converter. (a) Measured voltage and current of diode D_1, (b) measured voltage and current of diode D_2, (*c*) measured voltage and current of diode D_3, (d) measured voltage and current of diode D_4

dynamic response of the proposed converter, Figure 20 illustrates the output voltage within the load and input voltage variation. It can be concluded that the proposed converter performs a perfect load regulation and fast dynamic response. Figure 20(b) shows the experimental result of the dynamic response under input voltage variation from the dc voltage of 12 to 24 V. The fast dynamic response of the output voltage is obvious.

Theoretical values along with simulation and experimental results are provided in Table 4 to have a better comparison. Through this table, it is clear that theoretical values are higher than simulation and experimental ones; this is because of inaccurate modelling and ignoring parasitic effects of elements.

9 | LOSSES AND EFFICIENCY

The losses in this converter can be divided into coupled-inductor [29], switch, diode, and capacitor losses [30].

1. Switch losses (L_1 and L_2):

   Conduction losses (P_c).

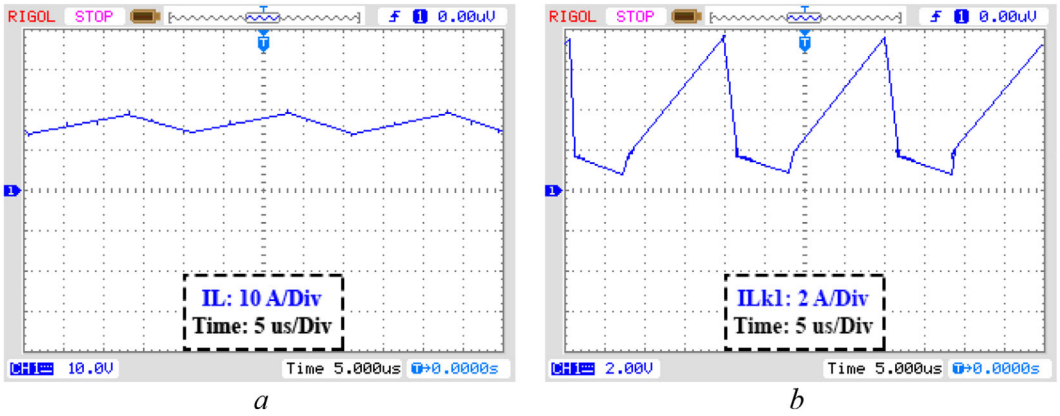


FIGURE 18 Experimental inductor currents of the proposed converter. (a) The measured current of inductor L, (b) the measured current of primary leakage of coupled inductor L_{k1}

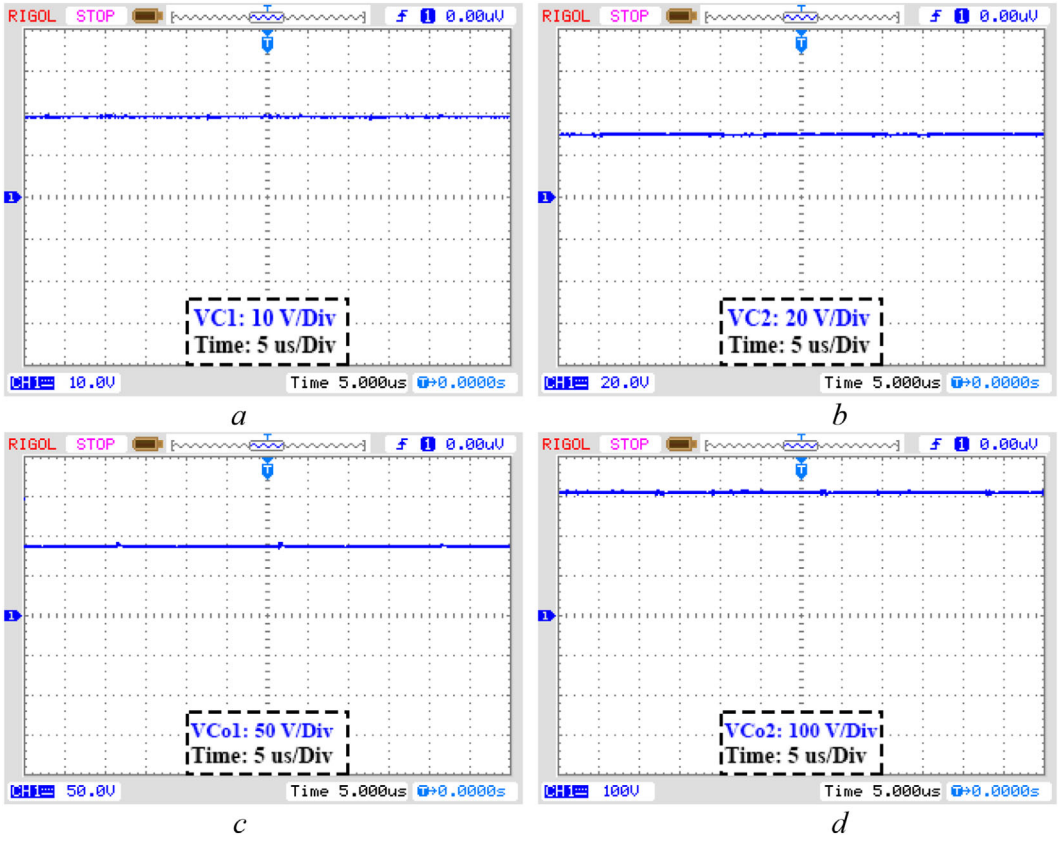


FIGURE 19 Experimental capacitors voltages of the proposed converter. (a) The measured voltage of the capacitor C_1, (*b*) the measured voltage of the capacitor C_2, (c) the measured voltage of the capacitor C_{o1}, *(d)* the measured voltage of the capacitor C_{o2}

Switching losses (P_s).

$$\begin{aligned} &L_1\,(Q_1 losses) = P_{C1} + P_{S1} \\ &L_1 = \left(I^2_{Q1\,(rms)} \times R_{DS(on)}\right) \\ &+ \left(\begin{aligned} &\frac{1}{2} \times V_{DS} \times I_{Q1(Low)} \\ &\times T_r \times f_s + \frac{1}{2} \times V_{DS} \times I_{Q1(Peak)} \times T_f \times f_s \end{aligned}\right) \end{aligned} \tag{80}$$

$$\begin{aligned} &L_2\,(Q_2 losses) = P_{C2} + P_{S2} \\ &L_2 = \left(I^2_{Q2\,(rms)} \times R_{DS(on)}\right) \\ &+ \left(\begin{aligned} &\frac{1}{2} \times V_{DS} \times I_{Q2(Low)} \\ &\times T_r \times f_s + \frac{1}{2} \times V_{DS} \times I_{Q2(Peak)} \times T_f \times f_s \end{aligned}\right) \end{aligned} \tag{81}$$

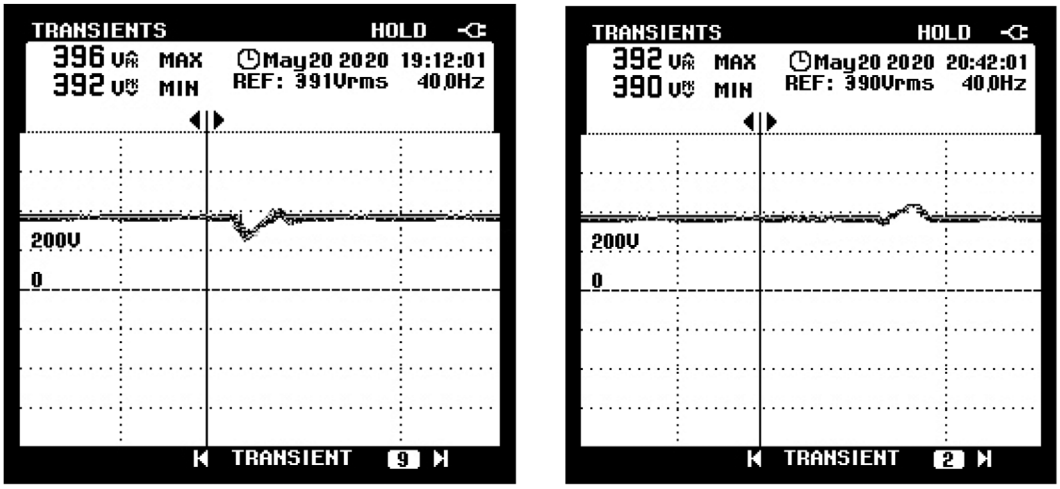


FIGURE 20 Dynamic response of the proposed converter. (a) Under step load variation from half load (191W) to full load (382W), (b) under step input voltage variation from dc voltage of 12 to 24 V

TABLE 3 Experimental parameters

Components	Parameters
Input voltage (V_{in})	12–24 V
Output voltage (V_o)	390 V
Power (rated)	230 W
Switching frequency (f)	50 kHz
Power switches (Q_1, Q_2)	IRFP260N
Diodes (D_1–D_2)	SFAF2004G
Diodes (D_3–D_4)	MUR840
Capacitor (C_1–C_2)	680 μF
Capacitor (C_{o1})	120 μF
Capacitor (C_{o2})	470 μF
Inductor (L)	120 μH (Toroid)
The coupled inductor (Lm)	400 μH (EE70)
Leakage inductance (L_{k1}–L_{k2})	20 μH
The primary winding (N_p)	50
Secondary winding (N_s)	75
R (load)	800 Ω
Duty cycle (D)	0.65
Microcontroller	At mega 8A

where T_r and T_f represent turn-on time (rise time) and turn-off time (falling time) of power switches, respectively, and $R_{DS(on)}$ is the on-state resistance of switches that is 0.027Ω and I_Q represents the RMS value of the current passing through the switch.

1. Diode conduction losses (L_3)

Diode forward-voltage losses (P_{df}).

Diode conduction losses (P_{dc}).

$$\begin{aligned} L_3 &= P_{df} + P_{dc} \\ L_3 &= \left(I_{D1(ave)} + I_{D2(ave)} + I_{D3(ave)} + I_{D4(ave)}\right) \times V_F + \\ &\left(I^2_{D1(rms)} + I^2_{D2(rms)} + I^2_{D3(rms)} + I^2_{D4(rms)}\right) \times r_F \end{aligned} \quad (82)$$

where V_F and r_F represent the forward-voltage drop and forward resistance of diodes, respectively.

1. Coupled inductor losses (L_4)

Copper losses (P_{cu})
Core losses (P_{fe})

$$\begin{aligned} L_4 &= P_{cu} + P_{fe} \\ P_{cu} &= R_L \times I^2_{Lp(rms)} + R_L \times I^2_{Ls(rms)} \\ P_{fe} &= 0.074 \times B^{2.85} \times f^{1.43} \times l_m \times A_c \end{aligned} \quad (83)$$

where R_L represents coupled-inductor winding resistance and B is the magnetic flux density, f, l_m and A_c represent frequency, magnetic path length, and cross-sectional area of the magnetic core, respectively.

1. Capacitor losses (L_5)

$$\begin{aligned} L_5 &= R_{C1} \times I^2_{C1(rms)} + R_{C2} \times I^2_{C2(rms)} + R_{Co1} \\ &\times I^2_{Co1(rms)} + R_{Co2} \times I^2_{Co2(rms)} \end{aligned} \quad (84)$$

The load current under the output voltage of 391 V is about 0.5 A. So, the efficiency can be calculated as

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{V_o \times I_o}{V_o \times I_o + P_{loss}} \quad (85)$$

TABLE 4 Theoretical, simulation, and experimental average values and stresses of the proposed converter

Parameter		Theoretical value		Simulation value		Experimental value	
Voltage gain		36		33.3		32.5	
V_{c1}		22.3 V		20 V		19 V	
V_{c2}		34.3 V		32 V		31 V	
V_{co1}		103 V		87 V		85 V	
V_{co2}		328 V		313 V		306 V	
V_{D1}	I_{D1}	22.3 V	4 A	21 V	3.5 A	19.5 V	3.3 A
V_{D2}	I_{D2}	22.3 V	4 A	21 V	3.5 A	19.5 V	3.3 A
V_{D3}	I_{D3}	270 V	0.53 A	260 V	0.51 A	254 V	0.49 A
V_{D4}	I_{D4}	96 V	0.53 A	91 V	0.51 A	88 V	0.49 A
V_{Q1}	I_{Q1}	12 V	16.7 A	11.5 V	15 A	11 V	14 A
V_{Q2}	I_{Q2}	53 V	4.33 A	50 V	3 A	44 V	2.7 A
$I_{D1\ (peak)} = I_{D2\ (peak)}$		11 A		10.5 A		8 A	
$I_{D3\ (peak)} = I_{D4\ (peak)}$		2.5 A		2 A		1.8 A	
$V_{D1\ (peak)} = V_{D2\ (peak)}$		34.3 V		31 V		30 V	
$V_{D3\ (peak)}$	$V_{D4\ (peak)}$	431 V	279 V	400 V	260 V	390 V	251 V
$I_{Q1\ (peak)}$	$I_{Q2\ (peak)}$	27 A	7 A	26.2 A	6.4 A	25 A	6 A
$V_{Q1\ (peak)}$	$V_{Q2\ (peak)}$	34.2 V	152 V	33 V	145 V	32 V	140 V

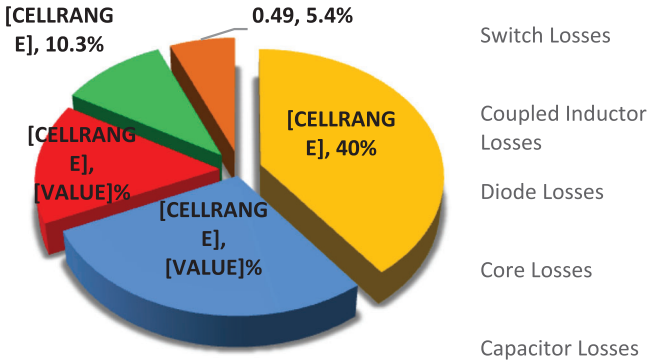


FIGURE 21 Component power losses at 230 W

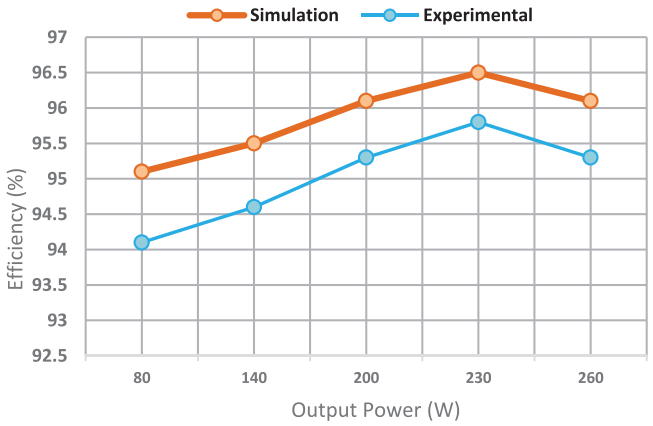


FIGURE 22 Practical and simulated efficiency of the proposed converter under different output powers

$$= \frac{391 \times 0.5}{391 \times 0.5 + 8.5} \times 100 \cong 95.8\%$$

Figure 21 shows the total losses of the proposed converter and its components share on the total losses. Switches and coupled-inductor losses are the major sources for converter total losses. By the use of Equation (85), the efficiency is calculated for different output powers and can be depicted as an efficiency diagram in Figure 22. It is clear that the experimental efficiency is less than the theoretical one. In both cases, the maximum efficiency has occurred at approximately 60% of rated power in 230 W.

10 | CONCLUSION

A coupled inductor-based boost converter is presented in this study, which has the following merits:

1. A high voltage gain, by medium-duty cycle, and the lower turns ratio of the coupled inductor, also lower number counts of components
2. In practice, there are some voltage spikes across the components like power switches and diodes due to leakage inductance of the coupled inductor. Utilising D_3 and D_4 reduce these spikes to an acceptable level.

3. Due to the reduced voltage stress across the power switches, which is lower than the output voltage, low on-state resistance power switches were implemented.

Complete comparison verifies that the proposed topology has high voltage gain, lower component number per voltage gain, and lower voltage stress on switching devices. CCM and DCM operations were thoroughly discussed. Experimental results showed that average conversion efficiency was higher than almost 94%, which makes it suitable for the low-voltage renewable energy resources (maximum efficiency was measured to be 95.8%). Theoretical analysis and dynamic response of the proposed converter from light load to heavy load were provided too. The experimental result of step variation of input voltage from 12 to 24V was presented and the well-regulated output voltage was obtained.

ORCID

Mohammad Ghaffarpour https://orcid.org/0000-0001-9095-135X
Reza Ebrahimi https://orcid.org/0000-0001-9094-8003

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APPENDIX

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{di_{Lm}(t)}{dt} \\ \frac{di_{Lk1}k(t)}{dt} \\ \frac{di_{Lk2}(t)}{dt} \\ \frac{du_{c1}(t)}{dt} \\ \frac{du_{c2}(t)}{dt} \\ \frac{du_{co1}(t)}{dt} \\ \frac{du_{co2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{d-1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{kd}{L_m} & \frac{k(nd+1)}{(n+1)L_m} & 0 & \frac{k(d-1)}{(n+1)L_m} \\ 0 & 0 & 0 & 0 & \frac{-d(k-1)}{L_{k1}} & \frac{-(nd+1)(1-k)}{(n+1)L_{k1}} & 0 & \frac{-(k-1)(d-1)}{(n+1)L_{k1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-n(d-1)}{(n+1)L_{k2}} & \frac{d}{L_{k2}} & \frac{n(d-1)}{(n+1)L_{k2}} \\ \frac{1-d}{2C} & 0 & \frac{-(d+1)}{2C} & 0 & 0 & 0 & 0 & 0 \\ \frac{1-d}{2C} & 0 & \frac{-(1+d)}{2C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-d}{C} & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \\ 0 & 0 & \frac{1-d}{C} & 0 & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L} \\ \frac{k}{L_m} \\ \frac{1-k}{L_{k1}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t) \quad u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ i_{Lm} \\ i_{Lk1} \\ i_{Lk2} \\ u_{c1} \\ u_{c2} \\ u_{co1} \\ u_{co2} \end{bmatrix} \tag{A.1}$$

$$
\begin{bmatrix} \frac{d\hat{i}_L(t)}{dt} \\ \frac{d\hat{i}_{Lm}(t)}{dt} \\ \frac{d\hat{i}_{Lk1}k(t)}{dt} \\ \frac{d\hat{i}_{Lk2}(t)}{dt} \\ \frac{d\hat{u}_{c1}(t)}{dt} \\ \frac{d\hat{u}_{c2}(t)}{dt} \\ \frac{d\hat{u}_{co1}(t)}{dt} \\ \frac{d\hat{u}_{co2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{d-1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{kd}{L_m} & \frac{k(nd+1)}{(n+1)L_m} & 0 & \frac{k(d-1)}{(n+1)L_m} \\ 0 & 0 & 0 & 0 & \frac{-d(k-1)}{L_{k1}} & \frac{-(nd+1)(1-k)}{(n+1)L_{k1}} & 0 & \frac{-(k-1)(d-1)}{(n+1)L_{k1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-n(d-1)}{(n+1)L_{k2}} & \frac{d}{L_{k2}} & \frac{n(d-1)}{(n+1)L_{k2}} \\ \frac{1-d}{2C} & 0 & \frac{-(1+d)}{2C} & 0 & 0 & 0 & 0 & 0 \\ \frac{1-d}{2C} & 0 & \frac{-(1+d)}{2C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-d}{C} & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \\ 0 & 0 & \frac{1-d}{C} & 0 & 0 & 0 & \frac{-1}{RC} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{i}_{Lm}(t) \\ \hat{i}_{Lk1}(t) \\ \hat{i}_{Lk2}(t) \\ \hat{u}_{c1}(t) \\ \hat{u}_{c2}(t) \\ \hat{u}_{co1}(t) \\ \hat{u}_{co2}(t) \end{bmatrix}
$$

$$
+ \begin{bmatrix} \frac{1}{L} \\ \frac{k}{L_m} \\ \frac{1-k}{L_{k1}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{in}(t) + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{k}{L_m} & \frac{kn}{(n+1)L_m} & 0 & \frac{k}{(n+1)L_m} \\ 0 & 0 & 0 & 0 & \frac{(1-k)}{L_{k1}} & \frac{n(1-k)}{(n+1)L_{k1}} & 0 & \frac{-(k-1)}{(n+1)L_{k1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{-n}{(n+1)L_{k2}} & \frac{1}{L_{k2}} & \frac{n}{(n+1)L_{k2}} \\ \frac{-1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 & 0 & 0 & 0 \\ \frac{-1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_L \\ I_{Lm} \\ I_{Lk1} \\ I_{Lk2} \\ U_{c1} \\ U_{c2} \\ U_{co1} \\ U_{co2} \end{bmatrix} \hat{d}
$$

$$
u_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ I_{Lm} \\ I_{Lk1} \\ I_{Lk2} \\ U_{c1} \\ U_{c2} \\ U_{co1} \\ U_{co2} \end{bmatrix}
$$

(A.2)