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ORIGINAL RESEARCH PAPER

Model-based control of four-leg inverter for UPS applications considering the effect of neutral line inductor

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Abstract

A control approach for three-phase four-leg LC-filtered voltage source inverters (VSIs) is proposed for an uninterruptible power supply (UPS) application. A filter inductor in the fourth (neutral) leg of the VSI is considered to enhance the output voltage quality when feeding different types of loads in such a system. The proposed approach is based on the modelling of UPS VSI system in the $dq0$ synchronous frame. First, the switching functions of the inverter under study are extracted from the achieved system model. Afterward, the control approach is developed by introducing a virtual time constant, which simultaneously affects the system's damping ratio, and a virtual undamped natural frequency in the switching functions. It offers flexibility for improving the system dynamic and steady-state responses as desired. While the final time constant decreases the transient response time and overshoot, the resulting undamped natural frequency leads to alleviation of steady-state error in the output voltage. The performance of the proposed control approach is evaluated via SIMULINK-based and real-time simulation results.

1 | INTRODUCTION

Uninterruptible power supply (UPS) inverters provide clean and uninterruptible power for critical loads like computers, medical equipment, and communication systems in case of low quality or failure in the power grid [1–6]. The output voltage of the UPS inverter should be sinusoidal and balanced with low total harmonic distortion (THD) irrespective of the loads connected to the UPS inverter system. In addition, appropriate tracking performance (preferably zero steady-state error in the output voltage), guaranteed stability, and quick dynamic response are the other features of a properly controlled UPS system. Many control schemes have been introduced so far for UPS inverter systems to obtain the demands, as mentioned above. In [7–9], repetitive controllers have been addressed to mitigate the harmonic components of the output voltage caused by non-linear loads, with its capability in removing periodic disturbance. But, slow dynamics, unsuccessful operation under non-periodic disturbances and poor tracking precision are the key drawbacks of this method. An internal model-based disturbance observer has been proposed in [10] and applied to a UPS inverter in order to improve the performance of the conventional repetitive

control. However, the achieved results by this scheme are not satisfactory. The deadbeat control technique provides a quick transient response [11–13]. An advantage is that even with its quick response, if properly designed, it avoids overshoots under transient operating conditions. In spite of the benefits it offers, this approach suffers from several problems such as sensitivity to the system parameters and load conditions, implementation complexity, and the steady-state error in the output voltage. In [14–17], the sliding-mode control (SMC) has shown quick dynamic response and robustness against model mismatches. Usually, this controller has a well-known chattering disadvantage. In addition to this, the controller suffers from the variable switching frequency. Many attempts have been carried out to reduce the chattering matter recently. For instance, in [18], a three-level hysteresis function in combination with SMC has been reported. Nevertheless, the time-varying switching frequency yet exists as a significant problem of this strategy. The SMC method presented in [19] has employed a fixed switching frequency at the expense of output voltage tracking error and weak robustness against model parameter variations. Also, the chattering problem still exists in this method. The model predictive control (MPC) approach has been lately applied for

controlling UPS inverters because of its benefit in obtaining a quick transient response [20–24]. Although many kinds of research on the MPC method were addressed for inverter applications as reviewed by [25], there are two emerging subjects regarding the MPC ones in the field of power electronic converters in company with an output filter. The first subject, which is related to robustness, is a common concern of a model-based approach consisting of the MPC owing to their weighty dependence on existing models of the plants [26]. Despite the obtainability of models in power converters, the precision of mathematical models is generally not ensured because of the system parameter uncertainties. Moreover, the model precision can be adversely affected via unmodelled parameters and noises [27]. Since the MPC method is highly dependent on the system model to predict the future behaviour, it cannot provide good performance when affected by noise. The other critical problem with MPC is the necessity for employing several sensors to predict the system behaviour, leading to costly implementation. A novel 3D space-vector diagram duty cycle control combined with MPC method has been suggested in [28] for four-leg UPS inverters. Although the suggested technique has provided a suitable operation, the aforementioned problems related to MPC method can still be observed in this work. The H_∞ control technique presented in [29] has provided a proper transient response as well as satisfactory THD. However, the complexity of implementation is its main weakness. Various multiloop control methods have been applied to UPS inverters [30–32], which have all gained limitations at fundamental frequency leading to high steady-state errors. A discrete-time voltage control on the basis of the system state-space model in the z-domain model has been suggested in [33], where the modelling of calculation and modulation delay can be exactly accomplished. However, the results do not exhibit the desired performance. In [34], the performance of discrete proportional-integral (PI) and proportional-resonant (PR) controls for UPS inverters has been examined and compared. With regard to the presented results, the THDs attained for both methods are high. A synchronous reference frame PI controller combined with PR control has been described in [35] in order to regulate the output voltage of the UPS inverter along with zero steady-state error. The chief drawback of this scheme is too many gains to be set. A selective frequency active damping scheme by means of the filter inductor current feedback has been addressed in [36]. However, the study on the impact of parameter variations which can impressively threaten the controller operation was overlooked. An output voltage tracking control via internal model principle (IMP) for UPS inverters has been reported in [37]. In the considered approach, the controller parameters were determined for the sake of guaranteeing the system's global stability. However, the operation of the reported controller against parameters mismatches and also when facing transient conditions is not satisfactory.

In this study, a control approach based on system modelling in the $dq0$ synchronous frame is presented for three-phase four-leg UPS inverters. The proposed control approach offers an
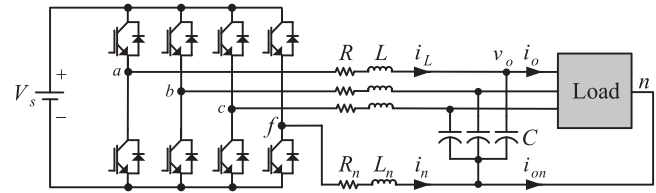

FIGURE 1 The layout of the three-phase four-leg UPS VSI with an output LC filter

opportunity to adjust the system dynamics as desired and also almost remove the steady-state errors by changing the system's basic characteristics without sacrificing the global stability of the closed-loop system. The proposed controller is based on solving the switching functions which are achieved through the $dq0$ synchronous frame mathematical model of the UPS inverter. The switching functions are determined in d- and q- and 0-axes. For each of the switching functions, inverter reference current generation is necessary. To this purpose, these currents are also taken out of the system model. A virtual time constant affecting the damping ratio is introduced into the proposed control approach to make the dynamic response of the UPS inverter currents quicker and to decrease the overshoot. Moreover, a virtual undamped natural frequency is also introduced to relieve the steady-state error in the output voltage. The performance of the proposed approach and its superiority over the SMC method reported in [19] are investigated by the real-time simulation results. Furthermore, the system operation, together with uncertainty on model parameters, is tested to show the high performance of the proposed control approach.

2 | SYSTEM DESCRIPTION

The layout of a three-phase four-leg UPS voltage source inverter (VSI) with an LC filter is depicted in Figure 1. Each phase of the inverter is connected to the system load by an LC low-pass filter, which is embedded at the output of the UPS VSI. To provide a path for the load current zero-sequence component, the fourth leg of UPS VSI is integrated to the neutral point of load. Consequently, the four-leg VSI can support highly unbalanced loads and reveal an outstanding operation under non-linear loads. For the sake of lessening the switching current ripple and enhancing the output voltage quality, the fourth leg of the UPS VSI should be equipped via an inductor similar to other legs. Besides, the considered inductor not only decreases the current rating of the fourth leg switches but also constrains the fault current in the case of short circuit occurrence. Thus, it is concluded that the application of a filter inductor in the output of the fourth leg is extremely preferable to its removal.

To reach a control design for the four-leg UPS VSI with an inductive filter at the output of the fourth leg, the system model should be obtained first. Applying the Kirchhoff's laws to the

considered system gives

$$
\begin{bmatrix} v_{af} \\ v_{bf} \\ v_{cf} \end{bmatrix} + R_n \begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} + L_n \frac{d}{dt} \begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} = \begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix}
$$

$$
+ R \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{1}
$$

$$
i_{La} + i_{Lb} + i_{Lc} + i_n = 0 \tag{2}
$$

By eliminating i_n from Equation (1) and after some simplification, the following relation can be expressed

$$
\begin{bmatrix} L + L_n & L_n & L_n \\ L_n & L + L_n & L_n \\ L_n & L_n & L + L_n \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \frac{1}{2} V_s \begin{bmatrix} u_{af} \\ u_{bf} \\ u_{cf} \end{bmatrix} - \begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix}
$$

$$
- \begin{bmatrix} R + R_n & R_n & R_n \\ R_n & R + R_n & R_n \\ R_n & R_n & R + R_n \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3}
$$

where u_{af}, u_{bf} and u_{cf} are the switching functions. Also, we have

$$
C \frac{d}{dt} \begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \tag{4}
$$

The system equations can be transformed into the $dq0$ reference frame as follows

$$
\begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L + 3L_n \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{1}{2} V_s \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix}
$$

$$
- \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R + 3R_n \end{bmatrix} \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} - \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} \tag{5}
$$

$$
- \begin{bmatrix} 0 & -L\omega & 0 \\ L\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix}
$$

where ω is the angular frequency of the system, and

$$
C \frac{d}{dt} \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} = \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} - \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix} - \begin{bmatrix} 0 & -C\omega & 0 \\ C\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix} \tag{6}
$$

Equations (5) and (6) form the final model of the UPS VSI along with a fourth leg inductor in the $dq0$ synchronous reference frame to describe the behaviour of the considered system.

3 | MODEL-BASED CONTROL APPROACH

Let us rewrite the system equations as follows

$$
\mathbf{L} \frac{d\mathbf{i_L}}{dt} = \frac{1}{2} V_s \mathbf{u} - \mathbf{R}\mathbf{i_L} - \mathbf{v_o} - L\boldsymbol{\omega}_{\mathbf{coup}} \mathbf{i_L} \tag{7}
$$

$$
C \frac{d\mathbf{v_o}}{dt} = \mathbf{i_L} - \mathbf{i_o} - C\boldsymbol{\omega}_{\mathbf{coup}} \mathbf{v_o} \tag{8}
$$

where

$$
\mathbf{L} = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L + 3L_n \end{bmatrix}, \quad \mathbf{R} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R + 3R_n \end{bmatrix},
$$

$$
\boldsymbol{\omega}_{\mathbf{coup}} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}
$$

$$
\mathbf{u} = \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix}, \mathbf{i_L} = \begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix}, \mathbf{i_o} = \begin{bmatrix} i_{od} \\ i_{oq} \\ i_{o0} \end{bmatrix}, \mathbf{v_o} = \begin{bmatrix} v_{od} \\ v_{oq} \\ v_{o0} \end{bmatrix}
$$

The switching functions (control variables) of the three-phase four-leg UPS VSI can be derived from the $dq0$ synchronous frame model via the solution of Equation (7) in the following form

$$
\mathbf{u} = \frac{2}{V_s} \left(\mathbf{R}\mathbf{i_L^*} + \mathbf{L} \frac{d\mathbf{i_L^*}}{dt} + \mathbf{v_o^*} + L\boldsymbol{\omega}_{\mathbf{coup}} \mathbf{i_L} \right) \tag{9}
$$

where $\mathbf{i_L^*}$ denotes the reference component of the three-phase four-leg UPS VSI current, and $\mathbf{v_o^*}$ denotes the reference component of the output voltage in the synchronous reference frame. It should be noted that the actual value of the term $L\boldsymbol{\omega}_{\mathbf{coup}} \mathbf{i_L}$ is employed in the control variables.

According to Equation (8), the UPS VSI reference current can be obtained as follows

$$
\mathbf{i_L^*} = C \frac{d\mathbf{v_o^*}}{dt} + \mathbf{i_o} + C\boldsymbol{\omega}_{\mathbf{coup}} \mathbf{v_o^*} \tag{10}
$$

Now, let us substitute Equations (8)–(10) into Equation (7):

$$
\frac{d^2 \Delta \mathbf{i_L}}{dt^2} + \mathbf{L}^{-1} \mathbf{R} \frac{d\Delta \mathbf{i_L}}{dt} + \frac{1}{C} \mathbf{L}^{-1} \Delta \mathbf{i_L}
$$

$$
+ \boldsymbol{\omega}_{\mathbf{coup}} \left(\frac{d\Delta \mathbf{i_L}}{dt} + \mathbf{L}^{-1} \mathbf{R} \Delta \mathbf{i_L} \right) = \mathbf{0} \tag{11}
$$

where $\Delta \mathbf{i_L} = \mathbf{i_L} - \mathbf{i_L^*}$ is the UPS VSI current error and $\mathbf{0}$ is the 3×1 zero matrix. The above equation can beneficially be stated in a more applicable form as

$$\underbrace{\frac{d^2 \Delta \mathbf{i_L}}{dt^2} + 2\zeta \boldsymbol{\omega_n} \frac{d \Delta \mathbf{I_L}}{dt} \boldsymbol{\omega_n^2} \Delta \mathbf{i_L}}_{\text{Term 1}}$$

$$\underbrace{+ \boldsymbol{\omega_{coup}} \left(\frac{d \Delta \mathbf{i_L}}{dt} + \boldsymbol{\tau}^{-1} \Delta \mathbf{i_L} \right)}_{\text{Term 2}} = \mathbf{0} \tag{12}$$

where

$$\boldsymbol{\omega_n^2} = \frac{1}{C} \mathbf{L}^{-1}, \zeta \boldsymbol{\omega_n} = \frac{1}{2} \mathbf{L}^{-1} \mathbf{R}, \boldsymbol{\tau} = \mathbf{R}^{-1} \mathbf{L} \tag{13}$$

where $\boldsymbol{\omega_n}$, ζ and $\boldsymbol{\tau}$ are the undamped natural frequency, damping ratio and time constant diagonal matrices, respectively. Terms 1 and 2 of Equation (12) are the second- and first-order differential equations, respectively. Equation (12) shows that $\Delta \mathbf{i_L}$ decreases to zero in company with ζ and $\boldsymbol{\tau}$ under all conditions. The mentioned specifications are completely significant since they must display permissible dynamic responses. It means that these parameters need to be corrected until the dynamic response of the considered system is satisfactory. In order to have a suitable dynamic response, the elements of the main diagonal of the matrices ζ and $\boldsymbol{\tau}$ should be selected equal to $1/\sqrt{2}$ and as low as possible, respectively. Evidently, $\Delta \mathbf{i_L}$ has a large overshoot and its decay rate is noticeably slow as the non-zero elements of the $\mathbf{R}$ including R and R_n are too small. On the other hand, Equation (9) achieves the control of $\mathbf{v_o}$ indirectly provided that $\mathbf{i_L}$ properly tracks its reference. Otherwise, there will exist steady-state errors in $\mathbf{v_o}$. Therefore, for the sake of modifying the overshoot and decay rate of $\Delta \mathbf{i_L}$ and steady-state error in $\mathbf{v_o}$, two constant matrices $\mathbf{K_i}$ and $\mathbf{K_v}$ multiplied by the inverter current and output voltage error vectors are embedded through correcting Equation (9) as

$$\mathbf{u} = \frac{2}{V_s} \left(\mathbf{Ri_L^*} + \mathbf{L} \frac{d\mathbf{i_L^*}}{dt} + \mathbf{v_o^*} + L \boldsymbol{\omega_{coup}} \mathbf{i_L} - \mathbf{K_i} \Delta \mathbf{i_L} - \mathbf{K_v} \Delta \mathbf{v_o} \right) \tag{14}$$

where $\Delta \mathbf{v_o} = \mathbf{v_o} - \mathbf{v_o^*}$ is the output voltage error and

$$\mathbf{K_j} = \begin{bmatrix} K_{jd} & 0 & 0 \\ 0 & K_{jq} & 0 \\ 0 & 0 & K_{j0} \end{bmatrix}, j = i, v \tag{15}$$

where the elements of the main diagonal of the matrix $\mathbf{K_j}$ are positive real constants. Now, replacement of Equations (8), (10)

and (14) into Equation (7) yields

$$\frac{d^2 \Delta \mathbf{i_L}}{dt^2} + \mathbf{L}^{-1} (\mathbf{R} + \mathbf{K_i}) \frac{d \Delta \mathbf{i_L}}{dt} + \frac{1}{C} \mathbf{L}^{-1} (\mathbf{K_v} + \mathbf{I}) \Delta \mathbf{i_L}$$

$$+ \boldsymbol{\omega_{coup}} \left(\frac{d \Delta \mathbf{i_L}}{dt} + \mathbf{L}^{-1} (\mathbf{R} + \mathbf{K_i}) \Delta \mathbf{i_L} \right) = \mathbf{0} \tag{16}$$

where $\mathbf{I}$ is the 3×3 unit matrix. The general form of Equation (16) is given by

$$\frac{d^2 \Delta \mathbf{i_L}}{dt^2} + 2\boldsymbol{\zeta'} \boldsymbol{\omega'_n} \frac{d \Delta \mathbf{i_L}}{dt} + (\boldsymbol{\omega'_n})^2 \Delta \mathbf{i_L}$$

$$+ \boldsymbol{\omega_{coup}} \left(\frac{d \Delta \mathbf{i_L}}{dt} + (\boldsymbol{\tau'})^{-1} \Delta \mathbf{i_L} \right) = \mathbf{0} \tag{17}$$

where

$$(\boldsymbol{\omega'_n})^2 = \frac{1}{C} \mathbf{L}^{-1} (\mathbf{K_v} + \mathbf{I}), \boldsymbol{\zeta'} \boldsymbol{\omega'_n} = \frac{1}{2} \mathbf{L}^{-1} (\mathbf{R} + \mathbf{K_i}),$$

$$\boldsymbol{\tau'} = (\mathbf{R} + \mathbf{K_i})^{-1} \mathbf{L} \tag{18}$$

where $\boldsymbol{\omega'_n}$, $\boldsymbol{\zeta'}$ and $\boldsymbol{\tau'}$ are the virtual undamped natural frequency, damping ratio, and time constant matrices that are able to be regulated through $\mathbf{K_i}$ and $\mathbf{K_v}$ to attain a better response for the system. According to Equation (18) and considering $\boldsymbol{\zeta'} = 1/\sqrt{2} \mathbf{I}$, the relationship between controller gains can be expressed as:

$$2\mathbf{L} (\mathbf{K_v} + \mathbf{I}) = C (\mathbf{R} + \mathbf{K_i})^2 \tag{19}$$

The block diagram of the UPS VSI and the proposed approach are shown in Figure 2.

4 | INFLUENCE OF CONTROLLER GAINS ON POLE LOCATIONS

Using Equations (7), (8), (10) and (14), the equations of the closed-loop system in the state-space form are written in the following form

$$\dot{\mathbf{X}} = \mathbf{AX} \tag{20}$$

where

$$\mathbf{X} = \begin{bmatrix} \Delta \mathbf{i_L} \\ \Delta \mathbf{v_o} \end{bmatrix}, \mathbf{A} = \begin{bmatrix} -\mathbf{L}^{-1} (\mathbf{R} + \mathbf{K_i}) & -\mathbf{L}^{-1} (\mathbf{K_v} + \mathbf{I}) \\ \frac{1}{C} \mathbf{I} & -\boldsymbol{\omega_{coup}} \end{bmatrix} \tag{21}$$

As can be observed in Equation (19), all the parameters except $\mathbf{K_i}$ and $\mathbf{K_v}$ are known which means that if the influence of one of these gain matrices is investigated, the influence of the
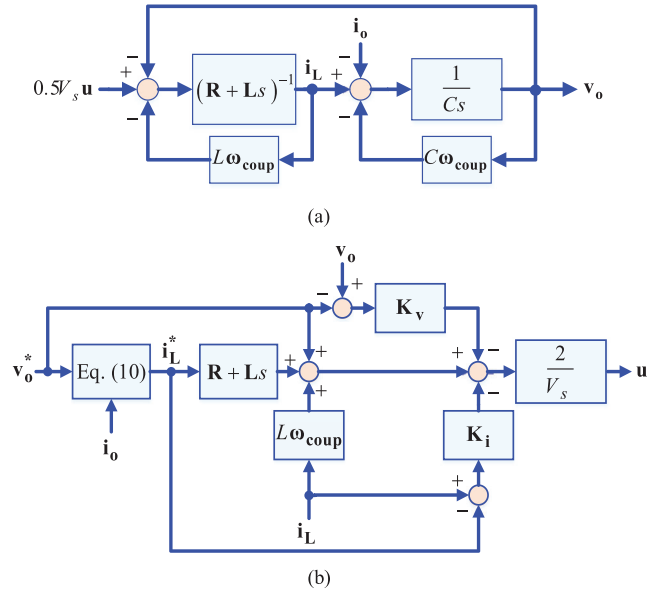
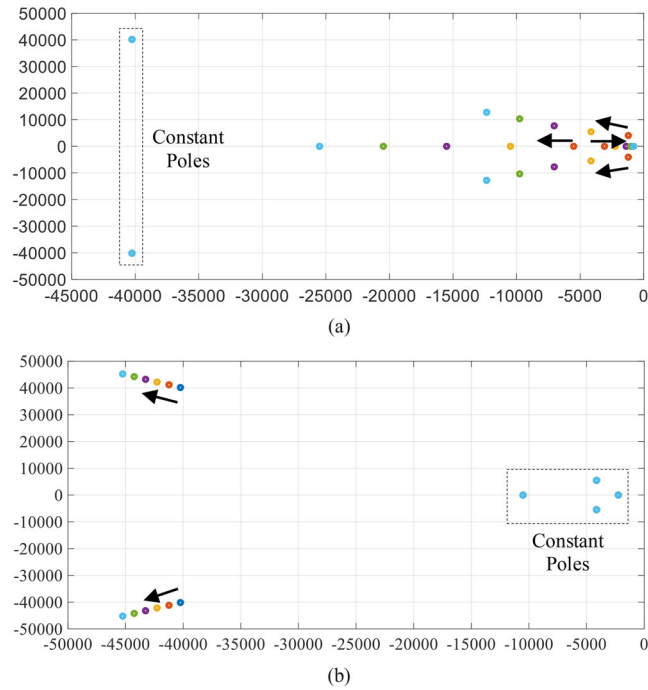FIGURE 2 Block diagram of the (a) UPS VSI and (b) the proposed control approach

FIGURE 3 The loci of closed-loop system poles obtained when (a) K_{id} is varied, (b) K_{i0} is varied
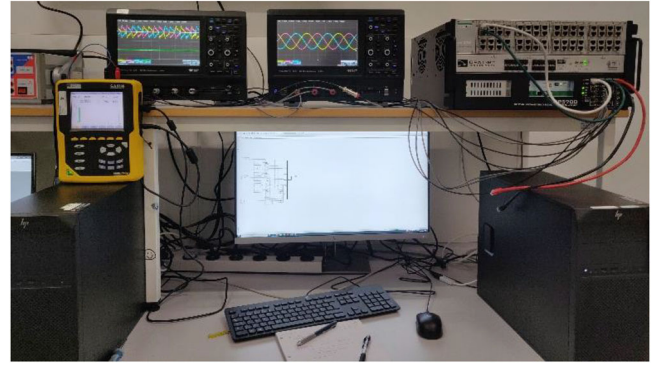
FIGURE 4 Laboratory setup

TABLE 1 System parameters

Symbol	Description	Value
P_o	Inverter nominal power	5 kW
V_s	DC link voltage	350 V
R	Filter resistance	0.1 Ω
L	Filter inductance	2 mH
C	Filter capacitance	100 μF
R_n	Neutral filter resistance	0.05 Ω
L_n	Neutral filter inductance	1 mH
V_o^*	Nominal output voltage amplitude	120 Vrms
ω	Angular frequency	100π rad/s
f_s	Switching frequency	15 kHz
$K_{id} = K_{iq}$	Current loop gains in d- and q-axes	58.4
K_{i0}	Current loop gain in 0-axis	37.7
$K_{vd} = K_{vq}$	Voltage loop gains in d- and q-axes	84.5
K_{v0}	Voltage loop gain in 0-axis	13.4

The extraction of optimal controller gains in an analytical process may be awkward owing to the high degree of the closed-loop system (six-order) under study. For this reason, selecting the desired controller gains is capable of being realised according to the system root locus. It is well-known that the closed-loop poles located away from the imaginary axis in the left-half of s-plane decay rapidly to zero. Taking this point into consideration, the system transient response can be dominated via other existing poles.

First, we investigate the influence of K_{id} on the location of the closed-loop system poles when K_{i0} is kept at a constant value of 37.7. This value is selected in such a way that the two corresponding poles are located enough distance from the imaginary axis. As can be seen in Figure 3a, under this condition, there are two fixed poles. These poles are complex conjugate pairs with the real components which are equal to the imaginary ones and located in the left half of s-plane. As $|K_{id}|$ is increased, two of the remaining poles move far from each other on the negative real axis and the other pole pairs get away from the point (0,0) in the negative side of the real axis and in an approximately linear

other is also investigated indirectly. Thus, in the following, only the influence of $\mathbf{K_i}$ will be investigated. In addition, in order to simplify the upcoming analysis, we consider
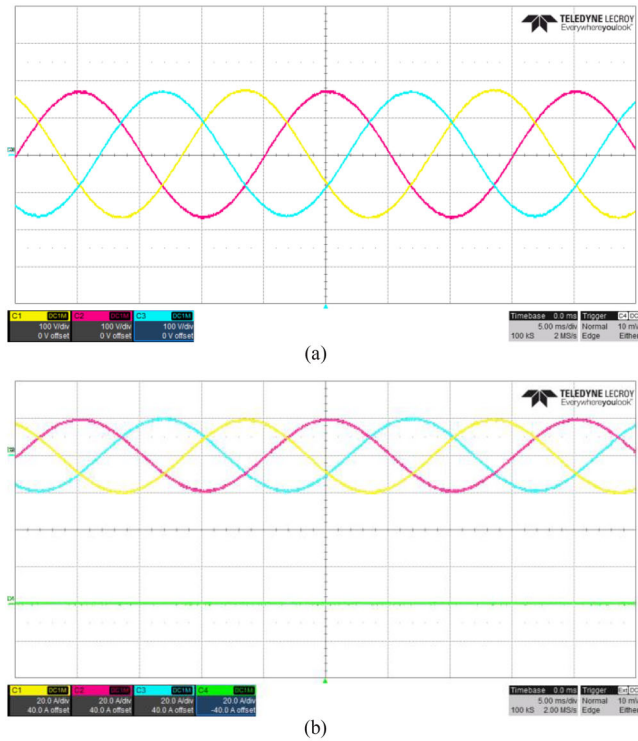
$$K_{id} = K_{iq} \tag{22}$$

(a)

(b)

(c)

FIGURE 5 Results of the proposed control approach under balanced resistive load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltage harmonic spectrum
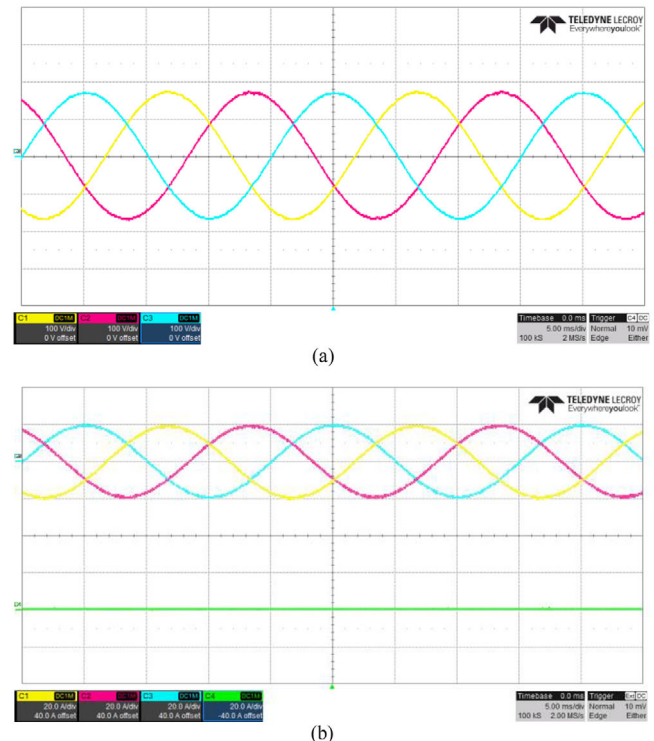

(a)

(b)

(c)

FIGURE 6 Results of the SMC method under balanced resistive load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltage harmonic spectrum

trajectory. This obviously indicates that K_{id} plays a significant role in defining the system convergence time.

Second, the influence of K_{i0} on the location of the closed-loop system poles is studied when K_{id} is kept at a constant value of 58.4. This value is selected with regard to Figure 3a. As shown in Figure 3b, there are four fixed poles in this case situated in the left half of s-plane. With an increment in $|K_{i0}|$, the two other poles which are complex conjugate pairs move far from the point (0,0) in a way similar to Figure 3a. Therefore, with respect to the aforementioned points, the global stability of closed-loop system can be guaranteed.

5 | PERFORMANCE VALIDATION

To assess the performance of the proposed control approach under the operation of a three-phase four-leg UPS VSI, the

system illustrated in Figure 1 has been taken into consideration for a real-time simulation. The system prototype has been implemented by means of an OPAL-RT simulator on MAT-LAB/Simulink software as shown in Figure 4 where the real-time simulation machine and its supporting computer dedicated for capturing the results are noticeable. Various load types, including linear/non-linear and balanced/unbalanced loads, have been utilised in the studies. Additionally, the SMC method presented in [19] has been adopted to exhibit a comparative analysis of the proposed approach. The values of the system parameters are listed in Table 1.

In the beginning, the steady-state performance of the proposed approach under a balanced 5 kW resistive load has been evaluated. The output voltages as well as the load and neutral currents responses are indicated in Figure 5a,b, where the sinusoidal output voltages with very low distortions are obtained.
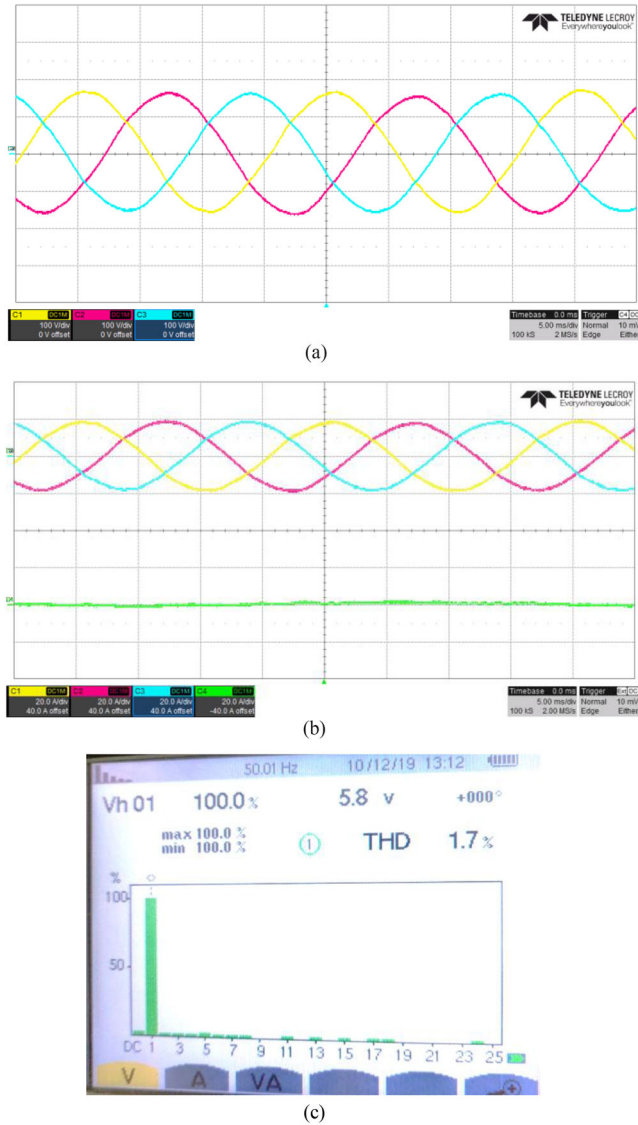
FIGURE 7 Results of the proposed control approach under balanced resistive load when the voltage loop gains are considered to be zero: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltage harmonic spectrum

FIGURE 8 Results of the proposed control approach under three-phase unbalanced resistive load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div)

FIGURE 9 Results of the SMC method under three-phase unbalanced resistive load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div)

Besides, the harmonic spectrum, along with the THD value of the output voltage, is represented in Figure 5c. The THD is measured to be 0.3% under linear load. This THD value is far below the 8% limit of IEC 62040-3 standard [38].

Figures 6a and 6b show the steady-state waveforms of the output voltages and also load and neutral currents in the natural frame respectively under a balanced 5 kW resistive load obtained with the SMC method. It is evident that the sinusoidal output voltages have been attained. Figure 6c shows the harmonic spectrums of the output voltage obtained with the SMC method which is 0.4%. Comparing Figure 5c with Figure 6c, one can easily observe that the output voltages under employing the SMC method are somewhat more distorted.

In order to verify the significance of the output voltage loops in the switching functions, the results of the proposed approach
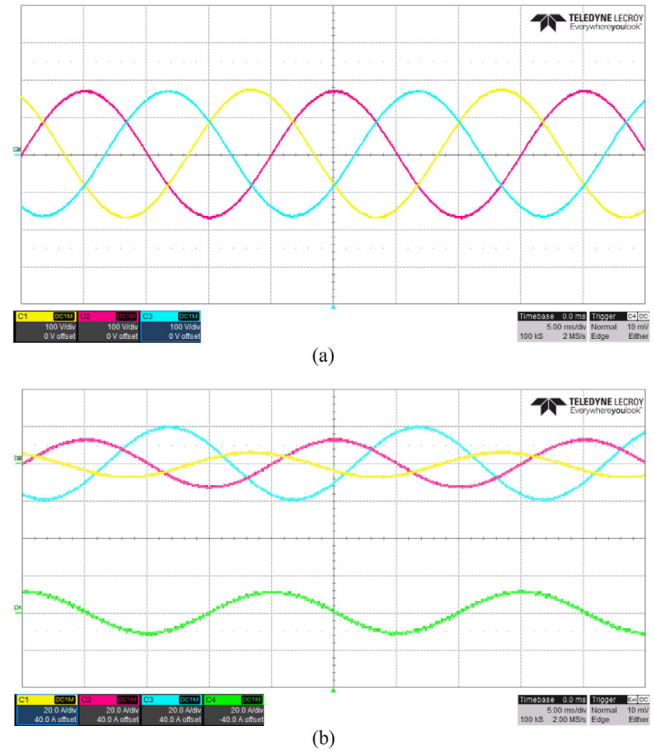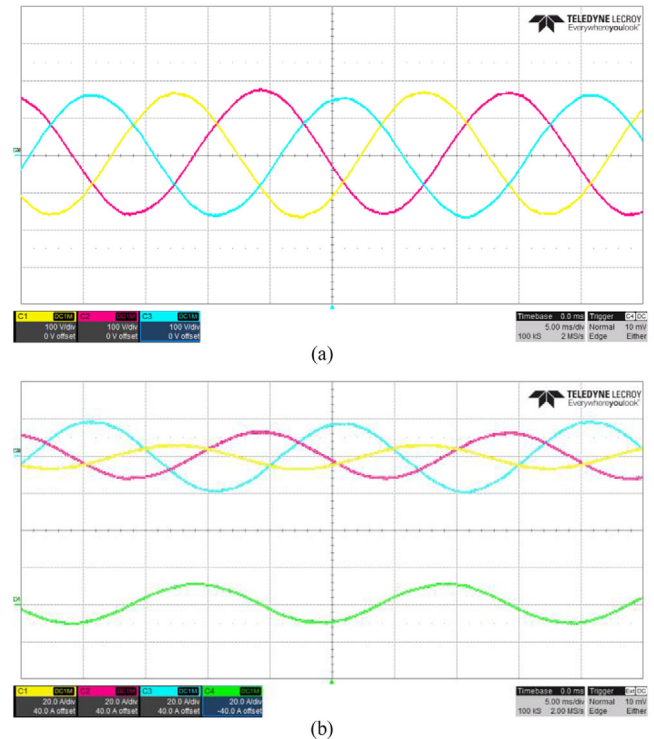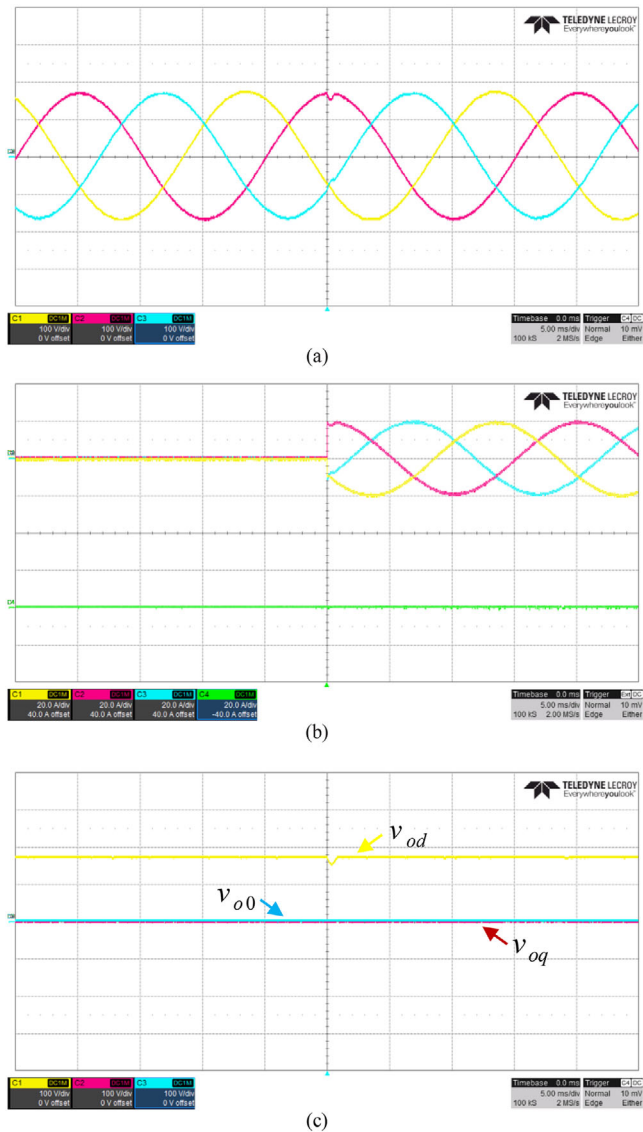
FIGURE 10 Results of the proposed control approach under no-load to balanced nominal resistive load step change: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltages in *dq*0 frame (100 V/div)

FIGURE 11 Results of the SMC method under no-load to balanced nominal resistive load step change: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltages in *dq*0 frame (100 V/div)

for the output voltages and also load and neutral currents under the connection of the balanced linear load when the output voltage loops are not activated are presented in Figure 7a,b. As it can be seen in Figure 7a, the output voltages are too much distorted as compared with Figure 5a and have steady-state error. The THD value of the output voltage at steady-state operation is shown in Figure 7c. This value is found as 1.7%. As a consequence, it is explicitly demonstrated that the voltage loop gains lead to lower THD.

A four-leg VSI in UPS applications must be able to deal with unbalanced loading conditions. Accordingly, the results in the case of three-phase unbalanced resistive load are depicted in Figure 8. The load currents circulate through phase leg and neutral pathway supplied via the fourth leg of the UPS VSI. Under this condition, the four-leg VSI provides sinusoidal output volt-
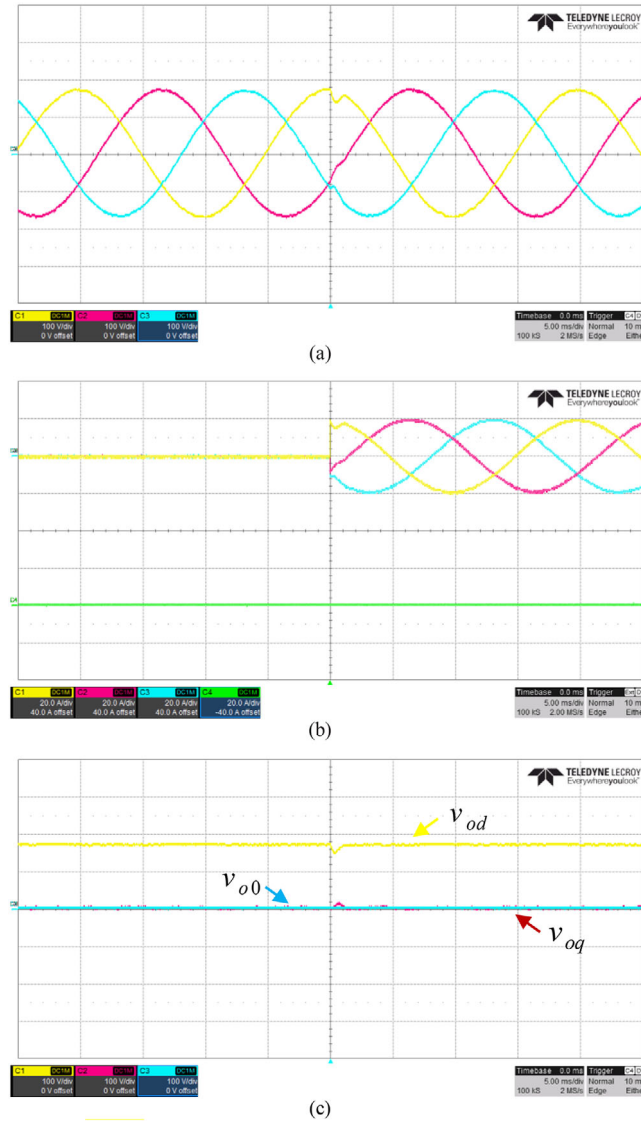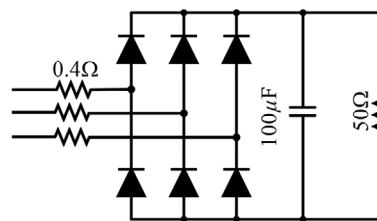

FIGURE 12 Used non-linear load

ages in all phases. It demonstrates one of the benefits of four-leg UPS VSI, that is, the fact that the output voltages are not influenced by each other, and each phase can be independently adjusted.
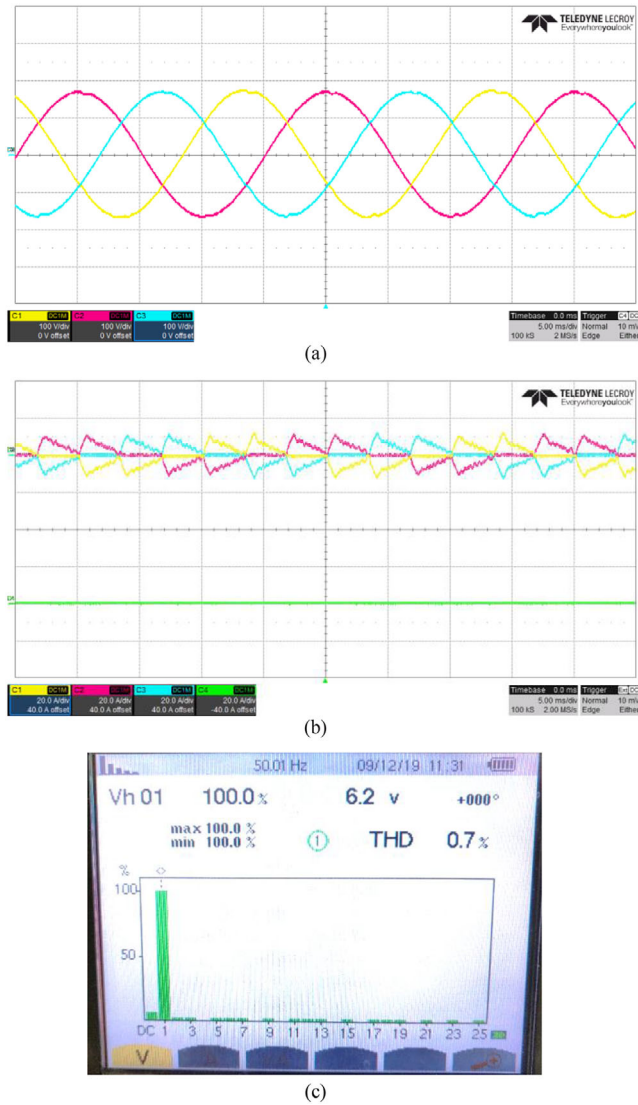
FIGURE 13 Results of the proposed control approach under non-linear load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltage harmonic spectrum

TABLE 2 Analysis obtained with proposed control and SMC schemes in cases of different mismatches under linear and non-linear loads

	Scheme	Parameter mismatch (%)	Steady-state error (V)	THD (%)
Linear load	Proposed control	+50	2	0.6
		+25	1	0.4
		0	0	0.3
		−25	1	0.4
		−50	3	0.6
	SMC	+50	6	0.9
		+25	3	0.4
		0	1	0.4
		−25	1	0.4
		−50	3	0.5
Non-linear load	Proposed control	+50	2	1
		+25	1	0.8
		0	1	0.7
		−25	2	0.8
		−50	2	1.1
	SMC	+50	3	1.3
		+25	1	1.1
		0	1	0.9
		−25	4	1.3
		−50	5	1.4

Figure 9 shows the responses of the output voltages as well as load and neutral currents in the *abc* frame obtained with the SMC method under the loading, same as the one of Figure 8. The steady-state errors and unbalance in the waveforms of output voltages are discernible in the achieved results. Therefore, it can be observed by comparing Figure 8 with Figure 9 that the proposed approach provides a better output voltage regulation in unbalanced loading conditions compared with the SMC method.

In another test, the dynamic performance for a step-change from no-load to the balanced nominal linear load has been investigated. The results of the output voltages as well as load and neutral currents in reply to this abrupt variation are illustrated in Figures 10a and 10b. Figure 10c shows the output voltage results in the *dq*0 frame. It can be observed that the proposed control approach recovers the output voltage within a time interval of about 0.85 ms. In contrast, an allowable voltage deviation of 19 V is achieved under the transient operating condition (according to IEC 62040-3 standard, a ±30% output voltage deviation from its reference value is permitted for time intervals less than 5 ms). In addition, it is seen that the stability of the UPS inverter system is not affected during this case.

Figures 11a and 11b show the dynamic waveforms of the output voltages as well as load and neutral currents for a sudden change in the balanced linear load from no-load to full load obtained with the SMC method. As depicted in Figure 11c, the voltage dip under the SMC method is 24V, and its recovery time is 1.1 ms that is longer than the one corresponding to the proposed control approach as compared with Figure 10c. In addition, as can be seen in Figure 11c, unlike Figure 10c, the *q*-component of the output voltage is impressed under the SMC method.

In the following, for the sake of further evaluating the steady-state performance of the proposed control approach, the UPS inverter behaviour has also been studied in the presence of a balanced non-linear load, as shown in Figure 12. The responses of the output voltages and also load and neutral currents are shown in Figure 13a,b. Despite these highly distorted currents, the output voltages remain sinusoidal and are approximately distortion-free. Furthermore, the THD of the output voltage is 0.7% as indicated in Figure 13c, while its fundamental amplitude is computed to be almost equal to the reference value as shown in Table 2. This evidently demonstrates the success of the proposed approach in closely obtaining zero steady-state error of
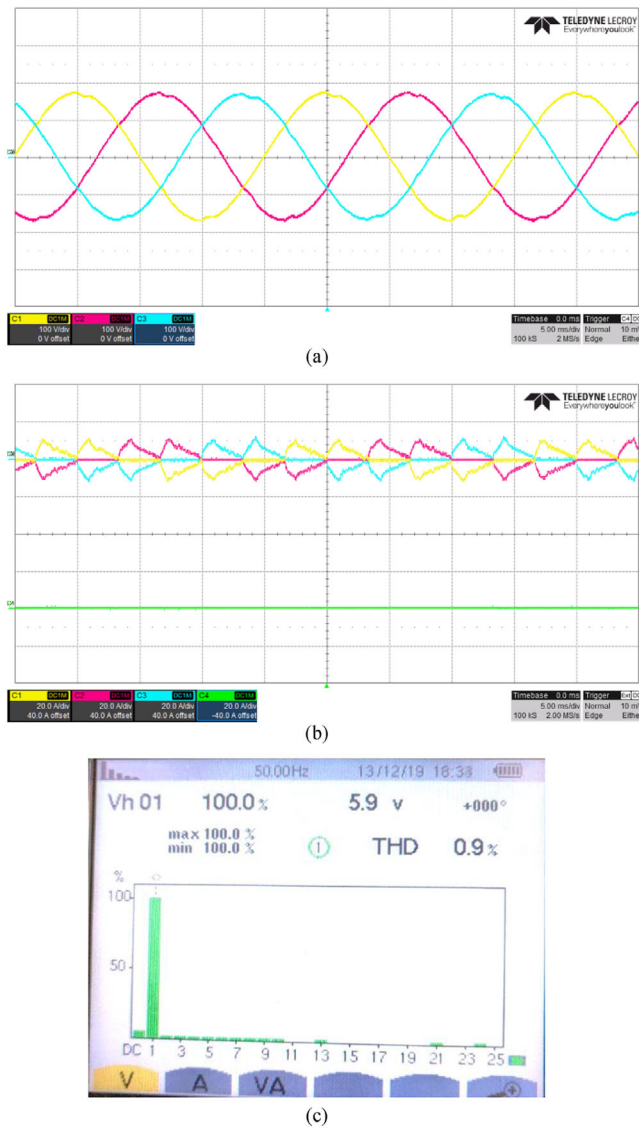
(a)

(b)

(c)

FIGURE 14 Results of the SMC method under non-linear load: (a) output voltages in *abc* frame (100 V/div), (b) load and neutral currents in *abc* frame (20 A/div), (c) output voltage harmonic spectrum

(a)

(b)

FIGURE 15 White noise: (a) added to i_{Labc}, (b) added to v_{oabc}

the output voltage. Accordingly, as stated by the attained results, the proposed control approach is capable of providing the high-quality output voltage which complies with the IEC 62040-3 standard limitations.

The steady-state operation of the UPS inverter controlled by the SMC has been assessed under the same non-linear loading. The results of the output voltages as well as load and neutral currents are presented in Figure 14a,b. The THD value of the output voltage is shown in Figure 14c. This value is found to be 0.9%. Comparing Figure 13c with Figure 14c, one can see that the output voltages obtained with the proposed control approach are less distorted.

As previously mentioned, the proposed control approach requires the system model to work properly. However, in practical applications, it is impossible to know the precise values of the system parameters. Therefore, the operation of the UPS VSI
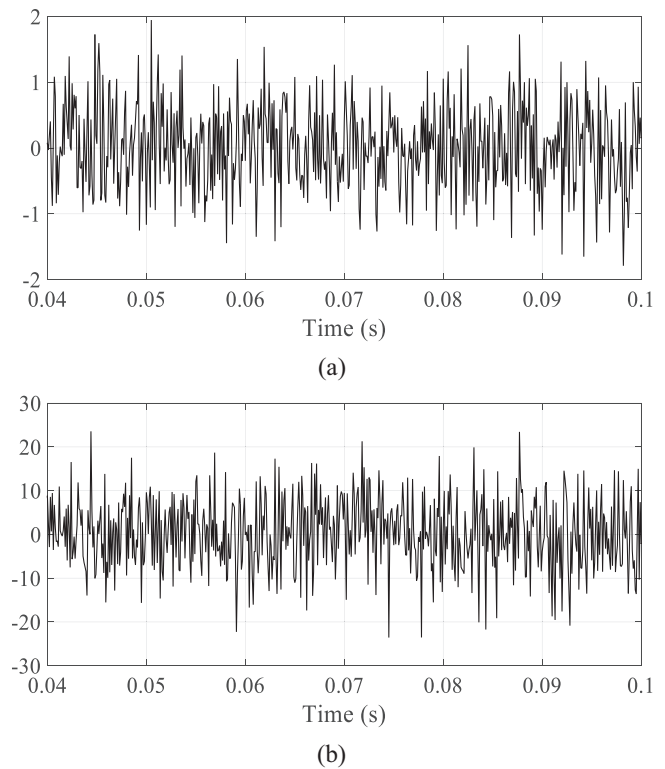
controlled by the proposed approach with the consideration of the system parameter mismatches should also be investigated. As a result, the performance of the proposed control approach and the SMC method, in terms of the THD and the steady-state error in the output voltage, considering mismatches in all the system filter parameters has been studied under the linear and non-linear loads. The results are presented in Table 2. It can be deduced that the performance of the proposed control approach is not considerably degraded even in the presence of an immense range of mismatch amounts. Furthermore, it is seen that except for one case (THD obtained with -50% parameter mismatch under linear load), the proposed control approach provides better performance than the SMC method.

5.1 | Effect of measurement noises in control loops

For the sake of evaluating the effect of the measurement noises in the control loops, a simulation study has been carried out with the consideration of two white noises shown in Figure 15 added to the measured values of i_{Labc} and v_{oabc}. These waveforms have been assumed to be the measurement noises. Also, in order to test the system under the condition similar to practical applications, i_{oabc} has been replaced with $i_{Labc} - C\frac{dv_{oabc}}{dt}$ in the proposed control approach. After applying Park's transformation to the final signals, they were incorporated into the control equations (10) and (14). The steady-state and transient responses of the output voltage and load current with the
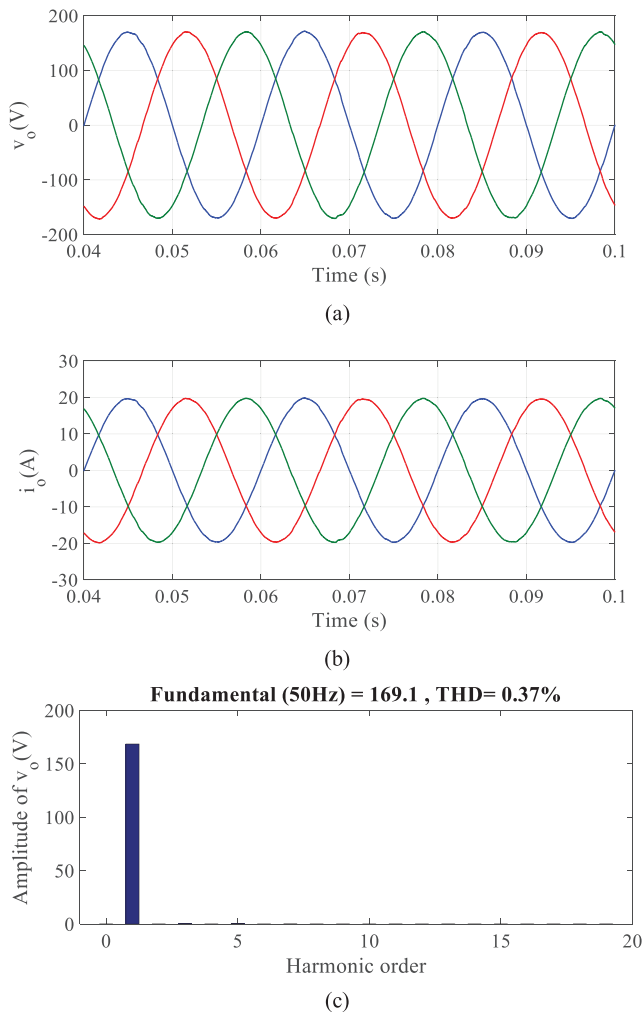
FIGURE 16 Steady-state responses considering the measurement noises: (a) output voltage, (b) load current, (c) output voltage harmonic spectrum

FIGURE 17 Transient responses considering the measurement noises: (a) output voltage, (b) load current

measurement noises under the connection of the linear load are shown in the following.

Figure 16 shows the steady-state responses of the output voltage as well as load current considering the measurement noises. As can be seen, the output voltage remains sinusoidal with the THD value of 0.37% and the steady-state error of 0.6V.

Figure 17 shows the transient responses of the output voltage as well as load current considering the measurement noises. Furthermore, the voltage dip and recovery time are 18V and 0.82 ms, respectively.

Therefore, according to the obtained results, it can be deduced that the performance of the proposed control approach is satisfactory under measurement noises.

6 | CONCLUSION

A control approach based on system modelling has been proposed for three-phase four-leg LC-filtered UPS VSIs through regulating the VSI currents in the $dq0$ synchronous frame. The at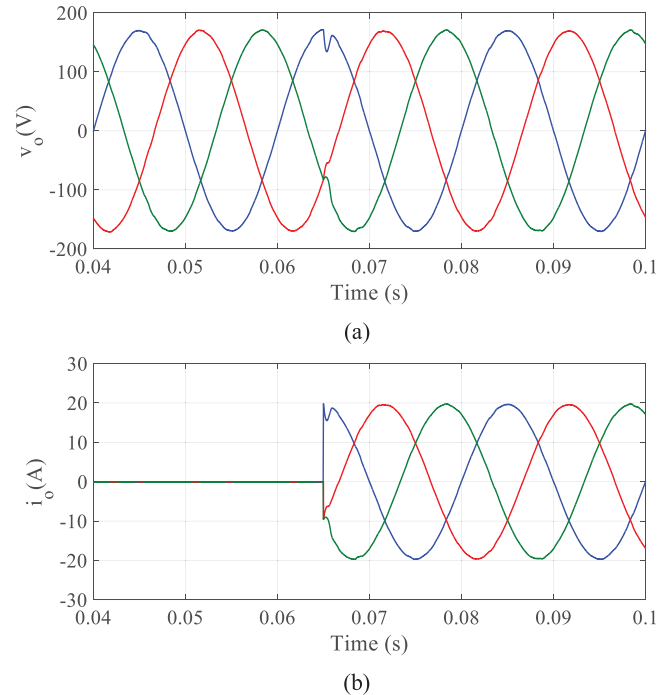titude presented in this paper can modify the system's basic characteristics such as undamped natural frequency, damping ratio and time constant and offer flexibility in order to improve the system dynamic and steady-state responses as desired. The efficacy of the proposed approach has been validated by the SIMULINK-based and real-time simulation results under linear/non-linear and balanced/unbalanced loads. The results have evidently exhibited that the proposed control approach not only ensures the global stability of the three-phase UPS VSI system but also successfully obtains the balanced steady-state output voltage adjustment specification as well as the dynamic response and the THD necessities of IEC 62040-3 standard even under large parameter mismatches.

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