A Fault Detection Scheme for Islanded-Microgrid with Grid-Forming Inverters

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A Fault Detection Scheme for Islanded-Microgrid with Grid-Forming Inverters

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***Abstract*— This paper proposes a fault detection scheme for microgrids with grid-forming inverters. In this paper, a superimposed phase-current scheme with a voltage-restraint element is proposed which identifies the faults in an islanded microgrid with grid-forming inverters. In the proposed method, different factors including the implemented fault-ride-through strategy, the fault current limiting scheme, and the control structure of the grid-forming inverter are considered. Furthermore, the moving window concept is included, which considerably increases the detection speed. The severity and type of short circuit fault do not affect the functionality of the proposed method, and both symmetrical/asymmetrical short circuit faults are properly identified by the proposed scheme. Finally, the performance of the proposed scheme is demonstrated by applying different symmetrical/asymmetrical faults in a test system.**

Keywords*— *fault detection scheme, grid-forming inverter, inverter-based microgrid, islanded mode, microgrid (MG), microgrid protection strategy

I. Introduction

THE environmental issues related to fossil fuels and security requirements for minimizing the electricity outage motivate more investments on implementation of the distributed generations (DGs) at the power grid. DGs include both types of conventional synchronous generators and new emerging inverter-based distributed energy resources. Using DGs at the load side decreases the overall generation cost, reduces the loss in the transmission line, and increases the power grid reliability. The collection of DGs and loads provides an opportunity for operation in an islanded mode, which introduces the concept of microgrid (MG) [1]. To benefit from the advantages of MG, the corresponding technical challenges should be highlighted and addressed including the MG protection. Integration of DGs into the power grid change the passive nature of grid into an active one with bi-directional flow of fault currents [2]. Furthermore, the short-circuit fault current amplitude considerably decreases in an islanded mode of operation [3, 4], specifically when the grid-forming converters are the sources of MG [3]. Such features of islanded MGs with grid-forming inverters cause mal-operation of conventional protective devices, and proper solutions have to be developed [5].

OC relays and reclosers are the conventional relays for the protection of both islanded and grid-connected microgrid with synchronous generators [6]. Also, optimal coordination of OC relays are discussed in the literature [7]. Such methods based on over-current are not effective in islanded inverter-based microgrids. As a result, several approaches are suggested in the literature as follows.

Using a voltage signal is the simplest remedy for detection of fault. Under-voltage (UV) relay and the total harmonic distortion (THD) quantity are the examples of using voltage signals [8]. However, UV relay scheme is not a precise method since the voltages in all busbars drop during fault condition. Also, the voltage THD is considerably affected by employed current limiting strategy, and the state-of-the-art limiting strategies avoid distortion of voltages [3, 9].

The use of current signal is another remedy for fault detection. Extracting the fault transients by wavelet transform [10], Monitoring the transient response of the inverter [11], using differential current method [12], using phase angle comparison of the current signals [13], extracting current sequence components [14, 15] are proposed for fault detection in the literature. The noise immunity, computation burden, mismatch of measured currents, requiring communication infrastructure, dependency on the system conditions, and variable detection threshold are concerns raised by using the mentioned schemes.

In this paper, a superimposed phase-current scheme with a voltage-restraint element is proposed which identifies the faults in an islanded microgrid with grid-forming inverters. The proposed method inherently considers the grid-forming inverter behavior, which considerably improves the accuracy and speed of the fault detection. Furthermore, the moving window concept is included in the proposed scheme, which considerably increases the detection speed. The severity and type of short circuit fault do not affect the functionality of the proposed method, and both symmetrical/asymmetrical short circuit faults are properly identified by the proposed scheme. The proposed method is independent of the magnitude of fault current, which makes it suitable for islanded inverter-based microgrids. As the fundamental component of currents are utilized in the proposed method, its performance is not affected by system harmonics and non-fundamental components.

The rest of the paper is organized as follows. Section II provides the control structure of a grid-forming inverter. The proposed fault detection scheme is presented in section III. Simulation results are presented in section IV. Finally, section V concludes the paper.

II. Control of Grid-Forming Inverters

A. Control Structure

Fig. 1 depicts a power circuit schematic diagram and control structure of a grid-forming inverter. The control system of grid-forming inverter plays an important role in the short-circuit behavior of the inverter. The control structure consists

of three different parts including (*i*)- voltage controller, (*ii*)- current limiter, and (*iii*)- current controller. The voltage controller adjusts the output voltages of the inverter to the reference values of $V^*_{o\alpha\beta}$. Conceptually, the voltage control process is done by producing proper current references of $i^*_{t\alpha\beta}$, and current controller is responsible for control of inverter terminal currents of $i_{t\alpha\beta}$. The voltage controller block of Fig. 1 consists of a compensator for voltage regulation as given in (1). In this compensator, two complex conjugate poles of $\pm j\omega_0$ guarantee the stable operation of voltage control loop with zero steady-state error. Also, zeros of z_1 and z_2 improve the compensator performance. The gain k_p determines the overall stability of the control system. The analysis and design of resonant compensator can be found in [16, 17].

$$k(s) = k_p \times \frac{(s+z_1)\times(s+z_2)}{s^2+\omega_0^2} \tag{1}$$

Under short-circuit fault condition, the needed current for voltage regulation exceeds the nominal ratings of the inverter. Then, the current limiter limits the current references of $i^*_{t\alpha\beta1}$ to $i^*_{t\alpha\beta2}$. Limiting the magnitude of the phase current with the maximum amplitude is the goal of the current limiting process. This mechanism determines the behavior of the inverter under short-circuit fault condition. The current control block of Fig. 1 also has a compensator similar to that of voltage control block, which guarantees the stable operation of current control loop. The basics of control of grid-forming converters can be found in [3, 18]. More details are not provided for the sake of brevity.

III. Proposed Fault Detection Scheme

By analyzing the behavior of the grid-forming inverter, a fault detection feature based on the voltage-restraint superimposed phase current is proposed. The current limiting strategy of Fig. 1 reduces the amplitude of the phase current with the maximum amplitude. This current limiting strategy determines the short-circuit behavior of the converter. Under short-circuit fault condition, the significant difference between the normal and faulty condition can be used for fault detection. Fig. 2 shows the proposed fault detection method, which consists of three parts of (a)- phase-current superimposed component calculation, (b)- calculation of voltage-restraint quantity, (c)- fault detection and trip signal calculation. The formulation and details of the different are presented in the following.

A. Superimposed Component Calculation

Under normal operating condition, the output current of the converter can be defined as given in (2). In this equation, n, I_m, ω, ΔT_s, φ are the sample number, current amplitude, angular frequency, sample time interval, and phase-angle, respectively.

$$i(n) = I_m \times \cos(\omega n \times \Delta T_s + \varphi) \tag{2}$$

Occurrence of fault changes the amplitude and phase-angle of the fault current as given in (3). The current amplitude I'_m is limited to the value below the maximum permissible current. The fault current of (3) is mainly reactive since the fault loop is inductive.

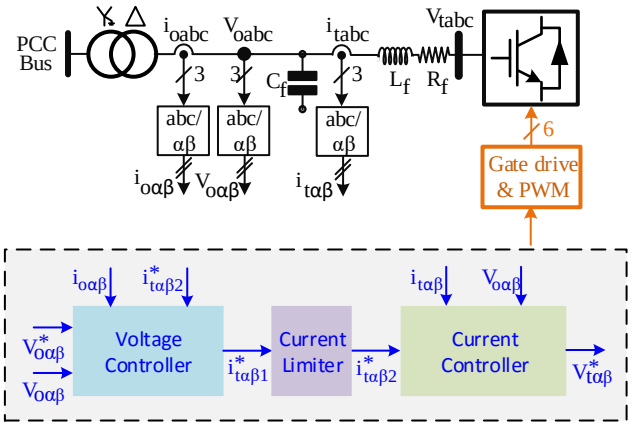

Fig. 1. Power circuit schematic diagram and control structure of a grid-forming inverter

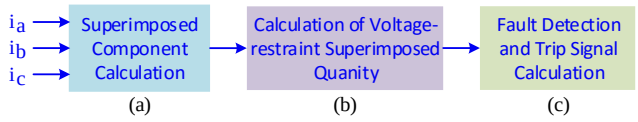

Fig. 2. The proposed fault detection method; (a)- superimposed component calculation, (b)- calculation of voltage-restraint superimposed quantity, (c)- fault detection and trip signal calculation.

$$i'(n) = I'_m \times \cos(\omega n \times \Delta T_s + \varphi') \tag{3}$$

The different between the nominal current of (2) and the fault current of (3) can effectively distinguish the occurrence of fault. The amplitude and phase of the difference are given in (4) and (5).

$$|i - i'| = \sqrt{I_m^2 + {I'_m}^2 - 2I_m I'_m \times \cos(\varphi - \varphi')} \tag{4}$$

$$\measuredangle(i - i') = \frac{I_m \cos(\varphi) - I'_m \cos(\varphi')}{I_m \sin(\varphi) - I'_m \sin(\varphi')} \tag{5}$$

Considering the high-amplitude of (4), the fault occurrence can be effectively detected using the differential current. To implement the differential current, the superimposed components of the current is suggested in this paper. The approach for the calculation of the superimposed components is shown in Fig. 3. In this figure, original current waveform (top), four cycle delayed of original current waveform (middle), and super-imposed current component (bottom) are depicted. The four-cycle delayed of original current waveform is utilized to produce the nominal current for super-impose component calculation. The number of cycles determines the time period in which the superimposed components take a high-amplitude component. The four-cycle time interval gives an appropriate time delay for operation of the protective relays.

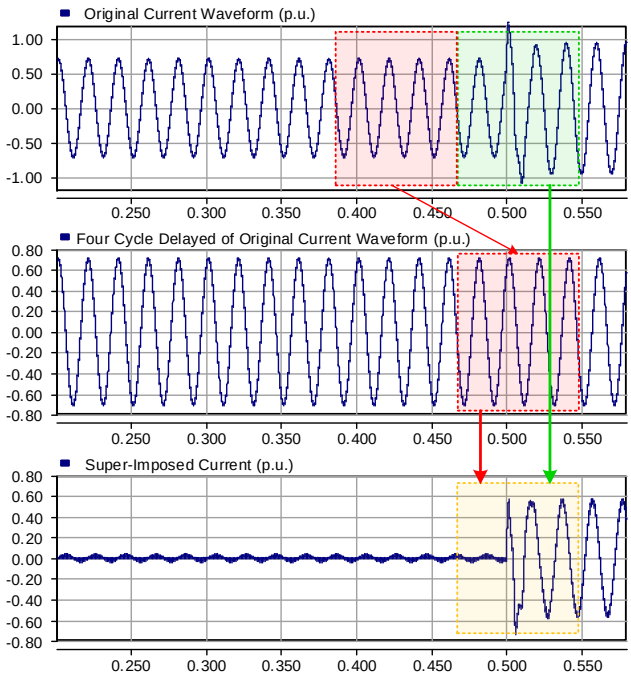

Fig. 3. Superimposed current calculation, original current waveform (top), four-cycle delayed of original current waveform (middle), super-imposed current component (bottom)

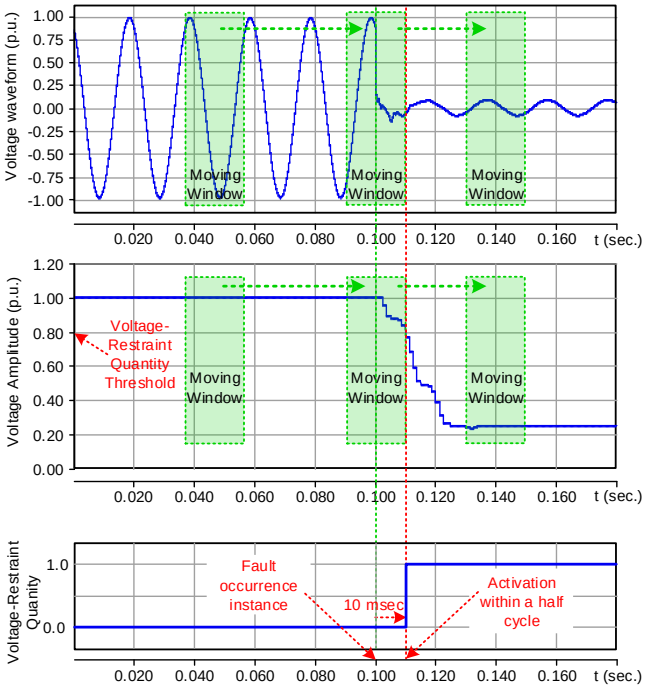

Fig. 4. Voltage-restraint quantity Superimposed current calculation, original current waveform (top), four cycle delayed of original current waveform (middle), super-imposed current component (bottom)

B. *Voltage-Restraint Quantity*

The superimposed component appropriately shows the occurrence of the short-circuit fault, considering the high-amplitude waveform during fault condition. However, the load step change may lead to the same waveforms, which may be regarded as a fault condition. This confusion should be avoided by reinforcing the fault detection scheme. To do so, a voltage restraint quantity is employed in this paper in addition to the superimposed components. Fig. 4 shows the voltage-restraint quantity in which a sample voltage waveform with its amplitude is included. In this scheme, the voltage amplitude is

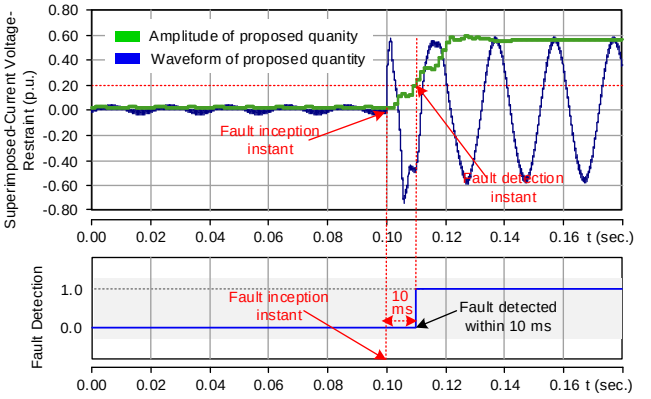

Fig. 5. The proposed superimposed-current voltage-restraint quantity (top), fault detection signal (bottom)

computed using Fast Fourier Transformation (FFT) through a moving window concept. As shown in the bottom waveform of Fig. 4, the restraint quantity is activated when the amplitude of voltage falls below the voltage level of 0.8 p.u., meaning a fault condition. The activation time delay is within a half cycle, which indicates a fast enough operation. Under load step change condition, the voltages barely drop below 0.8 p.u., which guarantees a robust operation of the fault detection method under such conditions.

C. *Fault Detection and Trip Signal Calculation*

The proposed superimposed-current voltage-restraint quantity has a sinusoidal waveform with a high-magnitude during short-circuit fault condition. To extract the fault detection signal, the amplitude of the proposed superimposed phase-current voltage-restraint quantity should be calculated. To do so, the moving window-based FFT analysis is used. Fig. 5 shows waveform and amplitude of the proposed superimposed-current voltage-restraint quantity (top), and the fault detection signal (bottom). As shown in this figure, the fault is detected within a half power cycle.

IV. Simulation Results

To show the effectiveness of the proposed method, different short-circuit fault conditions are analyzed. The details are provided in the following subsections.

A. *Single-Line-to-Ground Short-Circuit Fault Analysis*

Fig. 6 shows the voltage and current waveforms of an inverter under a single-line-to-ground short-circuit fault at PCC point of Fig. 1 (Y-side of YΔ transformer). In this figure, Fig. 6 (a) shows three-phase voltage waveforms of the inverter. The amplitude of the voltages are demonstrated at Fig. 6 (b). Fig. 6 (c) shows the output currents of the inverter, in which the magnitude of the phase with maximum value is limited to maximum value of 1.0 p.u. The superimposed current components and proposed fault detection quantities are depicted in Fig. 7 for phases “a”, “b”, and “c”. As shown in this figure, the value of the proposed quantity is close to zero under normal condition. Under short-circuit fault condition, it considerably increases, which shows the occurrence of short-circuit fault condition. Considering the significant difference between the value of proposed quantity under normal and faulty condition, the fault condition can be distinguished precisely. The trip signals for phases “a”, “b”, “c” are shown in Fig. 8. As shown in this figure, the proposed scheme can detect the fault within the half of one power cycle (10 ms), showing a desirable and fast operation. More case studies will be provided in the final version of the paper.

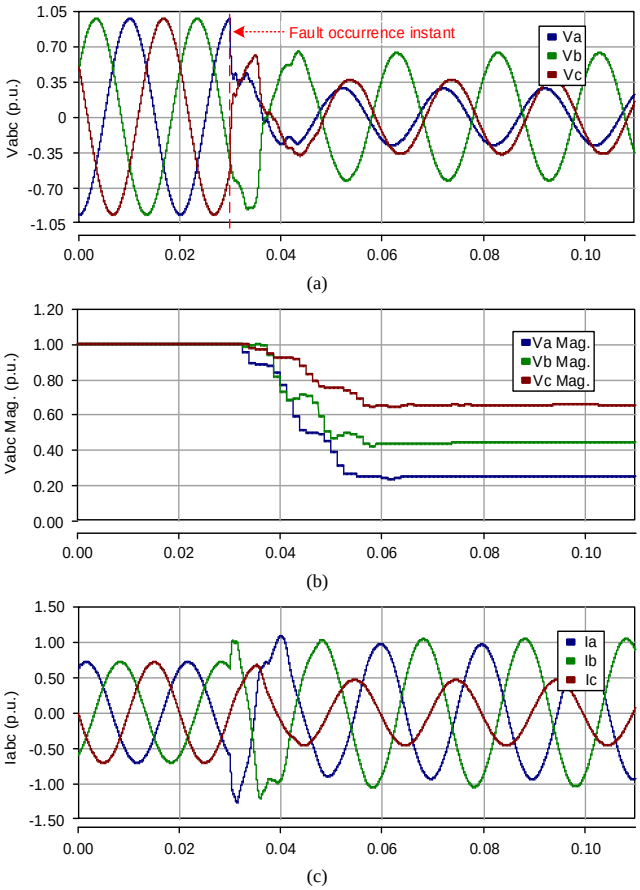

Fig. 6. Voltage and current waveforms of a grid-forming inverter under single-line-to-ground fault condition; (a)- three-phase voltage waveforms, (b)- amplitudes of three-phase voltages, (c)- three-phase current waveforms.

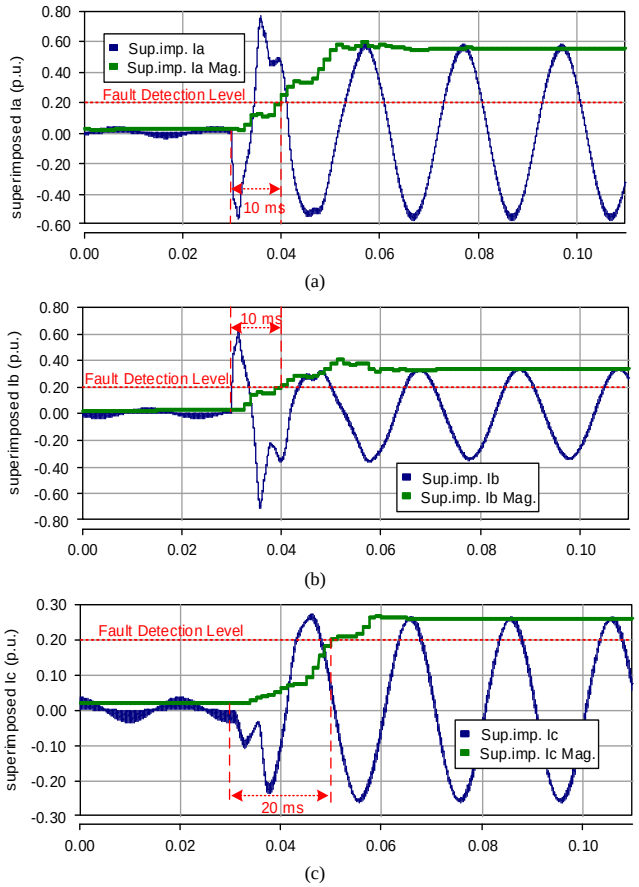

Fig. 7. Superimposed current components and proposed fault detection quantity under a single-line-to-ground short circuit fault; (a)- superimposed component for phase "a" with proposed voltage restraint superimposed quantity, (b)- superimposed component for phase "b" with proposed voltage restraint superimposed quantity, (c)- superimposed component for phase "c" with proposed voltage restraint superimposed quantity. Fault detection level is considered 0.2 p.u.

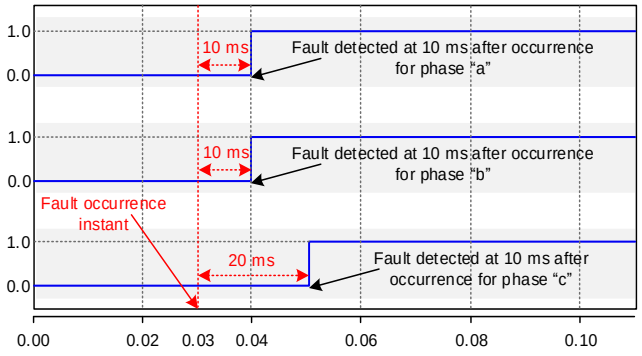

Fig. 8. Trip signal for phases "a", "b", "c"; the fault detected at 10 ms after fault occurrence.

B. *Balanced Three-Phase Short-Circuit Fault Analysis*

Fig. 9 shows the voltage and current waveforms of an inverter under a balanced three-phase short-circuit fault at PCC point of Fig. 1 (Y-side of YΔ transformer). In this figure, Fig. 9 (a) shows three-phase voltage waveforms of the inverter. The amplitude of the voltages are demonstrated at Fig. 9 (b). Fig. 9 (c) shows the output currents of the inverter. As shown in Fig. 9 (c), the magnitude of all three-phases are limited to maximum value of 1.0 p.u. The superimposed current components and proposed fault detection quantities are depicted in Fig. 10 for phases "a", "b", and "c". As shown in this figure, the proposed superimposed quantity considerably increases during short-circuit fault condition. The trip signals for phases "a", "b", "c" are shown in Fig. 11. As shown in this figure, the proposed scheme can detect the fault within the half of one power cycle (10 ms), showing a desirable and fast operation.

V. Conclusion

In this paper, a superimposed phase-current scheme with a voltage-restraint element is proposed which identifies the faults in an islanded microgrid with grid-forming inverters. In the presented work, the state-of-the-art control of grid forming converter is used for short-circuit fault modeling. Furthermore, the moving window concept is included in the proposed scheme, which considerably increases the detection speed. The amplitude of the superimposed phase-current component considerably increases during the fault condition, which provides a reliable criterion for fault detection. Also, voltage-restraint quantity avoids incorrect operation of the relay during load step changes. Different type of fault conditions including single-line-to-ground and balanced faults are analyzed. With refer to the results, the proposed fault detection scheme properly identifies both types of symmetrical/asymmetrical faults within half-cycle (<10msec). Considering the limited fault current of the converter to 1.0 p.u., the proposed method is independent of the magnitude of fault current, which makes it suitable for islanded inverter-based microgrids. The proposed fault detection approach can be included in both conventional and communication-assisted grading schemes for protection coordination purposes.

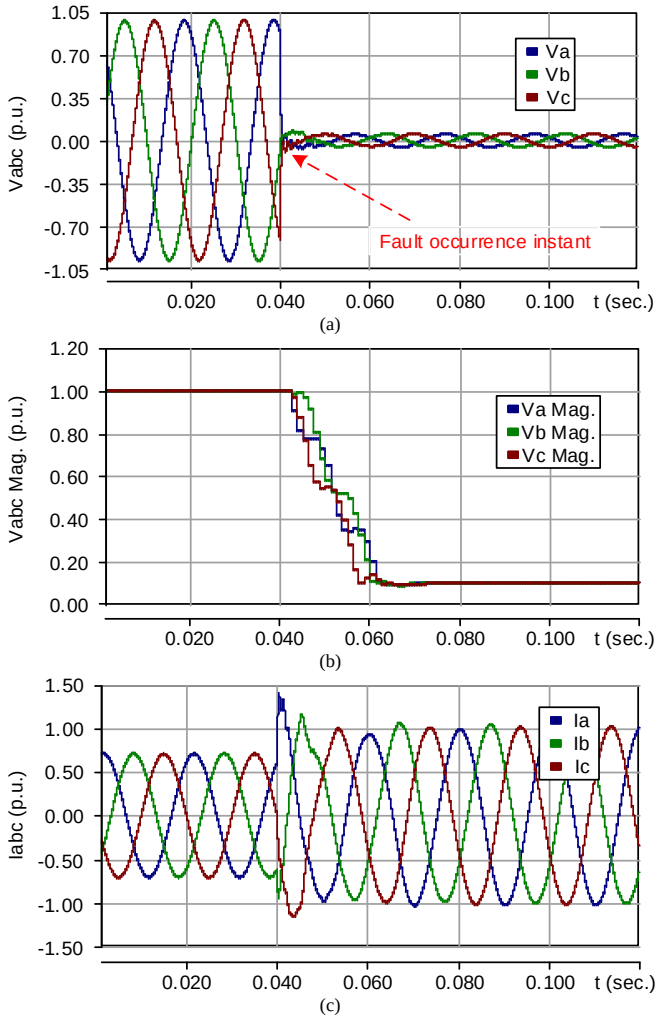

Fig. 9. Voltage and current waveforms of a grid-forming inverter under balanced three-phase short-circuit fault condition; (a)- three-phase voltage waveforms, (b)- amplitudes of three-phase voltages, (c)- three-phase current waveforms.

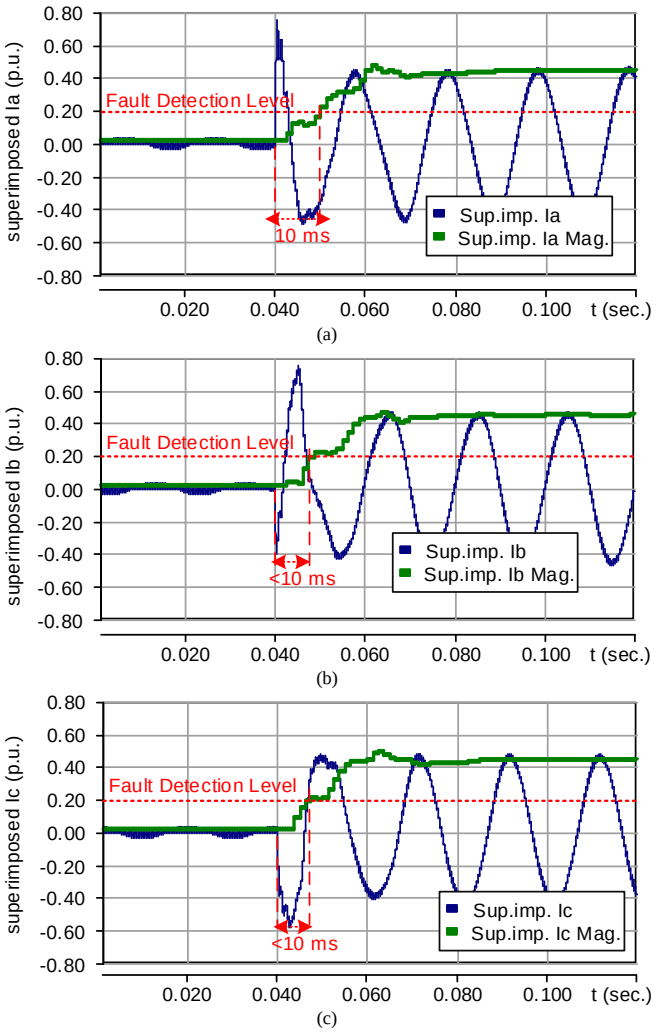

Fig. 10. Superimposed current components and proposed fault detection quantity under a balanced three-phase short circuit fault condition; (a)- superimposed component for phase “a” with proposed voltage restraint superimposed quantity, (b)- superimposed component for phase “b” with proposed voltage restraint superimposed quantity, (c)- superimposed component for phase “c” with proposed voltage restraint superimposed quantity. Fault detection level is considered 0.2 p.u.

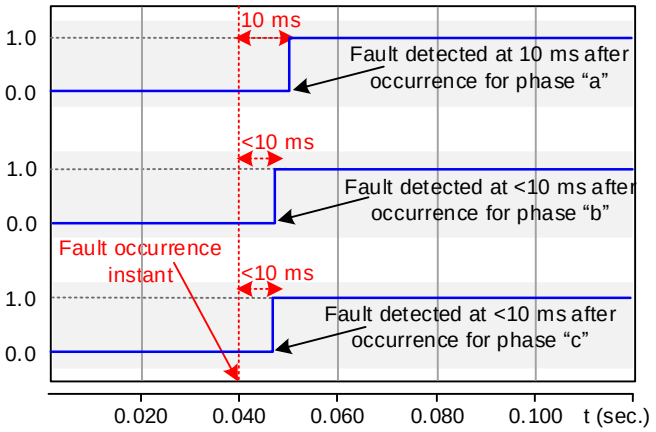

Fig. 11. Trip signal for phases “a”, “b”, “c” under a balanced three-phase short circuit fault condition; the fault detected at <10 ms after fault occurrence.

REFERENCES

[1] A. Dagar, P. Gupta, and V. Niranjan, "Microgrid protection: A comprehensive review," *Renewable and Sustainable Energy Reviews*, vol. 149, p. 111401, 2021.

[2] S. F. Zarei and S. Khankalantary, "Protection of active distribution networks with conventional and inverter-based distributed generators," *International Journal of Electrical Power & Energy Systems*, vol. 129, p. 106746, 2021.

[3] S. F. Zarei, H. Mokhtari, M. A. Ghasemi, and F. Blaabjerg, "Reinforcing Fault Ride Through Capability of Grid Forming Voltage Source Converters Using an Enhanced Voltage Control Scheme," *IEEE Trans. Power Delivery*, doi: 10.1109/TPWRD.2018.2844082, 2018.

[4] S. F. Zarei and M. Parniani, "A Comprehensive Digital Protection Scheme for Low-Voltage Microgrids with Inverter-Based and Conventional Distributed Generations," *IEEE Trans. Power Delivery*, vol. 32, no. 1, pp. 441-452, 2017.

[5] S. F. Zarei, H. Mokhtari, and F. Blaabjerg, "Fault detection and protection strategy for islanded inverter-based microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 472-484, 2019.

[6] P. Patil, A. Badar, and T. P. Hinge, "Application of Linear Programming for Overcurrent Protection," in *2021 International Conference on Intelligent Technologies (CONIT)*, 2021, pp. 1-4.

[7] W. K. Najy, H. H. Zeineldin, and W. L. Woon, "Optimal protection coordination for microgrids with grid-connected and islanded capability," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1668-1677, 2013.

[8] H. Al-Nasseri, M. Redfern, and F. Li, "A voltage based protection for micro-grids containing power electronic converters," in *Proc. of Power Engineering Society General Meeting, IEEE*, 2006, pp. 1-7.

[9] I. Sadeghkhani, M. E. H. Golshan, J. M. Guerrero, and A. Mehrizi-Sani, "A current limiting strategy to improve fault ride-through of inverter interfaced autonomous microgrids," *IEEE Trans. Smart Grid*, vol. 8, no. 5, pp. 2138-2148, 2017.

[10] S. Baloch, S. S. Samsani, and M. S. Muhammad, "Fault Protection in Microgrid Using Wavelet Multiresolution Analysis and Data Mining," *IEEE Access*, 2021.

[11] I. Sadeghkhani, M. E. H. Golshan, A. Mehrizi-Sani, J. M. Guerrero, and A. Ketabi, "Transient Monitoring Function-Based Fault Detection for Inverter-Interfaced Microgrids," *IEEE Trans. Smart Grid*, vol. 9, no. 3, pp. 2097 - 2107, 2016.

[12] A. Anand and S. Affijulla, "Ensemble empirical mode decomposition-based differential protection scheme for islanded and grid-tied AC microgrid," *IET Generation, Transmission & Distribution*, vol. 14, no. 26, pp. 6674-6681, 2021.

[13] H. F. Habib, T. Youssef, M. H. Cintuglu, and O. A. Mohammed, "Multi-Agent-Based Technique for Fault Location, Isolation, and Service Restoration," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 1841-1851, 2017.

[14] M. A. Zamani, T. S. Sidhu, and A. Yazdani, "A protection strategy and microprocessor-based relay for low-voltage microgrids," *IEEE Trans. Power Delivery*, vol. 26, no. 3, pp. 1873-1883, 2011.

[15] E. Casagrande, W. L. Woon, H. H. Zeineldin, and N. H. Kan'an, "Data mining approach to fault detection for isolated inverter-based microgrids," *IET Gener. Transm. Distrib.*, vol. 7, no. 7, pp. 745-754, 2013.

[16] S. F. Zarei, M. A. Ghasemi, S. Peyghami, P. Davari, H. Mokhtari, and F. Blaabjerg, "Characterization of proportional-integral-resonant compensator for DC link voltage control," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2018, pp. 1-8.

[17] S. F. Zarei, H. Mokhtari, M. A. Ghasemi, S. Peyghami, P. Davari, and F. Blaabjerg, "DC-link loop bandwidth selection strategy for grid-connected inverters considering power quality requirements," *International Journal of Electrical Power & Energy Systems*, vol. 119, p. 105879, 2020.

[18] S. F. Zarei, H. Mokhtari, and M. A. Ghasemi, "Enhanced control of grid forming VSCs in a micro-grid system under unbalanced conditions," in *2018 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 2018, pp. 380-385.