Aalborg Universitet

AALBORG UNIVERSITY

Energy Efficiency Enhancement in Full-Bridge PV Inverters with Advanced Modulations

Tang, Zhongting; Sangwongwanich, Ariya; Yang, Yongheng; Blaabjerg, Frede

Published in:
e-Prime: Advances in Electrical Engineering, Electronics and Energy

DOI (link to publication from Publisher):
10.1016/j.prime.2021.100004

Creative Commons License
CC BY 4.0

Publication date:
2021

Document Version
Publisher's PDF, also known as Version of record

Link to publication from Aalborg University

Citation for published version (APA):
Tang, Z., Sangwongwanich, A., Yang, Y., & Blaabjerg, F. (2021). Energy Efficiency Enhancement in Full-Bridge PV Inverters with Advanced Modulations. *e-Prime: Advances in Electrical Engineering, Electronics and Energy*, *1*, Article 100004. https://doi.org/10.1016/j.prime.2021.100004

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

Take down policy
If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

Downloaded from vbn.aau.dk on: December 06, 2025

e-Prime - Advances in Electrical Engineering, Electronics and Energy 1 (2021) 100004

Contents lists available at ScienceDirect

e-Prime - Advances in Electrical Engineering, Electronics and Energy

journal homepage: www.elsevier.com/locate/prime

Energy efficiency enhancement in full-bridge PV inverters with advanced modulations

Zhongting Tang[a], Ariya Sangwongwanich[a], Yongheng Yang[b,*], Frede Blaabjerg[a]

[a] AAU Energy, Aalborg University, Aalborg 9220, Denmark
[b] College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China

A B S T R A C T

Transformerless single-phase inverters are preferring in residential grid-connected PV systems when compared to galvanic-isolated ones (i.e., transformer-based inverters). In addition to the special leakage current issue, high efficiency, power quality and reactive power injection are of concern that should be considered in grid-connected applications. Nowadays, the fast development of wide-bandgap (WBG) devices brings new challenges to transformerless inverters, e.g., electromagnetic interference (EMI) issues, but efficiency can be improved. This paper first reviews the full-bridge PV inverters seen from the perspective of topology configuration. The oscillation during switching transitions is analyzed and compared in typical full-bridge inverters under a hybrid modulation method, which has a significant relationship with the EMI issue. Then, power loss distribution is discussed to reveal the thermal performance under the hybrid modulation scheme with reactive power injection. Simulations are carried out on the full-bridge prototype to validate the discussions of the hybrid modulation strategy.

1. Introduction

As one of the important renewable energy resources, photovoltaic (PV) energy has continued being installed across the globe with an increase of 127 GW in 2020 [1]. Correspondingly, it promotes a relatively fast development of PV panels, power electronics (i.e., including semiconductor devices, topologies and control strategies) as well as the grid-connected standard [2]. To catch up with the large-scale integration of PV energy, PV inverters play an essential role in converting and delivering solar energy to the grid and users. According to the power levels, PV inverters can be classified into three types, including module-level micro-inverters (e.g., residential PV systems) [3], string inverters for medium and high power applications (e.g., offices or industrial PV power systems) [4], and utility-scale central inverters (e.g., PV plants) [5,6]. PV plants require a large area for installation, while low- and medium-power PV systems are preferring and can be built on the rooftops or walls [7]. Referring to single-phase PV inverters in those occasions, the performances in terms of efficiency, power density and system costs as well as intelligence are of concern.

In addition to the inherent intermittency, another unique issue of grid-connected PV systems is the leakage current due to the parasitic capacitor between the PV panels and the ground [8]. Many standards for grid-connected PV systems have strict requirements on the leakage current level, such as the VDE 0126–1–1 and VDE-AR-N4105 from Germany and IEEE Std. 1547–2018 [9–11]. To achieve effective galvanic isolation and then low leakage current, the traditional way is adding a physical device in the single-phase PV inverter, i.e., a high-frequency (HF) transformer on the DC side or a line-frequency transformer (LFT) on the AC side, as shown in Fig. 2. Those transformer-based inverters are contrary to the requirements of small size and low cost. Besides, the demand for high power density is also the reason, why voltage source inverters are more popular than current source inverters [12]. Another way to mitigate this issue is by configuring transformerless single-phase topologies, as shown in Fig. 2(b). The main idea is to clamp the common-mode voltage (CMV) at a constant value through adopting modulation methods or auxiliary circuits [13,14]. Referring to the modulation method, the typical one is the full-bridge single-phase inverter with the bipolar pulse width modulation (BPWM) scheme. With two-voltage levels generation, the switching losses are high, leading to low power density with

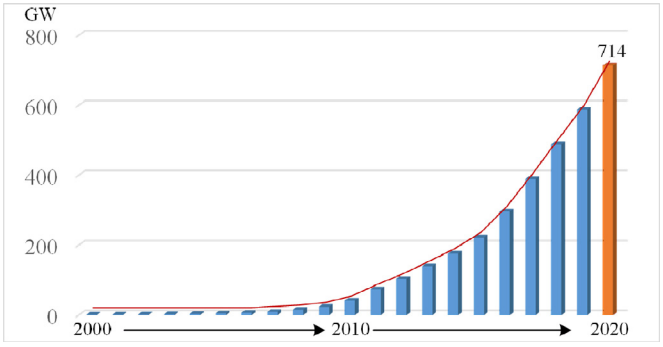

Fig. 1. Solar accumulative capacity from 2000 to 2020 based on the data available from IRENA [1], which includes photovoltaics and solar thermal.

* Corresponding author at: Electrical Engineering, Zhejiang University, Hangzhou, Zhejiang, China.
E-mail addresses: yang_yh@zju.edu.cn, yh.yang@ieee.org (Y. Yang).

https://doi.org/10.1016/j.prime.2021.100004
Received 7 September 2021; Accepted 6 October 2021
2772-6711/© 2021 The Author(s). Published by Elsevier Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/)

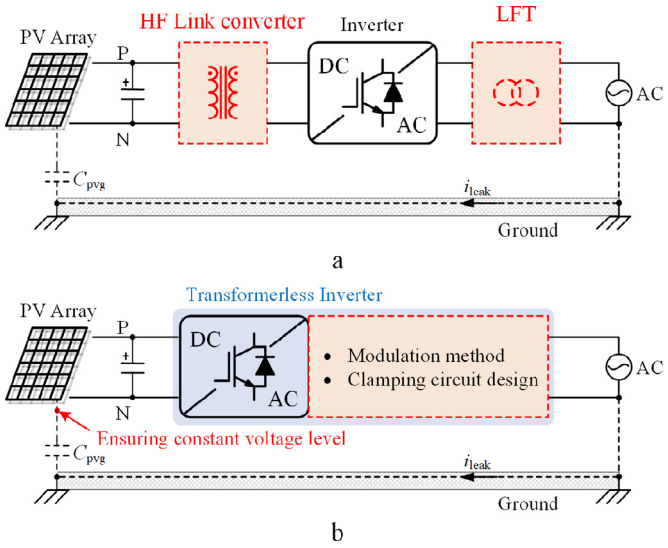

Fig. 2. Inverter structure schemetic, where C_{pvg} is the parasitic capacitor between the PV panels and the gound, and i_{leak} is the leakage current.
a Transformer-based topologies
b Transformerless inverters.

a large size heat sink [15]. As for new topologies, many review papers have explored various transformerless single-phase inverters from the perspective of leakage current suppression [4,13,14,16,17].

Seen from the CMV clamping perspective, transformerless single-phase PV inverters can be classified into two types. One is the common-ground type, and another is the full-bridge type with constant CMV clamping capability. The common-ground configuration is presented in Fig. 3, where the PV panels are connected directly to the grid with the common negative terminal, i.e., the ground. The common-ground transformerless inverters can be separated into two types. That is, the PV voltage V_{PV} is two times the DC-link voltage ($2V_{DC}$) and V_{PV} is equal to V_{DC} [18]. The representative transformerless inverters with $V_{PV} = 2V_{DC}$ are half-bridge inverters, such as the conventional half-bridge inverter [19,20], the multilevel transformerless half-bridge inverter (e.g., T-type, neutral point clamping (NPC) and active neutral-point clamping (ANPC) topologies) [21,22], Karschny inverter [23], and the dual-buck half-bridge inverter in series [24]. While the other ($V_{PV} = V_{DC}$) adopts extra active circuits to meet the voltage modulation requirement, such as virtual DC bus concept inverters [25] and the full-bridge dual-buck inverter [26]. The CMV is effectively clamped by the common-ground configuration of those transformerless inverters. However, the former type requires a high input voltage of the PV panels, and the latter type needs extra active switches as well as passive devices (e.g., capacitors providing virtual DC bus and inductors with low utilization in dual-buck half-bridge inverters). Thus, transformerless single-phase inverters based on symmetrical AC filter inductors with the full-bridge configuration are preferring in terms of high efficiency and high power density. The full-bridge inverters include DC-decoupling transformerless inverters [27–29], AC-decoupling transformerless inverters [31–35], and NPC transformerless inverters [37–46], as shown in Figs. 3(b)-(d), respectively.

Apart from leakage current issues and power density, reactive power injection has also been required in grid-connected PV systems. For instance, in the IEEE Std. 1547–2018, the minimum reactive power injection and absorption in distributed energy systems should be 44% and 25% of the rated apparent power, respectively [11]. Therefore, many modulation schemes have been proposed to enhance the reactive power capability of transformerless inverters, such as the combined modulation method [15]. Considering the performance of conversion efficiency and power quality, the bidirectional-path unipolar pulse width modulation method [47,48], and hybrid modulation techniques [49,50] have also been explored for applications in the above transformerless single-phase inverters.

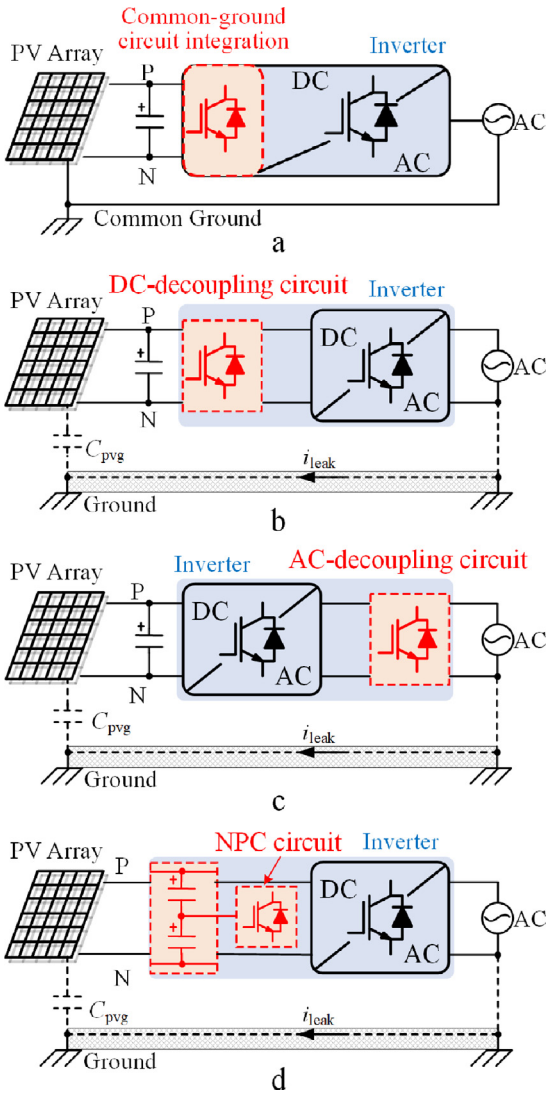

Fig. 3. Single-phase transformerless PV inverter configurations
a Common-ground type
b DC-decoupling type
c AC-decoupling type
d NPC circuit type.

However, there are very few review papers comparing the commutation oscillation performance induced by parasitic parameters, and loss distribution under the advanced hybrid modulation method. With the fast development of wide-bandgap (WBG) devices, e.g., silicon carbide (SiC) and gallium-nitride (GaN) power devices, the challenge of electromagnetic interference (EMI) issues (i.e., due to the parasitic oscillation) increase with their advanced switching performance (i.e., high switching speed) [51,52]. Another important aspect for PV inverters is the reliability-related system cost, where losses unbalance issues of the power devices play an important role. Consequently, this paper reviews the full-bridge PV inverters under the prior-art hybrid modulation schemes with reactive power injection from the two issues in Sections 2 and 3. In Section 4, an instructive discussion is presented for the design of residential transformerless PV inverters. Section 5 demonstrates the hybrid modulation method on the full-bridge inverter, which validates the discussions of the loss distribution. Finally, the conclusion is given in Section 6.

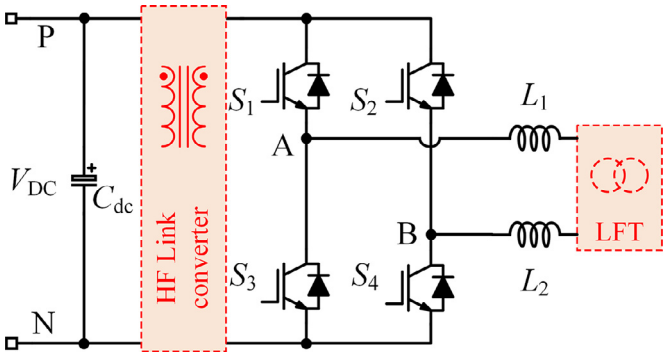

Fig. 4. Full-bridge inverter.

2. Review of full-bridge PV inverters

As mentioned previously, full-bridge single-phase PV inverters have better performance of power density due to their split symmetrical AC inductors structure. The full-bridge PV inverters discussed in this paper can be separated into four groups.

1) Transformer-based type: Transformer-based single-phase inverters always have two configurations, including the one with a DC-DC converter of a high-frequency transformer and the one with a low-frequency transformer, as shown in Fig. 2(a). Both have a full-bridge inverter with four semiconductor devices (e.g., IGBTs and MOSFETs), as shown as S_{1-4} in Fig. 4. Besides, the symmetrical AC filter inductors are L_1 and L_2, which are the same in all the following figures. With the transformer, a unipolar pulse width modulation (UPWM) scheme can be adopted in the full-bridge inverter to achieve galvanic isolation, small AC filter inductors, and reactive power injection. Otherwise, the full-bridge inverter must adopt the BPWM to ensure a constant CMV.
2) DC-decoupling type: As shown in Fig. 3(b), the DC-decoupling transformerless single-phase inverters employ an extra circuit at the DC bus, which can decouple the PV panels and the AC side during the freewheeling period (i.e., zero output voltage). The well-known DC-decoupling transformerless inverter is the H5 inverter [27]. As shown in Fig. 5(a), an active blocking switch can be inserted at the positive/negative rail of the DC bus. However, the blocking switch S_5 has two times more switching losses than others. Thus, the H6 DC-decoupling transformerless inverter adopts two blocking switches to share the switching losses, as shown in Fig. 5(b). The symmetrical blocking switches S_5 and S_6 can share the switching losses, yet increase the conduction losses since the current needs flow through four switches in the conduction period [28]. To improve this issue, advanced H6 transformerless DC-decoupling inverters adopt a bypass switch on the H5 topology [29,30]. As presented in Fig. 5(c), the bypass switch S_6 can be connected to terminals A, B, or C. That is the so-called redundant design to share the switching losses by extra switches.
3) AC-decoupling type: The AC-decoupling transformerless inverters add the decoupling circuit at the AC side port, as presented in Fig. 3(c). In [31], the derivation method of H6 AC-decoupling type inverters was presented, where the main structure is embedding an AC-decoupling circuit in the mid-point of the full-bridge cell for bidirectional freewheeling paths. For instance, Fig. 6(a) shows symmetrical H6 transformerless inverters [32,33], which have different structures, but similar modulation and CMV performances. Furthermore, a hybrid-bridge H6 inverter (see Fig. 6(b)) can be derived accordingly [34], where the AC-decoupling circuit only inserts in one leg of the full-bridge inverter. To realize bidirectional freewheeling by two active switches, a mid-switch H6-type inverter was proposed in [35], as depicted in Fig. 6(c). It can be seen from Figs. 6(a)-(c) that when the AC-decoupling circuit is inserted in the branches of the full-bridge inverter, the conduction losses are relatively increased. To alleviate this issue, the highly efficient and reliable inverter concept (HERIC) adopts two active switches as the AC-decoupling circuit [36], as presented in Fig. 6(d). As for the HERIC topology, the AC-decoupling circuit has various configurations, such as two active switches with two diodes, two active switches, and one active switch with a rectifier bridge [4]. By comparison, the HERIC inverter with two anti-series-connected active switches has good performance in terms of fewer power devices and higher efficiency.
4) Neutral Point Clamping (NPC) type: Being different from the physical switch (e.g., relay), the semiconductor devices exist switch junction capacitors, which have an unexpected impact on the leakage

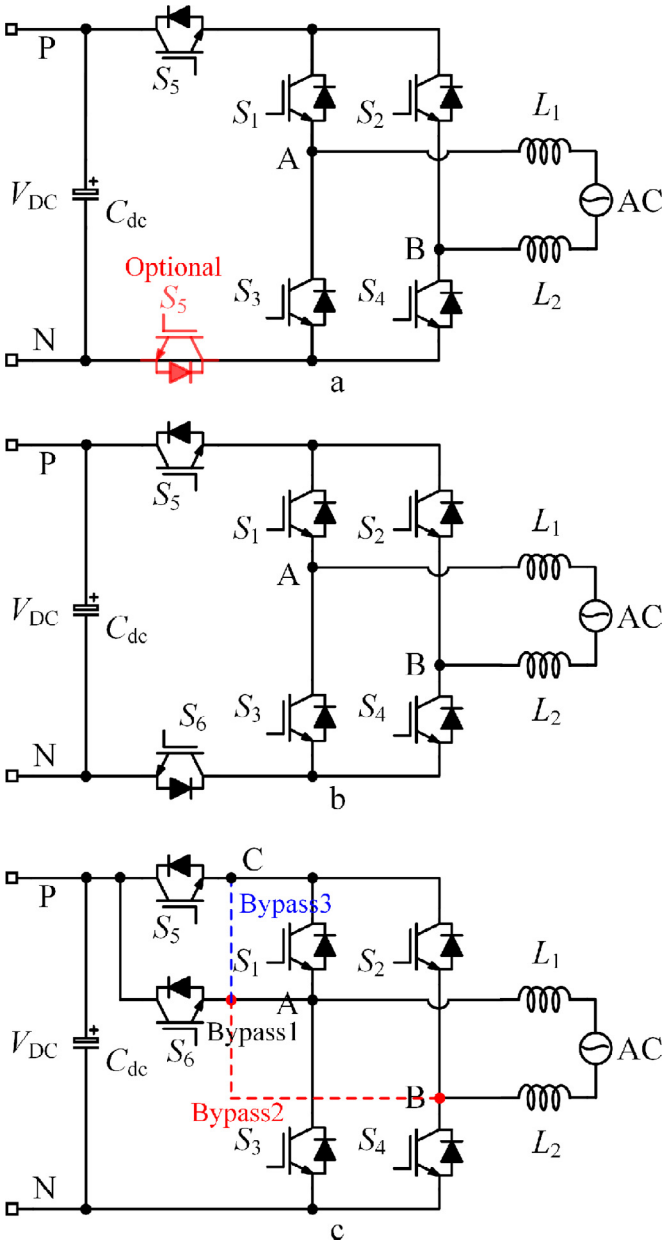

Fig. 5. DC-decoupling inverters
a H5 topology [27]
b H6-DC-decoupling topology [28]
c H6-bypass topologies [29,30], where there are three bypass ways, i.e., the bypass1is setting S_6 between terminals P and A, the bypass2 is placing S_6 between terminals P and B, and the bypass3 is locating S_6 between terminals P and C.

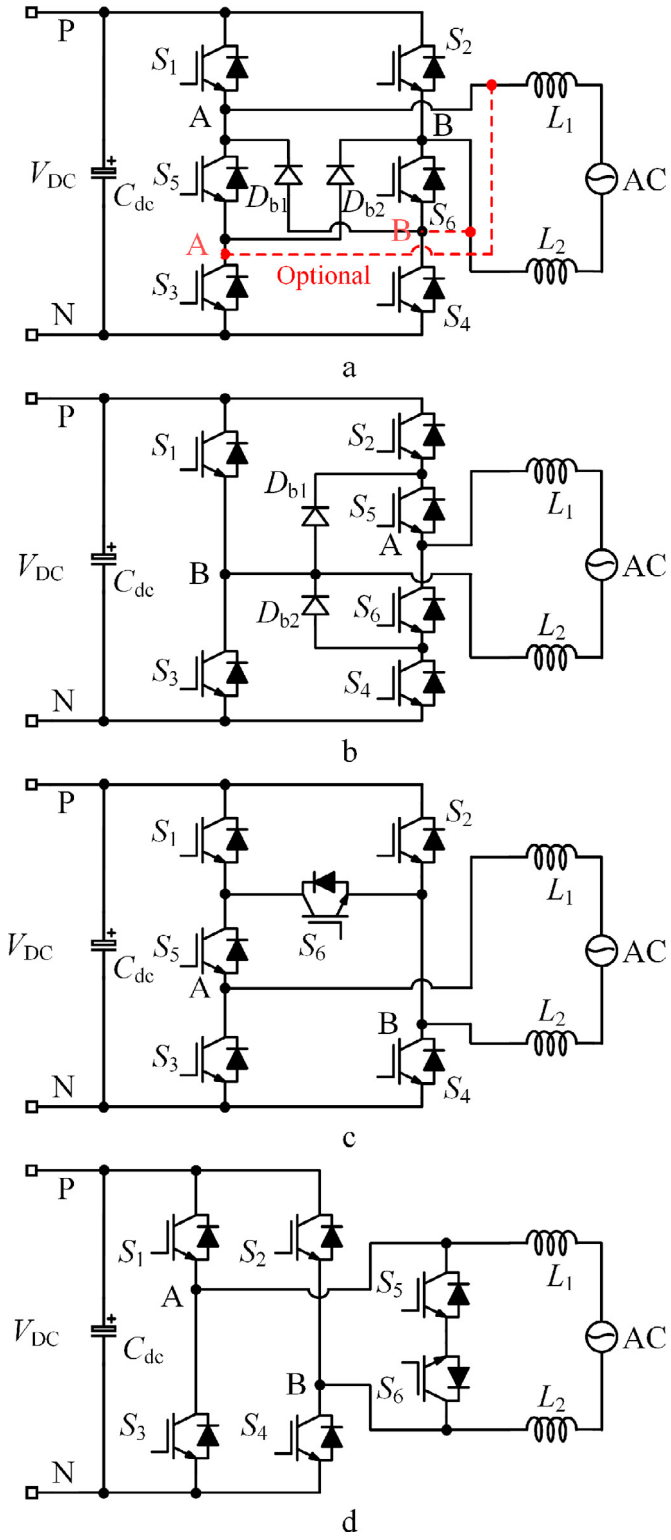

Fig. 6. AC-decoupling inverters
a H6-AC-decoupling topologies [32,33], where the circuit branches can also be embedded as indicated by the red line.
b Hybrid-bridge H6 topology [34]
c Mid-switch H6 topology [35]
d HERIC topology [36].

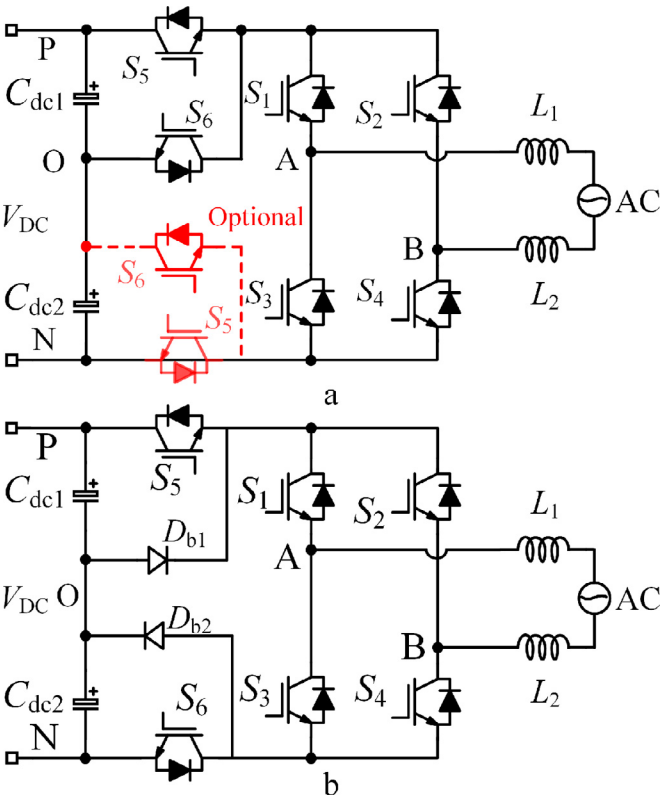

Fig. 7. DC-decoupling NPC inverters
a O–H5 topology [41], where S_5 and S_6 can be set at both the positive/negative DC-links
b H6-DC-decoupling NPC topology [43].

current performance [4,8]. For instance, [4] and [42] analyzed the inherent leakage current caused by the junction capacitors in the H5 inverter. The asymmetrical structure of the H5 topology cannot maintain a constant CMV, especially in high-power inverters with high-speed switching devices. Therefore, the NPC type inverters have been proposed to achieve a constant CMV by the capacitor clamping circuit, as shown in Fig. 3(d) [37–40]. The methodology of NPC topologies is to clamp the CMV to be half of the DC-link voltage during the freewheeling period, which can be easily built based on the DC/AC-decoupling inverters. Fig. 7 exhibits the DC-decoupling NPC transformerless topologies. The O–H5 topology has two structures, where S_5 and S_6 can be inserted in both the positive and negative rails, as shown in Fig. 7(a) [41]. In [42], an H5-D topology was proposed, which only uses a diode to provide NPC function, and S_5 is on the negative DC rail. The CMV clamping performance is worse than that for the O–H5 topologies (i.e., with active clamping). In addition, a diode bidirectional NPC circuit was adopted in the H6-DC-decoupling inverter, as depicted in Fig. 7(b) [43].

As for AC-decoupling NPC inverters, four typical topologies are exemplified in Fig. 8. Fig. 8(a) shows the H6-AC-decoupling NPC inverters, where an active switch connects the AC-decoupling circuit to the neutral point of the series capacitors. The diode bidirectional NPC circuit was added in the hybrid-bridge H6 inverter in [38], as shown in Fig. 8(b). Besides, the mid-switch H6 NPC topology was introduced, as shown in Fig. 8(c), which has relatively high efficiency. Based on the HERIC inverter, many NPC single-phase transformerless inverters have been proposed, such as the active voltage clamping HERIC (AVC–HERIC) topology (i.e., in Fig. 8(d)) [44], H-bridge zero-voltage state (HB-ZVR) topology [45], and full-bridge constant common-mode voltage (FB-CCV) [46].

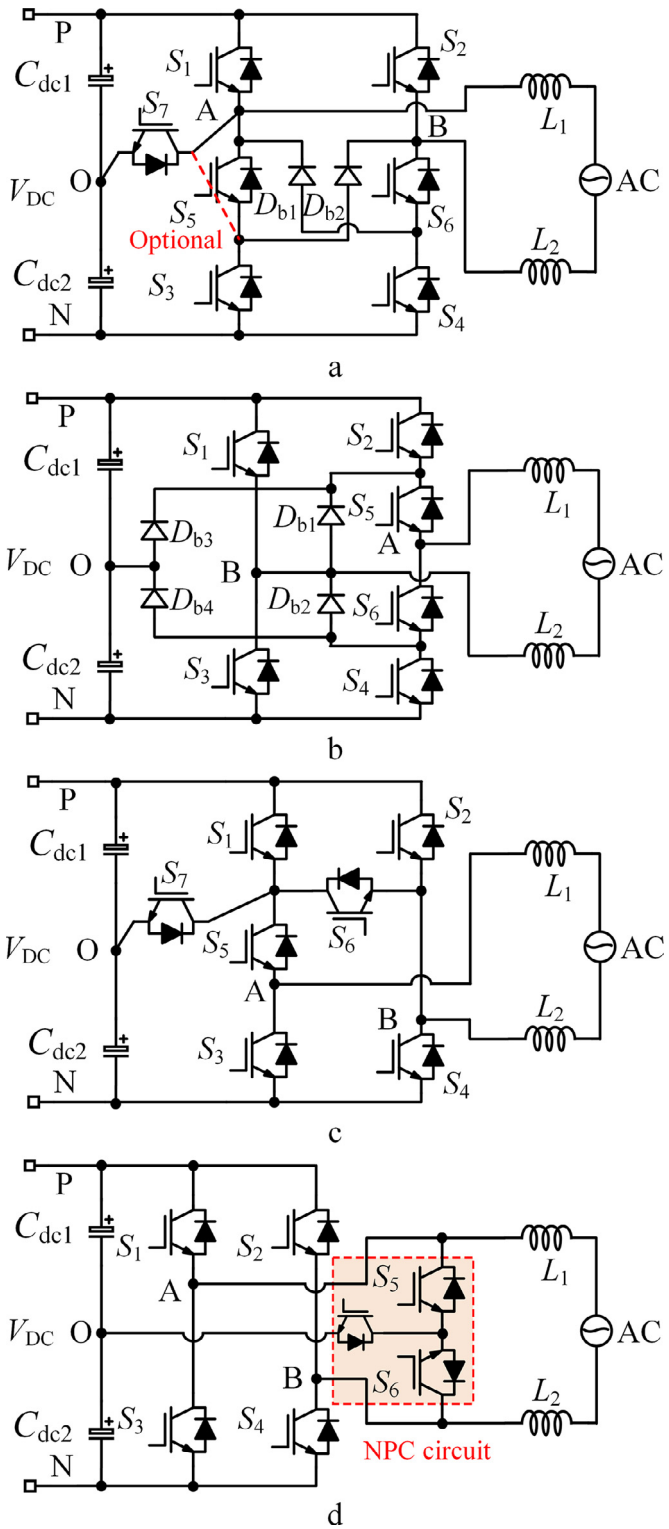

Fig. 8. AC-decoupling NPC inverters
a H6-AC-decoupling NPC topologies, where the red line shows the optional connection
b Hybrid-bridge NPC topology [38]
c Mid-switch H6 NPC topology [38]
d AVC–HERIC topology [44].

The above classification of PV inverters is based on the leakage current suppression schemes. In addition, many review papers have carried out various comparisons and analyses combined with the performance of efficiency and device count. It can be seen in [37,38] that the NPC topologies have the best CMV clamping characteristic, the HERIC inverter has the highest efficiency, and the H5 has the least device count. However, commutation oscillation and loss distribution issues, which have a close relationship with power density, are barely focused on. When the operation modes of inverters commute at a switching frequency, the parasitic inductor and capacitor in the current loop will generate high-frequency oscillation. The different parasitic parameters in different current loops lead to multi-frequency oscillation during the mode transitions (i.e., serious oscillation performance). In practice, many standards have strict EMI requirements (e.g., the Standard EN-61,800–3 has requirements for the main terminals disturbance voltage in the frequency band 150 kHz–30 MHz) [53,54], thus huge EMI filters should be added under the serious oscillation performance. On the other hand, the heat sink should be designed property to cool down the hottest component [55,56]. Therefore, the loss balance of switches in a converter can benefit the heatsink design and improve the lifetime of the entire PV inverters. This paper will discuss the parasitic oscillation and loss distribution performance of several typical single-phase PV inverters under the hybrid UPWM method with reactive power injection [48].

3. Parasitic oscillation and loss analysis

To meet the requirement of reactive power regulation, high efficiency, and high power quality, [48] summarized the hybrid UPWM scheme for various single-phase grid-connected transformerless PV inverters. With this modulation method, the parasitic oscillation and loss distribution performances are different for the above transformerless single-phase inverters [57,58]. Since the NPC topologies are almost based on the DC/AC decoupling topologies, the full-bridge inverter, H5 topology, H6-DC-decoupling topology, one H6-AC-decoupling topology, the mid-switch H6 topology, and HERIC topology are chosen to analyze and compare in this paper. Since the parasitic oscillation and loss distribution are analyzed under the modulation method, the DC-link voltage V_{DC} is assumed to be constant. Besides, a simple PR current controller is adopted to generate the duty cycle ratio, which is used in the hybrid modulation method [59]. To better benchmark the parasitic oscillation, the analysis only considers the parasitic parameters of the semiconductor devices. That means the parasitic inductances on the printed circuit boards (PCB) layout are assumed to be the same among the selected topologies.

3.1. Full-bridge inverter

Fig. 9 shows the full-bridge inverter with parasitic inductors, where $L_{\sigma 1\text{–}4}$ represents the parasitic inductances of the switches $S_{1\text{–}4}$ and $L_{\sigma 1\text{–}4}$ are assumed to be identical. The hybrid UPWM scheme is presented in Fig. 10, where its loss distribution is also shown. When the reference voltage $v_{ref} > 0$, S_1 is ON, S_3 is OFF, and S_2 and S_4 commute at the switching frequency. While $v_{ref} < 0$, S_3 is ON, S_1 is OFF, and S_2 and S_4 switch at the same high frequency. Since S_1 and S_3 operate at the grid frequency (i.e., 50/60 Hz) and S_2 and S_4 work at the switching frequency (i.e., being above tens kHz), the switching losses are almost distributed on S_2 and S_4, as the gray part in Fig. 10. As for conduction losses [60], the total losses on $S_{1\text{–}4}$ are the same, yet being unbalanced and distributed on IGBTs and diodes under different power factor angles φ.

According to the hybrid modulation scheme, the loop commutations in the positive and negative half-cycles are almost the same. Taking the positive half cycle for example, Fig. 11 presents the equivalent circuit with parasitic inductances of the full-bridge inverter, which includes two commutation modes. The total loop inductance in '+ V_{DC}' mode and '0'

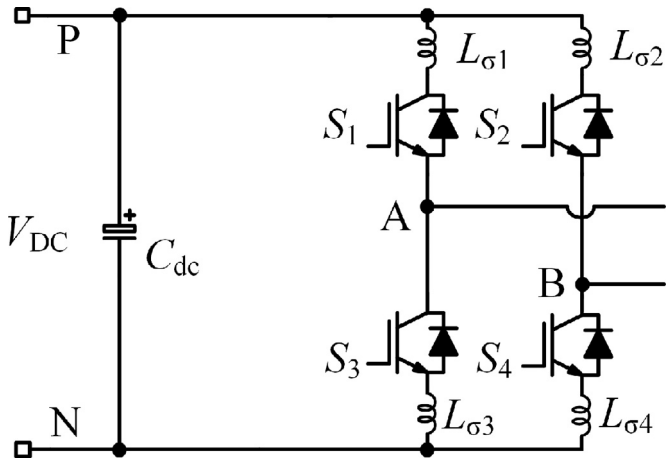

Fig. 9. Full-bridge inverter-equivalent circuit with parasitic inductances, where $L_{\sigma1-4}$ are the parasitic inductances of switches S_{1-4}.

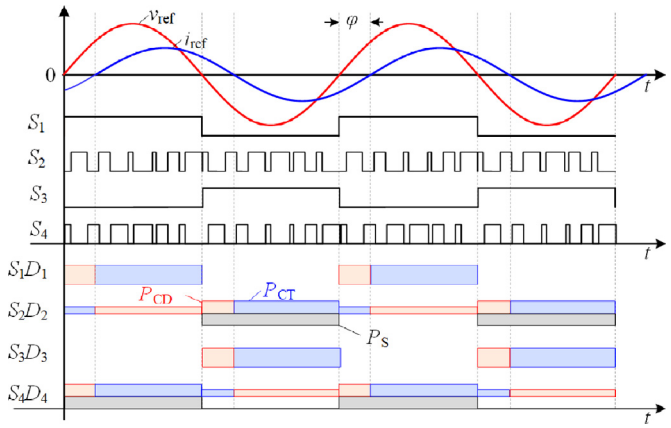

Fig. 10. Full-bridge inverter-hybrid modulation scheme and loss distribution, where P_{CD} and P_{CT} are the conduction losses of the anti-parallel diode and the IGBT, respectively, and P_S is the switching losses, v_{ref}, i_{ref} are the reference voltage and current for modulation signals, φ is the power factor angle. When outputting positive power, the conduction losses are almost on IGBT, which the conduction losses are on diodes during negative power generating.

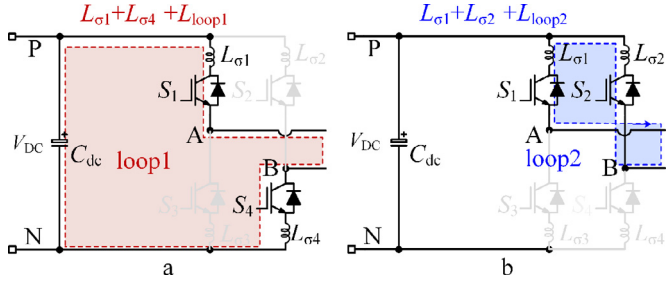

Fig. 11. Full-bridge inverter-operation commutation modes in the positive half-cycle, where L_{loop1} and L_{loop2} are the PCB routing inductances
a '+ V_{DC}' mode
b '0' mode.

mode can be given as

$$L_{+VDC\_FB} = L_{\sigma1} + L_{\sigma4} + L_{loop1} \tag{1}$$

$$L_{0\_FB} = L_{\sigma1} + L_{\sigma2} + L_{loop2} \tag{2}$$

Along with the semiconductor device output capacitor, high-frequency oscillations will be generated. When the loop inductances are

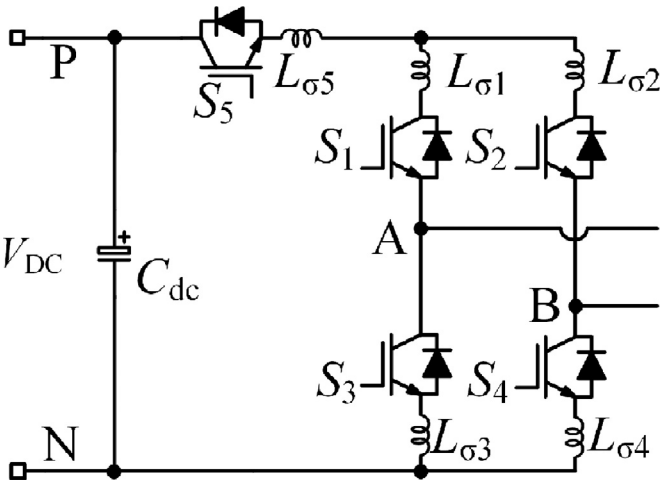

Fig. 12. H5 inverter-equivalent circuit with parasitic inductances, where $L_{\sigma1-5}$ are the parasitic inductances of switches S_{1-5}.

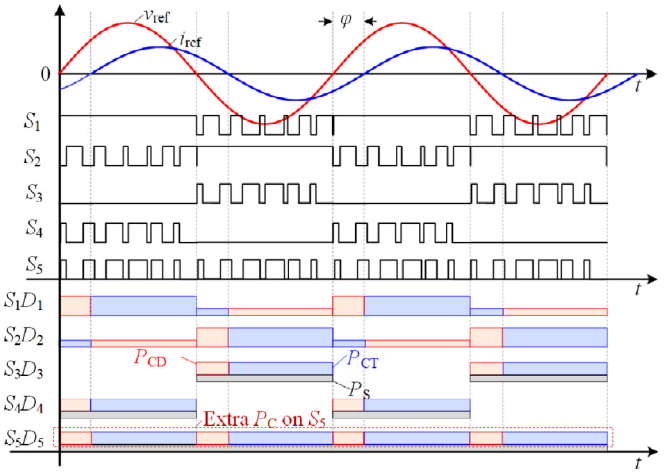

Fig. 13. H5 inverter-modulation scheme and loss distribution.

unbalanced in those two commutation modes, the oscillations have two frequencies. In that case, it will increase the design burden on the EMI filter [61]. It can be revealed from Eqs. (1) and (2) that the oscillation frequencies are almost the same in the full-bridge inverter under the hybrid modulation method if the PCB layout design can ensure the symmetry of the loop inductances, i.e., $L_{loop1} = L_{loop2}$. It should be mentioned that although only S_1 is ON in the deadtime during the mode transition, the current loop is the same as the '0' mode. Thus, the loop inductance of the deadtime period has not been further discussed.

3.2. H5 inverter topology

The equivalent circuit of the H5 topology with the parasitic inductances is shown in Fig. 12, which adopts an active switch S_5 at the positive DC-link rail to disconnect the DC side and the AC side. The improved hybrid UPWM method with reactive power injection is shown in Fig. 13 [47]. At the positive half-cycle, S_1 is ON, and S_2 and $S_{4,5}$ complementarily switch at a high frequency, generating a two-level voltage of + V_{DC} and 0. At the negative half-cycle, S_2 is ON, and S_1 and $S_{3,5}$ commutate at the switching frequency, obtaining a two-level voltage of – V_{DC} and 0. Correspondingly, loss distribution is presented at the lower part of Fig. 13, where S_5 has high conduction losses and switching losses due to its long operation time. From the thermal analysis, S_5 is the most fragile component in the H5 inverter [62,63].

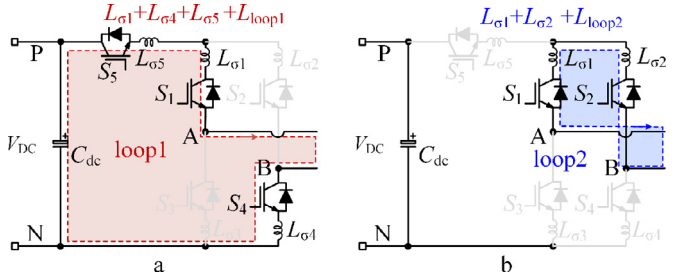

Fig. 14. H5 inverter-commutation modes in the positive half-cycle, where L_{loop1} and L_{loop2} are the PCB routing inductances
a '+ V_{DC}' mode
b '0' mode.

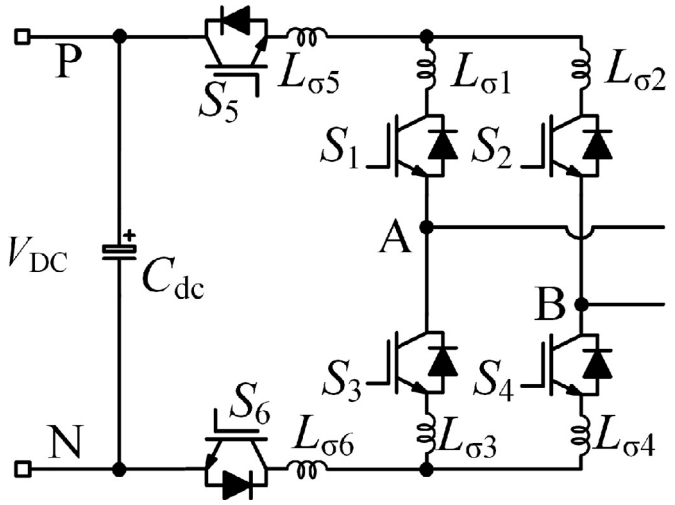

Fig. 15. H6-DC-decoupling inverter-equivalent circuit with parasitic inductances, where $L_{\sigma1-6}$ are the parasitic inductances of switches S_{1-6}.

Similarly, the commutation operation modes of the H5 topology in the positive half-cycle are shown in Fig. 14, which consider the parasitic inductances. The loop inductances of both the operation modes can be expressed as

$$L_{+VDC\_H5} = L_{\sigma1} + L_{\sigma4} + L_{\sigma5} + L_{loop1} \tag{3}$$

$$L_{0\_H5} = L_{\sigma1} + L_{\sigma2} + L_{loop2} \tag{4}$$

which can illustrate that the loop inductance of the '+ V_{DC}' mode (i.e., see Fig. 14(a)) is larger than that of the '0' mode (i.e., see Fig. 14(b)). The EMI filter for the H5 inverter should be designed to suppress the oscillation in a large range of frequencies, which means a larger volume and a higher cost. When compared to the symmetrical full-bridge inverter, the volume of the heatsink and the EMI filter increase although the transformer is removed.

3.3. H6 DC-decoupling topology

As mentioned in Section 2, the H6 DC-decoupling topology adopts two additional active switches on the DC rails to distribute the switching losses. Compared to the H5 topology, it benefits the thermal design of the PCB and the lifetime of the entire inverter [28]. The equivalent schematic of the H6 DC-decoupling inverter with parasitic parameters is shown in Fig. 15, where DC-decoupling switches S_5 and S_6 are set at the positive and negative DC rails, respectively. The improved hybrid modulation with reactive power injection has been discussed for the H6 DC-decoupling in [28,48], as shown in Fig. 16. During the positive half-cycle, S_1 is in ON-state, and S_2 and S_{4-6} complementarily change at

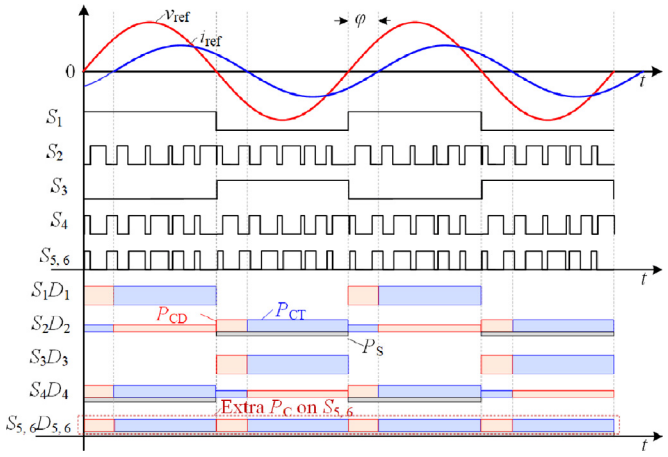

Fig. 16. H6-DC-decoupling inverter-modulation method and loss distribution.

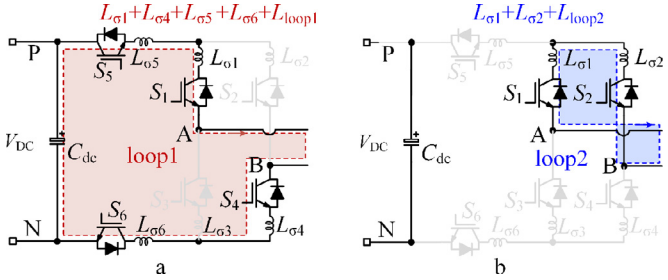

Fig. 17. H6-DC-decoupling inverter-operation modes in the positive half-cycle
a '+ V_{DC}' mode
b '0' mode.

the switching frequency. While at the negative half-cycle, S_3 is ON, and S_4 and $S_{2,5,6}$ are commutating at the same high frequency. Although the structure is fully symmetrical, the junction capacitances of switches will affect the leakage current with the hybrid UPWM method, where the detail has been analyzed in [28]. As for the loss distribution, the extra switch S_6 on the negative rail increases the conduction losses, yet shares the switching losses with S_5.

According to the fully symmetrical structure and the modulation scheme in Fig. 16, the oscillation performance of the H6 DC-decoupling inverter is the same at both the positive and negative half-cycles. Fig. 17 presents the commutation modes in positive half-cycle, where the loop inductances at the '+ V_{DC}' mode (i.e., Fig. 17(a)) and '0' mode (i.e., Fig. 17(b)) can be given as

$$L_{+VDC\_H6DC} = L_{\sigma1} + L_{\sigma4} + L_{\sigma5} + L_{\sigma6} + L_{loop1} \tag{5}$$

$$L_{0\_H6DC} = L_{\sigma1} + L_{\sigma2} + L_{loop2} \tag{6}$$

which reveals that the parasitic inductances of switches in Loop 1 are doubled compared to that in Loop 2. That is, the oscillation frequency is larger than the H5 topology.

It should be noted that the modulation method for H6-DC-decoupling NPC topology in [43] has a higher efficiency than the improved modulation scheme in Fig. 16 [28]. In [43], all the switches of the full-bridge part (i.e., S_{1-4}) are turned on during the freewheeling period, achieving two freewheeling current paths (i.e., low conduction losses) and eliminating the influence of the unbalanced junction capacitances.

3.4. H6-AC-decoupling topology

Fig. 18 shows the topology of one typical H6-AC-decoupling inverter, where the structure is symmetrical. Two extra diodes D_{b1} and D_{b2} are

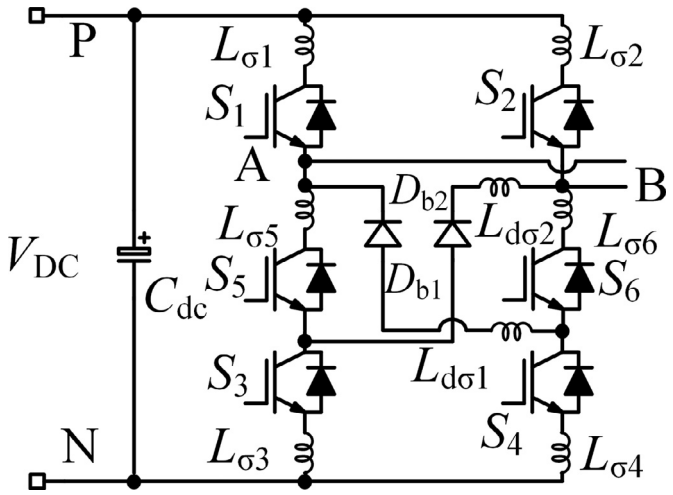

Fig. 18. One typical H6-AC-decoulping inverter-equivalent circuit with parasitic inductances, where $L_{\sigma1-6}$ are the parasitic inductances of switches S_{1-6}, and $L_{d\sigma1}$ and $L_{d\sigma2}$ are the parasitic inductances of diodes D_{b1} and D_{b2}.

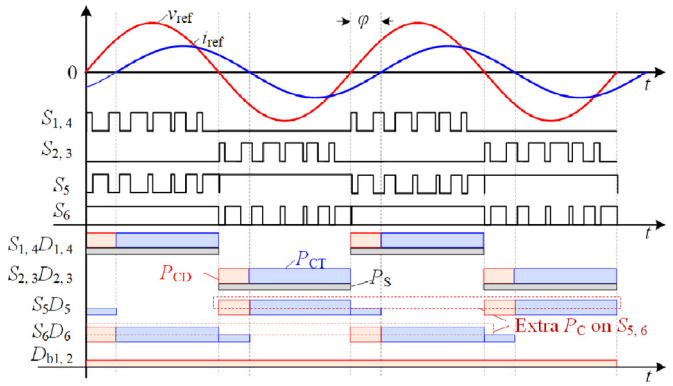

Fig. 19. H6-AC-decoupling inverter-modulation scheme and loss distribution.

added in the middle of the two bridge-legs along with S_5 and S_6, providing the freewheeling path and the AC-decoupling. Although the H6-AC-decoupling has an improved performance in leakage current suppression, the conversion efficiency is compromised since the current should flow through the two more extra active switches S_5 and S_6 [32,33]. The hybrid modulation method with reactive power injection applied in the H6-AC-decoupling inverter is detailed in Fig. 19. The switch S_6 is ON in the positive half-cycle, and $S_{1,4}$ and S_5 are changing in the switching frequency to generate the modulation voltage of + V_{DC} and 0. On the contrary, S_5 is in ON state in the negative half-cycle, and $S_{2,3}$ and S_6 switch at a high frequency, achieving the output voltage of – V_{DC} and 0. Since both S_5 and S_6 are ON in the freewheeling period, the hybrid modulation method can enable the bidirectional current path (i.e., reactive power injection). It can be seen from Fig. 19 that S_5 and S_6 have extra conduction losses, but the loss distribution is balanced in S_5 and S_6.

The H6-AC-decoupling topology in Fig. 18 has a symmetrical structure. Therefore, the commutation oscillation performances in the positive and negative half-cycles are the same, where Fig. 20(a) and (b) show the switching modes of '+ V_{DC}' and '0', respectively. Correspondingly, the loop inductors in those two modes can be expressed as

$$L_{+VDC\_H6AC} = L_{\sigma1} + L_{\sigma4} + L_{\sigma5} + L_{loop1} \tag{7}$$

$$L_{0\_H6AC} = L_{d\sigma2} + L_{\sigma6} + L_{loop2} \tag{8}$$

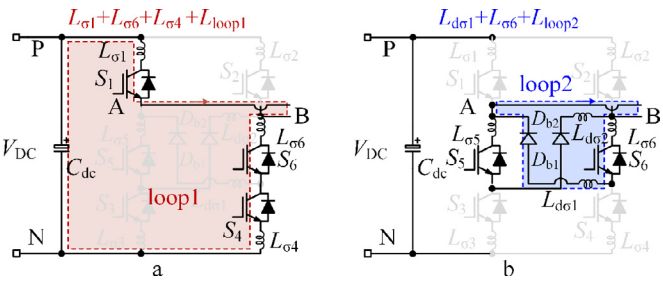

Fig. 20. H6-AC-decoupling inverter-commutation modes, where L_{loop1} and L_{loop2} are the PCB routing inductances
a '+ V_{DC}' mode
b '0' mode.

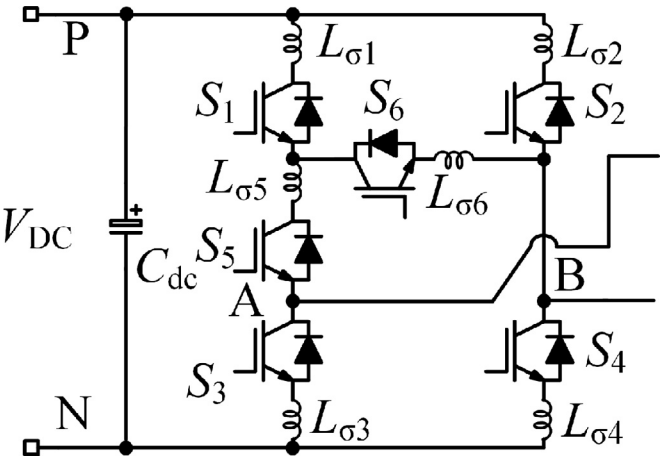

Fig. 21. Hybrid-bridge H6 inverter-equivalent circuit with parasitic inductances, where $L_{\sigma1-6}$ are the parasitic inductances of switches S_{1-6}.

where the parasitic inductor of diodes D_{b1} and D_{b2} are equal, i.e., $L_{d\sigma1} = L_{d\sigma2}$. Compared the loop inductors in Eqs. (7) and (8) with that of the H5 topology, they are almost similar if $L_{d\sigma1,2}$ are equal to $L_{\sigma1-6}$. However, the H6-AC-decoupling inverter has better performance in loss distribution.

3.5. Hybrid-bridge H6 topology

The hybrid-bridge H6 topology provides a bidirectional freewheeling path with two asymmetrical active switches, as shown in Fig. 21. As presented in Fig. 21, one additional switch is set on one bridge-leg, while another is connecting the negative terminals of both two upper switches of the bridge-legs. Compared with the H6-bypass topology in Fig. 5(c) [30], the hybrid-bridge H6 inverter has higher efficiency since the current only flows through two switches during the negative half-cycle. Fig. 22 shows the hybrid modulation method with reactive power injection. In the positive half-cycle, S_5 is ON, and $S_{1,4}$ and S_6 commutate at the switching frequency. In the negative half-cycle, S_6 is in ON-state, and $S_{2,3}$ and S_5 complementarily switch at the same high frequency. In that case, the hybrid-bridge H6 inverter can achieve three-level voltages, i.e., + V_{DC}, 0, and – V_{DC}. As depicted in Fig. 22, S_6 is ON during the negative half-cycle, and yet, there is no current flowing through S_6 during the '+ V_{DC}' mode. Therefore, the losses on S_5 and S_6 are unbalanced although the conduction losses are relatively less than the H6-bypass topology in Fig. 5(c) and the H6-AC-decoupling topology in Fig. 6(a).

Due to the asymmetrical structure, the oscillation performances in positive and negative half-cycles are different, Figs. 23(a)-(c) show the commutation modes of '+ V_{DC}', '0', and – 'V_{DC}', respectively. Accordingly, the loop inductances in each mode can be calculated by

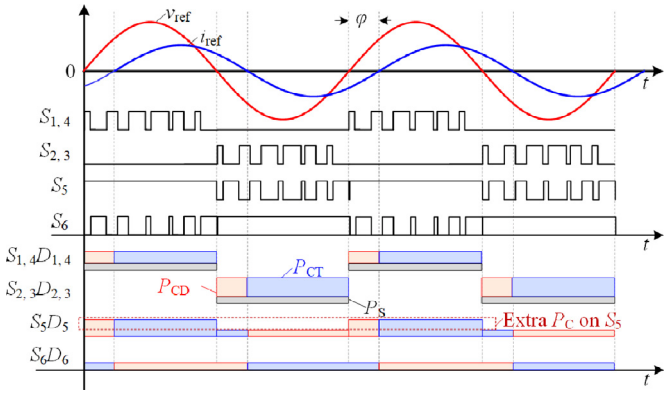

Fig. 22. Hybrid-bridge H6 inverter-modulation scheme and loss distribution.

$$L_{+VDC\_HB} = L_{\sigma 1} + L_{\sigma 4} + L_{\sigma 5} + L_{loop1} \tag{9}$$

$$L_{0\_HB} = L_{\sigma 5} + L_{\sigma 6} + L_{loop2} \tag{10}$$

$$L_{-VDC\_HB} = L_{\sigma 2} + L_{\sigma 3} + L_{loop3} \tag{11}$$

Since the parasitic inductances of switches and loop inductances are assumed to be the same, the oscillation frequency of the hybrid-bridge H6 inverter in positive half-cycle is similar to that of the H5 topology, while being the same as the oscillation performance of the full-bridge inverter in the negative half-cycle. In a word, the hybrid-bridge H6 inverter can achieve higher efficiency with the same EMI filter condition as what the H5 topology does.

3.6. HERIC topology

According to the HERIC topology, [36], two active switches and two diodes compose the AC-decoupling circuit. Fig. 24 shows the HERIC inverter using the AC-decoupling circuit with two active switches. In that case, the device count is reduced without any performance compromise. The hybrid UPWM method with reactive power injection and the corresponding loss distribution is then shown introduced in Fig. 25. At the positive half-cycle, S_6 is in ON-state, and $S_{1,4}$ and S_5 switch at a high frequency to achieve the output voltage of + V_{DC} and 0. At the negative half-cycle, S_5 is ON, and $S_{2,3}$ and S_6 change at the switching frequency to generate the voltage of – V_{DC} and 0. As for the loss distribution demonstrated in Fig. 25, the switching losses are equally shared by $S_{1–4}$, and only conduction losses are generated on S_5 and S_6. The fully symmetrical structure with the hybrid modulation can achieve balanced losses among switches $S_{1–4}$ and the AC-decoupling switches $S_{5,6}$. Besides, the total power losses of the HERIC topology are the same as the full-bridge inverter with the hybrid UPWM method.

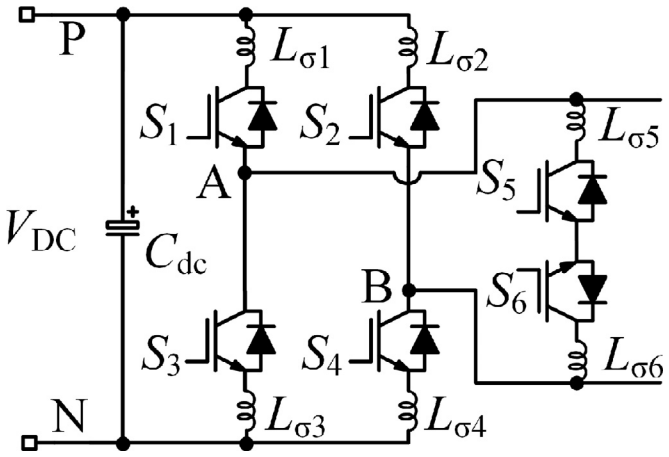

Fig. 24. HERIC inverter- equivalent circuit with parasitic inductances, where $L_{\sigma 1–6}$ are the parasitic inductances of switches $S_{1–6}$.

Referring to the commutation operation modes, Fig. 26 exhibits the switching states of the HERIC in the positive half-cycle. The corresponding loop inductances can be expressed as

$$L_{+VDC\_HERIC} = L_{\sigma 1} + L_{\sigma 4} + L_{loop1} \tag{10}$$

$$L_{0\_HERIC} = L_{\sigma 5} + L_{\sigma 6} + L_{loop2} \tag{11}$$

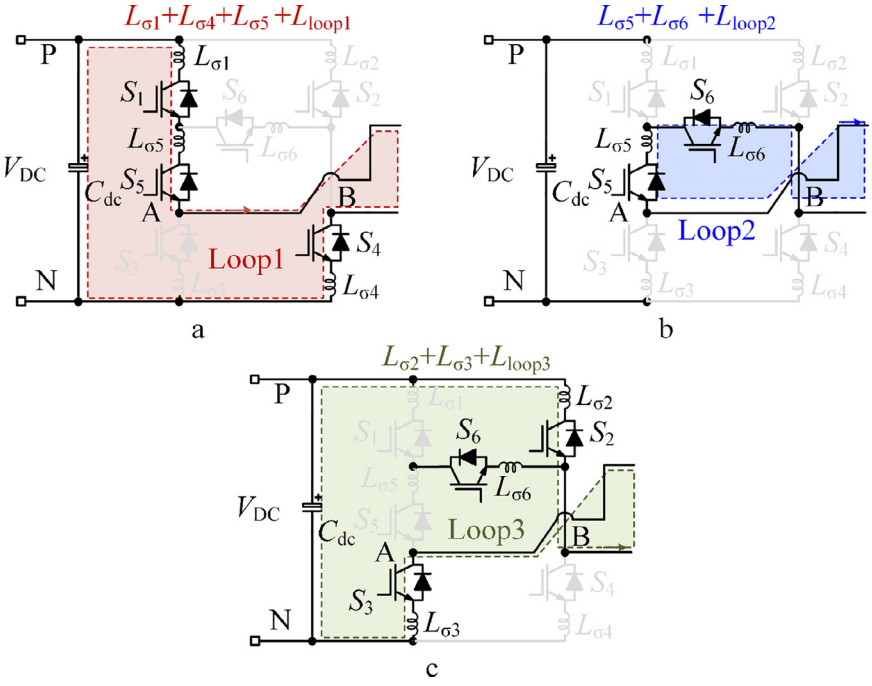

Fig. 23. Hybrid-bridge H6 inverter-commutation modes, where L_{loop1}, L_{loop2} and L_{loop3} are the PCB routing inductances
a '+ V_{DC}' mode
b '0' mode
c '– V_{DC}' mode.

Table. 1
Performance comparison of the full-bridge type PV inverters with the hybrid UPWM method [48].

Converter	Semiconductor devices No.		Leakage current suppression	Efficiency	Power density	Losses balance	Oscillation performance
	IGBT	Diode					
Full-bridge	4	0	Non	++++	+	++	+++
H5	5	0	+	++	++	+	++
DC-decoupling H6 [28]	6	0	+	+	++	+++	+
AC-decoupling H6 [32], [33]	6	2	++	+	++	+++	++
Mid-switch H6 [35]	6	2	++	+	++	+++	++
Hybrid-bridge H6 [34]	6	0	+++	+++	+++	++++	++
HERIC [36]	6	0	+++	++++	++++	+++++	+++

Note: The more '+' means the higher performance, representing the comparative level. 'Non' represents there is no such function.

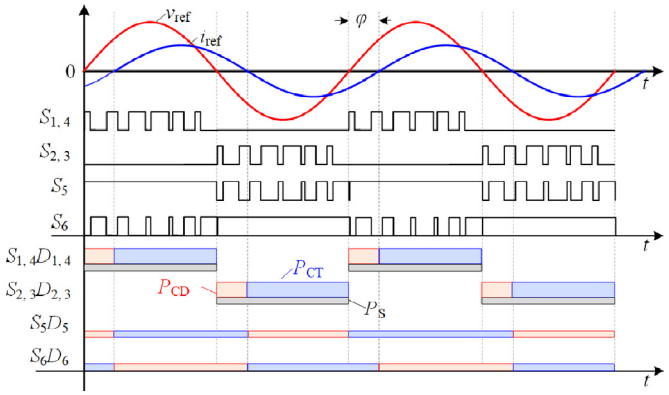

Fig. 25. HERIC inverter-hybrid modulation scheme and loss distribution.

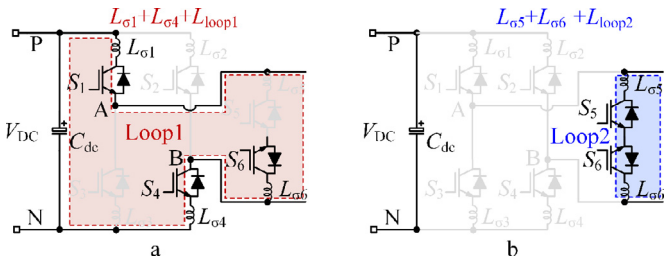

Fig. 26. HERIC inverter-commutation modes in the positive half-cycle, where L_{loop1} and L_{loop2} are the PCB routing inductances
a '+ V_{DC}' mode
b '0' mode.

By comparison, the loop inductances in each operation mode are almost the same if only considering the parasitic inductance of switches. Consequently, the oscillation frequency has a small range, reducing the design burden of the EMI filter.

4. Comparison discussion

The above five single-phase PV inverters under the hybrid UPWM method with reactive power injection have representative characteristics in terms of structure, leakage current suppression, conversion efficiency, loss distribution, and commutation oscillation. Since the NPC type inverters are almost based on DC/AC decoupling inverters, their performances of loss distribution and commutation oscillation under the hybrid modulation scheme are similar to DC/AC decoupling ones. Therefore, the performance of full-bridge type inverters compared in Table 1 has not included the NPC type. The specific discussions seen from the perspective of commutation oscillation and loss distribution are as follows.

1) Commutation oscillation: Considering the design of the EMI filter, it is expected that the frequency range of the commutation oscillation is small in the PV inverters. Thus, it is better to ensure the symmetrical loop inductances of all the commutation operation modes. From this, the full-bridge inverter and the HERIC have the best performance, while the DC-decoupling H6 inverter is the worst, as summarised in Table I. To improve this, the inductances in the loop routine can be improved by the PCB design, balancing the total loop inductances.
2) Loss distribution: According to the modulation scheme and loss distribution performance in Figs. 10,13,16,19, and 22, the HERIC has the best performance in losses balance, then decreasing, in the order of the hybrid-bridge inverter, the AC decoupling inverters [32,33] and the DC decoupling inverter [28], the full-bridge inverter and the H5 inverter [27]. The stable junction temperature of the power devices (i.e., relating to the balanced losses) benefits the lifetime of power devices [64]. When the losses unbalance is dominated by the conduction losses, the redundant design is a promising way, such as the bypass DC-decoupling H6 topologies in Fig. 5(c) (i.e., improved topology based on the H5 topology). While the unbalanced losses of the power devices are caused by the different switching frequencies, an improved modulation method is a proper solution, such as the circulating modulation control in [65] for the full-bridge inverter.

According to the performance comparison in Table I, the full-bridge inverter with the hybrid modulation method [48] has a fewer device count, higher efficiency, and better oscillation performance, and yet it needs extra transformers. Comparatively, the HERIC inverter is the most cost-effective one among those representative transformerless full-bridge type PV inverters, which can achieve an optimal trade-off of efficiency, leakage current suppression, losses balance, and commutation oscillation. In the future, the WBG devices will replace the Si switches gradually. The oscillation will be paid more and more attention due to strict EMI requirements [53,54]. To better the application of WBG devices, there are some challenges: 1) Building the EMI model from the semiconductor level to power system level; 2) accurately extracting parasitic parameters for modeling; 3) Methodology developing to alleviate the EMI issues, such as parasitic parameter reduction. In addition, the loss distribution has a close relationship with the heatsink design, impacting power density, reliability, and system cost. Many excellent redundant designs, improved modulation methods, and thermal control strategies will be encouraged.

5. Case studies

To demonstrate the loss distribution analysis under the hybrid modulation method, simulations are carried out on a full-bridge inverter prototype in PLECS. The thermal-loss models of active switches S_{1-4} are built according to the device datasheet (i.e., Infineon IGBT–FS25R12KT3). The system parameters are the DC-link voltage V_{DC} = 365 V, the output AC voltage v_{ac} = 220 V (the root mean square-RMS) / 50 Hz, the output power P = 5 kW, and the switching frequency f_{sw} = 20 kHz. There are two modulation methods compared in the full-bridge inverter, where the power factor angle φ is a variable between 0 to π.

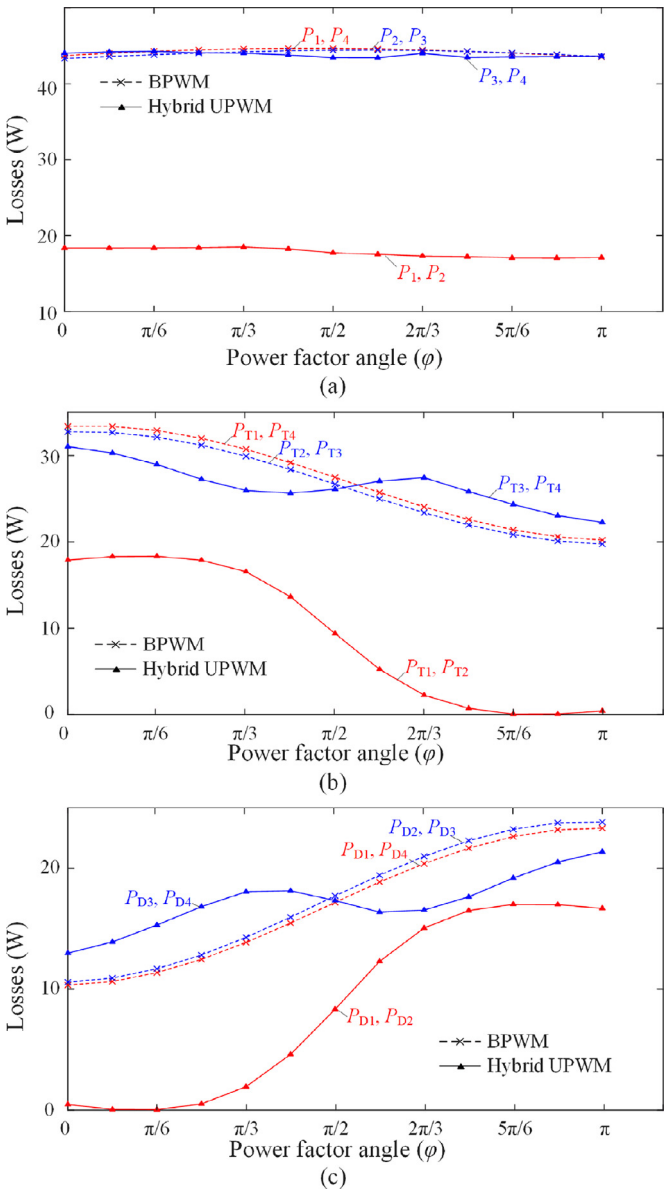

Fig. 27. Comparison of loss distribution of the full-bridge inverter, where P_{CT}, P_{CD} and P_S are the conduction losses on IGBT, the conduction losses on the anti-parallel diodes, and the switching losses when the full-bridge inverter operates under various power factors.
a Total losses
b Losses on unidirectional switches
c Losses on anti-parallel diodes.

Fig. 27 shows the comparison results, in which total losses of devices (P_{1-4}), losses of unidirectional switches (P_{T1-4}), and losses of anti-parallel diodes (P_{D1-4}) are depicted in Fig. 27(a)-(c), respectively. As shown in Figs. 27(a), the total losses of semiconductor devices S_{1-4} in the full-bridge inverter are equally distributed under the BPWM method. The losses of $S_{1,3}$ are far less than that of $S_{2,4}$ When the full-bridge inverter adopts the hybrid UPWM method [48]. However, the losses of the hybrid UPWM method are less than that of the BPWM. As presented in Fig. 27(b) and (c), the power losses of the body diodes and the unidirectional switches change with the power factor angle when the full-bridge inverter adopts both the BPWM and the hybrid UPWM methods. That is, the reactive power injection will influence the internal loss distribution of the power device, which can be considered in the power control strategy. In addition, the power losses of the unidirectional switches and body diodes are identical when the full-bridge inverter employs the BPWM method.

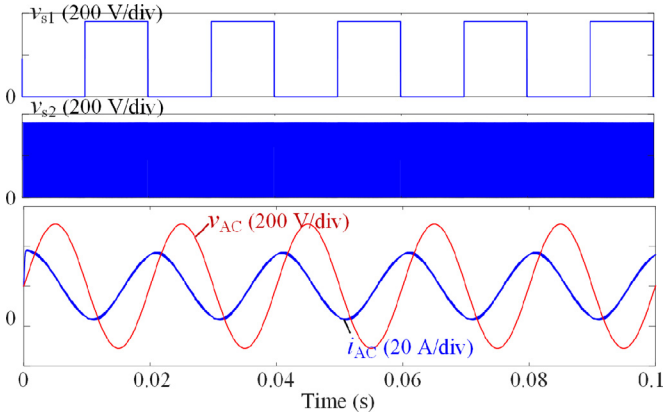

Fig. 28. Simulation performance of the full-bridge inverter with the hybrid UPWM method, where v_{s1}, v_{s2} are the voltages of S_1 and S_2, and v_{AC} and i_{AC} are the grid voltage and current.

Fig. 28 shows the modulation waveforms of the full-bridge inverter under the hybrid UPWM method, where v_{S1}, v_{S2}, v_{AC} and i_{AC} are the voltages of S_1 and S_2, the grid voltage and current. As shown in Fig. 27, v_{S1} changes at the grid frequency and v_{S2} changes at a high frequency. The comparison results agree well with the theoretical analysis in Section 3.1. In all, the simulation results validate the loss distribution of the full-bridge inverter under the hybrid modulation method with reactive power injection.

6. Conclusion

In this paper, the full-bridge type PV inverters have been classified and reviewed according to the leakage current suppression. Then, the commutation oscillation and loss distribution performances have been analyzed in selected full-bridge PV inverters under the hybrid UPWM method with reactive power injection. The identical loop inductances in different commutation modes have good oscillation performance, benefiting the EMI filter design. Then, a comprehensive comparison of the full-bridge inverters has been presented in leakage current suppression, efficiency, loss distribution, oscillation, and system costs. Finally, simulations validated the analysis of loss distribution under the hybrid modulation method with reactive power injection in the full-bridge inverter.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by the Novo Nordisk Fonden through the Interdisciplinary Synergy Programme (Award Ref. No.: NNF18OC0034952).

Data availability statement

Data sharing does not apply to this article as no datasets were generated or analyzed during the current study

References

[1] International Renewable Energy Agency (IRENA), Renewable capacity statistics 2021, Mar. 2021, https://www.irena.org/-/media/Files/IRENA/Agency/Publication/2021/Apr/IRENA_RE_Capacity_Statistics_2021.pdf, last accessed Apr. 06, 2021

[2] Z. Tang, Y. Yang, F. Blaabjerg, 'Power electronics-The enabling technology for renewable energy integration, CSEE J. Power Energy Syst., Early Access (2021).

[3] D. Meneses, F. Blaabjerg, O. García, J.A. Cobos, Review and comparison of step-up transformerless topologies for photovoltaic AC-module application, IEEE Trans. Power Electron. 28 (6) (2013) 2649–2663.

[4] W. Li, Y. Gu, H. Luo, W. Cui, X. He, C. Xia, 'Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression, IEEE Trans. Ind. Electron. 62 (7) (2015) 4537–4551.

[5] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, M. Sumner, 'Evaluation of three--phase transformerless photovoltaic inverter topologies, IEEE Trans. Power Electron. 24 (9) (2009) 2202–2211.

[6] X. Zhang, T. Zhao, W. Mao, D. Tan, L. Chang, 'Multilevel inverters for grid-connected photovoltaic applications: examining emerging trends, IEEE Power Electron. Mag. 5 (4) (2018) 32–41.

[7] D. Yang, H. Latchman, D. Tingling, A.A. Amarsingh, Design and return on investment analysis of residential solar photovoltaic systems, IEEE Potentials 34 (4) (2015) 11–17.

[8] W. Chen, X. Yang, W. Zhang, X. Song, Leakage current calculation for PV inverter system based on a parasitic capacitor model, IEEE Trans. Power Electron. 31 (12) (2016) 8205–8217.

[9] DIN VDE 0126, Automatic disconnection device between a generator and the public low-voltage grid, German Standard (2010).

[10] VDE-AR-N 4105Verband Der Elektrotechnik.: 'Power Generation Systems Connected to the Low-Voltage Distribution Network–Technical Minimum Requirements For the Connection to and Parallel Operation With Low-Voltage Distribution Networks', Verband der Elektrotechnik, Frankfurt, Germany, Aug. 2011.

[11] IEEE Standard 1547.2: 'IEEE standard for interconnecting and interoperability of distributed resources with associated electric power systems interfaces', 2018

[12] Y.P. Siwakoti, F.Z. Peng, F. Blaabjerg, P.C. Loh, G.E. Town, Impedance-source networks for electric power conversion part I: a topological review, IEEE Trans. Power Electron. 30 (2) (2015) 699–716.

[13] M.N.H. Khan, M. Forouzesh, Y.P. Siwakoti, L. Li, T. Kerekes, F. Blaabjerg, 'Transformerless inverter topologies for single-phase photovoltaic systems: a comparative review, IEEE J. Emerg. Sel. Top. Power Electron. 8 (1) (2020) 805–835.

[14] M. Shayestegan, M. Shakeri, H. Abunima, S.M.S. Reza, M. Akhtaruzzaman, B. Bais, S. Mat, K. Sopian, N. Amin, 'An overview on prospects of new generation single-phase transformerless inverters for grid-connected photovoltaic (PV) systems, Renew. Sust. Energ. Rev. 82 (1) (2018) 515–530.

[15] T. Wu, C. Kuo, H. Hsieh, Combined unipolar and bipolar PWM for current distortion improvement during power compensation, IEEE Trans. Power Electron. 29 (4) (2014) 1702–1709.

[16] S.B. Kjaer, J.K. Pedersen, F. Blaabjerg, 'A review of single-phase grid-connected inverters for photovoltaic modules, IEEE Trans. Ind. 41 (5) (2005) 1292–1306.

[17] A.A. Estévez-Bén, A. Alvarez-Diazcomas, G. Macias-Bobadilla, J. Rodríguez-Reséndiz, Leakage current reduction in single-phase grid-connected inverters—A review, Appl. Sci. 10 (7) (2020) 2384.

[18] H. Xiao, Overview of transformerless photovoltaic grid-connected inverters, IEEE Trans. Power Electron. 36 (1) (2021) 533–548.

[19] H. Fujimoto, T. Kagotani, H. Kidoguchi, 'Photovoltaic inverter with a novel cycloconverter for interconnection to a utility line, in: Proc. IEEE IAS'95 Conf, 1995, pp. 2461–2467.

[20] T. Shimizu, O. Hashimoto, G. Kimura, A novel high-performance utility-interactive photovoltaic inverter system, IEEE Trans. Power Electron. 18 (2) (2003) 704–711.

[21] P. Knaup, 'International patent application, WO Patent 048 420 A1 (May 3, 2007).

[22] R. Gonzalez, E. Gubia, J. Lopez, L. Marroyo, 'Transformerless single-phase multilevel-based photovoltaic inverter, IEEE Trans. Ind. Electron. 55 (7) (2008) 2694–2702.

[23] K. Dietrich, German Patent Wechselrichter: DE 19642522 C1 (Apr. 1998).

[24] Z. Yao, L. Xiao, Y. Yan, 'Control strategy for series and parallel output dual-buck half bridge inverters based on DSP control, IEEE Trans. Power Electron. 24 (2) (2009) 434–444.

[25] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, X. He, 'Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems, IEEE Trans. Power Electron. 28 (2) (2013) 793–805.

[26] F. Yang, H. Ge, J. Yang, R. Dang, H. Wu, A family of dual-buck inverters with an extended low-voltage DC-input port for efficiency improvement based on dual-input pulsating voltage-source cells, IEEE Trans. Power Electron. 33 (4) (2018) 3115–3128.

[27] M. Victor, K. Greizer, A. Bremicker, Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage, U.S. Patent 2005 028 6281 A1 (Apr. 23, 1998).

[28] B. Yang, W. Li, Y. Gu, W. Cui, X. He, Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system, IEEE Trans. Power Electron 27 (2) (2012) 752–762.

[29] L. Zhang, K. Sun, Y. Xing, M. Xing, 'H6 transformerless full-bridge PV grid-tied inverters, IEEE Trans. Power Electron. 29 (3) (2014) 1229–1238.

[30] M. Islam, S. Mekhilef, H6-type transformerless single-phase inverter for grid-tied photovoltaic system, IET Power Electron 8 (4) (2015) 636–644.

[31] B. Ji, J. Wang, J. Zhao, High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method, IEEE Trans. Ind. Electron. 60 (50) (2013) 2104–2115.

[32] W. Yu, J.J. Lai, H. Qian, C. Hutchens, High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC module applications, IEEE Trans. Power Electron. 4 (26) (2011) 1253–1260.

[33] W. Cui, B. Yang, Y. Zhao, W. Li, X. He, 'A novel single-phase transformerless grid–connected inverter, Proc. IEEE IECON Conf. (2011) 1126–1130.

[34] W. Cui, H. Luo, Y. Gu, W. Li, B. Yang, X. He, Hybrid-bridge transformerless photovoltaic grid-connected inverter, IET Power Electron 8 (3) (2015) 439–446.

[35] G. San, H. Qi, J. Wu, X. Guo, 'A new three-level six-switch topology for transformerless photovoltaic systems, Proc. IPEMCC' 7th Conf. (2012) 163–166.

[36] S. Heribert, S. Christoph, K. Jurgen, 'Inverter for transforming a DC voltage into an AC current or an AC voltage, Europe Patent 1 369 985 (A2) (May 13, 2003).

[37] L. Zhang, K. Sun, L. Feng, H. Wu, Y. Xing, 'A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters, IEEE Trans. Power Electron. 28 (2) (2013) 730–739.

[38] L. Zhou, F. Gao, T. Xu, 'A family of neutral-point-clamped circuits of single-phase PV inverters: generalized principle and implementation, IEEE Trans. Power Electron. 32 (6) (2017) 4307–4319.

[39] T. Freddy, N.A. Rahim, W.P. Hew, H.S. Che, Comparison and analysis of single-phase transformerless grid-connected PV inverters, IEEE Trans. Power Electron. 29 (10) (2014) 5358–5369.

[40] M. Islam, S. Mekhilef, M. Hasan, Single phase transformerless inverter topologies for grid-tied photovoltaic system: a review, Renew. Sustain. Energy Rev. 45 (2015) 69–86.

[41] H. Xiao, S. Xie, Y. Chen, R. Huang, 'An optimized transformerless photovoltaic grid–connected inverter, IEEE Trans. Ind. Electron. 58 (5) (2011) 1887–1895.

[42] H. Li, Y. Zeng, B. Zhang, T.Q. Zheng, R. Hao, Z. Yang, An improved H5 topology with low common-mode current for transformerless PV grid-connected inverter, IEEE Trans. Power Electron. 34 (2) (2019) 1254–1265.

[43] R. Gonzalez, J. Lopez, P. Sanchis, L. Marroyo, 'Transformerless inverter for single-phase photovoltaic systems, IEEE Trans. Power Electron. 22 (2) (2007) 693–697.

[44] S. Hu, W. Cui, W. Li, X. He, F. Cao, 'A high-efficiency single-phase inverter for transformerless photovoltaic grid-connection, proc. of IEEE ECCE conf. (2014) 4232–4236.

[45] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, E. Aldabas, 'A new high-efficiency single-phase transformerless PV inverter topology, IEEE Trans. Ind. Electron. 58 (1) (2011) 184–191.

[46] H.F. Xiao, K. Lan, L. Zhang, 'A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage, IEEE Trans. Power Electron. 30 (6) (2015) 3122–3132.

[47] T.K.S. Freddy, J.H. Lee, H.C. Moon, K.B. Lee, N.A. Rahim, Modulation technique for single-phase transformerless photovoltaic inverters with reactive power capability, IEEE Trans. Ind. Electron. 64 (9) (Sep. 2017) 6989–6999.

[48] Z. Ahmad, S.N. Singh, Improved modulation strategy for single phase grid connected transformerless PV inverter topologies with reactive power generation capability, Solar Energy 163 (Feb. 2018) 356–375.

[49] J. Wang, F. Luo, Z. Ji, Y. Sun, B. Ji, J. Zhao, An improved hybrid modulation method for the single phase H6 inverter with reactive power compensation, IEEE Trans. Power Electron. 33 (9) (Sep. 2018) 7674–7683.

[50] Z. Tang, M. Su, Y. Sun, B. Cheng, Y. Yang, F. Blaabjerg, L. Wang, 'A hybrid UP-PWM scheme for HERIC inverter to improve power quality and efficiency, IEEE Trans. Power Electron. 34 (5) (May 2019) 4292–4303.

[51] J.L. Hudgins, G.S. Simin, E. Santi, M.A. Khan, An assessment of wide bandgap semiconductors for power devices, IEEE Trans. Power Electron. 18 (3) (May 2003) 907–914.

[52] A. Bindra, Wide-Bandgap-Based Power Devices: reshaping the power electronics landscape, IEEE Power Electron. Mag. 2 (1) (Mar. 2015) 42–47.

[53] R. Araneo, S. Lammens, M. Grossi, S. Bertone, 'EMC issues in high-power grid–connected photovoltaic plants, IEEE Trans. Electromagn. Compat. 3 (51) (2009) 639–648.

[54] Schattner, S., Bopp, G., Erge, T., Fischer, R., Haberlin, H., Minkner, R., Venhuizen, R. and Verhoeven, B.: 'Development of standard test procedures for electromagnetic interference (EMI) tests and evaluations on photovoltaic components and plants - PV-EMI', Publishable Final Rep. EU Project number JOR3-CT98-0217.

[55] Y. Xiang, X. Pei, M. Wang, C. Yang, P. Zhou, Y. Kang, A separate floating heatsink based suppression method for conducted common-mode EMI, IEEE Trans. Ind. Electron. 68 (11) (2021) 10436–10448.

[56] N. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, P. Rimmen, 'Reliability oriented design tool for the new generation of grid connected PV-inverters, IEEE Trans. Power Electron. 30 (5) (2015) 2635–2644.

[57] Z. Zhang, H. Qiu, J. Wang, Research on eliminating parasitic oscillation of inverter by using PI and repetitive control, in: 2016 IEEE ICEICT conf., 2016, pp. 321–324.

[58] Y. Zhu, H. Li, C. Luo, Y. Liu, C. Wan, J. Ma, Influence of paralleled SiC MOSFET on turn-off gate voltage oscillation, in: 2020 IEEE ECCE conf., 2020, pp. 683–689.

[59] A. Sangwongwanich, A. Abdelhakim, Y. Yang, K. Zhou, in: Chapter 6 - Control of Single-Phase and Three-Phase DC/AC Converters, Editor(s): Frede Blaabjerg, Control of Power Electronic Converters and Systems, Academic Press, 2018, pp. 153–173.

[60] Graovac, D.D. and P¨urschel, M.: 'IGBT power losses calculation using the data-sheet parameters' (Infineon, 2009, pp. 1–17)

[61] M. Chen, D. Pan, H. Wang, X. Wang, F. Blaabjerg, 'Investigation of switching oscillations for silicon carbide MOSFETs in three-level active neutral-point-clamped inverters, IEEE Trans. Emerg. Sel. Topics Power Electron. 9 (4) (2021) 4839–4853.

[62] E. Koutroulis, F. Blaabjerg, 'Design optimization of transformerless grid-connected PV inverters including reliability, IEEE Trans. Power Electron. 28 (1) (2013) 325–335.

[63] M. Catelani, L. Ciani, E. Simoni, 'Thermal analysis of critical components in photovoltaic inverter, in: Proc. of I2MTC conf., 2012, pp. 1891–1895.

[64] U. Scheuermann, S. Schuler, Power cycling results for different control strategies, Microelectron. Reliab. 50 (9–11) (Sep.-Nov. 2010) 1203–1209.

[65] Z. Tang, Y. Yang, F. Blaabjerg, 'Loss unbalance issue of the full-bridge inverter with reactive power injection, in: 2021 IEEE APEC conf., 2021, p. 1451.

Zhongting Tang (S'18) was born in Sichuan, China, in 1990. She received her B.S. degree in Automation Control in 2012 and Ph.D. degree in Control Science and Engineering in 2020 from Central South University, Changsha, China. During 2018~2020, she studied as a guest Ph.D. student at the AAU Energy in Aalborg University, Aalborg, Denmark. Now, she is currently working as a postdoc here.

Her research focus is on the grid integration of photovoltaics, topology and modulation technology of transformerless converter and its application and reliability in Photovoltaic system.

Ariya Sangwongwanich (S'15-M'19) received the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. He is currently working as an Assistant Professor at the Department of Energy Technology, Aalborg University, where he is a Vice-Leader of Photovoltaic Systems research program. His research interests include control of grid-connected converters, photovoltaic systems, reliability in power electronics, and multilevel converters.

He was a Visiting Researcher with RWTH Aachen, Aachen, Germany from September to December 2017. Dr. Sangwongwanich was the recipient of the Danish Academy of Natural Sciences' Ph.D. Prize and the Spar Nord Foundation Research Award for his Ph.D. thesis in 2019.

Yongheng Yang (SM'17) received the B.Eng. degree in Electrical Engineering and Automation from Northwestern Polytechnical University, China, in 2009 and the Ph.D. degree in Energy Technology (power electronics and drives) from Aalborg University, Denmark, in 2014.

He was a postgraduate student with Southeast University, China, from 2009 to 2011. In 2013, he spent three months as a Visiting Scholar at Texas A&M University, USA. Since 2014, he has been with the Department of Energy Technology, Aalborg University, where he became a tenured Associate Professor in 2018. In January 2021, he joined Zhejiang University, China, where he is currently a ZJU100 Professor with the Institute of Power Electronics, College of Electrical Engineering. His current research interests include the grid-integration of photovoltaic systems and control of power converters, in particular, the mechanism and control of grid-forming power converters and systems.

Dr. Yang was the Chair of the IEEE Denmark Section (2019-2020). He is an Associate Editor for several IEEE Transactions/Journals. He is a Deputy Editor of the *IET Renewable Power Generation* for Solar Photovoltaic Systems. He was the recipient of the 2018 *IET Renewable Power Generation* Premium Award and was an Outstanding Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2018. He received the 2021 Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society (PELS). In addition, he has received two IEEE Best Paper Awards. He is currently the Secretary of the IEEE PELS Technical Committee on Sustainable Energy Systems and a Council Member of the China Power Supply Society.

Frede Blaabjerg (S'86M'88SM'97F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he served as a President of IEEE Power Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014-2020 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.