Switched capacitor based cascaded half-bridge multilevel inverter with voltage boosting feature

Jahan, Hosseint Khoun; Shotorbani, Amin Mohammadpour; Abapour, Mehdi; Zare, Kazem; Hosseini, Seyed Hossein; Blaabjerg, Frede; Yang, Yongheng

Published in:
CPSS Transactions on Power Electronics and Applications (CPSS TPEA)

DOI (link to publication from Publisher):
10.24295/CPSSTPEA.2021.00006

Publication date:
2021

Document Version
Publisher's PDF, also known as Version of record

Switched Capacitor Based Cascaded Half-Bridge Multilevel Inverter With Voltage Boosting Feature

Hossein KHOUN-JAHAN, Amin Mohammadpour SHOTORBANI, Mehdi ABAPOUR, Kazem ZARE, Seyed Hossein HOSSEINI, Frede BLAABJERG, and Yongheng YANG

***Abstract*—Cascaded multilevel inverter (CMI) topology is prevalent in many applications. However, the CMI requires many switches and isolated dc sources, which is the main drawback of this type of inverter. As a result, the volume, cost and complexity of the CMI topology are increased and the efficiency is deteriorated. This paper thus proposes a switched-capacitor-based multilevel inverter topology with half-bridge cells and only one dc source. Compared to the conventional CMI, the proposed inverter uses almost half the number of switches, while maintaining a boosting capability. Additionally, the main drawback of switched-capacitor multilevel inverters is the capacitor inrush current. This problem is also averted in the proposed topology by using a charging inductor or quasi-resonant capacitor charging with a front-end boost converter. Simulation results and lab-scale experimental verifications are provided to validate the feasibility and viability of the proposed inverter topology.**

***Index Terms*—Multilevel Inverter, switched-capacitor cell, switch reduction, voltage Boosting.**

Nomenclature

D_n	Number of charging diodes.
Sw_n	Number of switches.
R_{dn}	Resistance of a typical diode.
R_d	Resistance of the anti-parallel diode in the switch.
R_l	Resistance of the charging inductor.
R_{sw}	Resistance of a typical switch.
$i_{ch}(t)$	Instantaneous charging current.
$i(t)$	Instantaneous load current.
I_s	Current of a switch.
V_m, I_m	Peak values of the output voltage and load current
v_{dc}	Input dc voltage.
v_{os}	Voltage of a typical switch in the on state.
v_{odn}	Reverse voltage of a typical diode in the on state.
v_{sd}	Reverse voltage of the anti-parallel diode.
v_{ds}	Drain-source voltage of a semiconductor switch.
T_{dn}	Conducting time duration of a charging diode.
T_{ch}	Charging time duration.
$T_{dis,k}$	Discharging time duration of the k^{th} capacitor.
t_{on}, t_{off}	Turn-on, and turn-off times of switches.
ΔP^t_d	Total conduction power loss of the charging diodes.
$\Delta P_{d,j}$	Conduction power loss of a typical diode.
ΔP_s	Power loss of a switch due to load current.
$\Delta P_{s,ch}$	Conduction power loss of a switch in charging stage.
$\Delta P_{d,ch}$	Power loss of the charging inductor.
ΔP_{fm}	Switching power loss of a typical switch.
ΔP_{sw}	Total power loss of the charging switch.
$\Delta P_{sw,j}$	Total power loss of a switch.
ΔP^t_{ch}	Total power loss of switches in the charging part.
ΔP^t_s	Total power loss of the switches in the charging stage.
ΔP^t_{sw}	Total power loss of the switches.
ΔP_t	Overall power loss of the proposed SC-CHMI.
f	Fundamental frequency ($\omega = 2\pi f$).
f_{sw}	Switching frequency.
φ	Phase angle between the voltage and current.
l	Number of levels.
C_{oss}	Output capacitance of a switch.
n	Number of half-bridge cells.
η	Efficiency
d	Duty cycle

Manuscript received April 16, 2020; revised July 9, 2020; accepted August 17, 2020. Date of publication March 30, 2021; date of current version March 18, 2021. This work was supported under the research project – Reliable Power Electronic based Power Systems (REPEPS) by The Velux Foundations under Award No.: 00016591. (*Corresponding Author: Yongheng Yang*.)

H. Khoun-Jahan is with the University of Tabriz, Tabriz, Iran and the Department of Energy Technology, Aalborg University, DK-9220 Aalborg East, Denmark (e-mail: hosseinkhounjahan@yahoo.com).

A. M. Shotorbani is with the University of Tabriz, Tabriz, Iran and the University of British Columbia Okanagan, Kelowna, BC, Canada (e-mail: a.m.shotorbani@ubc.ca).

M. Abapour, K. Zare, and S. H. Hosseini are with the University of Tabriz, Tabriz, Iran (e-mail: abapour@tabrizu.ac.ir; kazem.zare@tabrizu.ac.ir; hosseini@tabrizu.ac.ir)

F. Blaabjerg and Y. Yang are with the Department of Energy Technology, Aalborg University, DK-9220 Aalborg East, Denmark (e-mail: fbl@et.aau.dk; yoy@et.aau.dk).

Digital Object Identifier 10.24295/CPSSTPEA.2021.00006

I. Introduction

MULTILEVEL inverters (MIs) play a promising role in modern power systems. The MIs offer several benefits such as low switching frequency, total harmonic distortion (THD) and electromagnetic interference (EMI) [1], [2].

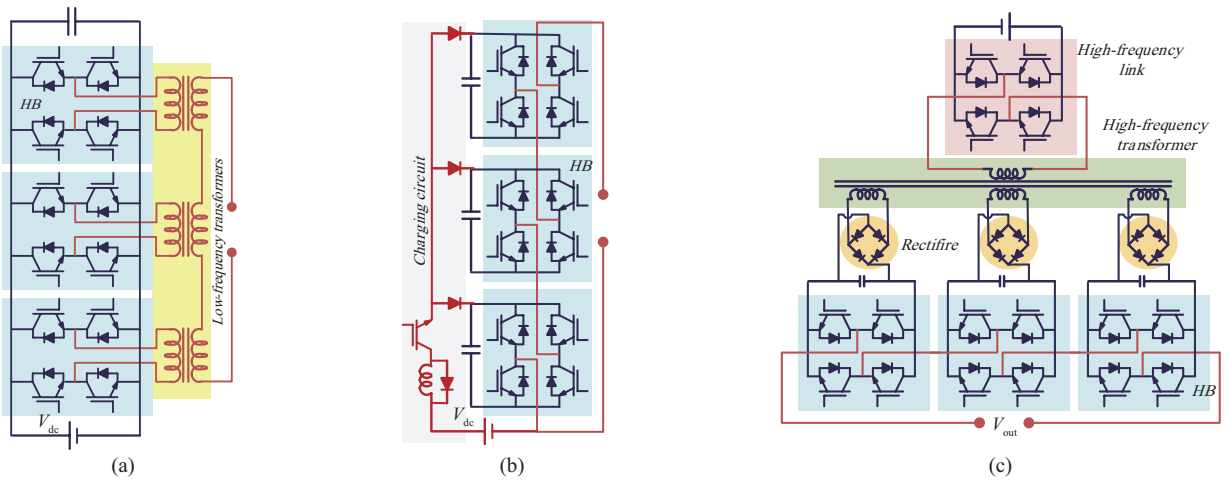

Fig. 1. Conventional single-source CMIs: (a) cascaded transformer CMI (CTMI), (b) switched-capacitor based CMI (SC-CMI), and (c) high-frequency link based CMI (HFLMI).

Additionally, MIs employ certain switch configurations in order to reduce the voltage stress on the switches to make it tolerable for the employed semiconductors. Utilizing many components makes MIs complicated and expensive [1]–[4]. Therefore, several attempts have been made to reduce the number of components in MIs [5]–[7], including the cascaded multilevel inverter (CMI) topology, the flying capacitor converters, and the diode-clamped converters [8].

Among the aforementioned MIs, the CMI stands out for its high modularity and providing a higher voltage amplitude from given input dc voltages. However, the CMI requires many switches and isolated dc sources. In order to reduce the switch count in this topology, full-bridge cells are replaced by half-bridge cells [9], [10]. The cascaded half-bridge cells configuration produces a periodic staircase waveform, since each half-bridge cell can only develop unity and zero per-unit voltages. Therefore, an unfolder H-bridge is used with the cascaded half-bridge cell MI (CHMI) to convert the stepped dc voltage into a staircase ac voltage [11]. Assuming a total constant value for the voltage stress of all switches in a CHMI, the voltage stress will increase if the number of switches is reduced [12]. The switches of the half-bridge cells in the CHMI topology tolerate only one per-unit voltage magnitude, whereas the switches in the unfolder H-bridge are exposed to the peak value of the output voltage.

Another issue with the CMI and the CHMI topologies is the need for several isolated dc sources. Different solutions have been proposed to decrease the number of dc sources in the CMI, which can be categorized into three groups. The first solution is to use individual low-frequency transformers instead of the dc-sources [13], [14]. As an advantage, the transformers provide galvanic isolation and can also convert the voltage with arbitrary magnitudes. On the contrary, transformers are expensive, bulky, and inefficient, Fig. 1(a) shows low-frequency transformer-based CMI. The second strategy is to employ switched-capacitor cells instead of the dc sources [15], [16], which may reduce the size, weight, and cost of MIs, since the capacitors are light and cheap in comparison with dc voltage sources and transformers. As a drawback, the failure rate of the capacitors is high. Moreover, the other shortcoming of the switched-capacitor cells is the sharp inrush current in the charging stage of the capacitors. This deficiency can result in failure of the capacitors and thus reduces the reliability of the switched-capacitor-based MIs. The switched-capacitor based CMI in [17], which is shown in Fig. 1(b), alleviated the inrush current through an inductor in dc side. The last solution is to use a high-frequency transformer and develop certain isolated dc voltages through a high-frequency link [18], [19], as shown in Fig. 1(c). However, the reliability and efficiency of this strategy are low, because numerous components are used to develop the dc voltages.

In light of the above and to avoid the mentioned deficiencies, this paper proposes a switched-capacitor cascaded half-bridge MI (SC-CHMI) with a modular structure, voltage boosting capability, and self-balancing control of the capacitor voltages. In the proposed SC-CHMI, only one dc source is employed and the other dc sources are replaced with switched-capacitor cells. Due to self-balancing feature, the charging process of the capacitors is executed spontaneously without any auxiliary device. In the proposed SC-CHMI, the capacitor inrush currents are mitigated by employing a charging inductor or a front-end boost converter. Moreover, the employed front-end boost converter can compensate voltage drop and limit the fault current. The proposed topology can be used as a versatile inverter in renewable energy systems, because of its voltage-boosting characteristic, minimum switch-count, and single dc source.

II. Proposed SC-CHMI Topology and Analysis

In the proposed SC-CHMI topology, the dc sources are replaced with the capacitors and only one dc source is used to charge the capacitors, in order to diminish the shortcomings of the conventional single-source CMI. Fig. 2 shows the general structure of the proposed topology, where the inductor (L_{ch})

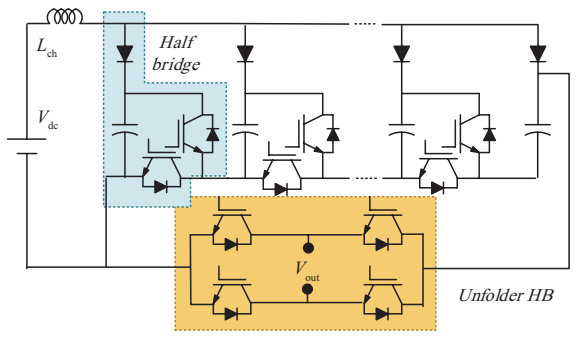

Fig. 2. Proposed SC-CHMI using an unfolder bridge and half bridge cells.

along with the diodes can smoothly charge the capacitors, limit the fault current and electromagnetic interference.

A nine-level SC-CHMI is depicted in Fig. 3(a) and is analyzed in the following, to illustrate the principle. Each capacitor in the proposed SC-CHMI experiences two different modes: the charging and discharging modes. Table I shows the switching states corresponding to the voltage levels, in which the charging and discharging modes are indicated by "C " and "D", and the "on" and "off " states of the diodes and switches are respectively shown by "0" and "1". As the switches in the half-bridge cell have an opposite action, only the states of the inner switches (i.e., S_1, S_2, S_3) are given in Table I. This is also the case for the unfolder switches. The switching modes and the current paths of the positive voltage levels are presented in Figs. 3(b)–(f).

A. Modulation Strategy

Several switching strategies can be adopted to compute the switching signals of the proposed topology. For simplicity, the level-shifted sine pulse width modulation (LS-SPWM) switching strategy is adopted to describe the operating principles of the proposed SC-CHMI. The capacitors are charged up to the input voltage in the charging mode. According to Fig. 3, C_4 takes part in all voltage levels, and S'_1 provides charging path for all the capacitors. Fig. 3(b) shows the current path for "0" voltage level and the charging paths. Fig. 3(c) depicts the current path for ±1 p.u. voltage levels which goes through the dc source (V_{dc}), L_{ch}, D_4, C_4, S'_3, S'_2, S'_1 , and unfolder switches (S_{L_1}, S'_{L_2} for positive and S'_{L_1}, S_{L_2} for negative voltage levels). The capacitor C_3 participates in the voltage levels other than the "0" and "±1" p.u. When C_3 is in the charging mode, the diode D_4 is reverse-biased. In this case, C_4 exclusively provides energy to the load, whereas C_2 and C_1 are already charged up to the input voltage value and C_3 is in the charging mode through the L_{ch}, D_3, C_3, S'_3, S'_2, S'_1, and the dc source. The same procedure happens individually for the remaining capacitors. This implies that only one capacitor is in the charging mode at each voltage level.

As mentioned above, a specific switching pattern is needed to guarantee at least one charging path for the capacitors. This is achievable by employing the LS-SPWM in such a way that the upper carriers are allocated to the switches in the lower cells and vice versa. For clarity, the LS-SPWM procedure for the nine-level SC-CHMI in Fig. 3(a) is presented in Fig. 4., where C_{rx},x = 1,2,3,4 indicates the carrier.

B. Power Loss Analysis

In order to determine the power losses, the number of active components for each voltage level is identified. In this regard, the number of the components for an l-level SC-CHMI are:

$$D_n = (l-1)/2 \tag{1}$$

$$Sw_n = l+1 \tag{2}$$

The power loss in the charging part consists of the power loss in the charging diodes and the charging inductor. For a typical diode, the conduction power loss is

$$\Delta P_{\mathrm{d},j} = 2f \int_{T_{\mathrm{d},n}} \left[R_{\mathrm{d},n} i_{\mathrm{ch}}^2(t) + v_{\mathrm{od},n} i_{\mathrm{ch}}(t) \right] \mathrm{d}t \tag{3}$$

Considering (1) and (3), and knowing that at any level only one diode appears in the charging path, the total conduction power loss of the diodes in the charging part of proposed SC-CHMI is calculated as

$$\Delta P_{\mathrm{d}}^t = \sum_{j=1}^{(l-1)/2} \Delta P_{\mathrm{d},j} \tag{4}$$

Moreover, the power loss of the charging inductor during the charging stage is

$$\Delta P_{L_{\mathrm{ch}}} = 2f \int_{T_{\mathrm{ch}}} R_1 i_{\mathrm{ch}}^2(t) \mathrm{d}t \tag{5}$$

For a semiconductor power switch, the conduction and the switching power losses are calculated as (6) and (7), respectively.

$$\Delta P_{\mathrm{Sch}} = 2f \int_{T_{\mathrm{ch}}} \left[R_{\mathrm{sw}} i^2(t) + v_{\mathrm{os}} i(t) \right] \mathrm{d}t \tag{6}$$

$$\Delta P_{\mathrm{fm}} = v_{\mathrm{ds}} f_{\mathrm{sw}} \left[(t_{\mathrm{on}} + t_{\mathrm{off}}) I_{\mathrm{s}} + C_{\mathrm{oss}} \right] \tag{7}$$

Thus, the total power loss of a switch in the charging path is

$$\Delta P_{\mathrm{sw}} = \Delta P_{\mathrm{Sch}} + \Delta P_{\mathrm{fm}} \tag{8}$$

The total power loss of all power switches in the charging path is then obtained as

$$\Delta P_{\mathrm{s}}^t = \sum_{i=1}^{(l-1)/2} \left(\frac{l-1}{2} - i \right) \Delta P_{\mathrm{Sch},i} \tag{9}$$

Consequently, the total power loss of the charging part is

$$\Delta P_{\mathrm{ch}}^t = \Delta P_{\mathrm{d}}^t + \Delta P_{L_{\mathrm{ch}}} + \Delta P_{\mathrm{s}}^t \tag{10}$$

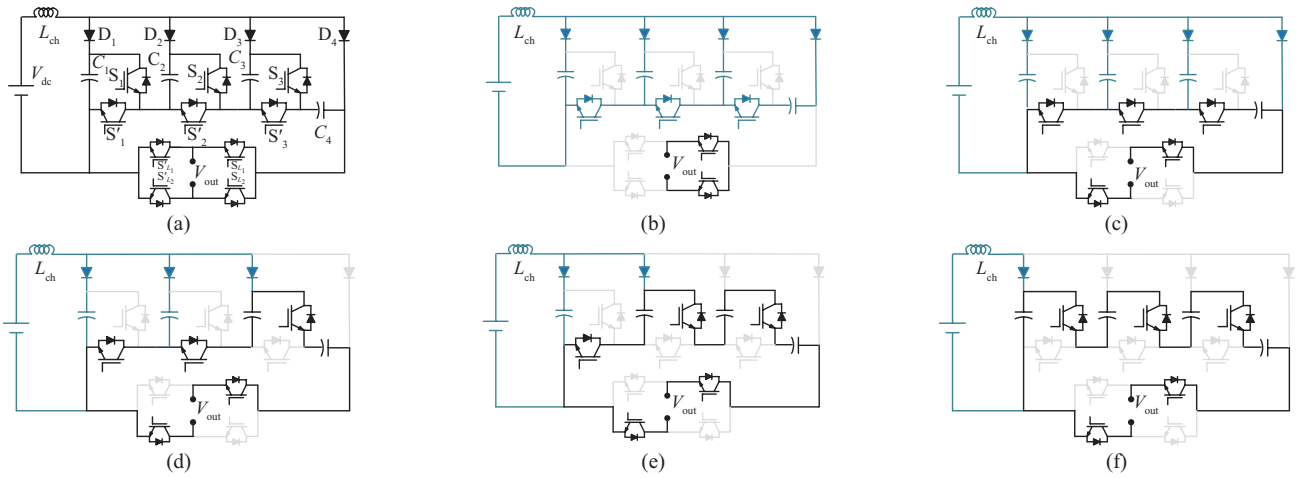

Fig. 3. Switching modes and current paths of the proposed SC-CHMI topology: (a) schematic of the nine-level SC-CHMI, (b) zero voltage level, (c) level +1, (d) level +2, (e) level +3, (f) level +4. Here, the load current and charging paths of the capacitors are in black and blue, respectively.

TABLE I
SWITCHING STATES OF THE SC-CHMI IN FIG.3.

Levels	Main switches	Unfolder switches	Charging Diodes	Capacitors	V_{out}
	S_1, S_2, S_3	S_{L1}, S_{L2}	D_1 – D_4	C_1 – C_4	
4	111	10	1000	D, D, D, D	$4V_{dc}$
3	011	10	1100	C, D, D, D	$3V_{dc}$
2	001	10	1110	C, C, D, D	$2V_{dc}$
1	000	10	1111	C, C, C, D	$1V_{dc}$
0	000	11	1111	C, C, C, C	0
−1	000	01	1111	C, C, C, D	$-1V_{dc}$
−2	001	01	1110	C, C, D, D	$-2V_{dc}$
−3	011	01	1100	C, D, D, D	$-3V_{dc}$
−4	111	01	1000	D, D, D, D	$-4V_{dc}$

The conduction and the total power losses of a typical switch in the proposed topology are

$$\Delta P_S = \frac{1}{\pi}\int_0^{\varphi}\left[v_{sd}\,i(t) + R_d\,i(t)^2\right]\mathrm{d}t + \frac{1}{\pi}\int_{\varphi}^{\pi}\left[v_{os}\,i(t) + R_{sw}\,i^2(t)\right]\mathrm{d}t \tag{11}$$

$$\Delta P_{sw,j} = \Delta P_s + \Delta P_{fm} \tag{12}$$

Knowing that half the numbers of switches participate in the load current path at each voltage level, the total power loss of the switches is

$$\Delta P_{sw}^{t} = \sum_{j=1}^{l+1}\Delta P_{sw,j} \tag{13}$$

Finally, the overall power loss of the proposed SC-CHMI topology is given as

$$\Delta P_t = \Delta P_{ch}^{t} + \Delta P_{sw}^{t} \tag{14}$$

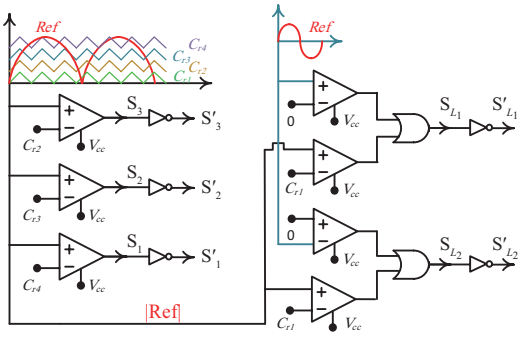

Fig. 4. The LS-SPWM for the nine-level SC-CHMI.

Therefore, the efficiency can be calculated by

$$\eta = \frac{V_{dc}\int_{T/2} i_{ch}(t)\mathrm{d}t - \Delta P_t}{V_{dc}\int_{T/2} i_{ch}(t)\mathrm{d}t} \tag{15}$$

C. Component Design

The capacitors and the charging inductor should be designed properly for a stable operation of the proposed topology. It is noted that the capacitors experience a higher voltage ripple in the purely-resistive loading condition. Hence, this loading is considered in the design stage of the capacitors. According to Fig. 5, the time duration of the discharging mode for the k^{th} capacitor is calculated as

$$T_{dis,k} = 2\sin^{-1}\frac{2k}{l-1} \tag{16}$$

For a desired maximum voltage ripple and discharging time (16), the capacitances can be designed

$$c_k = \frac{2I_s}{\omega\Delta v_k}\sin(T_{dis,k}/2) \tag{17}$$

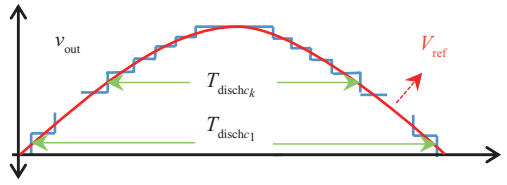

Fig. 5. Discharging time duration of the capacitors.

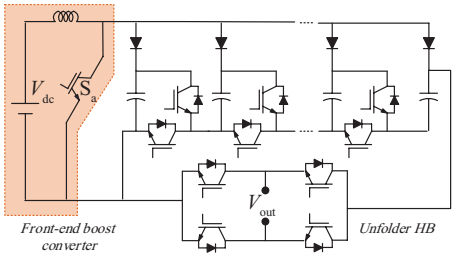

Fig. 6. The proposed SC-CHMI topology the front-end boost dc-dc converter.

However, in order to preserve the modularity of the proposed SC-CHMI, the capacitors can be chosen the same as the capacitor in the first half bridge and compensate the voltage ripple by adding an extra semiconductor switch to the topology and synthesize a front-end dc-dc converter at the input side, which is illustrated in the forthcoming section. The capacitors in the upper cells experience a higher voltage ripple with respect to Fig. 5 and (17), as their discharging time durations are longer than those in the lower cells.

If the proposed topology is started under the no-load condition, a large charging inductor can result in an overvoltages on the capacitors. In order to avoid the overvoltage, lower the electromagnetic interference, and limit the fault current, the charging inductor is designed as

$$L_{ch} \geqslant \frac{1}{(4\pi f)^2 C_t}, C_t = \sum_{k=1}^{(l-1)/2} C_k \tag{18}$$

However, if a larger inductor is employed to mitigate the inrush current, the soft starting strategy can be utilized to avoid the overvoltages of the capacitors.

D. Front-End DC-DC Boost Converter in Proposed Inverter

As shown in Fig. 6, by adding a semiconductor switch (S_a) to the proposed topology, it is possible to turn the charging circuit to a front-end dc-dc boost converter, which can help to compensate the voltage drop on the capacitors under heavy loading condition. This converter can also make the quasi-resonant charging of the capacitors available.

With the front-end boost converter, for a given peak value of the output voltage, the input dc voltage is calculated as

$$v_{dc} = \frac{1-d}{n+1} V_m \tag{19}$$

Assuming an ideal condition, in which the power losses are neglected, the average value of the input current is given as

$$I_{dc} = \frac{I_m}{2v_{dc}} V_m \tag{20}$$

The peak output voltage appears across the switches in the unfolder H-bridge. Since the voltage across the switches and capacitors in the half bridge cell is the same, the voltage stress of the components in the half-bridge cells is calculated as

$$v_{cell} = \frac{1}{n+1} V_m \tag{21}$$

and the voltage stress on the diode of the n^{th} cell is

$$v_{d,n} = \frac{n-1}{1-d} v_{dc} \tag{22}$$

TABLE II
COMPARISON OF THE SINGLE-SOURCE CMI TOPOLOGIES

Topology	Number of Components per Voltage Level			
	Switches	Diodes	Transformers	Capacitors
CTMI	$2(l-1)$	–	$(l-1)/2$	1
HFLMI	$2(l+2)$	$2(l-1)$	1	$(l-1)/2$
SC-CMI in [17]	$2l-1$	$(l+1)/2$	–	$(l-1)/2$
Proposed SC-CHMI	$l+1$	$(l-1)/2$	–	$(l-1)/2$

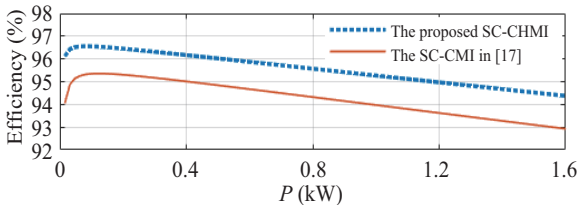

Fig. 7. Efficiencies of the SC-CMI in [17] and the proposed SC-CHMI under various output power.

E. Comparison of the Proposed SC-CHMI With the Single-Source CMI Topologies

In this section, the proposed SC-CHMI is compared with the conventional single-source CMI topologies described in Section II. Generally, the transformerless switched-capacitor topologies have a more compact structure and a higher efficiency compared to the CTMI topology. Table II shows the number of required components in different single-source CMI topologies. It is noted that the proposed SC-CHMI requires almost half the number of switches in comparison with other topologies. Moreover, the proposed SC-CHMI and the CTMI require half the number of diodes compared to the HFLMI, which uses almost two diodes per voltage level.

Furthermore, the proposed topology uses fewer switches in comparison with the SC-CMI in [17], and thus it can offer a higher efficiency, as illustrated in Fig. 7. A nine-level configuration with the peak output voltage of 320 V and the

TABLE III
COMPONENTS CHARACTERISTICS FOR EFFICIENCY ANALYSIS

Component	Characteristic
Switches in the cells	FDP86102LZ
Switches in the unfolder cell	FQA30N40
Diode	VS-60EPU04PbF
Resistance of the charging inductor	30 mΩ
Equivalent series resistance (ESR) of capacitors	18 mΩ
Input voltage	80 V
Switching frequency	6 kHz

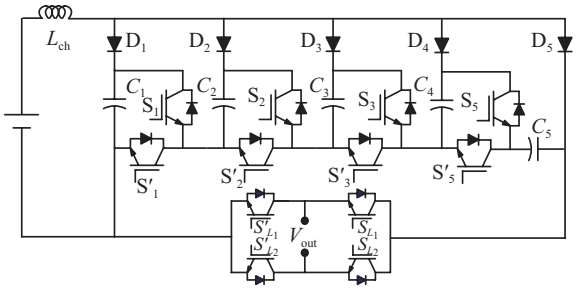

Fig. 8. Eleven-level configuration of the proposed topology.

TABLE IV
CHARACTERISTIC OF SIMULATED MODEL

Component	Value
DC voltage	65 V
Peak value of the output voltage	311 V
Fundamental frequency of the output voltage	50 Hz
L_{ch}	0.1 mH
C_1, C_2	470 µF
C_3, C_4	1200 µF
C_5	2200 µF
Switching frequency	6 kHz

components in Table III is assumed. As shown in Fig. 7, the proposed SC-CHMI offers a higher efficiency compared to the SC-CMI. The reason is that the proposed topology uses fewer switches, and thus switches are in the current path and the conduction power loss is lesser than that of the SC-CMI. It is worth mentioning that the SC-CMI and the proposed SC-CHMI provide higher efficiency in comparison with the CTMI and HFLMI topologies, due to eliminating the use of transformers.

III. SIMULATION RESULTS

In order to investigate the performance of the proposed SC-CHMI, an eleven-level configuration is simulated in Matlab/Simulink, which is depicted in Fig. 8. The LS-SPWM strategy is applied to compute the switching signals. The simulation parameters are listed in Table IV. The charging inductor and the capacitors are selected based on the calculations in (17) and (18). However, although the L_{ch} value obtained from (18) can avoid overvoltage under the no load condition, we choose a higher value for L_{ch}, in order to effectively mitigate the inrush current. Three scenarios including no-load, purely resistive, and resistive-inductive loading conditions, are considered to demonstrate the performance of the proposed SC-CHMI.

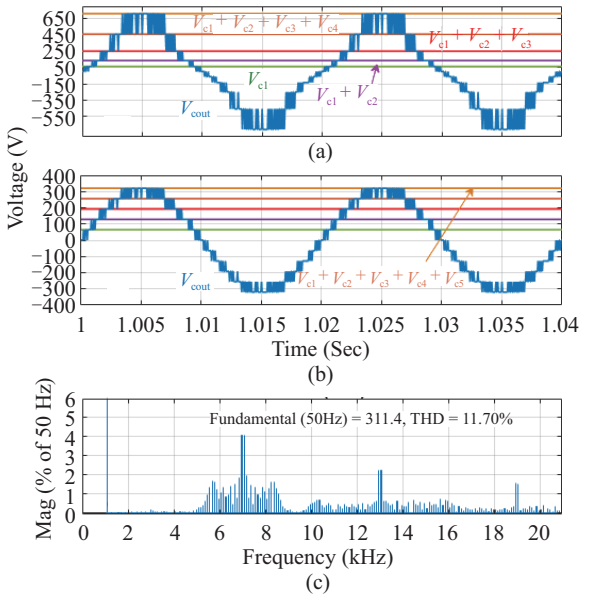

Fig. 9. Voltages of the capacitors and the output voltage at the start-up under no loading. (a) without and (b) with the soft-start strategy, and (c) FFT analysis.

Firstly, the no-load condition is simulated to investigate the overvoltages of the capacitors, which are depicted in Fig. 9(a). The peak voltage at the output is 630 V, which is twice the nominal voltage. This overvoltage under the no-load condition may damage the utilized components. Therefore, it is important to apply a soft starting strategy in order to avoid the overvoltage. There are several soft starting strategies [22]. One strategy is to increase the input voltage gradually and let the capacitors be charged gradually up to the rated voltage. In grid-connected mode, the gate signals are blocked for several cycles in order to get the capacitors charged to the rated voltage through the grid. The other solution is to connect a freewheeling diode to L_{ch}. This diode would provide a freewheeling path for the charging current as the voltage across the capacitors reaches the nominal value.

Using the soft starting strategy, the output and capacitors voltages are shown in Fig. 9(b) under the no-load condition, in which, the input voltage is gradually exerted to the inverter. It helps to keep the output voltage in the desired range as shown in Fig. 9(b). Moreover, the eleven-level configuration can boost the input dc voltage, with the input and output peak voltages being 65 V and 311 V, respectively. In addition, the capacitors are automatically charged up to the expected voltage value, without using any supplementary circuit.

The fast Fourier transform (FFT) analysis of the output voltage without an output filter under no-loading is exhibited in Fig. 9(c).

In the proposed SC-CHMI, the input current is mainly affected by the output active power. Therefore, a pure resistive load of 0.5 kW is considered, to investigate the dc side current.

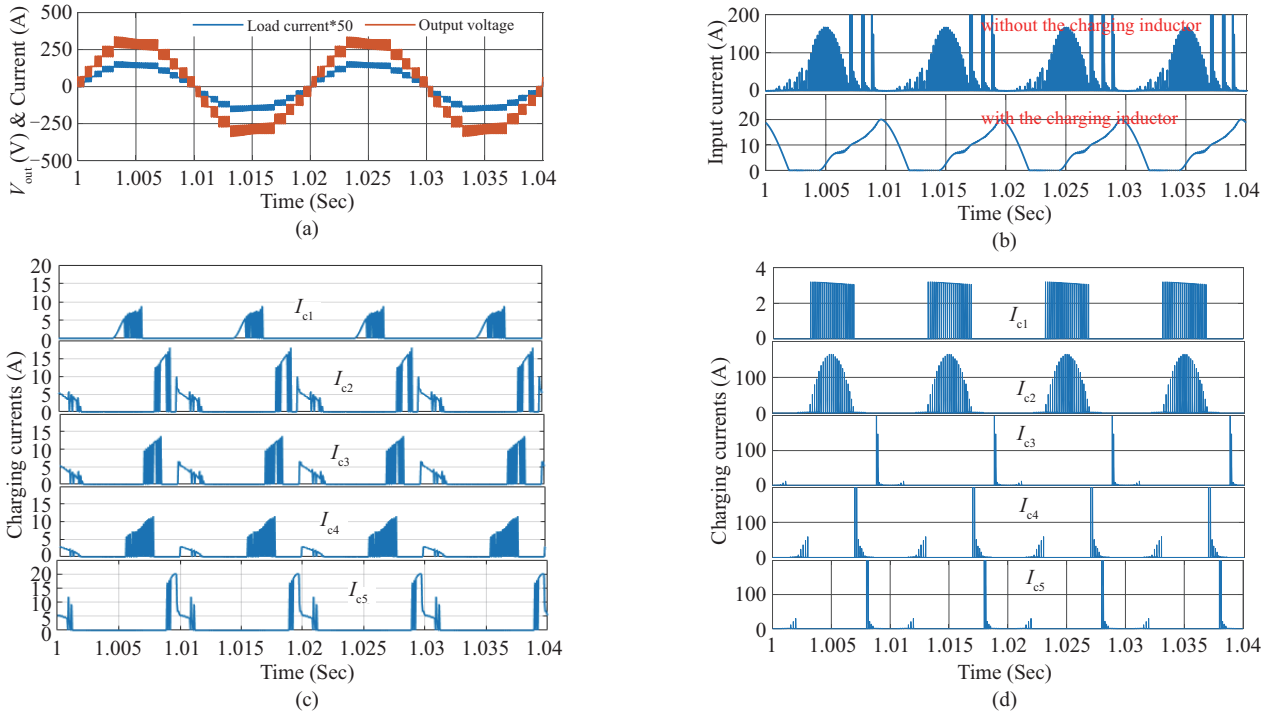

Fig. 10. Performance of the proposed SC-CHMI under purely resistive loading. (a) load current and output voltage, (b) input current with and without the charging inductor, (c) and (d) charging currents of the capacitors with and without employing the charging inductor.

Fig. 10(a) shows the output voltage and the load current. The input current is shown in Fig. 10(b), with and without the charging inductor in the proposed topology. As observed in Fig. 10, the input inrush current is significantly limited by the charging inductor. Moreover, the impact of the charging inductor on the capacitor charging currents is shown in Figs. 10(c) and (d). The results in Fig. 10 indicate that the charging inductor prevents the undesirable charging inrush currents.

The capability of the proposed SC-CHMI in providing reactive power, in accordance with the IEEE Standard 1547 [23], is evaluated with an inductive-resistive load of 0.461 kVA with the power factors (PF) of PF = 0.87. The output voltage and load current as well as the capacitor voltages under the mentioned load condition are depicted in Fig. 11(a) and (b), which shows that the proposed SC-CHMI can provide the required reactive power. As seen in Fig. 11(b) the capacitors in the uppermost cells experiences a higher voltage ripple compared with the lowermost capacitors. Furthermore, comparing the current in Fig. 11(a) with that in Fig. 10(a), it is evident that due to the inductive feature of the load, the high-frequency components of the load current are filtered out. Therefore, the load current is a purely sinusoidal waveform under inductive-resistive loading condition.

In order to assess the performance of the proposed topology with the front-end dc-dc boost converter under heavy loading condition, a purely-resistive load of 5 kW is considered. The developed voltages under the mentioned loading condition by considering the front-end boost converter and without it are, respectively, shown in Figs. 12 (a) and (b). Comparing

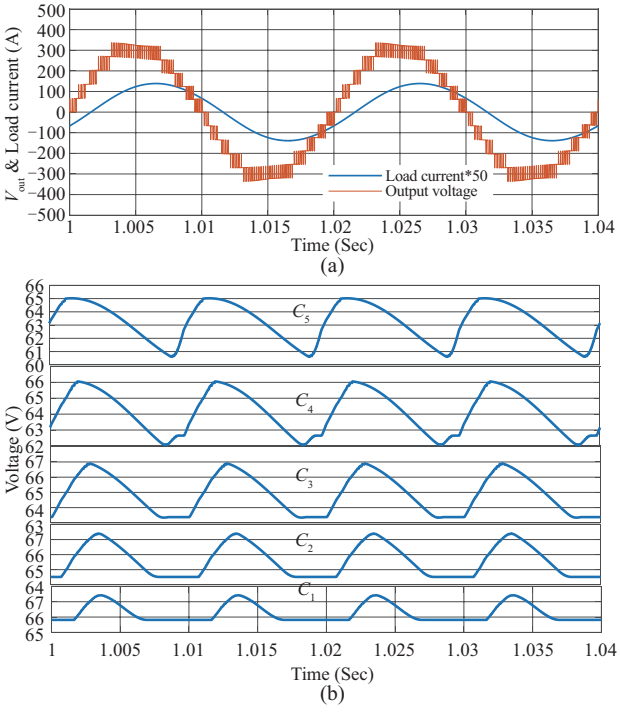

Fig. 11. Simulation results under inductive-resistive loading. (a) Load current and output voltage, and (b) voltages of the capacitors.

Figs. 12 (a) and (b), it can be seen that the voltage drop caused by the on-state impedances and voltages of the components is properly compensated by using the front-end dc-dc converter.

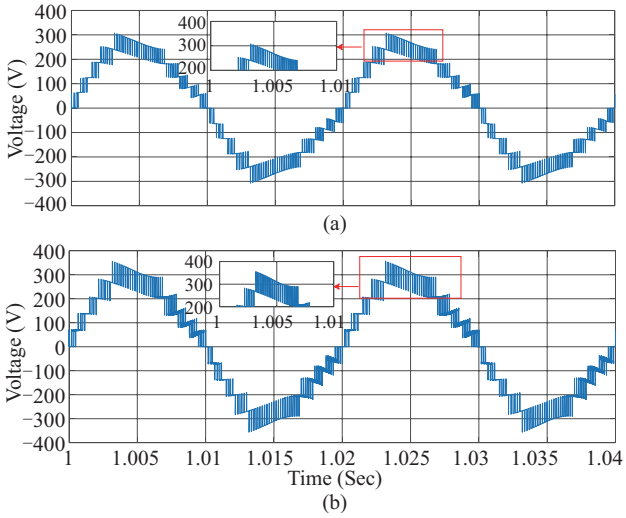

Fig. 12. Output voltage under a 5-kW load. (a) without and (b) with the frond-end dc-dc converter.

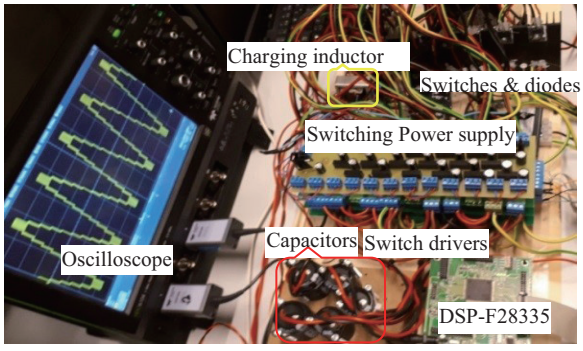

Fig. 13. Lab-scaled experimental setup of the proposed eleven-level inverter.

TABLE V
ELECTRICAL PARAMETERS AND COMPONENTS SPECIFICATIONS OF THE PROTOTYPE

Component	Specification	Electrical parameter	Value
Main Switches	IRFP250	Pure resistive load	500 W
Opto-coupler	TLP250	Inductive-resistive load	650 VA PF=0.89
Capacitors	3300 μF	Reference ac voltage	220 V, 50 Hz
Charging inductor	0.36 mH	Input dc voltage	65V
Diodes	RB238T100	Switching frequency	5 kHz

IV. EXPERIMENTAL RESULTS

In the following, a lab-scale eleven-level prototype is developed to investigate the viability and performance of the proposed SC-CHMI. The switching signals are computed using the digital signal processor DSP-F28335 and the LS-SPWM switching method. The implemented prototype is depicted in Fig. 13, and the components are shown in Table V.

Similar to the simulations, three scenarios are investigated for the proposed SC-CHMI topology. In the first scenario, the performance of the prototype is tested under a no-load condition. The output voltage and its FFT analysis in the

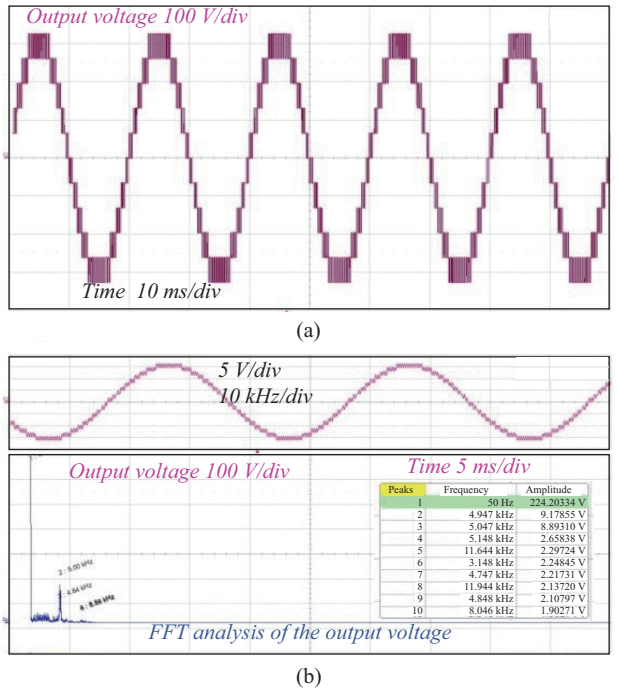

Fig. 14. Experimental results of proposed eleven-level topology under no-loading condition. (a) The output voltage and (b) FFT analysis of the output voltage.

first scenario (i.e. no loading) are shown in Figs. 14(a) and (b), respectively. The proposed topology has successfully developed the qualitative ac voltage of 220 V from the input dc voltage of 65 V, proving its boosting ability. As shown in Fig. 14(b), the frequencies of the voltage harmonics with the high magnitude are around the multiples of the switching frequency and thus far from the fundamental frequency. This is already proven in Section III, in which the switching frequency was 6 kHz and the high frequency harmonics appear around the multiples of 6 kHz, as shown in Fig. 14. Consequently, these harmonics can easily be eliminated by using a small low-pass filter (LPF). Moreover, the switching frequency in MIs can be decreased with respect to the number of voltage levels. There are several optimized switching methods to further reduce the switching frequency, e.g. the synchronous optimal PWM method can reduce the switching frequency to ten times the fundamental frequency [24]. Nonetheless, it is not aimed to optimize the modulation method in this paper and thus the switching frequency is arbitrary chosen to be 5 kHz for demonstration.

In the second scenario, the prototype is tested with a 500 W purely-resistive load. As mentioned before, the charging current of the proposed SC-CHMI is directly related to the output active power. The capacitors experience high charging currents in the purely resistive loading condition, as depicted in Fig. 15(a). According to Fig. 15(a), the charging inductor in the dc side significantly limits the inrush current of the capacitors. Moreover, the ac components of the capacitor voltage ripples are shown in Fig. 15(b). The capacitor C_5 takes part in all levels and thus experiences the largest voltage ripple, while

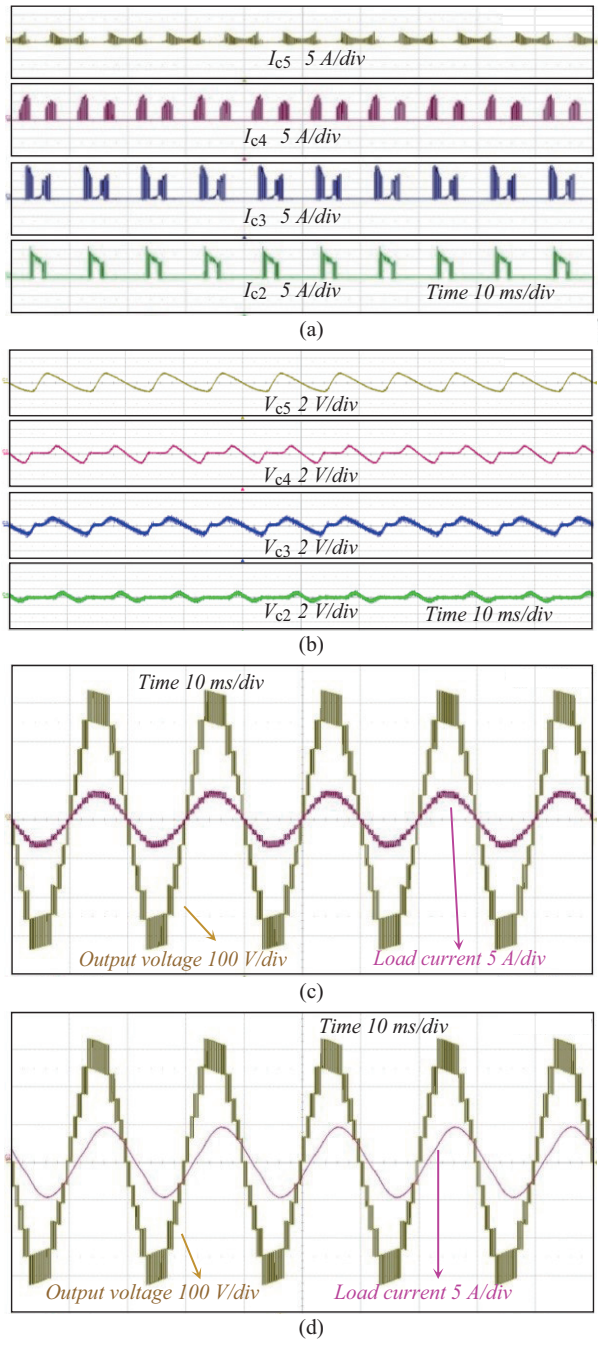

Fig. 15. Experimental verification of the proposed topology. (a) Charging currents of the capacitors, (b) the ac components of the capacitor voltages, (c) load current and output voltage under purly resistive loading, and (d) load current and output voltage under the resistive-inductive loading.

the capacitor C_1 participates only in the highest level and thus experiences the lowest voltage ripple, as observed in Fig. 15(b). Moreover, the load current and the output voltage in the second scenario (i.e. purely-resistive loading) are shown in Fig. 15(c).

In the third scenario, a resistive-inductive load with the power of 650 VA and the power factor of PF = 0.89 is used to evaluate the capability of the prototype in providing reactive power. The load current and output voltage are shown in Fig. 15(d). It is obvious that the proposed SC-CHMI provides reactive power in the output. The simulation results and the experimental tests have confirmed the viability of the proposed SC-CHMI topology in providing reactive power and generating low-harmonic voltages with one dc source.

V. Conclusion

This paper proposed a new single-source switched-capacitor cascaded half-bridge multilevel inverter (SC-CHMI) topology. The proposed SC-CHMI requires only one dc source and a reduced number of switches. The proposed topology features boosting capability and provides higher efficiency. Furthermore, the proposed SC-CHMI topology has a modular structure and can be scaled-up to a desired voltage level. In order to eliminate the inrush currents in the charging stages of the proposed topology, the capacitors are charged through a charging inductor. The feasibility and viability of the proposed topology are verified through the simulation results as well as the lab-scaled experimental tests. The performance of the proposed SC-CHMI was evaluated in no-load, purely resistive, and resistive-inductive loading conditions. The results have confirmed the applicability and improved performance of the proposed SC-CHMI in terms of the capacitor charging currents, the input inrush current, the output current waveform, and the capability to provide reactive power.

References

[1] M. Tariq, M. Meraj, A. Azeem, A. I. Maswood, A. Iqbal, and B. Chokkalingam, "Evaluation of level-shifted and phase-shifted PWM schemes for seven level single-phase packed U cell inverter," in *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 3, pp. 232–242, Sept. 2018.

[2] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[3] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," in *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, Mar. 2019.

[4] A. Yazdani and R. Iranvani, *Voltage source converters in power systems, Modeling, Control, and Applications*. Hoboken, New Jersey: John Wiley & Sons, Inc, 2010.

[5] H. N. Avanaki, R. Barzegarkhoo, E. Zamiri, Y. Yang, and F. Blaabjerg, "Reduced switch-count structure for symmetric multilevel inverters with a novel switched-DC-source submodule," in *IET Power Electronics*, vol. 12, no. 2, pp. 311–321, Feb. 2019.

[6] M. R. Banaei, H. Khounjahan, and E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," in *IET Power Electronics*, vol. 5, no. 9, pp. 1748–1753, Nov. 2012.

[7] K. A. Kim, Y. Liu, M. Chen, and H. Chiu, "Opening the box: Survey of high power density inverter techniques from the little box challenge," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 131–139, 2017.

[8] J. Rodriguez, J. -S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[9] S. Thamizharasan, J. Baskaran, S. Ramkumar, and S. Jeevananthan, "A modular multilevel inverter with cascaded half bridge cells," in *Proceedings of 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Bengaluru, India, Dec. 16–19, 2012,

pp. 1–6.
[10] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," in *Energy Conversion and Management*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.
[11] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio DC–DC conversion," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015.
[12] R. Raushan, B. Mahato, and K. C. Jana, "Optimum structure of a generalized three-phase reduced switch multilevel inverter," in *Electric Power Systems Research*, vol. 157, pp. 10–19, Apr. 2018.
[13] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one dc source in asymmetric cascaded multilevel inverters," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3884–3892, Sept. 2011.
[14] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Multilevel medium-frequency link inverter for utility scale photovoltaic integration," in *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3674–3684, Jul. 2015.
[15] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016.
[16] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A single DC source cascaded seven-level inverter integrating switched-capacitor techniques," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7184–7194, Apr. 2016.
[17] H. Khounjahan, M. Abapour, and K. Zare, "Switched-capacitor based single source cascaded H-bridge multilevel inverter featuring boosting ability," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019.
[18] S. G. Song, F. S. Kang, and S. J. Park, "Cascaded multilevel inverter employing three-phase transformers and single dc input," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2005–2014, Jun. 2009.
[19] H. Khoun-Jahan, M. Naseri, M. M. Haji-Esmaeili, M. Abapour, and K. Zare, "Low component merged cells cascaded-transformer multilevel inverter featuring an enhanced reliability," in *IET Power Electronics*, vol. 10, no. 8, pp. 855–862, Jun. 2017.
[20] Y. Zhou, and H. Li, "Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems," in *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5265–5277, Oct. 2014.
[21] H. Khoun Jahan, M. Abapour, K. Zare, S. H. Hosseini, F. Blaabjerg, and Y. Yang, "A multilevel inverter with minimized components featuring self-balancing and boosting capabilities for PV applications," in *IEEE Journal of Emerging and Selected Topics in Power* Electronics, Early Access.
[22] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," in *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 409–415, Feb. 2009.
[23] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces, *IEEE Std 1547-2018*, pp.1–138, Apr. 2018.
[24] A. Edpuganti and A. K. Rathore, "Optimal low switching frequency pulsewidth modulation of nine-level cascade inverter," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 482–495, Jun. 2015.

Hossein Khoun-Jahan received the M.S. degree in electrical engineering from the University of Shahid Madani of Azerbaijan, Tabriz, Iran, 2011. He received the Ph.D. in power electric system at the University of Tabriz, Tabriz, Iran, 2019. He spent six months as a Visiting Scholar at Aalborg University, Aalborg, Denmark. He is currently a senior engineer at Azerbaijan Regional Electric Company, Tabriz, Iran. His main research interests are power electronic based converter, reliability of power electronic devises. Electric machines, Grid-connected PV systems, Distribution and Transmission systems, and renewable energy.

Amin Mohammadpour Shotorbani received the B.Sc. degree from University of Tabriz, Tabriz, Iran in 2009, the M.Sc. degree from Azarbaijan Shahid Madani University, Tabriz, Iran in 2012, and the Ph.D. degree from University of Tabriz, Tabriz, Iran in 2017, all in electrical engineering. He was a visiting research scholar at the University of British Columbia, Kelowna, BC, Canada from January 2016 to June 2016, and a postdoctoral research fellow at University of Tabriz, Tabriz, Iran from Sept. 2017 to June 2018. He is currently a postdoctoral research fellow at the University of British Columbia Okanagan, Kelowna, BC, Canada since July 2018. His main area of research is nonlinear and distributed control applications, stability of power systems, control of MMC VSC and Multi-terminal HVDC grids, operation of intelligent energy systems, microgrids, and renewables integration.

Mehdi Abapour received the B.Sc. and M.Sc. degrees in electrical engineering from The University of Tabriz, Tabriz, Iran, in 2005 and 2007, respectively, and the Ph.D. degree in electrical engineering from The Tarbiat Modares University, Tehran, Iran, in 2013. He is currently an Associate Professor with the School of Electrical and Computer Engineering, University of Tabriz. His research interests include reliability, energy management, power system protection, Power electronics, and transients.

Kazem Zare received the B.Sc. and M.Sc.degrees in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2000 and 2003, respectively, and the Ph.D. degree from Tarbiat Modares University, Tehran, Iran, in 2009. He is currently a Professor with the Faculty of Electrical and Computer Engineering, University of Tabriz. His research interests include power system economics, distribution networks, micro-grid, energy management, smart building, demand response, and power system optimization.

Seyed Hossein Hosseini was born in Marand, Iran, in 1953. He received the M.S. degree from the Faculty of Engineering, University of Tabriz, Tabriz, Iran, in 1976 with first class honors, and the DEA and Ph.D. degrees from the Institute National Polytechnique de Lorraine, Nancy, France, in 1978 with first class honors and 1981, respectively, all in electrical engineering.

In 1982, he joined the University of Tabriz as an Assistant Professor in the Department of Electrical Engineering. From September 1990 to September 1991, he was a Visiting Professor with the University of Queensland, Brisbane, Australia. From 1990 to 1995, he was an Associate Professor at the University of Tabriz.

Since 1995, he has been a full Professor at the Department of Electrical Engineering, University of Tabriz. From September 1996 to September 1997, he was a Visiting Professor with the University of Western Ontario, London, ON, Canada. Since January 2017 he is Professor with the Near East University of North Cyprus, Turkey. He is the author of more than 700 Journal and Conference papers. Being announced by the Thomson Reuters in December 2017, he became one of the World's Most Influential Scientific Minds – 1% Top Scientist of the World. His research interests include power electronics, application of power electronics in renewable energy sources, power quality issues, harmonics and VAR compensation systems, electrified railway systems and FACTS devices.

Frede Blaabjerg was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the Ph.D. degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the *IEEE Transactions on Power Electronics* from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019–2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

He is nominated in 2014–2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

Yongheng Yang received the B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, Shaanxi, China, in 2009 and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2014.

He was a postgraduate student with Southeast University, China, from 2009 to 2011. In 2013, he spent three months as a Visiting Scholar at Texas A&M University, USA. Currently, he is an Associate Professor with the Department of Energy Technology, Aalborg University, where he also serves as the Vice Program Leader for the research program on photovoltaic systems. His current research is on the integration of grid-friendly photovoltaic systems with an emphasis on the power electronics converter design, control, and reliability.

Dr. Yang is the Chair of the IEEE Denmark Section. He serves as an Associate Editor for several prestigious journals, including the *IEEE Transactions on Industrial Electronics*, the *IEEE Transactions on Power Electronics*, and the *IEEE Industry Applications Society (IAS) Publications*. He is a Subject Editor of the *IET Renewable Power Generation* for Solar Photovoltaic Systems. He was the recipient of the 2018 *IET Renewable Power Generation* Premium Award and was an Outstanding Reviewer for the *IEEE Transactions on Power Electronics* in 2018.