Reliability Enhancement of 1500-V DC-link Photovoltaic Power Converters

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RELIABILITY ENHANCEMENT OF 1500-V DC-LINK PHOTOVOLTAIC POWER CONVERTERS

BY
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DENMARK

Reliability Enhancement of 1500-V DC-link Photovoltaic Power Converters

Ph.D. Dissertation
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Abstract

Photovoltaic (PV) systems are becoming ever more popular in the power industry. It is expected that PV energy will share a more significant part in the world's future energy production. In this energy transition, the reduction of PV energy cost is of great importance. One standard solution is adopting the 1500-V PV strings instead of the 1000-V ones. By doing so, the installation cost, as well as the power losses (e.g., due to cabling), can be reduced significantly, which contributes to the cost reduction of PV energy. However, the increased PV voltage also poses challenges to PV inverters. The increased voltage stress has pushed the inverter design from the conventional two-level topology toward multi-level topology for achieving efficient and reliable power conversion. Although a few commercial PV power converters are already available on the market, the converter reliability assessment for this particular application is of high interest. Moreover, the control strategy should also be improved in order to maintain high reliability under the 1500-V operation.

Thus, this Ph.D. project has explored the design and control of 1500-V PV power converters with a focus on reliability enhancement. The research work can be divided into three major aspects: 1) comparative evaluation of 1500-V PV power converters in terms of reliability, 2) investigation of system parameters on the reliability of 1500-V PV power converters, and 3) thermal optimized control for more reliable and cost-effective 1500-V PV power converters.

Firstly, to design a reliable PV power converter, an early-stage converter reliability evaluation is of great importance in the design phase. A comparative thermal performance evaluation of 1500-V PV inverters based on standard two-level and three-level topologies has been presented in Chapter 2, which is based on the thermal stress analysis under constant power generation (CPG) control operation. The result comparison indicated that, compared with the two-level topology, the three-level topologies are more suitable for 1500-V PV applications due to their lower thermal stresses. Furthermore, the reliability performance of the three-level topologies, i.e., I-type and T-type, has been evaluated considering the influence of voltage stress, switching frequency, and mission profile. The results reveal that these factors have a significant

influence on the inverter lifetime and can be used to justify the topology selection for the corresponding systems.

Secondly, except for the topology selection for designing a highly reliable 1500-V PV system, it is also important to consider the impact of system parameters on the performance and reliability of PV power converters, which has been presented in Chapter 3. The performance of 1500-V PV systems with centralized string inverter solutions has been discussed, where the power losses on the main components, i.e., DC wires, inverters, AC filters, and isolation transformers, are estimated considering the impact of system voltage ratings. The comparison results indicate that the centralized string inverter solutions with higher DC and AC voltages outperform the solutions with lower DC and AC voltages in terms of loss and cost reduction (lower wire loss and fewer inverter units). In addition, the 1500-V PV-battery system has been investigated with a comparison of DC- and AC-coupled configurations. With the reliability analysis from the component level to the system level, the most lifetime-critical part in each level has been identified, which will be beneficial to the design of the PV-battery systems in terms of reliability.

Thirdly, considering the 1500-V PV applications, new reliability concerns are raised, which are related to the increased DC-link voltage stress. Several methods for improving the reliability of 1500-V PV inverters have been presented in Chapter 4. For the SiC-based 1500-V two-level PV inverters, the possibility for improving their reliability through the variable gate resistance design was investigated considering mission profiles. Compared with the fixed gate resistance design for the highest voltage stress, the proposed approach, i.e., the variable gate resistance, could vary the external gate resistance based on the DC-link voltage variation, minimizing the power loss thus the thermal stress while keeping a safe blocking voltage margin. The reliability improvements can also be achieved through the control in operation. A junction temperature control strategy has been proposed in Chapter 4. By applying this control strategy, the device junction temperature would not exceed a certain threshold value during operation, hence extending the device lifetime. Moreover, the solution for improving the thermal performance of PV inverters during abnormal grid conditions has also been explored. With the proposal to achieve an improved thermal balance among the power devices of the three-level I-type 1500-V PV inverters, a modified discontinuous modulation strategy has also been proposed in Chapter 4, where enhanced reactive power support is expected during low-voltage ride-through operations.

Resumé

Fotovoltaiske (PV) systemer er ved at blive en af de væsentlige vedvarende energikilder og spiller en voksende rolle i dagens elnet. Flere solcelleanlæg forventes at blive installeret i den kommende fremtid og vil dække en stor del af elproduktionen. I denne overgang, bør omkostningerne til PV-energi reduceres yderligere. En standardløsning er at øge den maksimale DC-link-spænding i PV-systemet fra de traditionelle 1000 V til 1500 V. Fordelen ved at gøre det er et betydeligt fald i installationsomkostningerne, strømtab (f.eks. på grund af kabler) og dermed omkostningerne til PV-energi. Den øgede DC-link-spænding stiller dog også en udfordring for PV-invertere, som er nøglekomponenterne for at opnå effektiv og pålidelig strømkonvertering. Den øgede spændings ved DC-forbindelsen har skubbet inverterdesignet fra den konventionelle to-niveauer topologi til multilevel topologi. Selvom nogle få kommercielle produkter allerede er tilgængelige på markedet, er vurderingen af konverterens pålidelighed for denne særlige anvendelse af stor interesse at blive undersøgt. Desuden bør kontrolstrategien også forbedres for at opretholde høj pålidelighed under 1500-V driften.

Denne ph.d. projektet har udforsket design og styring af 1500-V PV-strømomformere med fokus på øget pålidelighed. Forskningsarbejdet kan opdeles i tre hovedaspekter: 1) Komparativ evaluering af 1500-V PV-effektomformere med hensyn til pålidelighed, 2) Undersøgelse af systemparametre vedrørende pålideligheden af 1500-V PV-effektomformere og 3) Termisk optimeret styring for mere pålidelige og omkostningseffektive 1500-V PV-strømomformere.

For det første, for at sikre en effektiv og pålidelig PV-effektkonvertering, er en tidlig pålidelighedsvurdering vigtig i designfasen af PV-strømkonverteren og derefter hele systemet. En sammenlignende termisk ydeevneevaluering af 1500-V PV-invertere baseret på to-niveau- og tre-niveau-topologier er præsenteret i kapitel 2, som er baseret på den termiske spændingsanalyse under konstant strømgenerering (CPG). Resultaterne indikerede, at sammenlignet med to-niveau-topologien er tre-niveau-topologierne mere egnede til 1500-V PV-anvendelser på grund af deres lavere termiske stress. Derudover blev pålidelighedsydelsen af de to tre-niveau topologier (dvs. I-type og T-type)

evalueret med hensyn til virkningen af spænding stress, switching frekvens og missionsprofil. Resultaterne afslører, at disse faktorer har en betydelig indflydelse på inverterens levetid og kan bruges til at retfærdiggøre valget af topologier for tre-niveau inverterne i de tilsvarende systemer.

For det andet, bortset fra topologivalget til at designe et yderst pålideligt 1500-V PV-system, er det også vigtigt at overveje indvirkningen af systemparametre på ydeevnen og pålideligheden af PV-strømomformere, som blev præsenteret i kapitel 3. Ydeevnen af 1500-V PV-systemer med centraliserede strenginverterløsninger blev diskuteret, hvor effekttabene på hver hovedkomponent, dvs. DC-ledninger, invertere, AC-filtre og isolationstransformatorer, er estimeret under med hensyn til forskellige DC- og AC-sider spændingsværdier. Sammenligningsresultaterne indikerer, at strenginverterløsningerne med højere DC- og AC-spændinger overgår løsningerne med lavere DC- og AC-spændinger med hensyn til tab og omkostningsreduktion (lavere ledningstab og mindre antal inverterenheder). Derudover er 1500-V PV-batterisystemet blevet undersøgt med en sammenlignende pålidelighedsanalyse af to konfigurationer, dvs. DC-kobling og AC-kobling. Med pålidelighedsanalysen på komponent-, konverter- og systemniveau er den mest skrøbelige del i hvert niveau blevet identificeret, hvilket bidrager til PV-batterisystemernes design-til-pålidelighed.

For det tredje, i betragtning af 1500-V PV-anvendelser, rejses nye pålidelighedsproblemer, som er relateret til den øgede DC-link spændingsstress. Visse metoder til at forbedre pålideligheden af 1500-V PV-invertere blev præsenteret i kapitel 4. For de SiC-baserede 1500-V to-niveau PV-invertere er en variabel hastighed gate-driver blevet foreslået. Den kan justere gate modstandmodstanden i henhold til variationen af DC-linkspændingen i takt med missionsprofilen. Ved at gøre det kan switching overshoot på grund af den spredte induktans i kommutationsloop reduceres, når PV-array-spændingen er høj, hvilket holder strømenhederne inden for deres spændingsværdier. De tilsvarende pålidelighedsvurderingsresultater indikerer, at PV-inverteren med det foreslåede design har en bedre levetidsydelse end den med gatedrivere med fast hastighed, hvor gatemodstanden typisk er designet til de højeste spændingstress. Pålidelighedsforbedringerne kan også opnås gennem kontrol i drift. En overgangstemperaturstyringsstrategi er foreslået i kapitel 4. Hermed kan overgangstemperaturen for effektenhederne i PV-inverteren holdes under en vis grænse under drift, og dermed reducere temperaturvariationerne. Desuden er løsningen til at forbedre den termiske ydeevne af PV-invertere under unormale netforhold også blevet undersøgt. Med forslaget om at opnå en forbedret termisk balance mellem effektenhederne i tre-niveau 1500-V PV-inverterne, er en modificeret diskontinuerlig moduleringsstrategi også blevet foreslået i kapitel 4, hvor en avanceret reaktive strøm sunderstøttelse forventes under low-voltage-ride-through tilfælde.

Preface

This Ph.D. thesis is written in connection to the Ph.D. project entitled "Reliability Enhancement of 1500-V DC-link Photovoltaic Power Converters". This Ph.D. project is supported by AAU Energy, Aalborg University, Denmark, and China University of Petroleum (East China). In addition, I would like to convey my acknowledgments to the Center Of Reliable Power Electronics (CORPE) and Otto Mønsteds Fond, who supported me in the conference participation and study abroad during my entire Ph.D. study.

This Ph.D. project was done under the supervision of Prof. Francesco Iannuzzo, Assist. Prof. Ariya Sangwongwanich, and Prof. Yongheng Yang. I would like to express my heartfelt gratitude to them, for their patient guidance and insightful suggestions during the study. It was their support and encouragement that made me feel confident to complete my Ph.D. study.

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Also, I would like to thank all my colleagues at AAU energy, Aalborg University for their help and support, as well as for the living environment and the endless friendship.

In particular, I take this opportunity to express my thanks to Prof. Rende Zhao from China University of Petroleum (East China). His encouragement and support gave me much strength during the entire Ph.D. study.

Finally, I would like to extend my deep gratefulness to my family, especially my wife Lu, for their unconditional love and care, which are the source of my energy.

Jinkui He
Aalborg University, November 24, 2021

Contents

Report

Chapter 1

Introduction

This chapter firstly introduces the background of the Ph.D. project. Then, a short state-of-the-art is presented, followed by the project motivation. Accordingly, the research questions and objectives are summarized. After that, the outline of the Ph.D. thesis is presented to show the overview of this research work. All the research outcomes during this Ph.D. study are provided at the end of this chapter.

1.1 Background

Photovoltaic (PV) systems have become dominant in renewable energy applications. It is expected that more utility-scale PV systems will be installed, and solar energy will account for a major part of the energy production in the future [1–3]. In order to increase the generation capacity of PV systems, the common strategy is to use a large number of combiner boxes to parallel the PV strings, and thus increasing the output current. However, this usually results in a high number of cables, increasing power losses and installation costs, and thereby limiting the competitiveness of large-scale PV power plants. In fact, recent studies have shown that, for increasing PV system capacity, higher PV string /DC-link voltage, i.e., with more PV panels connected in series, could be a cost-effective solution [4–7]. A higher DC-link voltage operation can considerably reduce the requirements of Balance of Systems (BOS), hence the installation cost. By doing so, the ohmic losses in the DC wires can be reduced, which brings the potential to increase the system efficiency. Accordingly, the maximum PV string voltage has been increased from 1000 V to 1500 V in the relevant international standards [8]. Adopting 1500-V PV inverters has quickly become the mainstream in the newly built large-scale PV plants due to its potential in reducing installation costs. As shown in Fig. 1.1, 1500-V PV inverters have already accounted for over 50% of high power PV inverter

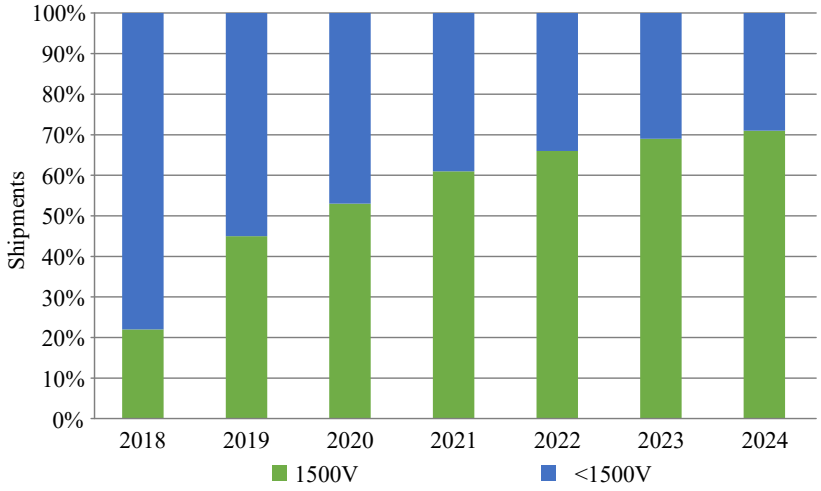


Fig. 1.1: Global trend of three-phase PV inverter shipments by voltage [9].

shipments in 2020, in comparison to just 22% two years earlier [9]. It is also predicted that, by 2024, 54% of new PV inverters will be utility-scale, and 1500-V PV systems are forecast to account for 70% of global three-phase shipments.

Nevertheless, the increased voltage stress at the DC-link imposes new challenges for the PV power inverter. Fig. 1.2 shows the generic structure of 1500-V grid-connected PV system. The increased PV voltage requires careful consideration when designing and controlling the PV inverters, which play a key role in achieving the power conversion reliably and efficiently. For instance, the use of two-level inverters, which is a popular solution in 600-/1000-V PV systems, may be challenging for 1500-V ones, as it would result in high power losses in the semiconductors and increased filtering efforts in the outputs. As a consequence, shifting to multi-level topologies is the trend. Although a number of commercial products [10, 11], based on two-level or multi-level topologies, are already available on the market, the converter reliability for this particular application is of high interest to be investigated. The main goal of 1500-V PV applications is cost reduction, which should be achieved without introducing adverse impacts on PV power converters.

The reliability improvements can be achieved in the design phase (Design for Reliability), but also in operation, via a smart control. For instance, by applying a proper active thermal control strategy, the thermal loadings of the lifetime-critical components (e.g., DC-link capacitors and power semiconductors) can be reduced, achieving improved reliability of the overall system [12, 13].

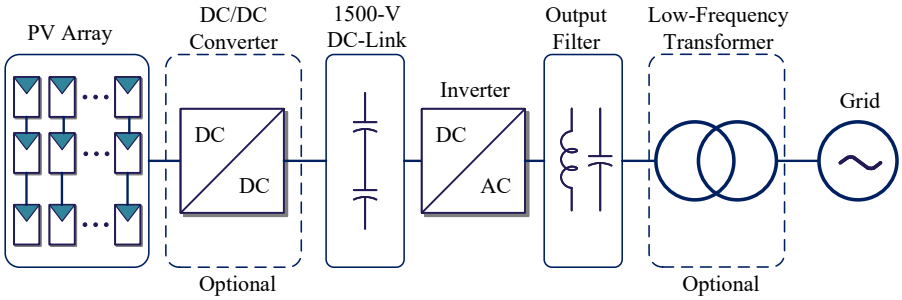


Fig. 1.2: Generic structure of a 1500-V grid-connected PV system.

1.2 State of the Art

As mentioned, to ensure a reliable PV system, the reliability performance of the 1500-V PV inverters should be investigated. At the same time, design and control may be explored and revised to achieve the reliability enhancement of the 1500-V PV power converters. The relevant state-of-the-art is reviewed in this section.

1.2.1 Topologies to Accommodate the 1500-V DC-Link Voltage

This 1500-V DC voltage requirement certainly affects the choice of the inverter topologies. The conventional two-level topology in Fig. 1.3(a), which is the mainstream for low-voltage applications thanks to its simplicity, has several drawbacks when the voltage stress at the DC-link is high. Power devices with high blocking-voltage capability are required, resulting in higher power losses, lower switching speeds, hence increased filtering efforts. To improve the inverter performance at the higher PV string voltage, i.e., 1500 V, multi-level topologies are preferred alternatives due to their superior features like low output harmonic distortion, decreased power losses, and reduced dv/dt stress [14]. The two standard three-level topologies, i.e. the I-type one in Fig. 1.3(b) and the T-type one in Fig. 1.3(c), are the most popular choices. For the inverter applications with lower DC voltage rating, i.e., $\leq$ 1000 V, the preferred choice is the T-type topology due to its advantages in efficiency and power quality [15]. However, at 1500 V, the I-type topology seems to be a more promising alternative due to its superiority in blocking-voltage capability [16]. For the I-type topology, All the IGBTs and diodes (referring to Fig. 1.3(b)) only require to withstand 50% DC-link voltage during blocking states. Thanks to this feature, power devices with 900-V to 1200-V voltage ratings would be enough to guarantee safety when applying the I-type topology in 1500-V PV applications. In contrast, the T-type topology would require switches with a higher blocking voltage ($\geq$ 1700 V). For an even higher DC-link voltage

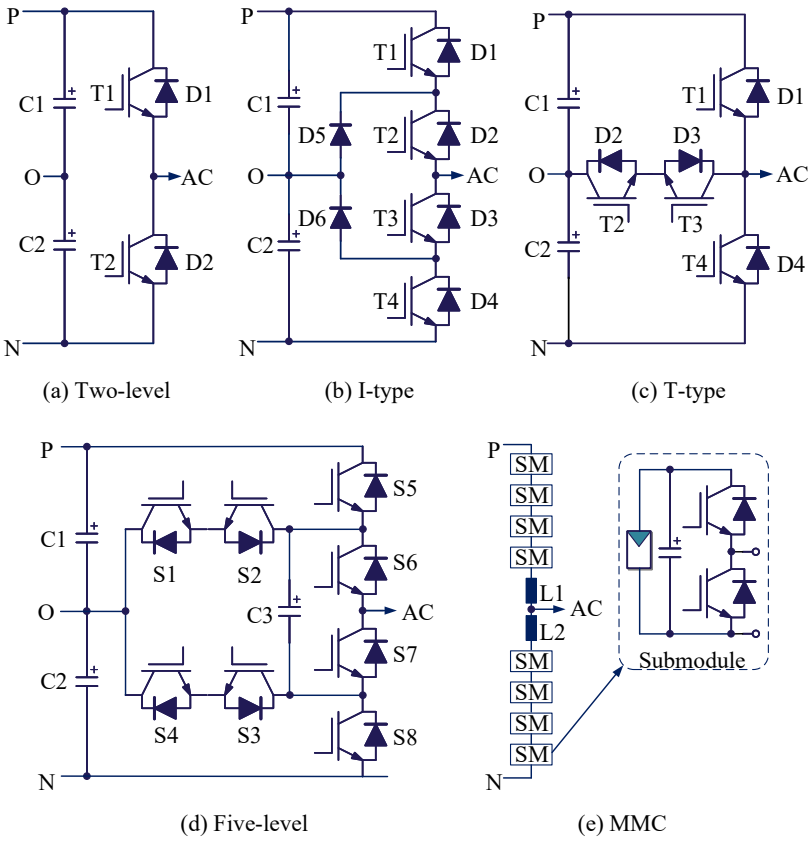


Fig. 1.3: Possible inverter topologies for 1500-V DC-link PV power inverters.

(> 1500 V), five-level topologies (see Fig. 1.3(d)) and modular multi-level converters (e.g., Fig. 1.3(e)) may be suitable with the trade-off in the control complexity and gate driving effort [17, 18]. These multi-level topologies can also be applied in the 1500-V PV systems with increased component count and control complexity. Overall, considering the 1500-V DC-link operation, a comprehensive comparison should be made to benchmark the performance of different PV inverter topologies.

1.2.2 Factors Affecting Reliability

considering a long-term operation, the PV power converters are less reliable in comparison to other components in PV systems. In general, the reliability of PV power converters is limited by two main critical components: power devices and DC-link electrolytic capacitors [19].

It has been reported that the thermal fatigue of power modules is one of

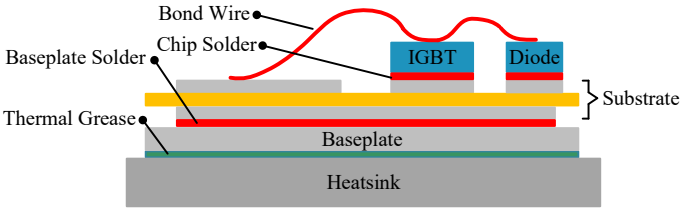


Fig. 1.4: Principle cross-section of an IGBT module.

the most wearing-out factors, which may lead to failures and destruction [20]. Fig. 1.4 shows the principle cross-section of an IGBT module, where different materials are used, also implying various coefficients of thermal expansion (CTE). Due to the CTE difference between the bond wire (aluminum) and the silicon chip, cracks occur at their interface due to temperature swings during operation. For the same reason, fatigue of the baseplate solder joint could appear.

For PV applications, the power converter's electrical and thermal stresses are strongly affected by the mission profiles of the installation sites, i.e., solar irradiance and the ambient temperature. Based both on real mission profiles and the knowledge of the PV system architecture, a meaningful reliability estimation of PV power converters can be performed. Bearing this in mind, the influence of PV array sizing [21], panel degradation [22], voltage and power control [12, 23], gate driver parameters [24], modulation methods [25], and battery energy storage integration [26], on remaining useful lifetime (RUL) has been analyzed for residential PV systems. These attempts provide guidelines for the design-for-reliability (DfR) of PV power converters with lower PV-array voltage (< 1000 V). However, for 1500-V PV power converters, the same conclusions may not apply as-is, e.g., due to the different topology adopted.

1.2.3 Design and Control for Improving Reliability

In general, there are various stressors, i.e., voltage, current, temperature, temperature cycling, humidity, and their combinations, that affect the reliability and failure rate of power semiconductors and DC-link capacitors [27]. Considering the 1500-V DC-link operation, one of the main reliability concerns is related to the increased voltage stress. In the case of adopting the two-level inverter topology for 1500-V PV inverters, the 1700-V power devices may not be specifically applicable [6, 28]. Moreover, the high voltage stress can increase the power semiconductor's failure rate caused by the impact of cosmic radiation [29]. For instance, the Sunny Central 2500-EV inverter of SMA Technology, which is based on the two-level topology, employs a series-connection (2 × 1200 V IGBTs), in order to ensure the voltage stress margin considering the

cosmic rays failure [30]. However, the series-connection method would increase the conduction losses and the gate driver effort. In [6], the performance characterization of 2500-V SiC MOSFETs was reported, and the potential application of this device for 1500-V PV inverters was also evaluated. However, the 2500-V SiC MOSFET has not yet been made commercially available.

Power device's reliability can also be significantly affected by thermal stresses (e.g., thermal cycling) [31]. Here, the operating conditions play an important role in the thermal stresses of these reliability-critical components. On the one hand, the operating condition is affected by the available PV power, which is determined by its mission profile, i.e., the solar irradiance and ambient temperature. On the other hand, control strategies like limiting power injection, reactive power injection, and Maximum Power Point Tracking (MPPT) operation also impose power loss variations and thereby thermal stress on the components [12, 32, 33]. Alternatively, advanced control strategies can be applied to reduce thermal loading. In [12], a hybrid power control strategy was proposed for PV applications, which can improve the PV inverter's thermal performance thus its utilization factor. In [33], a "lifetime-optimized" MPPT scheme was proposed to restrict the maximum junction temperature and reduce the thermal stress variation caused by fast-varying solar irradiance. In order to control the thermal stress of power devices, in [32], a thermal optimized control strategy for PV inverters was proposed considering the low-voltage-ride-through (LVRT) operation, where the thermal performance enhancement was achieved by reassigning the active and reactive power of the PV inverters. However, how to design control strategies for reducing thermal stresses on 1500-V PV inverters has not been extensively discussed yet.

In order to achieve the design and control for reliability, a reliability evaluation should be performed [34]. It mainly involves five steps, as shown in Fig. 1.5): 1) mission profile to thermal loading translation [35], 2) thermal cycling interpretation [36], 3) lifetime consumption estimation, 4) component-level reliability analysis, and 5) system-level reliability analysis [37]. This reliability evaluation approach will be used to investigate the reliability performance of the 1500-V PV power converters under different operating conditions.

1.3 Project Motivation

Based on the state-of-the-art, further attempts should be made to bridge the following research gaps. Firstly, it is necessary to make a comprehensive comparison to benchmark the performance of different inverter topologies for 1500-V applications. Secondly, it is important to consider the impact of system parameters on the reliability of 1500-V PV power converters. Thirdly, it is attractive to explore design and control solutions to guarantee the reliable operation of 1500-V PV power converters.

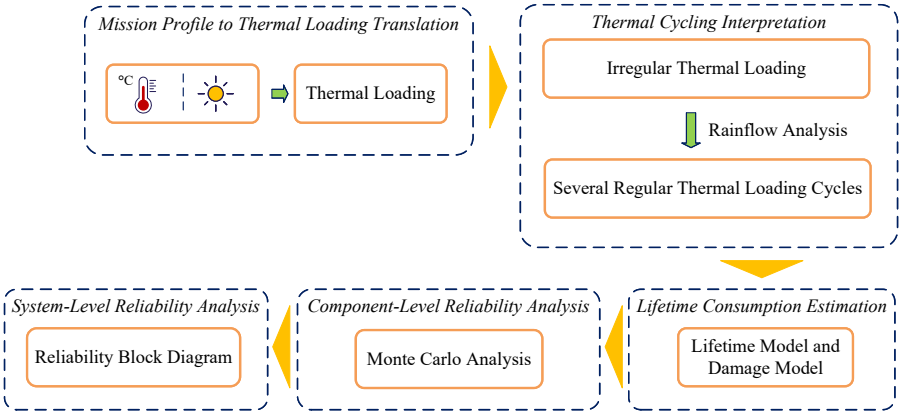


Fig. 1.5: Flowchart of the mission profile-based reliability assessment of PV inverters.

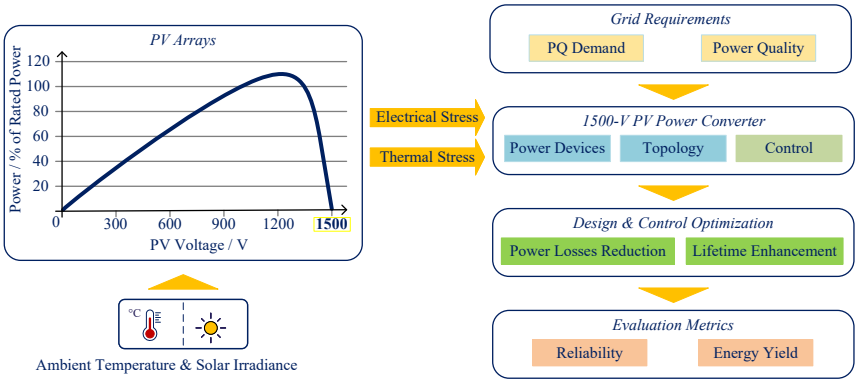


Fig. 1.6: Objective of this Ph.D. work: reliability enhancement of 1500-V PV power converters.

The above research gaps initiated this Ph.D. project. In summary, the main motivation is to investigate how the increased DC-link voltage affects the reliability performance of PV power inverters, hence developing viable design and control solutions to ensure a reliable energy conversion while fulfilling the grid requirements, as summarized in Fig. 1.6.

1.4 Research Questions and Objectives

1.4.1 Research Questions

The objective of this Ph.D. project is twofold: to reduce power losses hence reducing the temperature swing and to enhance the reliability of 1500-V DC-

link PV power converters. As a result, the fundamental research hypothesis is formulated as:

- How to improve the reliability of 1500-V DC-link PV power converters through design and control strategies?

Accordingly, some subsequent research questions can be formulated as:

- What is the most suitable inverter topology to be applied in the 1500-V technology considering reliability?
- How do the system parameters affect the reliability of the 1500-V PV power converters?
- How to improve the PV inverter's control to enhance its reliability?

1.4.2 Project Objectives

Bearing the above in mind, the objective of this Ph.D. project is to investigate the performance of inverters potentially used in 1500-V DC-link PV systems, with a special focus on design and control for enhancing reliability. More specifically, this project is dedicated to:

- Compare the performances of the state-of-the-art PV inverter topologies considering the 1500-V DC-link operation in terms of reliability.
- Investigate the impact of system parameters on the inverter reliability, and provide principles for achieving sufficient reliability performance.
- Propose viable design and control solutions to achieve high reliable 1500-V DC-link PV converters.

1.5 Thesis Outline

Fig. 1.7 shows the structure of this Ph.D. thesis, which includes two parts: the report and the selected publications. The report summarizes the research outcomes of this Ph.D. project and contains five chapters. Fig. 1.7 also illustrates the relationship between the selected publications and the main body of the report, i.e., *Chapters 2 to 4*. The list of publications is presented at the end of this chapter. A brief introduction of each chapter is given here below:

- **Chapter 1** has given the introduction of the Ph.D. project by presenting the background, state-of-the-art, motivation, research questions, and project objectives.

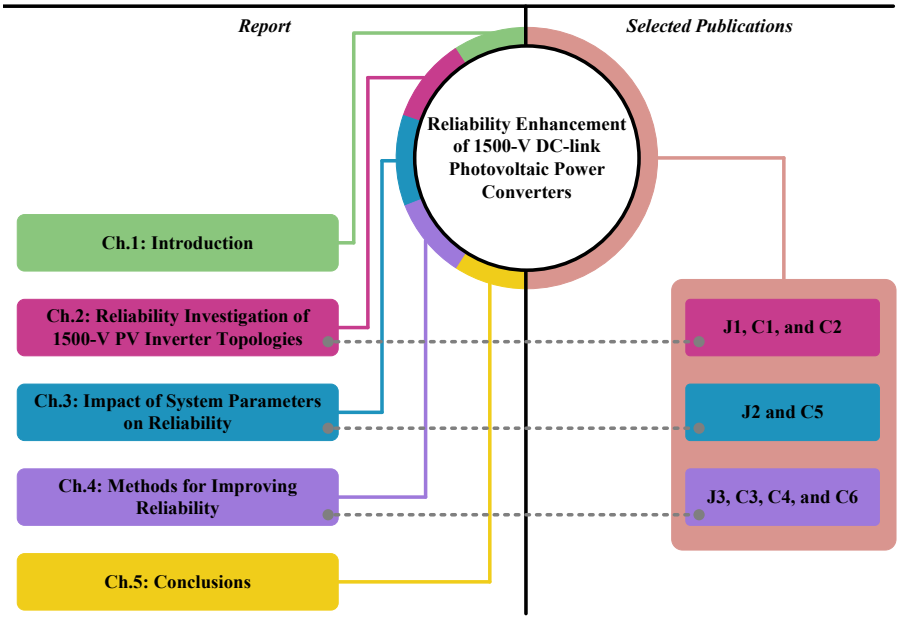


Fig. 1.7: Structure of this Ph.D. thesis: relationship between the report and the selected publications.

- Based on [J1], [C1], and [C2], **Chapter 2** presents a comparative reliability assessment of two-level and three-level 1500-V PV inverters on the base of the thermal stress analysis of these inverter topologies considering the impact of voltage stresses, switching frequencies, and mission profiles.
- Based on [J2] and [C5], **Chapter 3** investigates the impact of system parameters on the PV inverter reliability, where two aspects are considered, one is the system voltage rating, another is the integration of battery energy storage systems.
- Based on [J3], [C3], [C4], and [C6], **Chapter 4** presents design and control solutions to enhance the reliability of 1500-V PV inverters during operation. Possible solutions are discussed, i.e., variable gate resistance design for SiC-based two-level inverter, junction temperature limit control, and discontinuous modulation strategy during low-voltage ride through.
- Finally, **Chapter 5** gives the concluding remarks and the main contributions of this Ph.D. project. The future research perspectives are also outlined in this chapter.

1.6 List of Publications

The research outcomes from the Ph.D. project have been disseminated in the form of publications, i.e., journal papers and conference publications, as listed below. Selected papers are summarized and used in the Ph.D. dissertation as previously listed.

Journal Papers

J1. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime Evaluation of Three-Level Inverters for 1500-V Photovoltaic Systems" *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4285-4298, Aug. 2021.

J2. **J. He**, Y. Yang, and D. Vinnikov, "Energy Storage for 1500 V Photovoltaic Systems: A Comparative Reliability Analysis of DC- and AC-Coupling" *Energies*, vol. 13, no. 13, pp. 3355, Jul. 2020.

J3. **J. He**, A. Sangwongwanich, Y. Yang, K. Zhang, and F. Iannuzzo, "Design for Reliability of SiC-MOSFET-Based 1500-V PV Inverters with Variable Gate Resistance" *IEEE Trans. Ind. Appl.*, awaiting submission, Nov. 2021.

Conference Papers

C1. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Thermal Performance Evaluation of 1500-VDC Photovoltaic Inverters Under Constant Power Generation Operation," in *Proc. IEEE CPERE*, pp. 579-583, Oct. 2018.

C2. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime Evaluation of Power Modules for Three-Level 1500-V Photovoltaic Inverters," in *Proc. IEEE APEC*, pp. 430-435, Mar. 2020.

C3. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Design for Reliability of SiC-MOSFET-Based 1500-V PV Inverters with Variable Gate Resistance," in *Proc. IEEE ECCE*, pp. 1850-1855, Oct. 2020.

C4. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Enhanced Reliability of 1500-V Photovoltaic Inverters with Junction Temperature Limit Control," in *Proc. IEEE ECCE-Asia*, 2020, p. 1850-1855, May 2021.

C5. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Performance Comparison of PV Inverter Systems Considering System Voltage Ratings and Installation Sites," in *Proc. IEEE APEC*, pp. 2620-2625, Jun. 2021.

C6. **J. He**, A. Sangwongwanich, Y. Yang, Z. Quan, Y. Li, and F. Iannuzzo, "Discontinuous Modulation for Improved Thermal Balance of Three-Level 1500-V Photovoltaic Inverters under Low-Voltage Ride-Through," in *Proc. IEEE ECCE*, pp. 103-108, Oct. 2021.

The publications done during the study but not included in the Ph.D. thesis are listed below:

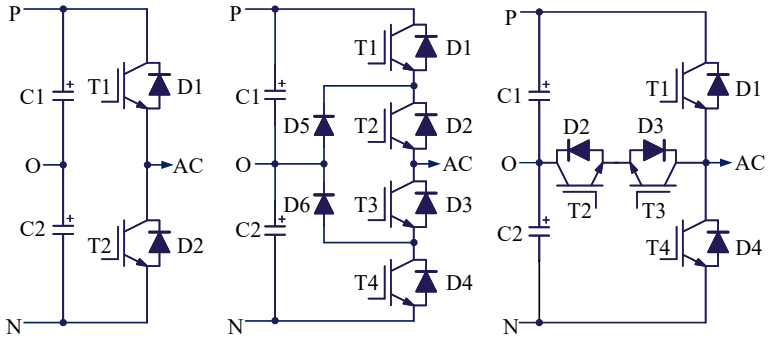
- A. Sangwongwanich, **J. He**, and Y. Pan, "Advanced Power Control of Photovoltaic Systems," Control of Power Electronic Converters and Systems, 1st ed., Frede Blaabjerg, Ed.: Academic Press, 2021, ch. 15.

- K. A. Khan Niazi, Y. Yang, **J. He**, A. Z. Khan, and D. Sera, "Switched-Capacitor-Inductor-based Differential Power Converter for Solar PV Modules," in *Proc. IEEE ECCE*, pp. 4613-4618, Sep. 2019.
- G. Li, R. Zhao, **J. He**, H. Xu, and Q. Yan, "An Improved Boost Dual-Loop Control for Improving the MPPT Efficiency in Photovoltaic Systems," in *Proc. IET RPG*, pp. 1-8, Sep. 2019.

Chapter 2

Reliability Investigation of 1500-V PV Inverter Topologies

This chapter presents a comparative reliability investigation of the two-level and three-level 1500-V PV inverters. The comparison presented in this chapter includes the three topologies shown in Fig. 2.1, namely, the two-level, the I-type three-level and the T-type three-level topologies, which are the most common inverter topologies for 1500-V PV systems in the industry. Firstly, I provide the system description, the selected IGBT power modules, and thermal modeling principle, followed by a thermal performance comparison of these inverter topologies considering constant power generation operations, reflecting their thermal stress under different DC-link voltages. Then, the lifetime of the most stressed power semiconductors within the three-level topologies is evaluated. Based on that, a converter-level reliability evaluation is presented. Finally, a summary is provided at the end of this chapter.



(a) Two-level (b) I-type three-level (c) T-type three-level

Fig. 2.1: Considered topologies for 1500-V DC-link PV inverters: (a) two-level, (b) I-type three-level, and (c) T-type three-level. Source: **[C1]**.

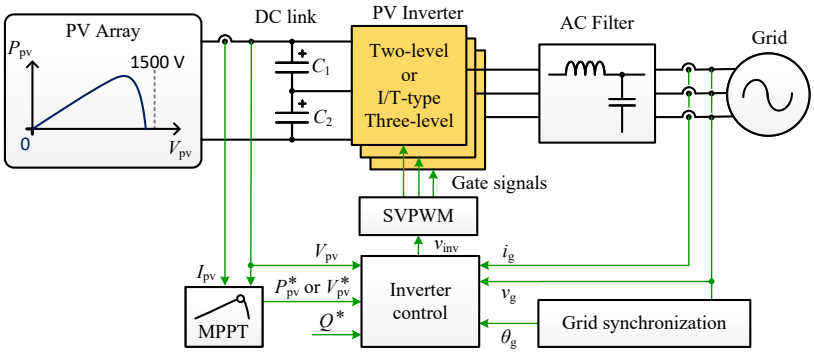


Fig. 2.2: Circuit diagram of the PV system and its maximum power point tracking (MPPT) control structure. Source: [**J1**].

Table 2.1: Specifications of the 1500-V PV System. Source: [**J1**].

PV inverter specifications	
Nominal power P_{nom}	160 kW
Grid voltage V_{LL}[1] (RMS[2])	600 V
Grid frequency f_g	50 Hz
Power factor $\cos(\varphi)$	1.0
Switching frequency f_{sw}	$2-6$ kHz
PV panel configuration	
PV panel type	JKM360M-72-V [38]
Number of PV panels	27 in series (PV string), 16 strings in parallel

[1] V_{LL}: line-to-line voltage

[2] RMS: Root-Mean-Square.

2.1 System Modeling

A 160-kW single-stage PV system is considered in this project. The circuit diagram of the PV system and its general control structure are shown in Fig. 2.2, where either two-level or three-level inverters can be employed to transfer the energy from the 1500-V PV array to the AC grid. The specifications of the PV system and the selected IGBT modules are given in Tables 2.1 and 2.2, respectively. The nominal power of the PV system is 160 kW, where the switching frequency is chosen to be between $2-6$ kHz to analyze its impact on inverter reliability. As for the PV array, the 1500-V PV panels from Jinko are adopted to match the ratings of the PV system.

Power losses on the power devices, i.e., IGBTs or diodes, cause the self-heating effect, which lead to large temperature gradients and thus affect the reliability. The switching losses and conduction losses of power devices can be modeled based on the switching energy E_{sw} during switching transition and the forward voltage drop v_{CE}

Table 2.2: Adopted IGBT Modules for Building up the 1500-V PV Inverters. Source: **[C1]**.

Parameter	453GB17E4p	305MLI12E4	305TMLI17E4
Topology	Half-bridge	I-type	T-type
Nominal voltage (V)	1700	1200	1700
Nominal current (A)	450	300	300
Junction temp. (^{o}C)	-40 to 150	-40 to 150	-40 to 150

during conduction, respectively. Besides, the impact of the temperature variation on the power loss cannot be ignored, which can be considered in the loss model, e.g., in form of look-up tables.

With the obtained power losses, the device junction temperature can be modeled based on their thermal models [35]. The typical diagram of the thermal model is illustrated in Fig. 2.3, where the junction-to-case thermal impedance, i.e., $Z_{\text{th(j-c)}}$, is modeled by means of a thermal RC network, also referred to as Foster model. Accordingly, the junction temperature can be expressed as [35]

$$T_{\text{j}}(t) = P_{\text{tot(T/D)}}\,(t) \cdot Z_{\text{th(j-c)}}(t) + T_{\text{c}}(t) \tag{2.1}$$

$$T_{\text{c}}(t) = P_{\text{tot(T/D)}}(t) \cdot \left[Z_{\text{th(c-s)}}(t) + Z_{\text{th(s-a)}}(t)\right] + T_{\text{a}}(t) \tag{2.2}$$

where T_{c} and T_{a} are the case temperature (for modules with base plate) and ambient temperature, respectively, $Z_{\text{th(c-s)}}$ and $Z_{\text{th(s-a)}}$ represent the thermal impedance of the case-to-heatsink and the heatsink-to-ambient, respectively, $P_{\text{tot(T/D)}}$ is the total power losses of the power device (Transistor or Diode). The model parameters (i.e., R_{th} and C_{th} in Fig. 2.3) can be acquired by using a three-/four-layer RC network to fit the transient thermal impedance curves in the module datasheet. These RC parameters determine the junction temperature dynamic.

2.2 Thermal Performance Analysis

The thermal performance of the aforementioned 1500-V PV inverters is compared under steady-state conditions, where they are assumed to operate under constant power generation (CPG) mode with the ambient temperature and the solar irradiance being constant, 25 ^{o}C and 1000 W/m^2, respectively.

It is known than the PV inverters can operate on the left- or right-hand maximum power point (MPP) side during CPG operation. Fig. 2.4 shows the power-voltage (P-V) curve of the 1500-V PV array and two possible power references (P_{ref1} and P_{ref2}) for CPG operations. With the system modeling in the previous section, the thermal performance of the 1500-V PV inverters based on different topologyies can be compared at these operating points. The comparison results have been discussed in **[C1]**, and will be summarized in the following.

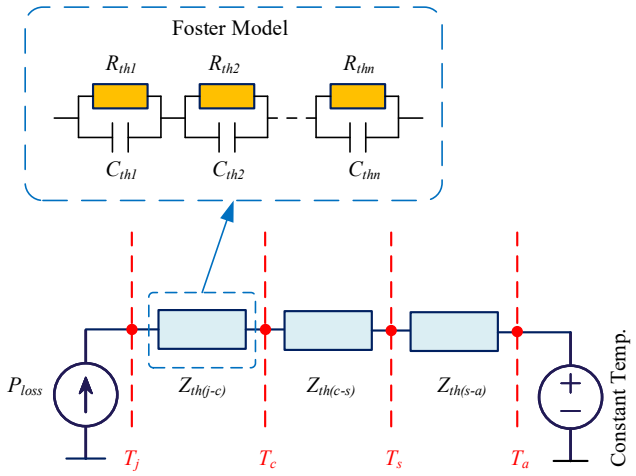


Fig. 2.3: Structure of the thermal model. Source: **[C1]**.

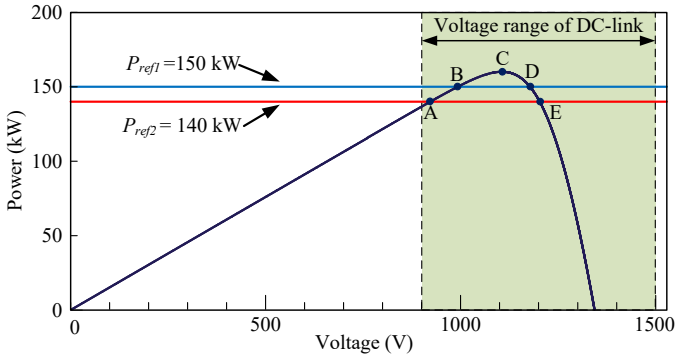


Fig. 2.4: P-V curve of the 1500-V PV array and possible power control reference for constant power generation. Source: **[C1]**.

Fig. 2.5 shows the semiconductor power losses under different operating points. As can be seen in it, the power losses of the two-level inverter are dramatically higher than that of the three-level I-type/T-type inverter. Also, by comparing between the three-level inverters, it can be observed from Fig. 2.5 that the power losses of the I-type inverter are slightly higher than that of the T-type one for the considered switching frequency, i.e., 5 kHz. Overall, the higher the operating point voltage, the higher the inverter power losses, especially for the two-level and T-type three-level cases. On the contrary, the PV inverters have lower power losses when they operate at the left-side of the MPP, e.g., points A and B, and the power loss reduction is mainly contributed by the decrease in switching losses. Hence, it can be expected that, when the two-level or the T-type inverter operates at the left-hand side of the MPP, a higher efficiency can be achieved. As for the I-type inverter, it can be observed in Fig. 2.5 that its

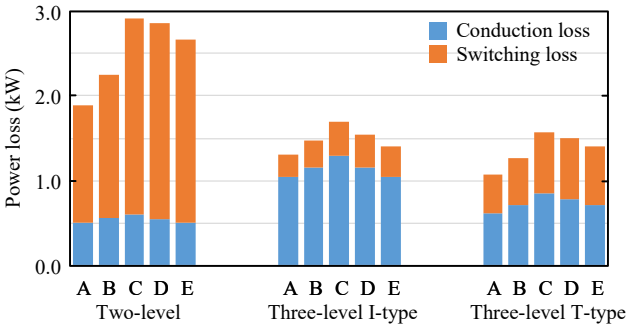


Fig. 2.5: PV inverter power losses under different operating points (referring to Fig. 2.4). Source: [**C1**].

switching losses are relatively small compared to the conduction losses under the 5-kHz switching frequency, and thus its total power losses under the left-hand MPP side are similar to that under the MPP right-hand side.

The thermal stresses of these two-level and three-level inverters are compared in Fig. 2.6 (a and b) in terms of the mean junction temperature T_{jm} and the corresponding cycle amplitude ΔT_{j}. It can be observed from Fig. 2.6 that, overall, the relationship between the thermal stress and operating point is consistent with the power loss analysis, and the thermal stress of the two-level inverter is much higher than that of the three-level ones. In this case, much more cooling efforts are expected for the two-level inverter, otherwise, its reliability is challenged.

On the other hand, when the two-level and T-type inverters operate under the right-hand MPP side, their IGBTs have higher T_{jm} and higher ΔT_{j} due to the high power losses in such a case. For the I-type inverter, similar to the power loss distribution, there is not much difference for the thermal stress under each side. It should be pointed out that, although the mean junction temperature of IGBT T1 (most stressed) in the I-type inverter is slightly higher in comparison to that in the T-type one, the cycle amplitude of the latter is higher. Both of these two stress indicators, i.e., T_{jm} and ΔT_{j}, are critical parameters in the empirical lifetime model [39]. The lifetime performance of the three-level inverters has been discussed in [**C2, J1**] and will be summarized in the following sections.

2.3 Lifetime Evaluation

As discussed in *Chapter 1*, the PV inverter lifetime is influenced by their mission profiles. To evaluate the inverter lifetime, firstly, the mission profile should be translated into the device thermal loading. Then, a proper lifetime model can be applied to estimate the device lifetime based on the obtained thermal loading. The overall process is summarized in Fig. 2.7, where several look-up tables (LUTs) are used to deal with the long-term mission profiles [35].

First, as indicated in Fig. 2.7, the available power of the 1500-V PV array is

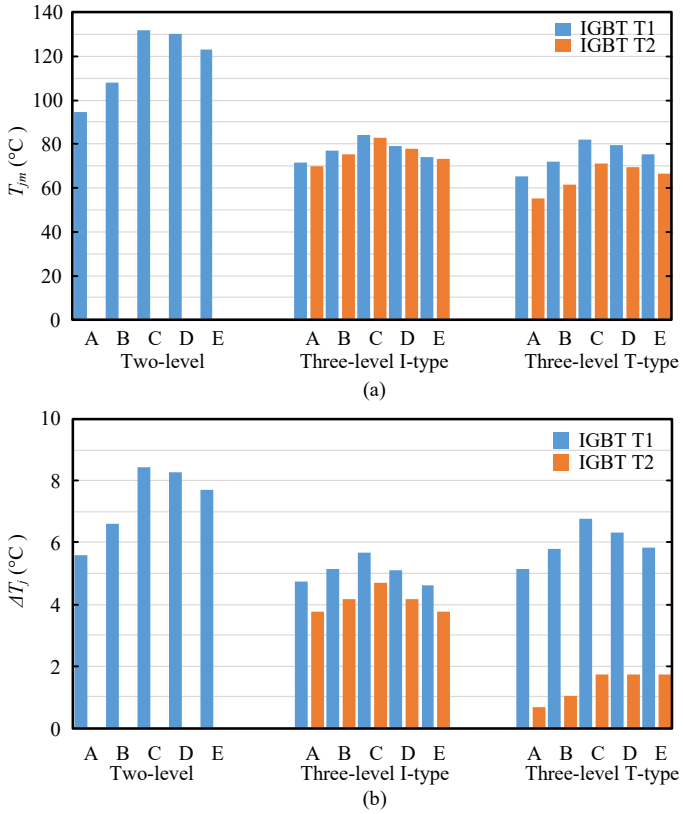


Fig. 2.6: IGBT thermal stress comparison of the 1500-V PV inverters under different operating points (referring to Fig. 2.4). Source: **[C1]**.

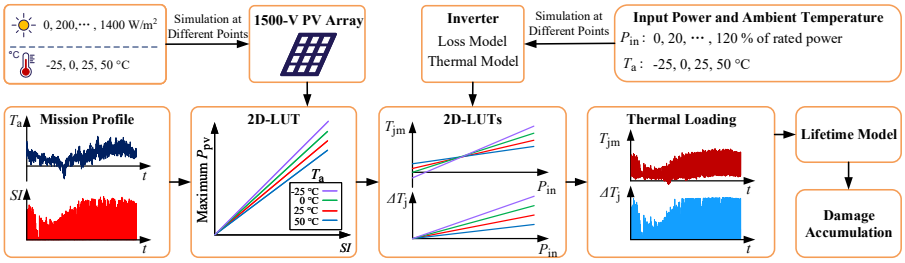


Fig. 2.7: Block diagram of the mission-profile based lifetime evaluation for the power devices of the 1500-V PV inverters. Source: **[C2, J1]**.

determined under different operating points to obtain the LUT for translating the mission profile to the inverter's operating conditions, i.e., input power and ambient temperature. In parallel, the PV inverter is also simulated under a certain set of

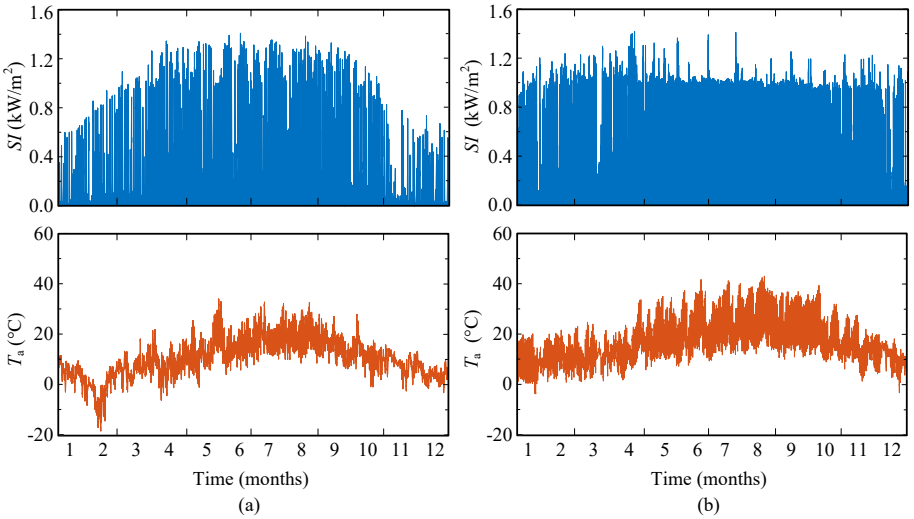


Fig. 2.8: One-year mission profiles, i.e., solar irradiance SI and ambient temperature T_a, which are recorded with a sampling rate of 1 min/sample in: (a) Aalborg and (b) Sacramento. Source: [**c2, J1**].

operating points. Then, the LUTs for translating the operating conditions to the thermal loadings of the power devices can be built up. With these LUTs, the thermal loading of the power devices can be acquired when the long-term mission profiles are provided as the inputs, following the process in Fig. 2.7. Finally, an appropriate empirical lifetime model and damage model can be applied to estimate the device lifetime consumption under the mission profiles. With this procedure, a benchmarking of the three-level inverter topologies could be done in terms of component lifetime.

As for the mission profiles, the yearly solar irradiance and ambient temperature data of Aalborg (Denmark) and Sacramento (California) are adopted in this project, which are recorded with 1 minute/data sampling rate, as shown in Fig. 2.8. In Aalborg, the annual average temperature is 9.88 °C. Also, it can be observed from Fig. 2.8(a) that the temperature and solar irradiance in Aalborg fluctuate over a wide range. In contrast, the annual average temperature in Sacramento is 16.56 °C, and the solar irradiance and temperature are more stable as shown in Fig. 2.8(b), which are respectively higher than that in Aalborg.

According to the translation process in Fig. 2.7 and take the above mission profiles as inputs, the thermal loadings of IGBT T1 (referring to Fig. 2.1) of the three-level topologies have been obtained, which are shown in Fig. 2.9. It can be observed from Fig. 2.9 that the inverter IGBT installed in Aalborg experience lower thermal stresses in comparison to that in Sacramento due to the lower average irradiance and temperature in Aalborg. Moreover, it can be observed from Fig. 2.9 that, the cycle amplitude ΔT_j of the IGBT in the I-type inverter is lower than that in the T-type inverter. According to the lifetime model [39], the lifetime consumption of the IGBT for the I-type topology would be lower than that of the T-type one. The impact of thermal loadings on the

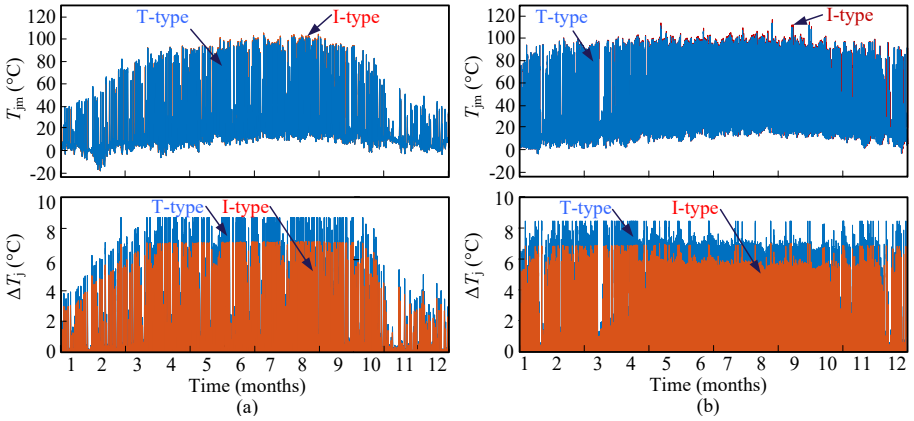


Fig. 2.9: One-year mean junction temperature T_{jm} and cycle amplitude ΔT_j profiles for the IGBT T1 in the three-level inverters with 6-kHz switching frequency: (a) Aalborg and (b) Sacramento. Source: **[C2, J1]**.

inverter reliability will be discussed in the following section.

2.3.1 Damage Caused by the Line-Frequency Power Cycling

The damage due to the power cycling with line frequency, i.e., 50 Hz, can be calculated directly, e.g., by Miner's rule [40]. The obtained thermal loadings have the same sampling rate as the mission profiles, i.e., 1 minute/sample. Thus, the damage during every minute can be calculated with the corresponding thermal stress data, i.e., mean junction temperature and cycle amplitude. Then, according to Miner's rule, the total damage due to a minute line-frequency power cycling can be calculated as

$$LC = \sum_i \frac{n_i}{(N_f)_i} = \sum_i \frac{3000}{(N_f)_i} \tag{2.3}$$

where n_i is a constant value and equals to 3000, i.e., the number of 50-Hz power cycles in one minute, $(N_f)_i$ can be calculated according to the lifetime model and the thermal loading data. Table 2.3 summarizes the obtained damage results for both line-frequency and low-frequency damage type.

2.3.2 Damage Caused by the Low-Frequency Thermal Cycling

Typically, a cycle counting algorithm is required to take into account the irregular temperature loading profile. In this project, a rainflow counting analysis is used to categorize the irregular thermal cycles into a certain set of regular ones [36]. By doing so, the dynamics under the mission profiles, i.e., the number of cycles n_i for a certain set of thermal stress conditions (i.e., cycle amplitude ΔT_j, mean junction temperature T_{jm}, and cycle period) can be extracted. The rainflow counting results are shown in Fig. 2.10. A total of 121,699 and 62,890 low-frequency thermal cycles have been extracted

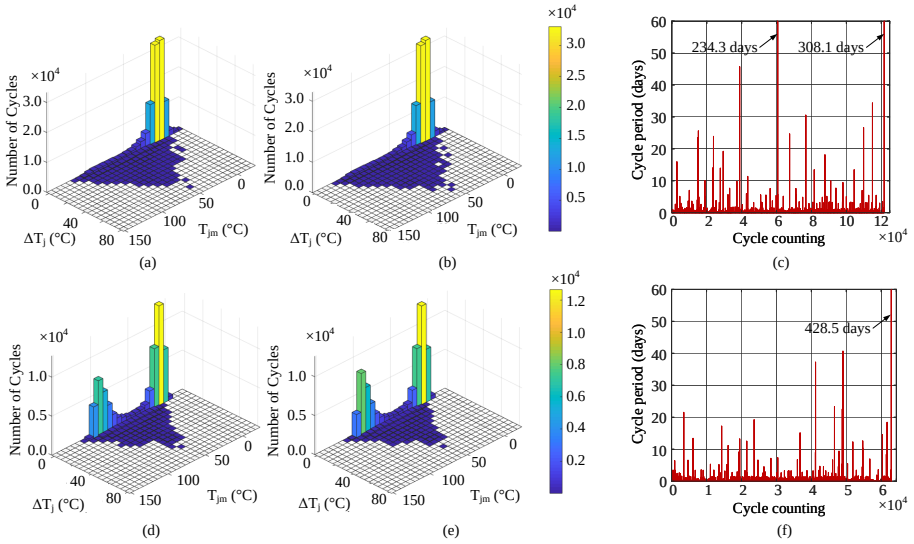


Fig. 2.10: Rainflow counting results of the one-year junction temperature profile of the IGBT T1 in the three-level inverters with a switching frequency of 6 kHz: (a) thermal cycles in Aalborg (I-type), (b) thermal cycles in Aalborg (T-type), (c) cycle period in Aalborg, (d) thermal cycles in Sacramento (I-type), (d) thermal cycles in Sacramento (T-type), (f) cycle period in Sacramento. Source: [**C1, J1**].

for the IGBT thermal loading under the Aalborg and Sacramento mission profiles, respectively, and their periods vary from minutes to tens of days. Similarly, the same damage model as for the line-frequency power cycling can be applied on the rainflow counting results to obtain the corresponding damage results, which are summarized in Table 2.3 as well.

2.3.3 Lifetime Consumption Results

The one-year damage results in Table 2.3 are further summarized in Fig. 2.11. As can be seen in it, with the Aalborg mission profile, the IGBT for the I-type topology has lower lifetime consumption when the switching frequency is lower than 4 kHz compared to that in the T-type topology. In the case of a 2-kHz switching frequency under the Sacramento mission profile, the IGBT of the T-type inverter also has a lower lifetime consumption. However, when the switching frequency is higher than 4 kHz, the I-type topology is preferred for the Sacramento mission profile due to its lower lifetime consumption.

The lifetime consumption results can be summarized as: 1) the operation conditions, i.e., mission profile and switching frequency, have a considerable influence on the device reliability of the three-level 1500-V PV inverters, and 2) caused by the increased DC-link voltage stress, compared to PV systems with lower DC-link voltage, e.g., < 1000 V, the lifetime performance of the T-type inverter may be worse than that of the I-type one even for low switching frequencies, e.g., 4 kHz to 6 kHz. A converter-level

Table 2.3: One-Year Lifetime Consumption. Source: **[C1, J1]**.

Mission profile	Power module	Damage type	Switching frequency		
			2 kHz	4 kHz	6 kHz
Aalborg	I-type	Line-freq.	0.0002	0.0005	0.0009
		Low-freq.	0.0027	0.0044	0.0070
	T-type	Line-freq.	0.0003	0.0009	0.0032
		Low-freq.	0.0012	0.0035	0.0087
Sacramento	I-type	Line-freq.	0.0014	0.0025	0.0051
		Low-freq.	0.0026	0.0041	0.0063
	T-type	Line-freq.	0.0014	0.0050	0.0164
		Low-freq.	0.0013	0.0033	0.0078

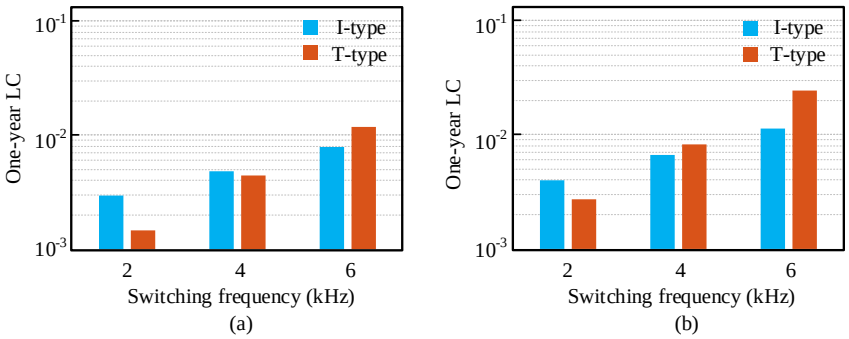


Fig. 2.11: One-year lifetime consumption of the IGBT T1 under various switching frequencies and two installation sites: (a) Aalborg and (b) Sacramento. Source: **[C1, J1]**.

reliability assessment will be given in the next section.

2.4 Reliability Assessment

With the above lifetime evaluation, the component damage under the mission profiles can be calculated and obtained for a given fixed lifetime value. However, it is known that the component lifetime varies within a certain range due to the variation at manufacturing time. Consequently, for lifetime prediction, the results are usually expressed in the form of statistical values instead of fixed ones. In this section, the converter-level reliability of the three-level inverter candidates is discussed statistically, which is done by applying Monte Carlo analysis [37, 41, 42]. Fig. 2.12 presents the block diagram of this reliability assessment. As can be seen in it, with the lifetime consumption results in the previous section, the equivalent static thermal stress parameters (i.e., $T'_{\mathrm{j(min)}}$, $\Delta T'_{\mathrm{j}}$, and t'_{on}) are obtained, which can result in the

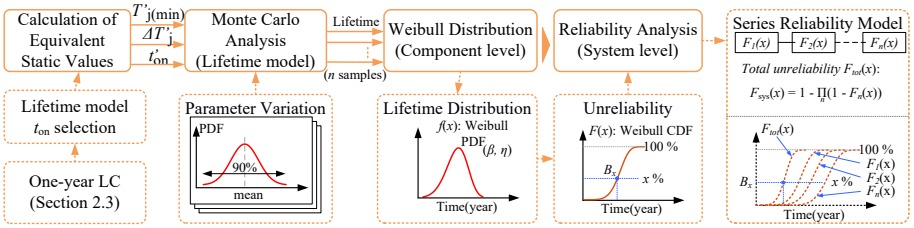


Fig. 2.12: Block diagram of the reliability assessment based on Monte Carlo analysis. Source: **[J1]**.

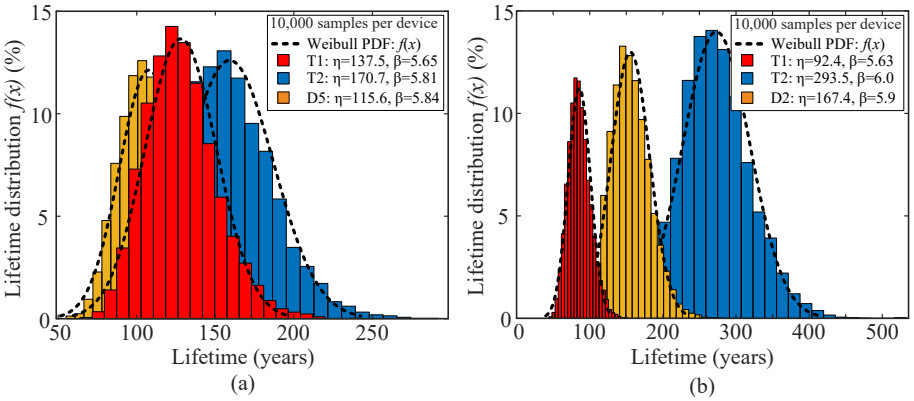


Fig. 2.13: Lifetime distribution of the most stressed power devices in the 1500-V PV inverters installed in Aalborg: (a) three-level I-type inverter and (b) three-level T-type inverter. Source: **[J1]**.

same one-year lifetime consumption as the dynamic parameters (i.e., $T_{j(min)}$, ΔT_j, and t_{on}) of the thermal loading profiles in the previous section. Then, the parameter variations have been considered to introduce uncertainties, where the equivalent static thermal stress parameters and all the parameters in the adopted lifetime model [39] are assumed to have a 5% variation (99% confidence level). After that, the corresponding lifetime distributions can be obtained. More importantly, a comparative evaluation of the converter-level reliability can be done according to the reliability block diagram (RBD) of the three-level topologies [34, 41, 43].

Considering 10,000 samples for each case, the lifetime distributions of the most stressed power devices of the three-level inverters have been obtained by Monte Carlo simulations, as shown in Figs. 2.13 and 2.14. As it can be seen in Figs. 2.13 and 2.14, overall, the lifetime distributions for the I-type inverters are less spread compared with that for the T-type inverters, where the lifetime distribution of IGBT T1 is far away from those of T2 and diode D2. This is more critical for a more severe mission profile, e.g., Sacramento, as shown in Fig. 2.14(b). This means that the device lifetime performance of the I-type inverter is more balanced in comparison to that of the T-type inverter. It can be expected that, when seeing the reliability performance from converter-level, the I-type inverter would be better in comparison to the T-type one in both cases (i.e., Aalborg and Sacramento), due to the high stressed 1700-V IGBTs in the T-type inverter.

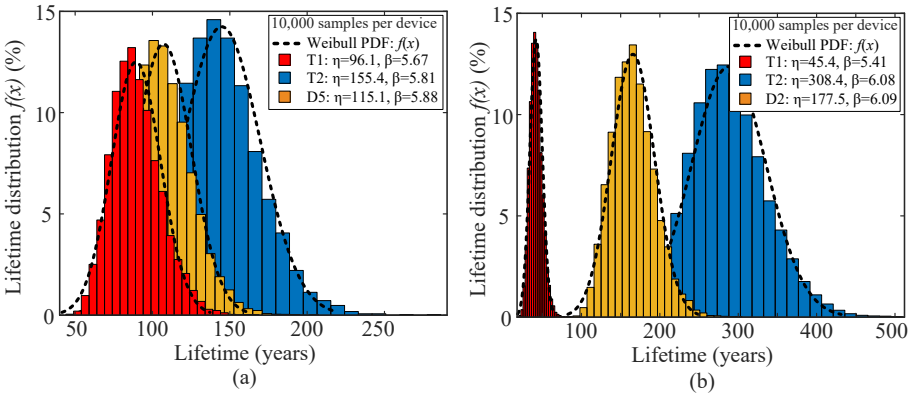


Fig. 2.14: Lifetime distribution of the most stressed power devices in the 1500-V PV inverters installed in Sacramento: (a) three-level I-type inverter and (b) three-level T-type inverter. Source: [**J1**].

With the obtained lifetime distributions, the reliability of the three-level inverter candidates can be further evaluated with the cumulative density function (CDF), which can present the failure proportion as a function of operating time. It is also referred to as the Weibull unreliability function and can be given by

$$F(x) = \int_0^x f(x)dx, \quad f(x) = \frac{\beta}{\eta}\left(\frac{x}{\eta}\right)^{\beta-1} e^{-\left(\frac{x}{\eta}\right)^{\beta}} \tag{2.4}$$

where x is the operating time, $f(x)$ represents the probability density function (PDF) of the lifetime distribution, η and β denote the scale and shape parameters, respectively. Then, the lifetime prediction can be given in the form of B_x lifetime, which equals to the operating time when x% of the population reaches the end of life.

With the component-level unreliability functions, the unreliability function of the inverters (converter-level) can be obtained according to the reliability block diagram (RBD) of the inverter topologies, which describes the relationship between the component reliability and the reliability of the whole inverter [43]. For the three-level candidates, their fault-tolerant operation is not considered in this case study, since if any power device (IGBT or diode) fails, the inverter would fail or could not be operated up to the designed ratings (e.g., reduced output voltage/power [44, 45]). Thus, a series connection of the component-level RBDs is adopted to obtain the converter-level results, as shown in Fig. 2.15. Accordingly, the system unreliability function $F_{\text{sys}}(x)$ can be expressed as

$$F_{\text{sys}}(x) = 1 - \prod_{i=1}^{n}(1 - F_i(x)) \tag{2.5}$$

with $F_i(x)$ being the unreliability function of the i^{th} power device.

Figs. 2.16 and 2.17 present the unreliability functions of the considered three-level inverters, where dashed and solid lines indicate the component-level and the converter-level, respectively. As it can be observed from Figs. 2.16 and 2.17, the

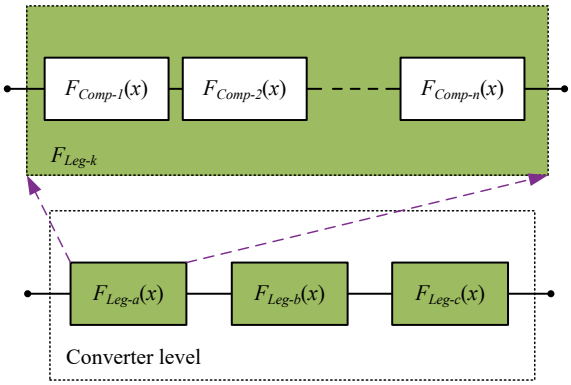


Fig. 2.15: Reliability block diagram of the three-level inverters, where a series connection is considered both for the phase leg and the whole three-phase inverter. Source: **[J1]**.

inverter candidates have considerably various B_x lifetime for the different mission profiles, reflecting their impact on inverter reliability. Under both cases, the three-level I-type inverter outperforms the T-type one in terms of reliability. Notably, for the Sacramento mission profile, it is not recommended to use the T-type inverter for the current heatsink/cooling condition due to its distinctly low B_x lifetime.

Table 2.4 summarizes some B_x lifetimes of the inverter candidates with switching frequencies from 2 kHz to 6 kHz. The results are consistent with the component lifetime evaluation in the previous section. On the one hand, for very low switching frequencies, e.g., 2 kHz, either inverter candidate can present a high B_x lifetime. On the other hand, for higher switching frequency, e.g., 6 kHz, the promising candidate is the I-type one, which can achieve a higher B_x lifetime. This is especially true for the Sacramento mission profile, where the B_x lifetime of the I-type inverter is more than twice as much as the T-type one. Besides, when it comes to an intermediate switching frequency, e.g., 4 kHz, the topology selection could depend on the mission profiles of the installation sites. In this work, the I-type topology is preferred for the Sacramento site, while for Aalborg, the T-type one is superior for this switching frequency. It is worth mentioning that it is still an open challenge when trying to verify the actual lifetime [31]. However, the reliability assessment can still be used for a qualitative comparison among the inverter candidates in the 1500-V range.

2.5 Summary

In this chapter, the reliability of the 1500-V PV inverters with standard two-level and three-level topologies has been investigated. Their power losses and thermal stresses were compared under different operating points on the P-V curve of the 1500-V PV arrays. The comparison results indicated that, compared with the two-level topology, the three-level ones are more suitable alternatives for 1500-V PV systems due to their higher efficiency and lower thermal stresses. Furthermore, the reliability

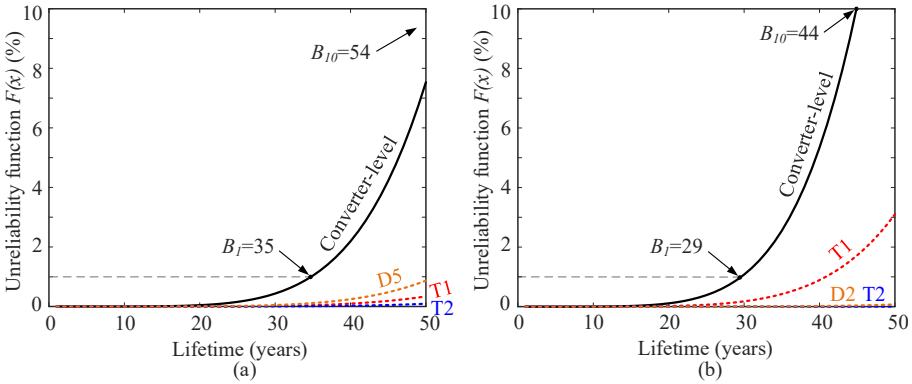


Fig. 2.16: Component-level and converter-level unreliability functions of the 1500-V PV inverters installed in Aalborg: (a) three-level I-type inverter and (b) three-level T-type inverter. Source: [**J1**].

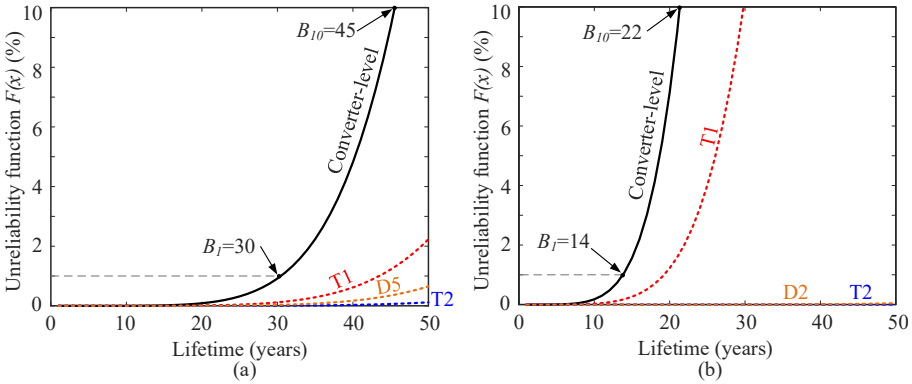


Fig. 2.17: Component-level and converter-level unreliability functions of the 1500-V PV inverters installed in Sacramento: (a) three-level I-type inverter and (b) three-level T-type inverter. Source: [**J1**].

performance of the three-level inverters has been evaluated considering the impact of mission profiles and switching frequencies. The component- and converter-level reliability analyses reveal that these factors have a considerable influence on the inverter reliability, hence affecting the selection of topologies for the implementation of the three-level 1500-V PV inverters.

The lifetime of the power devices, i.e., IGBTs and diodes, of the three-level topologies was estimated with an empirical lifetime model. On this basis, the most critical power device of the three-level topologies has been identified in the component-level reliability analysis. Also, following converter-level reliability assessment presented how the most stressed IGBTs and diodes affect the reliability of the entire inverter. It should be mentioned that the reliability investigation was conducted with a number of assumptions (e.g., ideal grid, MPPT control, and linear and cumulative damage model) for a comparative analysis. However, this reliability assessment provides an indication

Table 2.4: B_x Lifetime of the Three-Level Inverter Candidates. Source: [**J1**].

Mission profile	Topology	B_x lifetime (year)	switching frequency 2 kHz	4 kHz	6 kHz
Aalborg	I-type	B_{10}	142	86	54
		B_1	97	58	35
	T-type	B_{10}	381	123	44
		B_1	264	83	29
Sacramento	I-type	B_{10}	118	77	45
		B_1	80	52	30
	T-type	B_{10}	210	66	22
		B_1	144	44	14

of the reliability of 1500-V PV inverters, hence, the investigation is beneficial for the topology selection of the 1500-V PV systems for a given mission profile.

Related Publications

J1. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime Evaluation of Three-Level Inverters for 1500-V Photovoltaic Systems" *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4285-4298, Aug. 2021.

C1. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Thermal Performance Evaluation of 1500-VDC Photovoltaic Inverters Under Constant Power Generation Operation," in *Proc. IEEE CPERE*, pp. 579-583, Oct. 2018.

C2. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime Evaluation of Power Modules for Three-Level 1500-V Photovoltaic Inverters," in *Proc. IEEE APEC*, pp. 430-435, Mar. 2020.

Chapter 3

Impact of System Parameters on Reliability

In addition to the topology selection for designing a highly-reliable 1500-V PV system, it is also essential to consider the influence of the system parameters on the reliability of PV power converters. The selection of system parameters plays a vital role in improving the performance of the PV systems in terms of energy production and reliability. This chapter aims to present the impact of system voltage ratings and integration of battery energy storage system (BESS) on the performance of 1500-V PV systems.

With a strong demand to guarantee the high availability of multi-megawatt (MW) PV plants, 1500-V string PV inverters are superior to centralized configurations [46, 47]. Normally, string PV inverters can provide wide operating voltage ranges both for the DC and the AC side [48, 49], e.g., they can be equipped with 1000-V/1500-V PV strings and connected to various AC voltages, e.g., 400 V or 690 V. Thus, the performance of 1500-V PV systems with centralized string inverter solutions, as depicted in Fig. 3.1, will be compared in this chapter, where the power/energy losses of on the main system components, i.e., DC wires, inverters, AC filters, and isolation transformers, will be estimated considering various DC- and AC-side voltage ratings.

On the other hand, with an ever-increasing demand for enhancing the flexible grid-integration of PV systems, BESS integration is becoming increasingly popular, since it can smooth out the PV power fluctuation. The selection of system configuration, i.e., DC- or AC-coupling, should be carefully considered during the design stage of a 1500-V PV-battery system. Thus, it is essential to assess both the PV converters and the battery converters in terms of reliability, since they are the most lifetime-critical parts and determine the reliability of the entire PV-battery system. This Ph.D. project investigates the reliability of 1500-V PV-battery systems with a benchmarking of DC- and AC-coupled BESS configurations. In this chapter, the impact of BESS on the PV inverter reliability will be addressed, and the performance of all the power converters in these configurations will be assessed with reliability analysis from component- to system level.

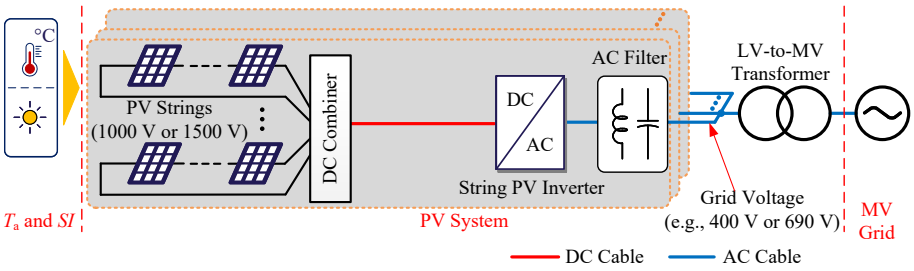


Fig. 3.1: PV system based on centralized string inverter solution (T_a: ambient temperature, SI: solar irradiance). Source: **[C5]**.

Table 3.1: Specifications of the String PV Inverter. Source: **[C5]**.

Parameter	Value
Nominal output power P_n [kW]	60 / 72 / 90 / 100
Nominal output current I_n	87 A
AC operating voltage V_{LL}[1] (RMS[2]) [V]	400 / 480 / 600 / 690
Grid frequency f_g	50 Hz
Power factor $\cos(\varphi)$	1.0
Maximum input voltage	1500 V
Input voltage range for nominal power	$1.44 \times V_{LL}$ to 1300 V
Switching frequency f_{sw}	6 kHz
Adopted IGBT module	Semikron 39MLI12T4V1

[1] V_{LL}: line-to-line voltage
[2] RMS: Root-Mean-Square.

3.1 Large-Scale Photovoltaic Architecture

The influence of PV system voltage ratings on the system performance has been discussed in **[C5]**, where a large-scale PV system based on the centralized string inverters is considered for case study, as presented in Fig. 3.1. In the case study of **[C5]**, the impact of system voltage ratings (both DC and AC sides) and mission profiles on the power losses (on inverters, DC wires, AC filters, and transformers) and yearly energy yield of the PV system has been analyzed and will be summarized in this section.

3.1.1 System Configuration

Generally, the nominal power of string 1500-V PV inverters is not a fixed value. It can be varied from tens kW to over 100 kW, which is determined by the grid voltage. For the same reason, for a given PV system capacity, based on the grid voltage ratings, a certain number of string inverters are required. The considered string PV inverter is based on the three-level I-type topology, and its specifications are summarized in

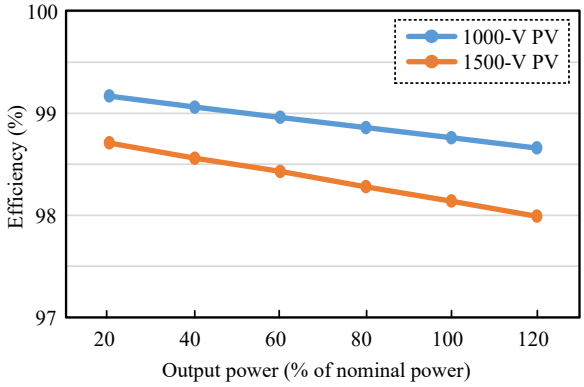


Fig. 3.2: Inverter efficiency comparison considering two PV string configurations, i.e., 1000-V PV and 1500-V PV. Source: [**C5**].

Table 3.1. The IGBT module is from Semikron [50], and its current and voltage ratings are 150 A and 1200 V, respectively.

By using an electro-thermal model, the efficiency characteristics of the string inverter have been obtained considering different PV string configurations, as shown in Fig. 3.2. Notably, the inverter efficiency with the 1500-V PV is slightly lower in comparison to that of the 1000-V PV. This reflects one of the drawbacks of the 1500-V configuration, i.e., increased inverter loading stress.

As for the DC wires between the PV arrays and the string inverters, in accordance with the National Electrical Code (NEC) [51], the wire ampacity, i.e., the maximum current carrying capacity, should be at least 1.25 times the PV array's short-circuit current. Regarding the wire length, the average DC wire length can be estimated based on the system capacity as discussed in [52]. Regarding the inverter output, as shown in Fig. 3.1, LCL filters are adopted to suppress the harmonics of the inverter and their outputs are connected to the low-frequency transformer, with which, the low-voltage (LV) outputs of the PV inverters are elevated to the medium voltage (MV) for connecting utility network. For the power losses on the LCL filters and the transformer, both comprise core losses and copper losses, which can be estimated by their loss models [53].

3.1.2 Comparative Study

Based on combinations of various DC and AC voltage ratings, three different centralized string PV inverter solutions have been considered for a 1.8-MW PV system, as summarized in Table 3.2, including the grid voltage, i.e., 400 V or 690 V, the PV string configuration, i.e., 1000- or 1500-V PV string, the DC wire size, and the number of inverter units. Notably, as it can be observed from Table 3.2, the PV string configuration and the grid voltage respectively determine the DC wire size and the number of inverter units, which will affect the amount of power losses and energy yield of the entire PV system. The procedure for the power loss analysis is summarized in Fig. 3.3. Similar to the mission profile translation presented in *Chapter 2*, the output

Table 3.2: Considered Centralized String PV Inverter Solutions. Source: **[C5]**.

Solution 1: 400-V grid voltage, 1000-V PV	
PV panel configuration	N_s = 18, N_p = 9
DC wire gauge	2 AWG
Inverter units	30
Solution 2: 400-V grid voltage, 1500-V PV	
PV panel configuration	N_s = 27, N_p = 6
DC wire gauge	4 AWG
Inverter units	30
Solution 3: 690-V grid voltage, 1500-V PV	
PV panel configuration	N_s = 27, N_p = 10
DC wire gauge	1 AWG
Inverter units	18

[1] N_s: Number of PV panel in series

[2] N_p: Number of PV string in parallel

profiles of the PV strings, i.e., output power and voltage, are translated from the mission profiles with the look-up table of the PV panel characteristics. By doing so, the inputs for calculating the ohmic loss on the DC wires are obtained. On the other hand, the string inverter along with the AC filter is simulated covering a certain set of operating points to make the look-up tables for obtaining the power loss profiles on the inverter and the filter. In this way, the performance of the PV systems with different system voltage ratings can be compared in terms of power/energy losses on each part, following the procedure in Fig. 3.3.

The power loss profiles on the DC wires and inverters under the Aalborg and Sacramento mission profiles are shown in Fig. 3.4, and the yearly energy losses on each part are summarized in Fig. 3.5. As it can be observed from Figs. 3.4 and 3.5, by using the 1500-V PV strings, the power losses on the DC wires can be considerably reduced, and this power loss reduction would be more significant if a higher grid voltage, e.g., 690 V, is considered as well. Also, the solution with higher DC and AC voltage ratings, i.e., 1500-V PV and 690-V AC, has the lowest inverter losses due to the minimum number of inverter units. As for the filter and transformer losses, as shown in Fig. 3.5, they are much smaller than those on other parts and with negligible difference among the different solutions. Nevertheless, it can be observed from the comparison that, for both mission profile cases, the 1500-V PV solutions outperform the 1000-V one with regards to energy production, and the number of inverter units if a higher grid voltage, e.g., 690 V, is considered.

It should be pointed out that the DC and AC voltage parameters also determine the DC-bus voltage ranges and thus affect the yearly energy yield [5]. The operating ranges for the considered solutions are presented in Fig. 3.6. It can be observed from Fig. 3.6 that the 1500-V PV along with 400-V AC offers a much wider operating range in comparison to the other solutions. Also, it is worth mentioning that the influence of system voltage parameters on the yearly energy production varies with mission profiles. As indicated in Fig. 3.5, the solution based on 1500-V PV and 690-V AC

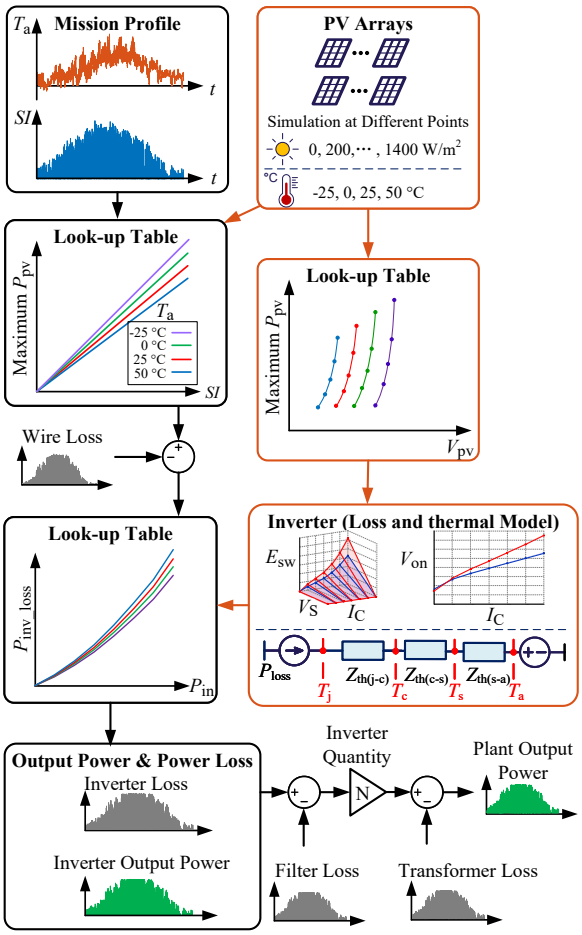


Fig. 3.3: Block diagram of the procedure for analyzing the power losses, where black and red boxes represent the main steps and the subsidiary steps, respectively. Source: **[C5]**.

has the highest energy yield in Sacramento. In contrast, this solution has the lowest energy yield in Denmark, where the solution based 1500-V PV and 400-V AC, i.e., high operating range, is preferred when achieving high energy yield is the highest priority.

The comparison results reveal that, on the one hand, the 1500-V PV solutions generate lower power losses in comparison to the 1000-V PV solution, due to the considerable reduction on wire losses and inverter units. On the other hand, for a cold climate like in Aalborg, higher AC voltage, e.g., 690 V, may negatively affect energy production. In such a case, 1500-V PV along with a relatively lower AC voltage, e.g., 400 V, is a better option, achieving wider operating voltage range hence higher energy production.

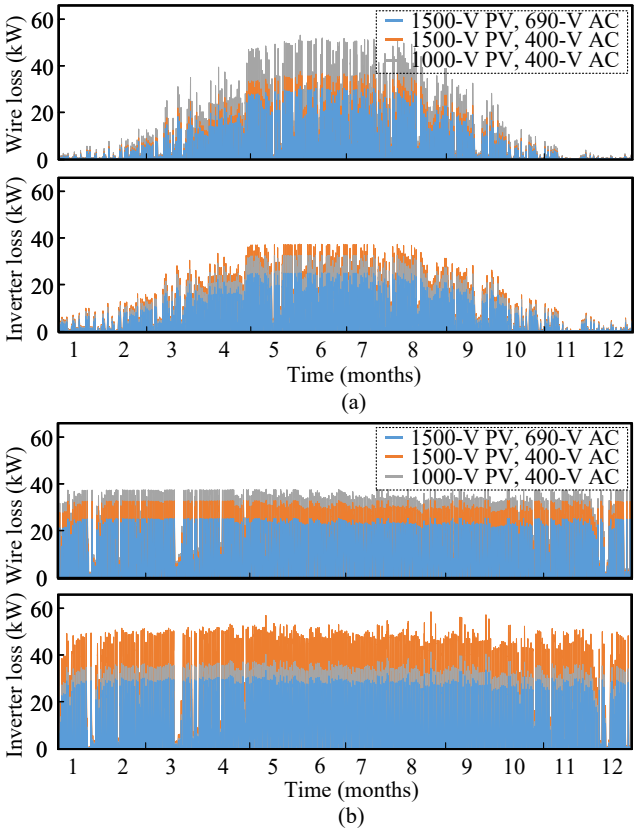


Fig. 3.4: One-year power loss profiles on DC wires and inverters with various system voltage ratings for the PV system installed in: (a) Denmark and (b) Sacramento. Source: **[C5]**.

3.2 Energy Storage Integration

With the development of 1500-V PV technology, the market share of solar power is growing and its grid penetration is rising. However, the high variability of solar power also raises challenges for the grid penetration of these PV systems. In such a case, the integration of BESS could be a promising solution to smooth the solar power and thus enhance its grid-integration. There are two possible configurations for BESS integration, i.e., DC coupling and AC coupling, as shown in Fig. 3.7. As it can be observed from Fig. 3.7(a), In the DC-coupled PV-Battery system, the BESS is connected to the PV inverter's DC side. In contrast, for the AC-coupled one, as illustrated in Fig. 3.7(b), the BESS is connected to the point of common coupling at the AC side. Both the DC-coupled and the AC-coupled BESS configurations can be applied to 1500 V PV systems and improve their grid-penetration ability. In this way, a more flexible power management of such power systems is also enhanced to a large extent.

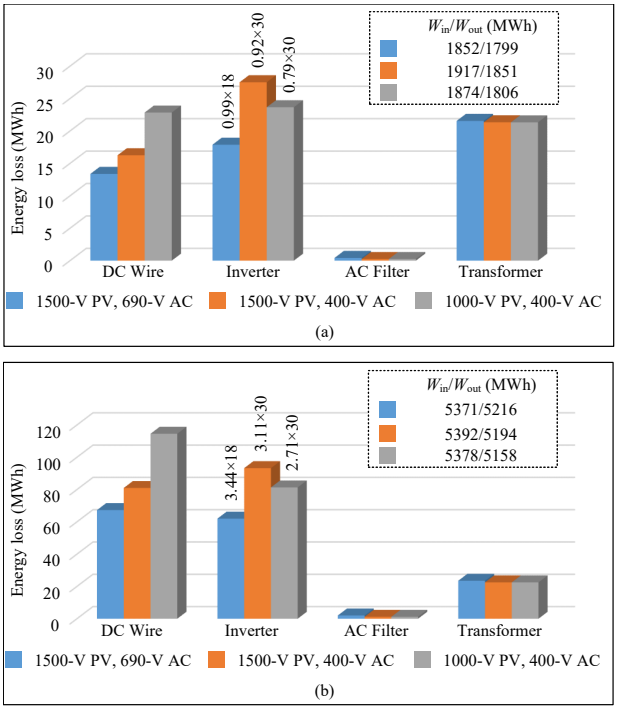


Fig. 3.5: One-year energy losses for the PV systems with various DC and AC voltage ratings installed in: (a) Denmark and (b) Sacramento (W_{in}: available PV energy, W_{out}: energy production). Source: **[C5]**.

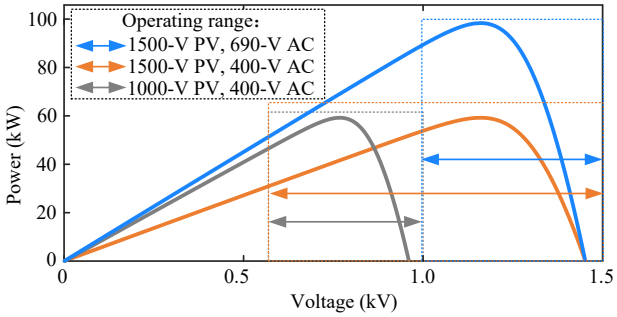


Fig. 3.6: Impact of system voltage rating on DC-bus voltage range. Source: **[C5]**.

Many research efforts have been made to enhance the performance of PV-battery systems with design and control improvements [54–59]. However, the reliability of the 1500-V PV-battery systems has not been fully covered yet. The two configurations could have different reliability performance due to the loading difference of the power conversion units for these two configurations, which may influence the final

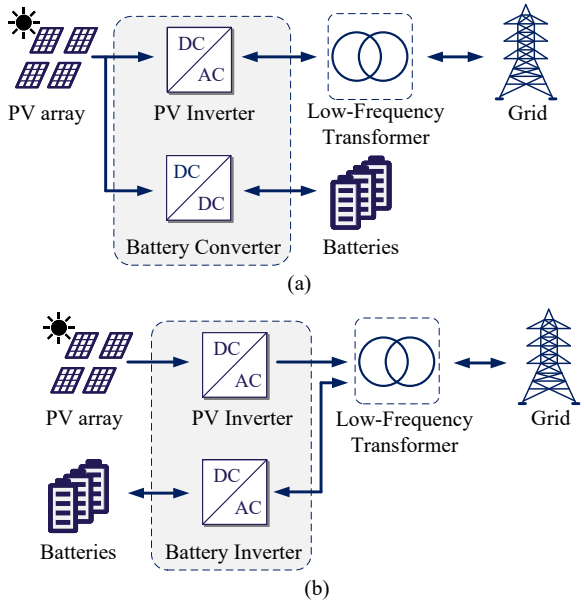


Fig. 3.7: Two possible 1500-V PV-battery systems: (a) DC-coupling and (b) AC-coupling. Source: [**J2**].

design when considering reliability. Therefore, it is essential to evaluate the reliability performance of the power converters for utility-scale PV-battery systems, especially considering 1500-V operations. The 1500-V PV-battery systems have been investigated in [**J2**] with an emphasis on the reliability comparison between DC-coupling and AC-coupling, which will be summarized in this section.

3.2.1 System Description

The 1500 V PV system in *Chapter 2* is considered in this study, with the three-level I-type topology for achieving single-stage power conversion and the switching frequency being 5 kHz. As depicted in Fig. 3.7, a DC- or AC-coupled BESS is deployed to the PV system for smoothing the PV power, hence controlling the power ramping-rate. The reliability comparison concentrates on the power semiconductors of the power conversion units as presented in Fig. 3.7. Similarly to the mission profile translation process in *Chapter 2*, the thermal loading of the PV-battery system can be obtained following the system modeling as depicted in Fig. 3.8, in which, T_a and SI represent the ambient temperature and the solar irradiance, respectively; V_{pv} and P_{pv} are the PV arrays' voltage and power, respectively; P_{inv_in} and P_{inv_out} represent the power to and from the PV inverters; P_{bat_dc} and P_{bat_ac} represent the power to the battery converter (DC-coupling) and the power to the battery inverter (AC-coupling), respectively; V_{bat_dc}, V_{bat_ac}, and V_g, are the DC-coupled BESS's input voltage, the AC-coupled BESS's input voltage, and the grid voltage, correspondingly; P_{sys_out}

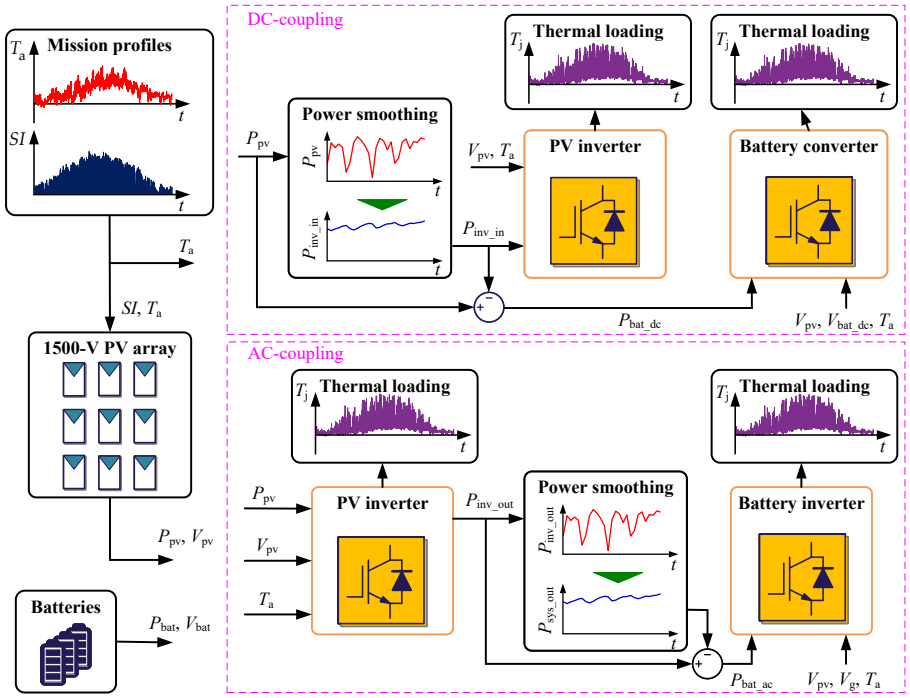


Fig. 3.8: Block diagram of the system modeling for the 1500-V PV-battery systems considering two possible configurations, i.e., DC-coupling and AC-coupling. Source: **[J2]**.

denotes the output power of the AC-coupled PV-battery system; T_j represents the power device's junction temperature.

According to previous studies [55, 57], with the BESS integration, the target ramp-rate limit is assumed to be 10% of the nominal power per minute according to the definition from PREPA (the Puerto Rico Electric Power Authority) [60]. Therefore, a ramp-rate control algorithm is applied to smooth the PV power [57]. Fig. 3.9(a) shows the power smoothing results. The power difference before and after smoothing in Fig 3.9(a), can be regarded as the charging/discharging power reference of the BESS, which is mainly within 100 kW, as it can be seen in Fig. 3.9(b). Fig. 3.10 further compares the ramp-rate variations with and without a 100 kW BESS. As it can be seen in Fig. 3.10, with a 100-kW BESS, in most of days, the ramp rate can be limited within the 10% reference. In contrast, without the BESS, the PV power can frequently experience large rises or drops (> 50%) within 1 minute.

Regarding the BESS, as presented in Fig. 3.11(a), the half bridge-based DC/DC topology is selected for the DC-coupled BESS to implement the battery converter with an interleaved solution (three stages in parallel). As for the AC-coupled BESS, as shown in Fig. 3.11(b), the three-level I-type topology is employed to implement the battery inverter. Table 3.3 summarizes the BESS specifications.

Based on the mission profiles, the thermal loadings of the power semiconductors

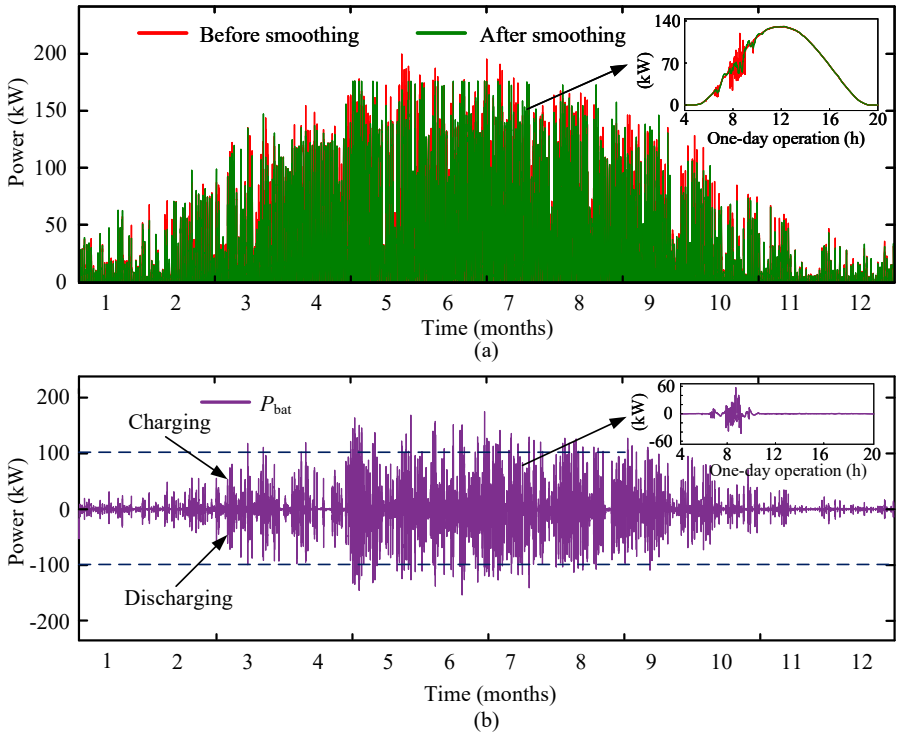


Fig. 3.9: Power smoothing analysis: (a) PV inverter input power with- and without smoothing and (b) battery power of the DC-coupled BESS. Source: **[J2]**.

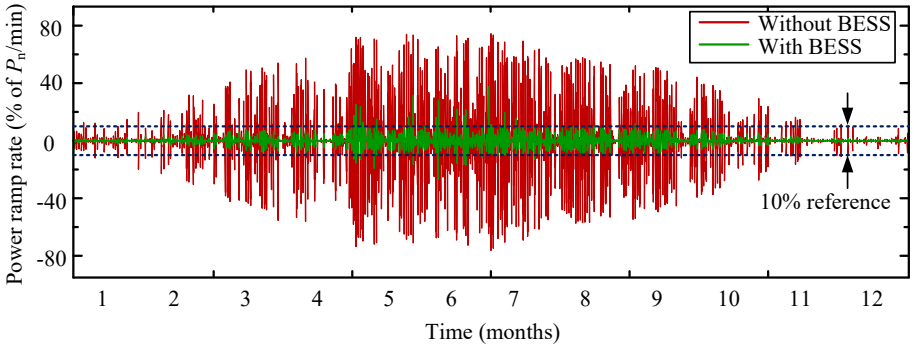


Fig. 3.10: One-year ramp-rate profiles with- and without BESS integration. Source: **[J2]**.

of the PV-battery systems can be acquired through the mission profile translation process, which has been discussed in *Chapter 2*. Fig. 3.12 shows the one-year thermal loading of the most stressed IGBT of the PV inverter under the two BESS configurations. As can be seen in it, the junction temperature fluctuation is lower in the DC case,

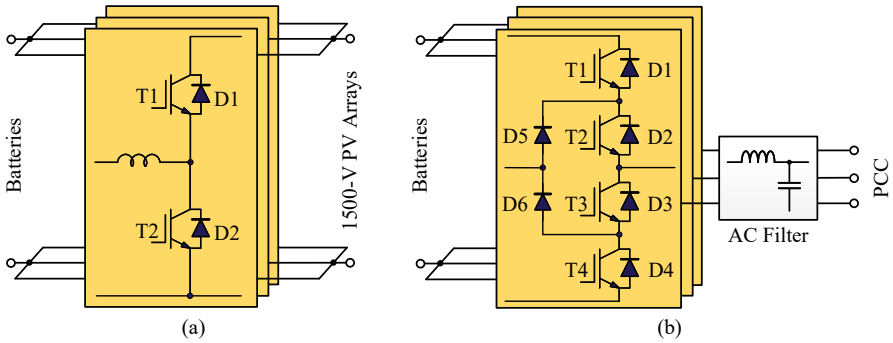


Fig. 3.11: Power converters for the battery energy storage systems: (a) DC-DC converter for DC-coupling and (b) inverter for AC-coupling. Source: **[J2]**.

Table 3.3: BESS Specifications. Source: **[J2]**.

Battery Converter for DC Coupling	
Nominal power P_{nom}	100 kW
Switching frequency f_{sw}	5 kHz
IGBT module	Semikron SKM150GB17E4G
Battery Inverter for AC Coupling	
Nominal power P_{nom}	100 kW
Switching frequency f_{sw}	5 kHz
IGBT module	Semikron SEMiX205MLI12E4
Battery	
Battery type	Samsung, 3.68 V, 94 Ah
Nominal cell voltage / Operating voltage P_{nom}	3.68 V / 3.2-4.15 V
DC voltage range of DC-coupled BESS	670-870 V
DC voltage range of AC-coupled BESS	860-1120 V

hence the inverter's thermal stress is significantly lower when there is a DC-coupled BESS, compared with that under the AC-coupled configuration. The one-year junction temperature profiles of the power semiconductors for the BESS converters are shown in Fig. 3.13, where the DC- and AC-coupled configurations present different thermal loadings. For the battery inverter, as shown in Fig. 3.13(a), the IGBTs and diodes experience a similar thermal stress. In contrast, for the battery converter, a significant thermal loading difference among the power devices can be observed from Fig. 3.13(b). The corresponding reliability analysis will be summarized in the next sub-section.

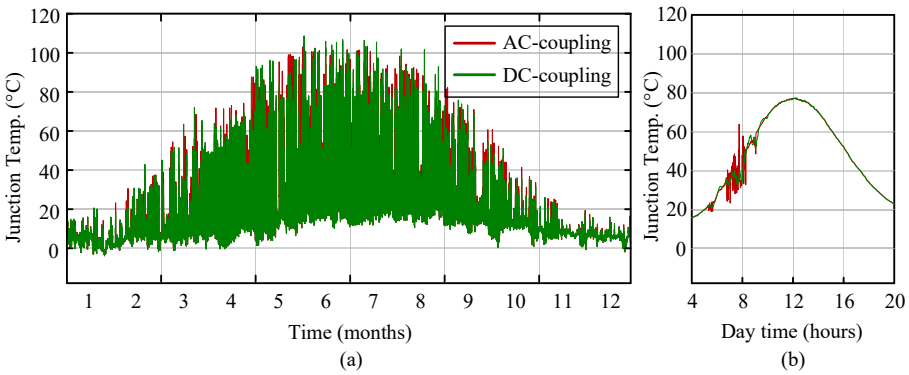


Fig. 3.12: Junction temperature profile of the most stressed PV inverter IGBT in the AC-coupled and DC-coupled configurations: (a) one-year operation and (b) one-day operation. Source: [**J2**].

3.2.2 Reliability Comparison

A. Component-Level Reliability

As it has been discussed in *Chapter 2*, the power device reliability can be evaluated in terms of lifetime consumption during operation, which can be calculated based on a certain lifetime model and damage model with the thermal loading profile as an input. Considering the Denmark mission profile, the one-year lifetime consumptions of the power devices in the 1500-V PV-battery systems are summarized in Fig. 3.14. For the PV inverters, as it can be seen in Fig. 3.14(a-b), the lifetime consumption in the DC-coupled configuration is much lower than that in the AC-coupled configuration. The reason behind this is the reduced PV inverter loading when a DC-coupled BESS is integrated, which yields a smoothed power fed to the PV inverter. Notably, the clamping diodes, i.e., D5 and D6 (referring to Fig 3.11), are ones with the highest lifetime consumption, which means that they are the ones limiting the expected life. Regarding the power devices of the batteries converters, as it can be observed from Fig. 3.14(c-d), in both cases, there are power devices that have higher lifetime consumption compared to the corresponding PV inverter, especially for the DC-coupled configuration. Therefore, it can be expected that the battery converters either in DC-coupling or AC-coupling will have a stronger influence on the system's overall reliability performance.

B. System-Level Reliability

The above lifetime consumption results have been integrated with reliability analysis at converter level and system level, based on the Monte-Carlo analysis presented in *Chapter 2*. The obtained unreliability functions for the AC-coupled and DC-coupled configurations are shown in Fig. 3.15. For the PV inverters, as shown in Fig. 3.15(a-b), the inverter reliability performance is mainly limited by the clamping diodes. In the DC-coupled configuration, the PV inverter's B_1 lifetime is more than two times as much as the AC-coupled configuration. Notably, the B_1 lifetime results indicate that, in both cases, the PV inverter has excessive design margin for the Denmark mission

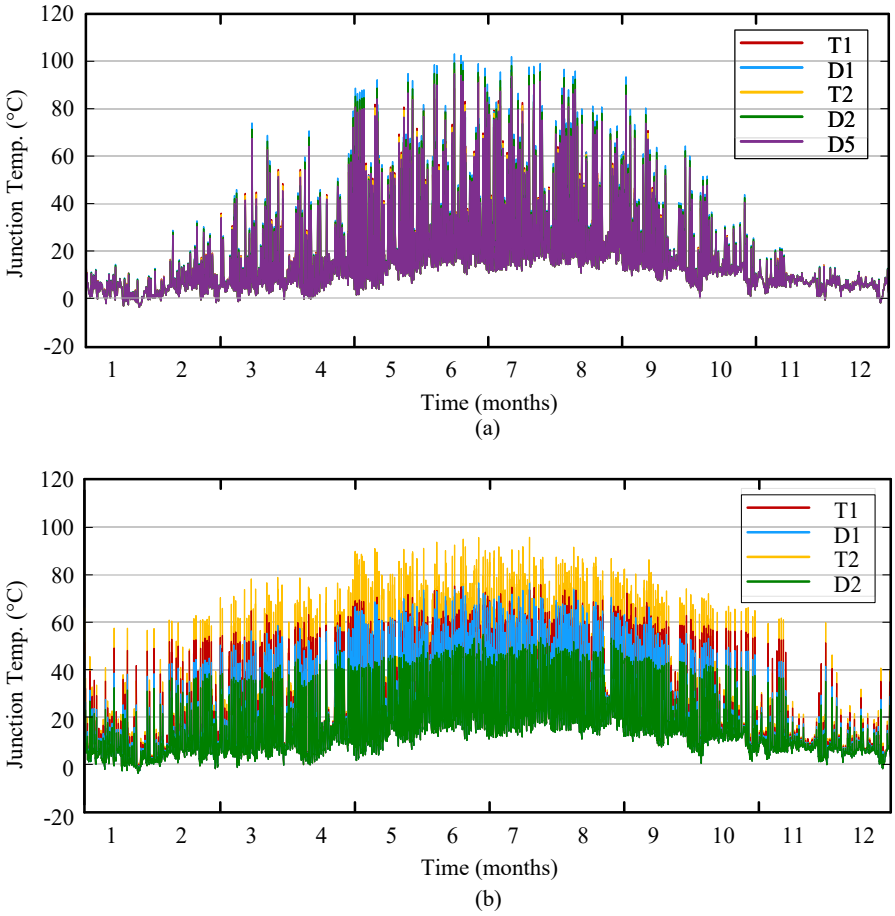


Fig. 3.13: One-year junction temperature profiles of the individual devices (referring to Fig. 3.11) in: (a) battery inverter for AC-coupling and (b) battery converter for DC-coupling. Source: [**J2**].

profile. As for the battery converters, in the case of AC-coupling, the diode D1 becomes the most stressed device due to the bidirectional power flow, as shown in Fig. 3.15(c). For the DC-coupling case, the converter reliability is mainly limited by IGBT T2, as shown in Fig. 3.15(d). Notably, for both configurations, the battery converters are less reliable compared to their PV inverter counterparts.

The system-level unreliability functions have been obtained, as shown in Fig. 3.16 (solid lines). As expected, for both configurations, the system-level reliability is mainly affected by the reliability performance of the battery converter, compared to the corresponding PV inverter. This is pretty obvious in the DC-coupled case, where the unreliability functions of the system and the battery converter are overlapped, as can be seen in Fig. 3.16(b). Although the DC-coupled battery integration can considerably improve the PV inverter reliability, the reliability performance of the

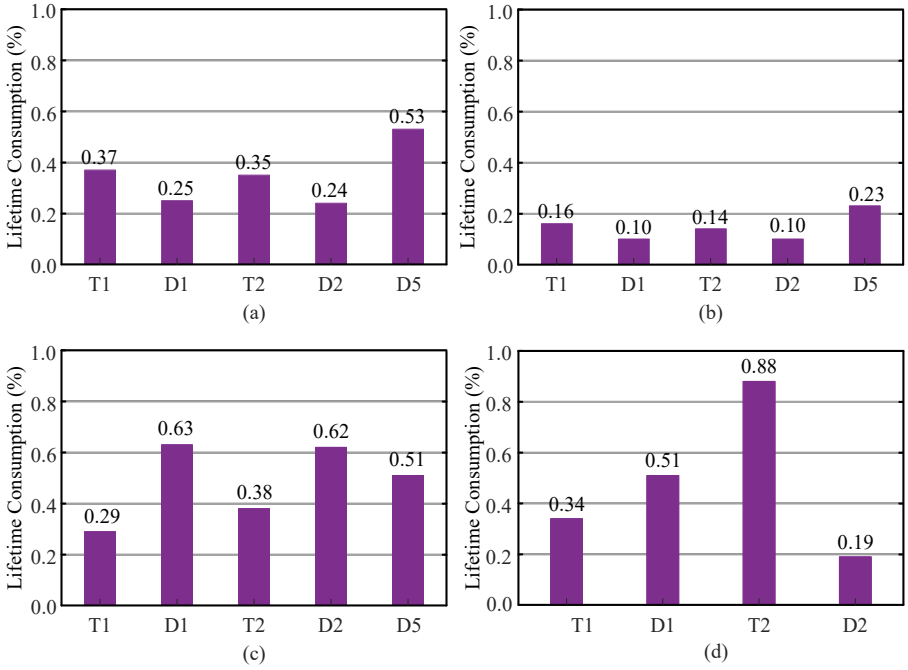


Fig. 3.14: One-year lifetime consumption of the individual devices (referring to Fig. 3.11) in: (a) PV inverter in AC-coupling, (b) PV inverter in DC-coupling, (c) battery inverter for AC-coupling, and (d) battery converter for DC-coupling. Source: [**J2**].

battery converter limits the overall system reliability. Consequently, the AC-coupled configuration is better than the DC-coupled configuration due to its higher and more balanced reliability performance.

3.3 Summary

In this chapter, the performance of the large-scale PV systems based on centralized 1500-V string inverter solutions was studied, which is based on the power loss analysis on the main parts of the PV system (i.e., DC wires, PV inverters, AC filters, and transformers) considering various DC- and AC-voltage ratings as well as different mission profile characteristics. Three string inverter solutions were considered for comparison, i.e., 1500-V PV with 690-V AC, 1500-V PV with 400-V AC, and 1000-V PV with 400-V AC. The comparison results indicate that, in both mission profile cases, the 1500-V solutions outperform the 1000-V one. More in detail, in the case of a hot climate with high irradiance, e.g., Sacramento, the string inverter solution with higher DC and AC voltages, e.g., 1500-V PV and 690-V AC, outperforms the other solutions in terms of loss and cost reduction (lower wire loss and fewer inverter units). In contrast, for the mission profile with low solar irradiance, e.g., Denmark, the solution with high

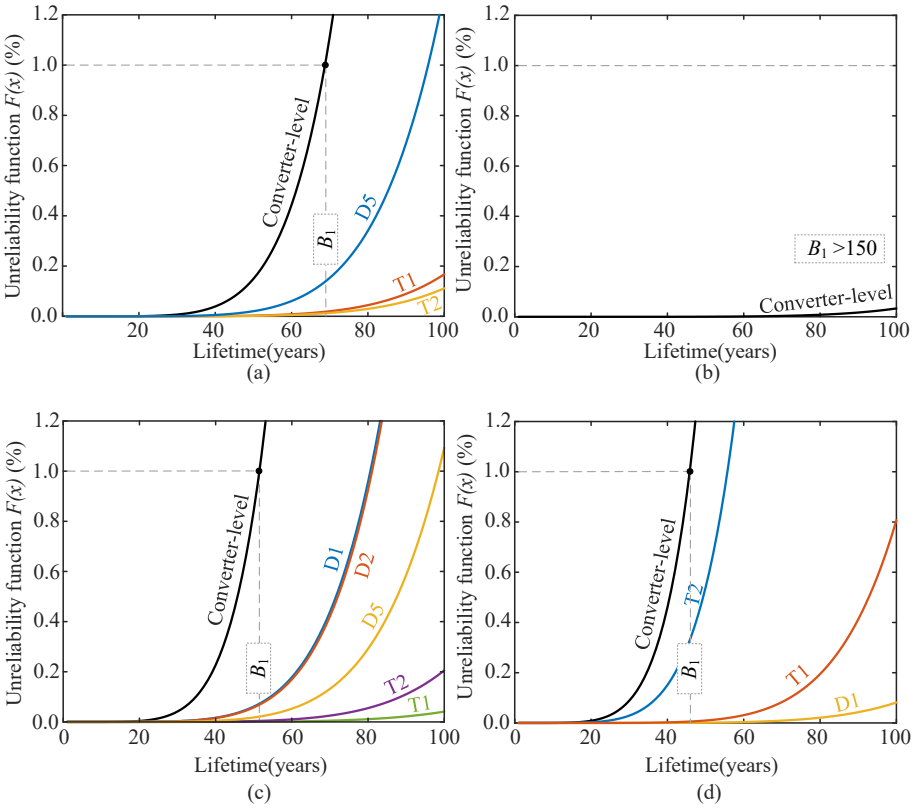


Fig. 3.15: Component-level and converter-level unreliability functions for the AC-coupled and DC-coupled configurations: (a) PV inverter in AC-coupling, (b) PV inverter in DC-coupling BESS, (c) battery inverter for AC-coupling, and (d) battery converter for DC-coupling. Source: **[J2]**.

DC voltage but low AC voltage, i.e., higher DC-bus voltage range, is preferred for achieving higher energy production.

On the other hand, the reliability of 1500-V PV-battery system was investigated considering both DC- and AC-coupled configurations. The impact of different BESS configurations on power converter reliability was assessed. By doing so, the selection of BESS configurations considering 1500-V operation can be justified in terms of reliability performance. Also, the most lifetime-critical part in the system has been identified by means of reliability evaluation, which will be beneficial to the design-for-reliability of the 1500-V PV system with BESS integration. The reliability benchmarking results reveal that, for both the BESS configurations, the reliability performance of the battery converter limits the overall system reliability. Overall, the reliability performance of the AC-coupled one is slightly better than that of the DC-coupled one.

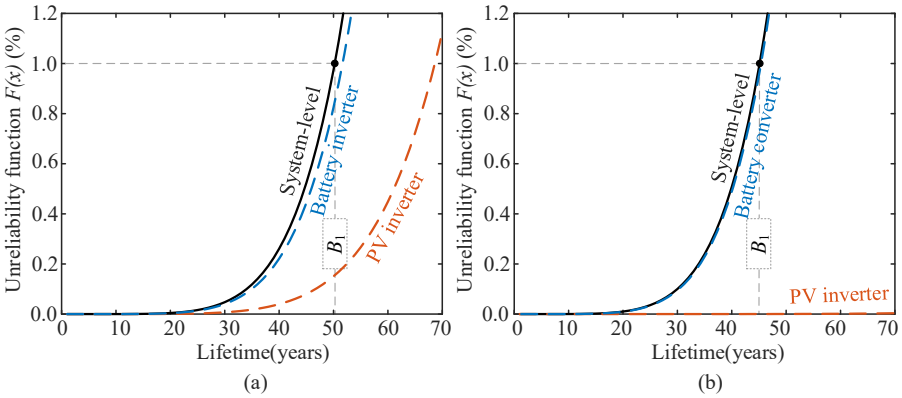


Fig. 3.16: Unreliability function of PV-battery systems: (a) AC-coupling and (b) DC-coupling. Source: **[J2]**.

Related Publications

C5. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Performance Comparison of PV Inverter Systems Considering System Voltage Ratings and Installation Sites," in *Proc. IEEE APEC*, pp. 2620-2625, Jun. 2021.

J2. **J. He**, Y. Yang, and D. Vinnikov, "Energy Storage for 1500 V Photovoltaic Systems: A Comparative Reliability Analysis of DC- and AC-Coupling" *Energies*, vol. 13, no. 13, pp. 3355, Jul. 2020.

Chapter 4

Methods for Improving Reliability

Although many efforts have been made to improve the reliability of PV inverters, considering the 1500-V PV applications, new reliability concerns are raised, which are related to the increased DC-link voltage stress and have not been fully addressed yet. Therefore, this chapter presents three methods, i.e., variable gate resistance design, junction temperature limit control, and discontinuous modulation strategy, to improve the thermal performance and reliability of the 1500-V PV inverters considering both normal and abnormal operating conditions. The effectiveness of these methods has been verified through simulations and experiments.

4.1 Variable Gate Resistance Design

The Silicon-Carbide (SiC) power modules outperform the IGBT ones in terms of switching loss, switching speed, and conduction loss, which are pretty suitable for 1500-V PV inverters, even in the form of a simple two-level topology. However, the two-level 1500-V PV inverters based on 1700-V power modules (either IGBTs or SiC MOSFETs) have a limited margin on blocking voltage. This is mainly caused by the stray inductance in the commutation loop, which will cause a voltage overshoot during switching transients. This is even more critical for SiC MOSFETs. During cold days in winter, the PV string voltage at the maximum power point (MPP) is up to 80-85% of the open-circuit voltage, i.e., 1500 V [28]. In this context, the voltage overshoot should be lower than 400 V to keep the SiC MOSFET modules within their voltage rating, i.e., 1700 V.

It is known than the gate resistance of SiC MOSFETs would influence the voltage overshoot since it can change the switching speed. Fig. 4.1 shows the turn-off transients of a 1700-V SiC MOSFET module with various gate resistance values, where the DC-link voltage and the drain current are 1300 V and 250 A (rated current), respectively. As can be seen in it, smaller gate resistance gives rise to higher voltage overshoots.

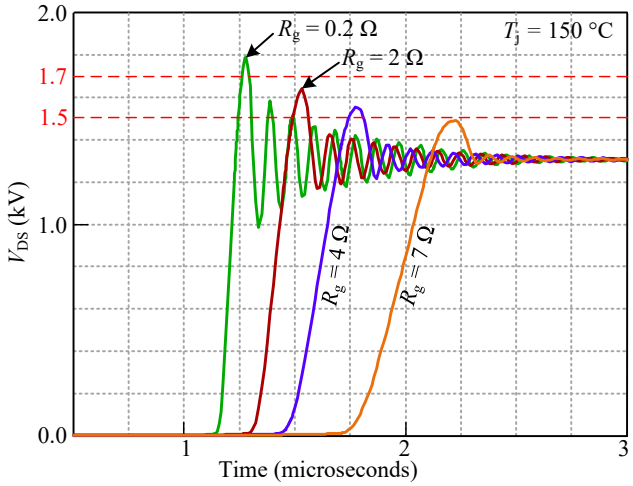


Fig. 4.1: Turn-off transients of a 1700-V SiC MOSFET power module with various external gate resistance values under 1300-V DC-link and 250-A load current. Source: **[C3]**.

Therefore, to reduce the overshoot, the external gate resistance could be increased. However, as it can be seen in Fig. 4.1, a high gate resistance also means a greater rise time, which will result in higher switching losses, affecting the inverter efficiency and reliability, as discussed in [24]. Many efforts have been made to develop active gate driving technologies [61–63], which can dynamically change the gate resistance during the switching transients, thus limiting the voltage overshoot without increasing the switching losses. However, their implementation is complicated and challenging due to the quick switching transient of the SiC MOSFETs. A more viable and robust way for the considered PV systems, i.e., single-stage two-level 1500-V PV inverters, is to select the gate resistance at each switching period according to the DC-link voltage. This variable gate resistance design has been presented in **[C3, J3]**, and will be summarized in the following.

4.1.1 Proposed Approach

Fig. 4.2 presents the circuit diagram of the proposed variable gate-resistance design. As it can be seen in Fig. 4.2, according to the input signals of the signal conditioning unit, i.e., the DC-link voltage signal and the pulse width modulation (PWM) signal, various external gate resistors are selected. As a consequence, the SiC switch could be equipped with a large external gate resistance, i.e., R_{main}, when the DC-link voltage exceeds a certain level. Also, in the case of low DC-link voltages, the applied gate resistance could be reduced to $R_{\text{main}} \| R_{\text{aux1}}$ or $R_{\text{main}} \| R_{\text{aux2}}$. By doing so, a safer blocking voltage margin can be ensured during the operation, in comparison to that with fixed gate resistance. Considering the Denmark mission profile in *Chapter 2*, a power loss analysis was carried out. The results in Fig. 4.3 indicates that the proposed approach can reduce the energy loss, hence improving reliability, compared to a fixed

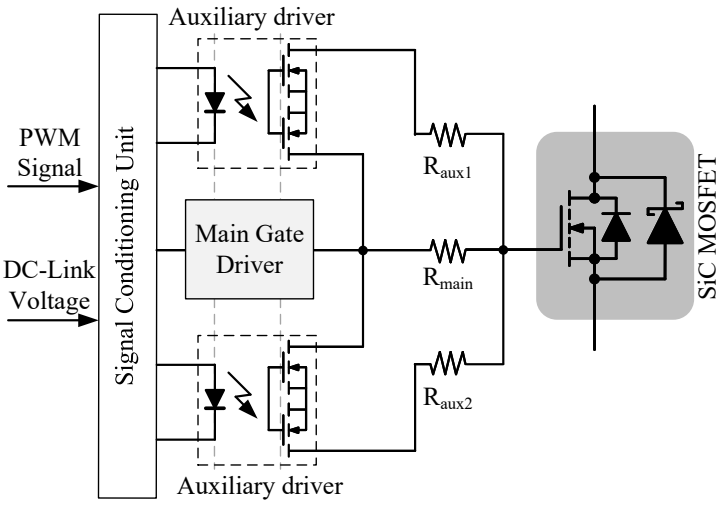


Fig. 4.2: Circuit diagram of the proposed variable gate-resistance design. Source: [**J3**].

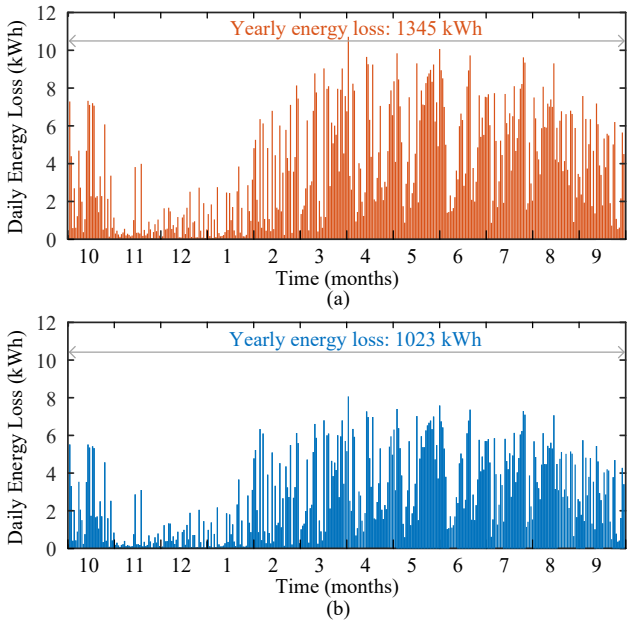


Fig. 4.3: Daily energy loss profile under the Denmark mission profile: (a) with the fixed gate resistance and (b) with the proposed approach. Source: [**C3**].

gate-resistance design, in which a fixed resistance of the highest value is used to withstand the highest voltage stresses.

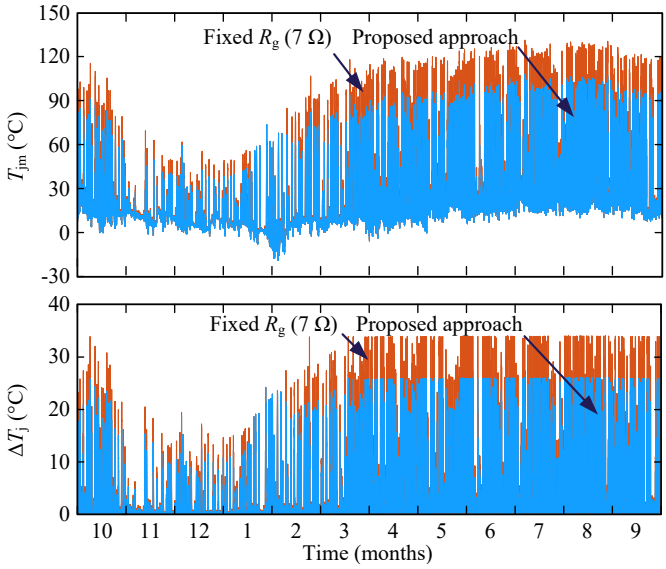


Fig. 4.4: One-year thermal loading (mean junction temperature and cycle amplitude) profiles of the inverter SiC MOSFET: fixed gate resistance vs. proposed approach. Note: the evident cycle-amplitude temperature clipping occurring from March to October is related to the maximum power limitation of the considered inverter. Source: **[C3]**.

4.1.2 Reliability Assessment

A reliability assessment was carried out to investigate the potential for improving the reliability of the SiC-MOSFET two-level 1500-V PV inverters with the proposed approach. The thermal loadings of the inverter SiC MOSFET during one-year operation were obtained, which are shown in Fig. 4.4. Correspondingly, the one-year lifetime consumption has been calculated, which is summarized in Table 4.1. As it can be seen in Fig. 4.4, the thermal stress of the SiC MOSFET driven by the proposed variable gate resistance is much lower in comparison to that with a fixed one. The lifetime consumption results in Table 4.1 show that, with the proposed approach, the one-year lifetime consumption can be reduced by 72.8% in comparison to the fixed case (i.e., R_g = 7 Ω). The proposed design can achieve a similar reliability performance as case 4, i.e., R_g = 4 Ω. However, compared to cases with low gate resistance, e.g., cases 3-4, the proposed approach can ensure a safer blocking voltage margin.

Table 4.2 further summarizes the impact of the gate-resistance design on the switching loss, the voltage overshoot, and the lifetime consumption. The comparison in Table 4.2 indicates that, when applying a fixed-resistance gate driver, a trade-off should be always considered between voltage overshoot and switching loss. In contrast, the variable gate-resistance design pushes this trade-off forward and improves the inverter reliability.

Table 4.1: Lifetime Consumption (LC) Comparison. Source: **[C3]**.

Gate driving methods	LC	LC compared to Case 1
Case 1: fixed $R_g = 7\ \Omega$	0.0261	–
Case 2: fixed $R_g = 6\ \Omega$	0.0198	24.1% lower
Case 3: fixed $R_g = 5\ \Omega$	0.0134	48.7% lower
Case 4: fixed $R_g = 4\ \Omega$	0.0070	73.2% lower
Case 5: variable R_g: 2-7 Ω	0.0071	72.8% lower

Table 4.2: Gate-Resistance Design Comparison. Source: **[C3]**.

Gate resistance	Voltage overshoot	Switching loss	Lifetime consumption
Large	Low	High	High
Small	High	Low	Low
Variable	Low	Low	Low

4.2 Junction Temperature Limit (JTL) Control

The junction temperature of power semiconductors, reflecting the thermal stress level in terms of mean value and cycle amplitude, is one of the key factors that affects device reliability hence lifetime, which is determined by the mission profile characteristics [64]. A reduction of power device's mean junction temperature, by using power control/regulation, can contribute to the reliability enhancement of PV systems with no need for improving the power device itself or the converter design [31, 65]. Bearing this in mind, to enhance the reliability of the 1500-V PV inverters, a junction temperature limit (JTL) control concept has been proposed in this section. The proposed control scheme combines a power control strategy for junction temperature limitation with a Maximum Power Point Tracking (MPPT) control strategy, which could be alternated during operation according to the mission profiles. Fig. 4.5 presents the benefit of JTL control. As can be seen in it, the mean junction temperature would not exceed 90 °C at any time. In contrast, with the JTL control, it would hit 100 °C. This control concept has been discussed in **[C4]**, and is summarized in the following.

4.2.1 Proposed Approach

To limit the mean junction temperature, the input power of the PV system should be reduced, i.e., below the maximum power point (MPP), as demonstrated in Fig. 4.6. This can be achieved by means of PV voltage regulation, which is expressed as

$$V_{\mathrm{pv}}^{*} = \begin{cases} V_{\mathrm{MPPT}}, & \text{when } T_{\mathrm{jm}} \leq T_{\mathrm{jm,limit}} \\ V_{\mathrm{pv}} - V_{\mathrm{step}}, & \text{when } T_{\mathrm{jm}} > T_{\mathrm{jm,limit}} \end{cases} \tag{4.1}$$

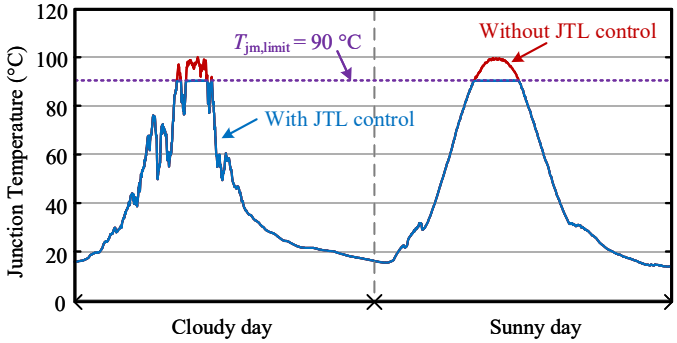


Fig. 4.5: Daily mean junction temperature profiles with- and without the junction temperature limit (JTL) control. Source: **[C4]**.

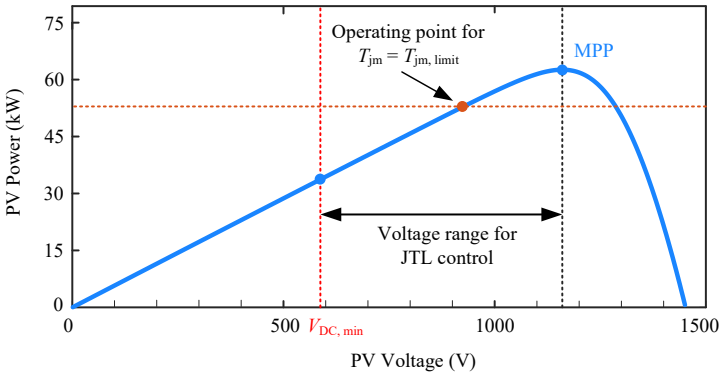


Fig. 4.6: Principle operating point and voltage range for the proposed control at a given irradiance- and ambient- temperature level, where the minimum DC-link voltage $V_{DC,min}$ is determined by the grid voltage. Source: **[C4]**.

where V_{MPPT} is the voltage reference for MPPT, V_{step} represents the step size for perturbation & observation (P&O) [66], T_{jm} denotes the mean junction temperature of the power device, and $T_{jm,limit}$ is the target temperature for the proposed approach.

According to (4.1), when the junction temperature does not exceed the limit reference, the applied control is the MPPT control. On the contrary, once it exceeds the limit reference, the system will decrease the PV voltage reference hence the output power to reduce the PV inverter's thermal loading. Obviously, the lower the temperature limit reference, the higher the reliability it will have. However, the tradeoff between reliability performance and energy yield should be considered. The implementation of the proposed approach is shown in Fig. 4.7 in form of a flowchart, where an extra measurement is performed to avoid the influence caused by fast changing of irradiance [66].

Considering a 1500-V single-stage PV system interfacing the grid with a three-level I-type inverter, Fig. 4.8 shows the variations of the PV inverter's DC-link voltage

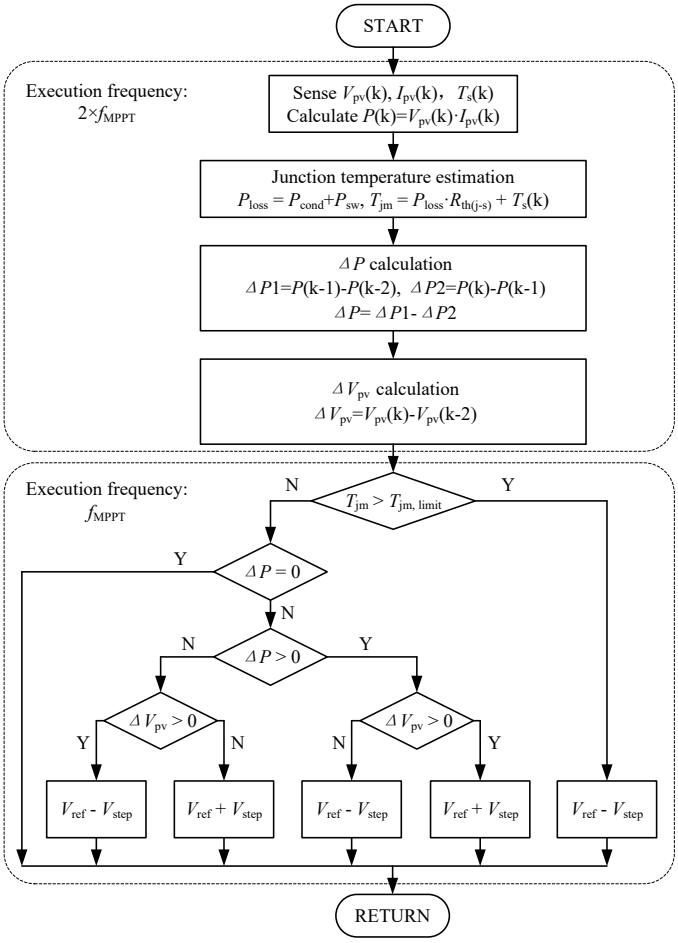


Fig. 4.7: Flowchart of the proposed approach. Source: **[C4]**.

and output power caused by a trapezoidal irradiance profile considering two cases, i.e., with- and without the proposed control. Correspondingly, Fig. 4.9 presents the variation of the junction temperature. As it can be observed from Fig. 4.8(a), without the proposed control, the output power follows the irradiance change, and the DC-link voltage just slightly fluctuates with the irradiance change. As a consequence, a rise of the mean junction temperature, from 85.7 °C to 95.8 °C in Fig. 4.9(a), comes with the irradiance increase. In contrast, in case of applying the proposed control, the DC-link voltage has dropped to a certain level to reduce the output power as shown in Fig. 4.8(b). Correspondingly, during the high irradiance period, the mean junction temperature is maintained at the target value (i.e., 90 °C) as shown in Fig. 4.8(b). Notably, the cycle amplitude ΔT_j is also decreased to 13.2 °C in comparison to the 16-°C cycle amplitude without the proposed control.

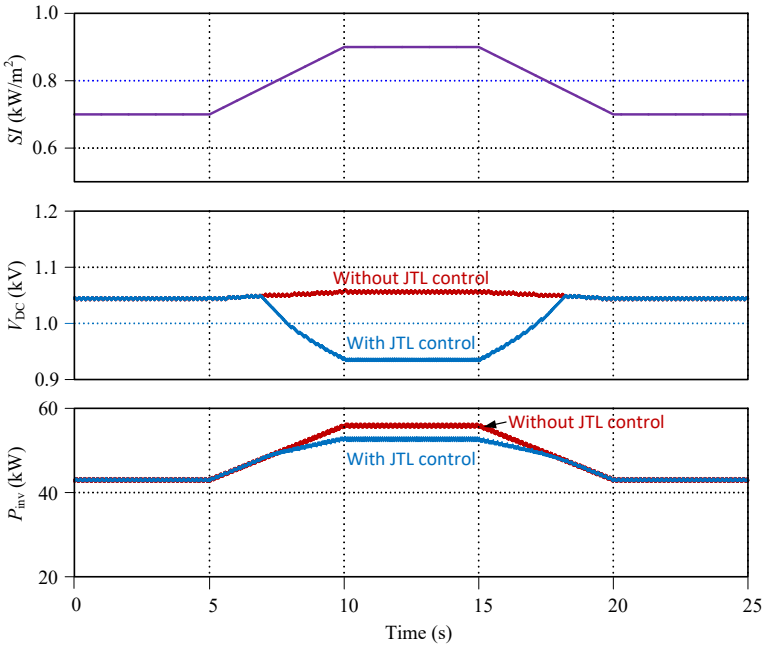


Fig. 4.8: Variations of the DC-link voltage V_{DC} and output power P_{inv} along with a trapezoidal solar irradiance SI profile with- and without the junction temperature limit (JTL) control. Source: [**C4**].

4.2.2 Reliability Assessment

A reliability assessment was carried out to present the benefit of the proposed approach on the inverter reliability. Fig. 4.10 shows the thermal loadings of the most stressed device during one-year operation. As shown in Fig. 4.10, when the proposed approach is applied with the limit reference being 90 °C, overall, the power device suffers from much lower thermal stress (mean value and cycle amplitude) compared to that with the standard control, i.e., MPPT control, which will contribute to the reliability enhancement of the PV inverter.

The thermal stress mitigation is achieved at the expense of a certain decrease of energy yield. Therefore, a tradeoff should be considered between the reliability enhancement and the decrease of energy yield. The value of the normalized power device lifetime (to the device lifetime under MPPT scheme) has been calculated for temperature limits from 80 °C to 120 °C, as well as the energy yield percentage against that under MPPT mode, as shown in Fig. 4.11. It can be observed from Fig. 4.11 that, when the limit reference is below 100 °C, a considerable lifetime extension is achieved, e.g., by setting the temperature limit to 90 °C, the device lifetime can be improved to 1.45 times at the cost of 0.7% reduction in yearly energy yield. At the same time, as presented in Fig. 4.11, the energy yield would be decreased rapidly with further lifetime extension, where a comprehensive system-level reliability assessment is further

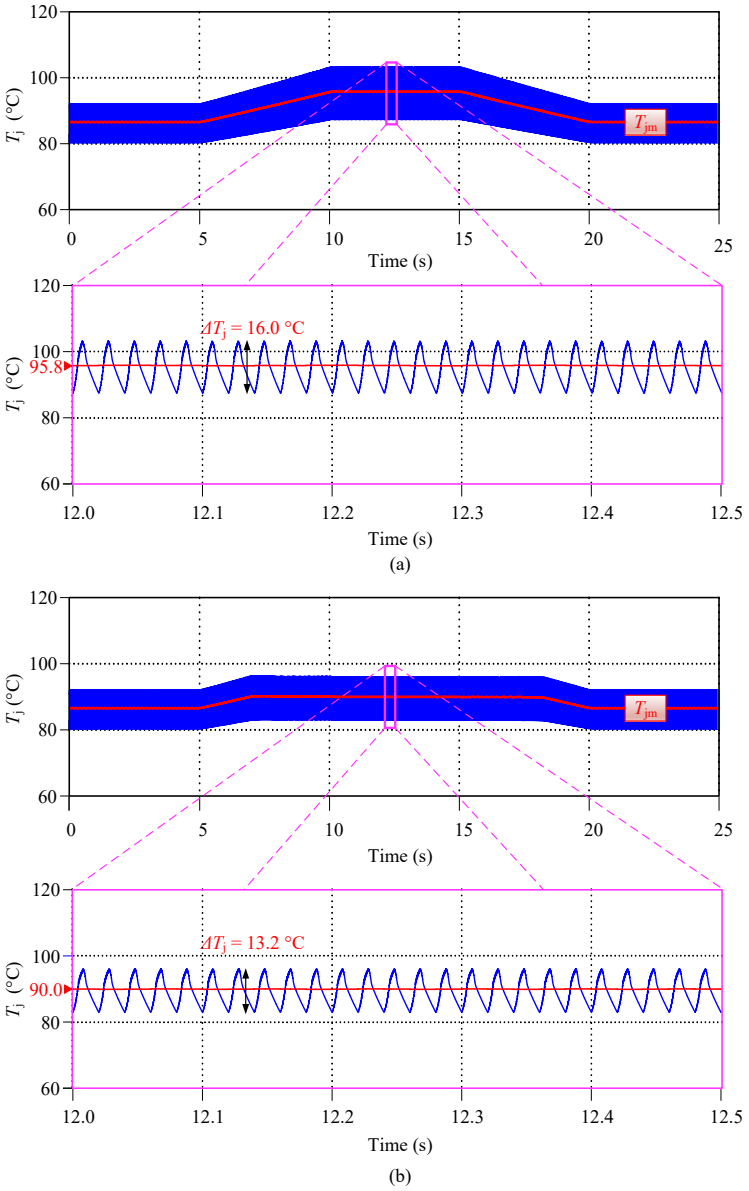


Fig. 4.9: Variations of the mean junction temperature T_{jm} along with a trapezoidal irradiance profile: (a) without the proposed control and (b) with the proposed control. Source: **[C4]**.

required to determine the best tradeoff. Nevertheless, the evaluation results suggest that the proposed control is able to extend the power device lifetime considerably at the expense of a slight energy yield reduction.

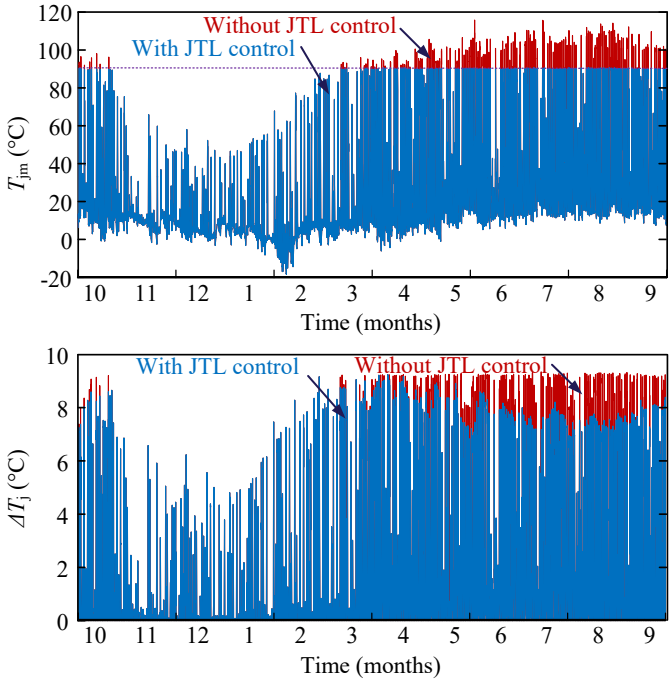


Fig. 4.10: One-year mean junction temperature T_{jm} and cycle amplitude ΔT_j profiles of the most stressed inverter device with- and without the junction temperature limit (JTL) control. Source: **[C4]**.

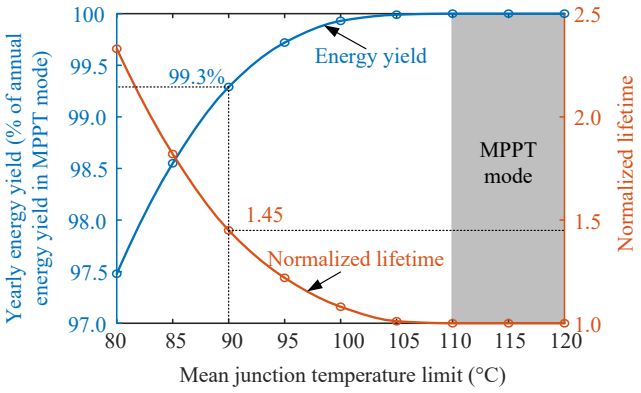


Fig. 4.11: Comparison of the yearly energy yield and the device lifetime under various temperature limits. Source: **[C4]**.

4.3 DPWM for Improved Thermal Balance during LVRT

Generally, reactive power support during low-voltage ride-through (LVRT) operation is an indispensable requirement for 1500-V PV systems. However, the PV inverters may experience high loading stress when doing so [67]. For 1500-V PV inverter based on three-level I-type topology, the power devices, i.e., IGBTs and diodes, are not equally utilized thus have different loading stress when using the traditional continuous pulse-width modulation (PWM) strategies [15, 68]. This is more critical during reactive power support at severe LVRT events, where two things happen to a single-stage PV system: 1) 100% rated reactive current under seriously reduced grid voltage [69], and 2) high DC-link voltage at the input, i.e., the PV string's open-circuit voltage [70]. These extreme operating conditions along with the low modulation indices make the inner power devices of each inverter leg carry much higher RMS currents in comparison to the outer devices. As a consequence, these power devices will have a considerably unequal power loss which leads to severely unbalanced thermal distribution. As it can be seen in Fig. 4.12, where two possible LVRT operating conditions, i.e., 0.1 p.u. and 0.5 p.u., are considered to present the junction temperature difference. This unbalanced thermal distribution will affect the thermal performance of the PV inverter. However, for a single-stage PV system based on the three-level I-type topology, the thermal distribution analysis during LVRT events has not been thoroughly studied yet, especially considering the 1500-V operations. This issue has been mitigated in **[C6]** through a discontinuous PWM (DPWM) strategy, which will be summarized in the following.

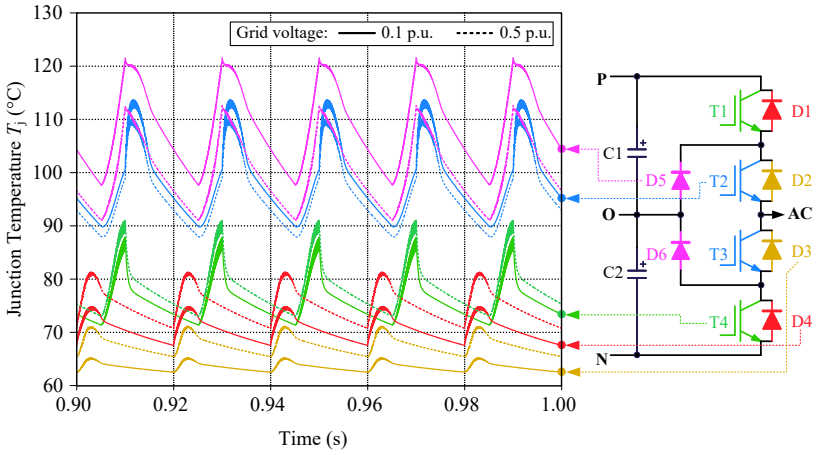


Fig. 4.12: Junction temperature of the inverter power devices during LVRT operating conditions. Source: **[C6]**.

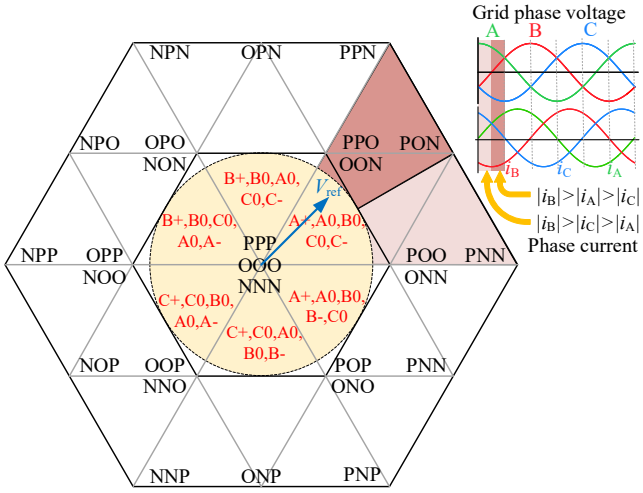


Fig. 4.13: Vector space of the three-level I-type inverter. Source: **[C6]**.

4.3.1 Proposed Approach

For a three-phase three-level I-type inverter, each phase has three available switching states, i.e., "P" , "O", and "N" , as shown in Fig. 4.12. Consequently, 27 space vectors are available, forming a vector space as illustrated in Fig. 4.13 [71]. Generally, with three-level DPWM strategies, each phase X (X = A, B, C) can be clamped to the "P" , "O", or "N" point of the DC link for switching loss reduction [72, 73], namely, "X+", "X0", or "X-" clamping state, respectively. All the available clamping states for each inner sub-sector (modulation index $m \leq 0.5$), which are possible during LVRT events, are labeled in Fig. 4.13. For instance, if the vector reference V_{ref} is located in the sub-sector as indicated in Fig. 4.13, five clamping states are available, i.e., A+, A0, B0, C0, and C-.

Typically, it is expected that the DPWM strategies can reduce the switching losses as much as possible. Consequently, their modulation objective is to make the clamping states correspond to the positions of current peaks [73], which could be completely satisfied if $m \leq 0.5$. Since each type of the clamping state is available in such a case as shown in Fig. 4.13. However, considering a 100% reactive current injection during LVRT, as indicated in the inset of Fig. 4.13, with the maximum switching loss reduction objective, only "X0" will be selected for current peaks. Nevertheless, by doing so, the utilization of the clamping diodes will increase, which means higher thermal stress on them. Thus, the selection of "X0" clamping state should be avoided in such a case, as it will further aggravate the clamping diodes' overloading.

In this work, the proposed DPWM strategy, which is summarized in Fig. 4.14, gives priority to achieve thermal balance when selecting the clamping states. In Fig. 4.14, $u_{\text{i-max}}$ and $u_{\text{i-mid}}$ represent voltage of the phase with the maximum current i_{max} and the middle current i_{mid}, respectively; i_{X} denotes phase current; u_{X}, u_{com}, and u'_{X} represent the original phase voltage reference, the injected common-mode voltage,

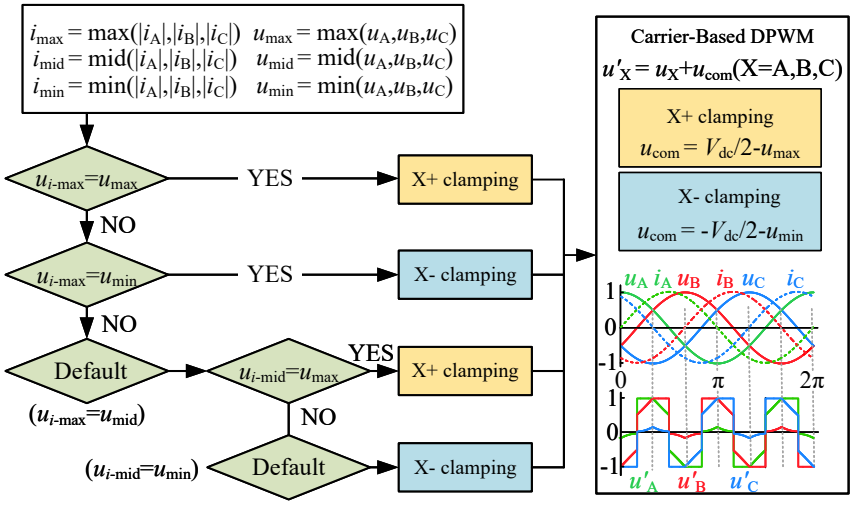


Fig. 4.14: Block diagram of the proposed DPWM strategy. Source: **[C6]**.

and the modulation voltage, respectively. When the current lags the voltage by 90°, i.e., during reactive power support, the modulation waves generated by the proposed DPWM are also presented in Fig. 4.14, where it can be seen that only “X+” and "X-" are selected, even though "X0" would be better for switching loss reduction in this case. For the proposed DPWM, when “X+” or “X-” is not corresponding to current peaks, the middle current is considered for selecting “X+” and “X-”. By doing so during LVRT operation, the thermal stress of the clamping diodes will be reduced, and the thermal stress among the power semiconductors will be redistributed.

4.3.2 Analysis of Thermal Redistribution

To verify the proposed approach, the junction temperature dynamic has been simulated considering a 0.5-s 0.5-p.u. voltage sag. During normal operation, the PV inverter is assumed to inject 50% rated active power to the grid under 1100-V DC-link voltage with the conventional SPWM and MPPT control. During the voltage sag, 100% rated reactive current is injected to the grid under 1300-V DC-link voltage, and the applied modulation strategy is switched to the proposed approach or other PWM strategies for comparison.

The proposed DPWM has been compared with another two modulation strategies: 1) the conventional SPWM, and 2) the DPWM strategy in [73], where the clamping states corresponding to the current peaks are selected to reduce switching loss as much as possible (referred to simply as SLDPWM in this section). The junction temperature dynamics under these PWM schemes are shown in Fig. 4.15. It can be seen in Fig. 4.15(a) that continuing to use the conventional SPWM during LVRT operation brings increased thermal stress to the clamping diode D5. If the applied PWM during LVRT is the SLDPWM, as shown in Fig. 4.15(b), the thermal stress of IGBT T1 will be considerably

reduced in comparison to that with the conventional SPWM. However, the junction temperature of the most stressed device, i.e., the clamping diode D5, is even higher than that with the conventional SPWM. As mentioned earlier, this is due to the neutral point clamping "X0", which is selected by the SLDPWM for switching loss reduction in such a case. When it comes to the proposed DPWM, the thermal stress of D5 is reduced to a large extent as shown in Fig. 4.15(c). The cost for achieving so is the increased thermal stress on diodes D1 and D2. It can be further seen from the perspective of power losses that, as presented in Fig. 4.16, with the SLDPWM or the proposed DPWM, a considerable reduction in switching losses (thus the total power losses) is achieved in comparison to that with the conventional SPWM. More importantly, seen from the perspective of power loss distribution, the proposed DPWM is superior than the SLDPWM. As it can be observed from Fig. 4.15(b) and (c), with the proposed DPWM, the power losses are redistributed from diode D5 to diodes D1 and D2, i.e., the most stressed device to the less stressed ones, achieving a balanced power loss distribution, hence balanced thermal distribution.

4.3.3 Experimental Validation

An experimental platform, as shown in Fig. 4.17, has been constructed to further verify the effectiveness of the proposed DPWM. Three IGBT modules (Skiip 39MLI12T4V1 from Semikron) are adopted to build up the three-phase three-level I-type inverter. This one is supplied by a 1500-V DC power source from ITECH. Regarding the AC side, there are LC filters (2.4 mH, 10 μF) along with an isolation transformer (10 kVA) between the inverter and the AC grid (400-V line voltage). The device junction temperature can be measured by the optic fiber sensor, which is installed on the IGBT module with openings to reach the device chips. Fig. 4.18 presents the steady-state voltage and current waveforms of the inverter's AC side. These waveforms are captured when injecting 10-A reactive current to the 400-V grid at 1300-V DC-link voltage, which are similar to the operating conditions during severe LVRT events. It can be seen in Fig. 4.18 that only the positive and negative clamping states, i.e, "X+" and "X-", exist in the phase voltage when applying the proposed approach. This is the way in which the proposed approach is original and differs from the previous DPWM strategies, where "X0" is preferred to reduce the overall switching losses as discussed in [73].

Fig. 4.19 shows the junction temperature variations of the clamping diode D5, which are captured with the reactive current's ramp-up. As it can be seen in Fig. 4.19(a), the junction temperature rises linearly from 24 °C to 37 °C when using the SPWM strategy. In contrast, when the applied modulation strategy is switched to the proposed DPWM during operation, as shown in Fig. 4.19(b), the highest junction temperature is only 30 °C. More importantly, a considerable decreasing in D5's junction temperature can be observed in Fig 4.19(b) even if the current is still increasing. Comparing to the junction temperature variation under the SPWM strategy, A 2-°C drop has been achieved with the proposed DPWM in one second.

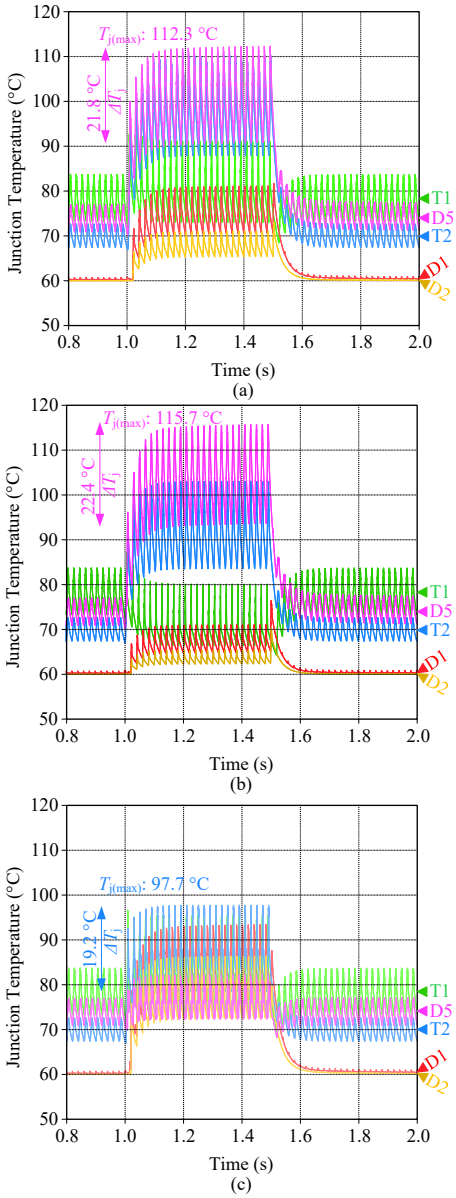


Fig. 4.15: Simulated dynamic of the power devices' junction temperature when a 0.5-p.u. 0.5-s voltage sag occurs: (a) SPWM, (b) SLDPWM [73], and (c) proposed DPWM. Source: **[C6]**.

4.4 Summary

In this chapter, three original methods for enhancing the thermal and reliability performance of the 1500-V PV inverters have been presented. The reliability enhance-

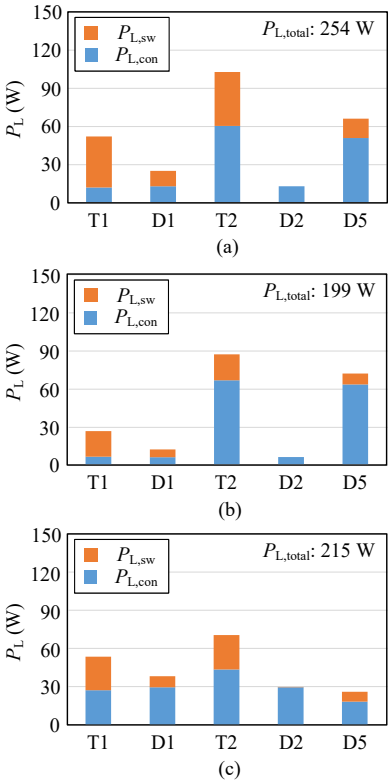


Fig. 4.16: Power loss of each inverter device (referring to Fig. 4.12) during the voltage sag under different modulation strategies: (a) SPWM, (b) SLDPWM, and (c) proposed DPWM ($P_{L,sw}$ – switching loss, $P_{L,con}$ – conduction loss). Source: **[C6]**.

ments have been achieved by reducing the inverter thermal stress through variable gate resistance, junction temperature limit control, and discontinuous modulation, respectively.

1) The possibility for improving the reliability of the SiC-based 1500-V PV inverter through the variable gate resistance design was investigated considering mission profiles. Compared with the fixed gate resistance design for the highest voltage stress, the proposed method, i.e., the variable-resistance gate driver, could change the external gate resistance based on the DC-link voltage variation, minimizing the power loss hence the thermal stress while keeping a safe blocking voltage margin.

2) A reliability enhancement method through junction temperature limit control has also been proposed. The objective of the proposed control is to limit the mean junction temperature of the most stressed power device, thus reducing the temperature variations. By doing so, the PV inverter reliability could be enhanced at the cost of a certain energy loss. The case study results indicate that, compared with the conventional MPPT control, by limiting the mean junction temperature to 90 °C with the proposed control, the lifetime performance of the most stressed power device can

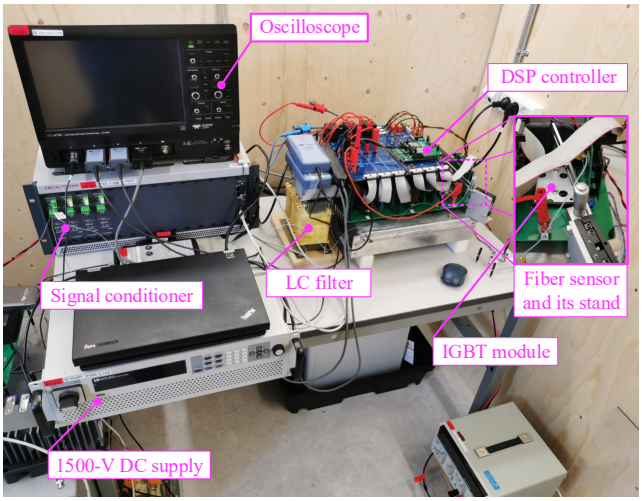


Fig. 4.17: Experimental platform for verifying the proposed DPWM. Source: **[C6]**.

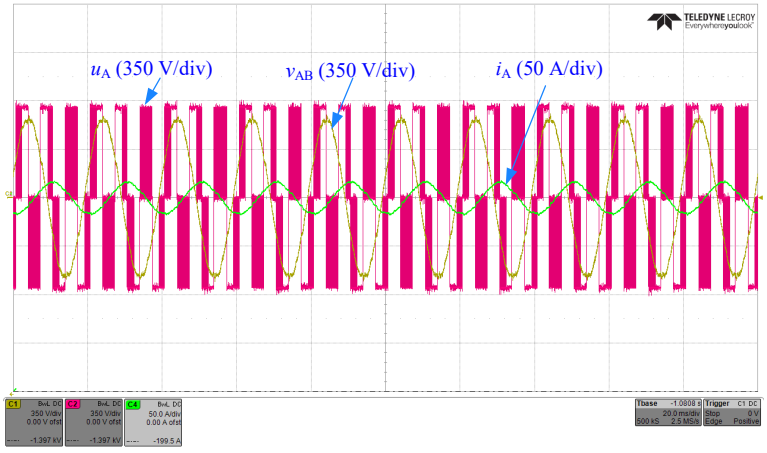
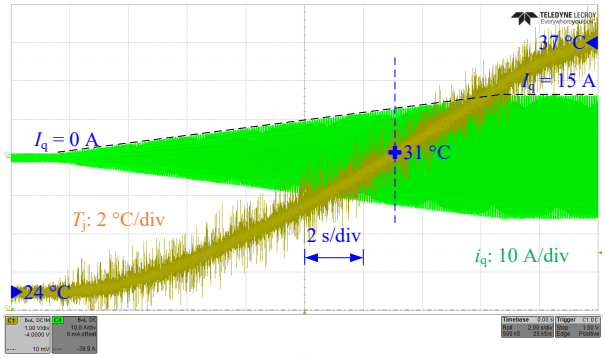


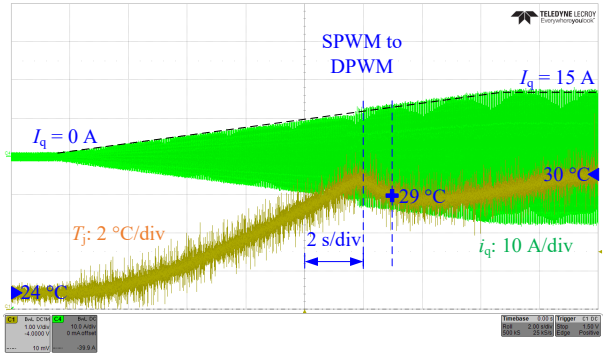
Fig. 4.18: Steady-state output waveforms when injecting reactive currents to the grid with a 1300-V DC link voltage (u_A – phase voltage, i_A – phase current, v_{AB} – line voltage). Source: **[C6]**.

be improved to 1.45 times at the cost of 0.7% reduction of yearly energy yield.

3) In the case of severe unbalanced thermal distribution of the three-level I-type PV inverter during LVRT operation, a DPWM approach has been proposed to redistribute the thermal stresses of the inverter power devices. The basic principle of the proposed modulation strategy is to avoid the neutral-point clamping state during LVRT operation, i.e., each phase of the PV inverter would only clamp to the DC link's positive or negative point when it is carrying the maximum or middle current. By doing so during LVRT operations, the thermal stress of the most stressed components can be reduced since they would not carry the maximum current, achieving an improved thermal balance



(a)



(b)

Fig. 4.19: Junction temperature variations under the reactive current's ramp-up (1 A/second): (a) SPWM only, (b) SPWM first, switching to the proposed DPWM if $I_q > 10$ A. Source: **[C6]**.

among the inverter power devices. The performance of the proposed methods has been validated by simulations and experiments.

Related Publications

J3. **J. He**, A. Sangwongwanich, Y. Yang, K. Zhang, and F. Iannuzzo, "Design for Reliability of SiC-MOSFET-Based 1500-V PV Inverters with Variable Gate Resistance" *IEEE Trans. Ind. Appl.*, awaiting submission, Nov. 2021.

C3. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Design for Reliability of SiC-MOSFET-Based 1500-V PV Inverters with Variable Gate Resistance," in *Proc. IEEE ECCE*, pp. 1850-1855, Oct. 2020.

C4. **J. He**, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Enhanced Reliability of 1500-V Photovoltaic Inverters with Junction Temperature Limit Control," in *Proc. IEEE ECCE-Asia*, 2020, p. 1850-1855, May 2021.

C6. J. He, A. Sangwongwanich, Y. Yang, Z. Quan, Y. Li, and F. Iannuzzo, "Discontinuous Modulation for Improved Thermal Balance of Three-Level 1500-V Photovoltaic Inverters under Low-Voltage Ride-Through," in *Proc. IEEE ECCE*, pp. 1-6, Oct. 2021.

Chapter 5

Conclusions

This chapter summarizes the results and outcomes of the Ph.D. project - *Reliability Enhancement of 1500-V DC-link Photovoltaic Power Converters*. The main contributions are highlighted and the research perspectives are discussed at the end of this chapter.

5.1 Summary

The main research focus of this Ph.D. project is on enhancing the reliability performance of 1500-V PV power converters. The reliability investigation of 1500-V PV inverter topologies has been carried out, and the impact of system parameters on reliability has been discussed. Furthermore, some original methods to enhance the reliability performance of 1500-V PV inverters through design and control have been explored. A brief summary of this Ph.D. thesis is presented below.

In *Chapter 1*, the state-of-the-art for the reliability enhancement of the 1500-V PV power converters has been discussed in three aspects, i.e., 1) topologies to accommodate the 1500-V DC-link voltage, 2) factors affecting reliability, and 3) design and control for improving reliability. Seen from the discussion, it is necessary to carry out a reliability investigation on 1500-V PV power converters, and explore design and control solutions to improve their reliability performance. Accordingly, three research objectives have been outlined: 1) performance comparison of the state-of-the-art PV inverter topologies in terms of reliability considering the 1500-V DC-link operation; 2) investigation of the impact of system parameters on the inverter reliability; 3) development of design and control methods to achieve highly-reliable 1500-V PV power converters.

In *Chapter 2*, the reliability investigation of the 1500-V PV inverters with standard two-level and three-level topologies has been presented. The thermal performance of these inverters was compared under different operating points on the P-V curve of the 1500-V PV arrays. The comparison results indicated that, compared with the two-level topology, the three-level topologies are more suitable for 1500-V PV applications thanks to their reduced thermal stresses. Furthermore, the reliability performance of the three-level inverters has been evaluated considering the impact of mission profiles and switching frequencies. The reliability assessment provides an indication of the

lifetime performance of the three-level 1500-V PV inverters, which is beneficial for the topology selection of the 1500-V PV systems for a given mission profile.

In *Chapter 3*, the performance of the large-scale PV system based on centralized 1500-V string inverter solutions was studied, which is based on the power loss analysis on the main parts of the PV system, i.e., DC wires, PV inverters, AC filters, and transformers, considering various DC- and AC-voltage ratings as well as different mission profile characteristics. In addition, the reliability of 1500-V PV-battery systems was investigated considering two configurations, i.e., DC-coupling and AC-coupling. The impact of different BESS configurations on the reliability of power converters for PV and battery was assessed. By doing so, the selection of BESS configurations for the 1500-V PV system can be justified in terms of reliability.

Finally, in *Chapter 4*, three methods for enhancing the thermal and reliability performance of the 1500-V PV inverters have been presented. Reliability enhancements are achieved by reducing the thermal stresses of the power devices through 1) variable gate resistance, 2) junction temperature limit control, and 3) discontinuous modulation, respectively. The possibility for improving the reliability of the SiC-based 1500-V PV inverter through the variable gate resistance design was investigated considering mission profiles. Compared with the fixed gate resistance design for the highest voltage stress, the proposed method, i.e., the variable gate resistance, could change the external gate resistance according to the DC-link voltage variation, minimizing the power loss hence the thermal stress while keeping a safe blocking voltage margin. A reliability enhancement method through junction temperature limit control has also been proposed. The objective of the proposed control is to limit the mean junction temperature of the most stressed power device, hence reducing the temperature variations. By doing so, the PV inverter reliability can be enhanced at the cost of a certain energy loss. Considering the severe unbalanced thermal distribution of the three-level I-type inverter during LVRT events, a discontinuous modulation strategy has been proposed to redistribute the thermal stresses among the inverter power devices. The principle of the proposed modulation strategy is avoiding the neutral-point clamping state, in such a way not let the clamping diodes carry the maximum current. By doing so during LVRT events, the thermal stress of the clamping diodes can be reduced, achieving an improved thermal distribution among the inverter power devices. The performance of the proposed methods has been validated by simulations and experiments.

5.2 Main Contributions

Based on the research outcomes of this Ph.D. project, the main contributions are summarized as follows:

A) Reliability Investigation of 1500-V PV Inverter Topologies

- The thermal performance analysis and benchmarking of the 1500-V PV inverters with standard two-level and three-level topologies were conducted considering constant power generation, where the three-level topologies are promising candidates for thermal performance enhancement;

- A reliability performance of the 1500-V PV inverters based on the I-type and T-type three-level topologies has been evaluated considering the impact of mission profiles and switching frequencies, where the I-type topology is preferred for improving inverter reliability.

B) Impact of System Parameters on Reliability

- The performance of large-scale 1500-V PV system based on centralized string inverter solutions was evaluated. The impact of system voltage ratings on the power losses of the main parts (i.e., inverters, DC wires, AC filters, and transformers) and yearly energy production of the PV system were analyzed by case studies, where 1500-V PV can contribute to the reduction on wire losses and inverter units;
- The reliability investigation of 1500-V PV-battery system was conducted. The impact of different BESS configurations, i.e., DC-coupling and AC-coupling, on the system reliability was assessed, where the largest impact on system-level reliability is the reliability of the battery converters under both configurations.

C) Methods for Improving Reliability

- A variable gate resistance design for enhancing the reliability performance of the 1500-V PV inverters based on SiC-based two-level topology was proposed, achieving improved reliability performance and safe blocking voltage margin;
- A junction temperature limit control for enhancing the reliability performance of 1500-V PV inverters was proposed, which achieved considerable reliability at the cost of a slightly-reduced energy loss;
- A discontinuous modulation strategy for thermal balance improvement of the three-level 1500-V PV inverters during LVRT was proposed, which yielded improved thermal balance by redistributing the power losses from the most stressed devices to the less stressed ones.

5.3 Research Perspectives

Although this Ph.D. project has brought several outcomes for enhancing the reliability of the 1500-V PV power converters, there are still some scientific challenges that are unresolved and worth to be addressed in the future.

- The optimal design of 1500-V PV systems in terms of reliability has not been discussed. For future research, a systematic design tool, which could provide clear design-for-reliability guidance, is worth to be explored. This one could be beneficial for the design of 1500-V PV systems, e.g., to choose the most suitable topology and system parameters for a given mission profile.
- As for the variable gate resistance design, only its potential to enhance the inverter reliability has been discussed and validated with case study. The resistance design criteria have not been fully discussed. In addition, it is also applicable under other operation modes, e.g., reactive power generation, which is also worth to be explored in future research. Also, variable gate-source voltage

design is another promising solution, and it may be more beneficial to combine these two solutions, i.e., the variable resistance and variable driving voltage, to provide a wider regulating range.

- The estimation of the optimal junction temperature limit reference has not been discussed, which should be addressed in future research with a more comprehensive assessment of system reliability and energy yield.
- Regarding the discontinuous modulation for thermal balance improvement during LVRT, only the thermal redistribution has been discussed. In fact, the improved thermal balance also means a possibility of high reactive current rating for grid recovery support, which is very attractive for LVRT capability and worth to be investigated in the future.

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