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A Distributed-Controlled Harmonic Virtual Impedance Loop for AC Microgrids

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***Abstract*—Proportional harmonic current sharing among inverters is desired in ac microgrid with non-linear loads. Usually, virtual impedance is emulated to achieve good harmonic current sharing at the cost of increased harmonic voltage distortion in the system. Existing schemes overcome this issue by communicating voltage and/or current values among inverters, thereby requiring significant data exchange. Further, some of them suffer from single point of failure because of their centralized architecture. This paper proposes a distributed controller, which emulates harmonic voltage sources in addition to the virtual impedance, thereby reduces voltage distortion in the system. Furthermore, the proposed scheme reduces congestion in the communication network, as compared to the existing communication-based methods, as only two bits per harmonic frequency is communicated among inverters. The effect of virtual impedance on the stability of the system is investigated. Additionally, the impact of communication delay on the current sharing error is studied in this paper. Finally, the proposed technique is validated through simulation and experimentation on a scaled-down laboratory prototype.**

***Index Terms*—AC Microgrid, non-linear loads, proportional current sharing, total harmonic distortion, voltage source inverters.**

NOMENCLATURE

$\tilde{()}$	Small signal perturbation.
θ_i^j	Inverter j^{th} harmonic voltage phase.
λ	Voltage step size.
τ_{12}, τ_{21}	Communication delay between inverter 1 and 2 and vice versa.
$i_i^0(t)$	i^{th} Inverter output current.
$i_i^{0,h}(t)$	Harmonic current of i^{th} inverter.
$i_{load}(t)$	Load current.
$i_b(t)$	Branch current.
$v_i^{ref}(t)$	Inverter voltage reference.
$\Delta v_i^{ref,h}(t)$	Emulated total harmonic voltage reference.
$\Delta v_i^j(t)$	Emulated j^{th} harmonic voltage for i^{th} inverter.
$v_i^h(t)$	Total harmonic voltage reference for i^{th} inverter.
$v_i^{ref,f}(t)$	Fundamental voltage reference.
v_b	Branch voltage.
v_{DC}	DC-link voltage of rectifier.
$v_i^0(t)$	i^{th} inverter output voltage
ED_i^j	Enable decrease bit at j^{th} harmonic frequency of i^{th} inverter.
EI_i^j	Enable increase bit at j^{th} harmonic frequency of i^{th} inverter.
G_1	Conductance of AC linear load.
G_2	Conductance of DC load.
I_1^j, I_2^j	j^{th} harmonic current of inverter-1 and 2.
$INTS_i^j$	Intermittent set bit at j^{th}harmonic of i^{th} inverter.
$INTR_i^j$	Intermittent reset bit at j^{th} harmonic of i^{th} inverter.
L_b	Interconnecting cable inductance.
P, Q	Average real and reactive power
R_{inv}^j	Virtual resistance at j^{th} harmonic frequency.
R_i^j	Reset bit at j^{th} harmonic frequency of i^{th} inverter.
R_b	Interconnecting cable resistance.
S_i^j	Set bit at j^{th} harmonic frequency of i^{th} inverter.
T_s	Voltage updation period.
$\Delta V_{i,rms}^j$	RMS value of emulated j^{th} harmonic voltage for i^{th} inverter.
$V_{limit,h}^j$	Upper limit (RMS value) of j^{th} harmonic voltage.
$V_{limit,l}^j$	Lower limit (RMS value) of j^{th} harmonic voltage

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I. INTRODUCTION

In an islanded ac microgrid, multiple inverters may be used to feed power to the loads [1]. Current sharing among the inverters along with system voltage and frequency regulation are key control objectives in ac microgrid. Droop controllers ($P-\omega$, $Q-V$ or $P-V$, $Q-\omega$ droop) are popularly used to ensure fundamental active and reactive power sharing [2]–[4]. These controllers use the average value of active (P)

and reactive power (Q) and therefore, do not affect harmonic current sharing [5]. Harmonic current supplied by the inverters depends on the value of inverter output impedance and line impedance. Conventionally, virtual impedance/resistance is emulated in inverters [6], [7] to reduce the effect of line impedance mismatch, thereby achieving good harmonic current sharing. However, virtual impedance emulation leads to an increase in output voltage distortion of the inverter. A high value of harmonic voltage distortion may result in additional losses in transformers and distribution line, increase in torque ripple in rotating machines etc.

Several communication-less techniques [8], [9] are discussed to address harmonic voltage distortion problem. In [8] a harmonic current feed-forward technique is proposed. In this work, the harmonic components of the inverter current are used as feed-forward components in the inner current loop of the inverter to reduce the effect of inverter impedance. Thus, with this technique, a good voltage profile at the inverter output is achieved. However, current sharing error between the inverters can persist in case the line impedance mismatch is significant. In [9], a harmonic droop control technique is discussed to achieve the same objective. In this work, a harmonic voltage is emulated from a power-voltage droop controller in individual harmonic frequency, thereby reducing total harmonic distortion (THD) of the inverter output voltage. However, the problem of current sharing error due to the mismatch in the line impedance is not addressed in this work. To achieve both the objective of harmonic current sharing and good voltage profile, an R-C (resistance-capacitance) type virtual impedance emulation technique is discussed in [10]. The virtual resistance is emulated to ensure proportional harmonic current sharing among inverters, and the emulated capacitance cancels out the inductance of the transmission line thus improves the load voltage profile. However, this method is not effective for a low voltage (LV) microgrid, where the interconnecting lines are predominantly resistive. To address this limitation, a negative virtual resistance emulation technique is discussed in [11]. This technique performs satisfactorily in an LV system. In this work, the negative resistance is calculated depending on the available power capacity of inverters. Insertion of negative impedance reduces system stability margin and may lead to instability in case the negative impedance value is greater than the line impedance. Moreover, in [8]–[11], only local measurements are used, which limits the performance of these schemes.

Various communication-based methods are discussed in the literature to reduce voltage harmonic distortion. Among these techniques, [12]–[15] use central microgrid controller. In [12], the load voltage harmonic compensation loop is implemented in the central controller. The technique is realized by communicating the output of the central controller and the load voltage information to the local controllers. In [13], a virtual admittance/impedance is calculated in the central controller depending on the harmonic voltage distortion. This value of virtual admittance is communicated to local inverters through the communication channel. A similar type of control techniques is discussed in [14], [15]. In both of these techniques, harmonic compensation references are generated in the central controller, and they are communicated to the local controllers. The techniques discussed in [12]–[15] are based on a centralized controller which may result in a single point of failure, and also limit the expandability of the system [16]. To alleviate this problem, control schemes without the use of the central controller are discussed in [17], [18]. In [17], [18], inverter output impedance is adjusted by measuring the harmonic component of load side voltage. In these techniques, the load voltage is communicated to individual inverters and are multiplied with gain (G) to generate harmonic voltage references. This results in a reduction of total output impedance (inverter and line) by a factor $(1 + G)$. However, in [17], prior information of line and load parameters are required to design G. Hence, in case of a deviation in line and/or load parameters the current sharing performance of the system may deteriorate due to fixed value of G. In [18], the value of G is adaptively determined depending on the available power rating of inverter and the harmonic distortion of load side voltage. However, with the increase in G, the poles of the system tend to move toward the right half of the s plane. Hence, in case of the high value of G, the system may become unstable. Moreover, [17], [18] are realized by communicating each harmonic components of the load voltage to the individual inverters. Therefore, in case of low bandwidth communication (LBC) or shared communication infrastructure with other services in the area, delays in communicated values may be significant. In such a case the system may continue to operate; however, the harmonic current sharing performance may significantly deteriorate.

To address the aforementioned issues, the technique for reduced harmonic voltage distortion along with accurate harmonic current sharing is proposed in this paper. Following are the key features of the proposed scheme:

- It emulates harmonic voltage sources in addition to the virtual resistance, thereby reducing the voltage harmonic distortion in the system voltage. The proposed scheme utilize distributed control architecture for increased reliability and scalability.
- Communication of only two bits per harmonic frequencies is required. This helps in reducing the congestion in the communication channel and facilitates the use of LBC network.

The concept of emulating harmonic voltage source in inverters to reduce distortion using LBC network is introduced in [19]. The scheme discussed in [19] is capable of good steady-state performance. However, the performance for change in load is not satisfactory. In [19] for a reduction in load, the emulated voltage and algorithm is reset, which leads to significant settling time after each load change. This issue is addressed in this paper modifying the "Harmonic Voltage Emulation" control. Also, a detailed stability analysis is included in this paper, which was not available in [19]. The effect of communication delay on the performance of the proposed scheme is mathematically analysed in this paper. Further, to evaluate the performance of the controller, a laboratory-scale prototype is developed, and results are included in this paper.

The paper is organised as follows: proposed low bandwidth

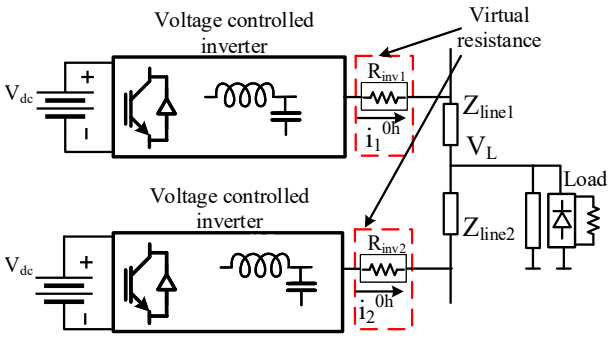

Fig. 1. Two inverter ac microgrid with linear and non linear load.

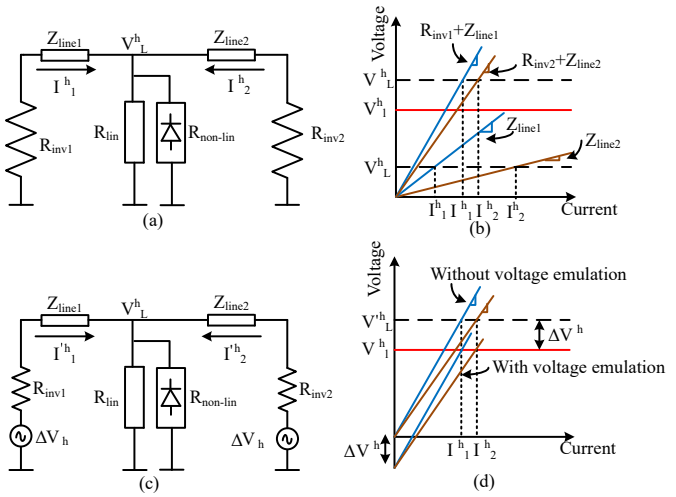

Fig. 2. Harmonic equivalent circuit and characteristics: (a) harmonic equivalent circuit with virtual resistance (b) current vs voltage characteristics with and without virtual resistance (c) harmonic equivalent circuit with emulated harmonic voltage source (d) current vs voltage characteristics with and without emulated voltage source.

communication-based control scheme is presented in section II. Small signal modelling of the system is done in section III to observe the effect of virtual resistance on the stability of the system. Furthermore, the performance of the proposed controller in the presence of communication delay is analysed in this section. In section IV, the scheme is validated through detailed simulation studies. The comparison of the proposed scheme with the existing methods is presented in this section. Also, the efficacy of the proposed scheme is verified by experimentation and results are included in section IV. Finally, section V concludes this paper.

II. Problem Identification and Proposed Solution

A. Problem Due to Impedance Emulation

Fig. 1 shows two inverter microgrid with linear and non-linear loads. Inverters are controlled using conventional droop controllers and operating in ac voltage control mode. Fig. 2(a) shows the harmonic equivalent circuit of the system shown in Fig. 1. The plot of load harmonic voltage versus inverter currents are shown in Fig. 2(b). For a low voltage system with predominantly resistive line, the currents supplied by the two inverters are given by I_1^h and I_2^h, which are inversely proportional to the corresponding line and inverter impedances. To reduce the current sharing error, virtual resistance (R_{inv}) is emulated in each inverter, such that the emulated resistance is much more than the line impedance. Value of the emulated resistance is inversely proportional to the power rating of the inverter. This ensures that the inverters share the harmonic current in proportion to their power rating.

B. Motivation of Harmonic Voltage Emulation

A large value of emulated resistance may lead to increased harmonic voltage distortion in the system. To address this issue, a harmonic voltage source is emulated in each inverter. The harmonic equivalent circuit of the system after the emulation of the harmonic voltage source is shown in Fig. 2(c). In case the magnitude of the emulated voltages of the two inverters are not equal, it would lead to the flow of harmonic current between the inverters. Hence, the instantaneous value of emulated voltage in all the inverters must be equal, to avoid any deterioration in current sharing performance. Fig. 2(d) shows the load harmonic voltage versus inverter currents, with and without emulated harmonic voltage sources. It is observed that the currents drawn from the corresponding inverters are not affected by the inclusion of harmonic sources. Further, the harmonic content in the system voltage is reduced by the amount of emulated harmonic voltage. This principle is used in the proposed scheme to reduce voltage harmonic distortion, without affecting harmonic current sharing performance. Some of the important issues, to be considered while emulating harmonic voltage sources are:

- Harmonic voltage of the same magnitude must be emulated in all the inverters. Considering inverters are placed away from each other, a suitable communication link is required. The rate of data exchange between inverters should be minimized while achieving this objective.
- The value of emulated harmonic voltage depends on the non-linear loads connected in the system. The value should be determined to compensate for the harmonic distortion in the system. In case of under or overcompensation, the load voltage distortion may be higher than the limits. In case of a change in loads, the value of all harmonic voltage sources must be adjusted to avoid over or under-compensation.
- Phase of the emulated voltage must be determined to ensure effective cancellation of harmonic voltage drop produced by line and inverter impedance.

C. Proposed Controller With All-to-All Communication

1) Inverter Voltage Reference: The proposed control scheme, along with the inverter primary controller, is shown in Fig. 3. The inverter primary controller includes power calculation block, droop control, voltage control and current control. The i^{th} inverter reference voltage ($v_i^{ref}(t)$) includes three components, as given below,

$$v_i^{ref}(t) = v_i^{ref,f}(t) - i_i^0(t) \times R_{inv} + \Delta v_i^{ref,h}(t). \quad (1)$$

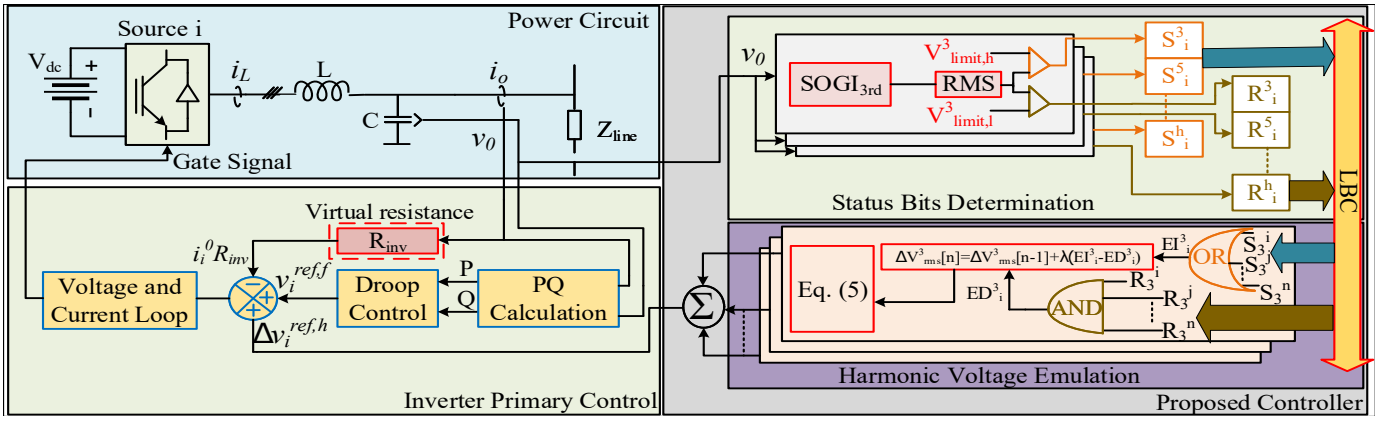

Fig. 3. Block Diagram of the Proposed Controller.

The fundamental reference voltage ($v_i^{ref,f}(t)$) is generated by droop controller using the average value of active (P) and reactive (Q) power. Another component ($i_i^0(t) \times R_{inv}$) is used to emulate virtual resistance (R_{inv}), which improves the harmonic current sharing performance. The third component in inverter reference voltage is the emulated harmonic voltage ($\Delta v_i^{ref,h}(t)$), which is the sum of all the individual harmonic voltage components and is given as,

$$\Delta v_i^{ref,h}(t) = \sum_{j=2}^{j=N} \Delta v_i^j(t). \tag{2}$$

The magnitude of emulated harmonic voltage Δv_i^j is generated using "Status Bit Determination" and "Harmonic Voltage Emulation" blocks.

2) Status Bit Determination: In the "Status Bit Determination" block, shown in Fig. 3, individual harmonic components in the inverter output voltage ($v_i^0(t)$), are extracted using Second Order Generalized Integrators (SOGI). Subsequently, the root-mean-square (RMS) values of these components are determined. Each harmonic voltage is compared with maximum limit value ($V_{limit,h}^j$), and corresponding set bits (S_i^j) are generated. For instance, by comparing the third harmonic voltage with its maximum limit ($V_{limit,h}^3$), the set bit, S_i^3 is generated for the i^{th} inverter. Therefore, the set bit (S_i^j) equals to 1, represents that the j^{th} voltage harmonic of i^{th} inverter is above its allowed value. The reset bits (R_i^j) are generated by comparing the harmonic component with lower limit ($V_{limit,l}^j$). The lower limit is defined to avoid overcompensation of the inverter harmonic voltage. In case the voltage harmonic is within $V_{limit,h}^j$ and $V_{limit,l}^j$, both the bits would be zero. All these bits of an inverter are communicated to other inverters.

3) Harmonic Voltage Emulation: Each inverter receives the set (S) and reset (R) bits of other inverters. These bits are processed to generate Enable Increase (EI_i^j) and Enable Decrease (ED_i^j) bits, as shown in Fig. 3. An OR operation is performed on set bits S_i^j of a specific harmonic, received from all the inverters (for $\forall i \in$[1,n]). For instance, OR operation is performed on S_1^3, S_2^3, ...S_i^3...S_n^3 (representing 3rd harmonic set bits for all the inverters), to generate EI_i^3, for i^{th} inverter. All the other inverters also perform the same operation to generate their EI_i bits. In case, the harmonic voltage of even one of the inverter exceeds its maximum value, the corresponding EI_i^j is set to one in each inverter. This indicates that the emulated harmonic voltage in each inverter must be increased due to jth component. To realize this, the emulated harmonic voltage is determined using,

$$\Delta V_{i,rms}^j[n] = \Delta V_{i,rms}^j[n-1] + \lambda EI_i^j \tag{3}$$

where, $\Delta V_{i,rms}^j[n]$ and $\Delta V_{i,rms}^j[n-1]$ represent the RMS value of j^{th} harmonic voltage of i^{th} inverter at $[n]$ and $[n-1]^{th}$ instant. λ is the step size by which the harmonic voltage is updated after every T_s period.

Above discussion represents the case of harmonic voltage exceeding its higher limit. If the harmonic voltage falls below its lower limit, indicating overcompensation of the harmonic voltage, the following process is followed. To reduce the magnitude of the emulated voltage an AND operation is performed on reset bits (R_i^j) of a specific harmonic component, received from all the inverters, to generate ED_i^j. In case the j^{th} harmonic voltage all the inverter is lower than $V_{limit,l}^j$, the ED_i^j corresponding to the j^{th} harmonic would become one. This indicates that the harmonic voltage Therefore, in this case all inverters reduce the magnitude of emulated harmonic voltage source. This is realized by adding additional term in (3), as below

$$\Delta V_{i,rms}^j[n] = \Delta V_{i,rms}^j[n-1] + \lambda(EI_i^j - ED_i^j). \tag{4}$$

Equation (4) gives the RMS value of individual harmonic components, using which, the instantaneous emulated voltage is determined as,

$$\Delta v_{i,ref}^h(t) = \sqrt{2} \sum_{j=3}^{n} \Delta V_{i,rms}^j sin(\theta_i^j(t)) \tag{5}$$

the phase $\theta_i^j(t)$ is such that the injected harmonic voltage cancels the effect of harmonic voltage drop due to emulated impedance. This is achieved by using a Phase Lock Look (PLL) on ($i_i^0(t) \times R_{inv}$).

D. Proposed Controller With Reduced Communication

The proposed technique discussed in the previous subsection requires all-to-all communication between inverters. This may

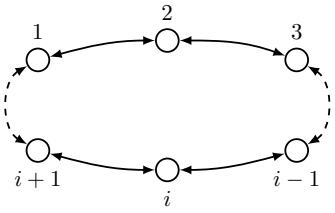

Fig. 4. Reduced Communication Network Topology in a Microgrid

not be suitable for large systems. Therefore, for easy scalability and increased reliability, the aforementioned technique is modified to operate with reduced communication / only neighbor communication. In the modified control technique, the communication link between every inverter is not required. Instead, as shown in Fig. 4 communication link between the neighbor inverters is needed. The "Harmonic Voltage Emulation" block in Fig. 3 is modified and shown in Fig. 5 to obtain the improved control technique. The rest of the control blocks are the same as discussed in the previous subsection.

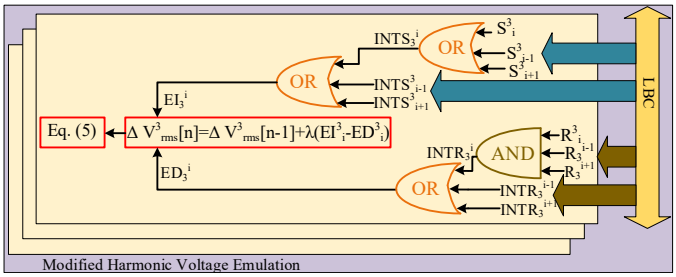

Fig. 5. Proposed Modified Harmonic Voltage Emulation

1) Modified Harmonic Voltage Emulation: As shown in Fig. 5, in the modified control technique, four bits per harmonic frequency are communicated between neighbor inverters. Each inverter receives the set (S), reset (R), intermittent set ($INTS$), and intermittent reset ($INTR$) bits from the neighbor inverters only. As shown in Fig. 5, an OR operation is performed on the set bits (S_i^j) of a specific harmonic frequency, received from the neighbor inverters to generate intermittent set bit ($INTS_i^j$) for i^{th} inverter at j^{th} harmonic frequency. The Enable Increase bit (EI_i^j) is generated from an OR operation performed on the $INTS_i^j$ received from the inverters in the neighborhood. For instance, OR operation is performed on S_{i-1}^3, S_i^3 and S_{i+1}^3 to generate $INTS_i^3$ for i^{th} inverter at 3^{rd} harmonic frequency. A further OR operation on $INTS_{i-1}^3$, $INTS_i^3$ and $INTS_{i+1}^3$ generate EI_i^3 for i^{th} inverter. Depending on the states of EI_i^j, the emulated voltage magnitude is determined based on (3).

Similarly, AND operation is performed on the reset bits (R_i^j) of the neighborhood inverters to generate intermittent reset bit ($INTR_i^j$) for i^{th} inverter at j^{th} harmonic frequency. Enable Decrease (ED_i^j) bit is generated by performing OR operation on the $INTR_i^j$. Therefore, depending on the states of ED_i^j and EI_i^j, the emulated voltage is updated as (4).

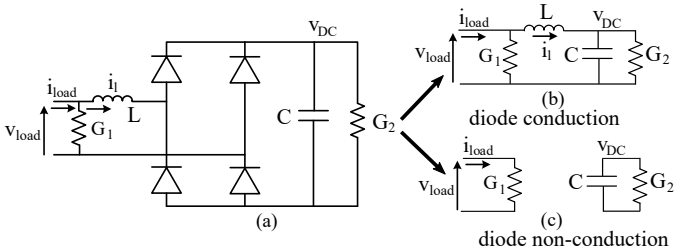

Fig. 6. Load circuit diagram: (a) Linear and non linear load used for modelling, (b) Equivalent circuit of load when diodes are conducting, (c) Equivalent circuit of load when diodes are not conducting.

III. Mathematical Analysis

This section includes system modelling, stability analysis and effect of communication delay on the performance of the proposed controller. Small signal linearised models of various components of the system including non-linear load, inverter output characteristics and interconnecting cables are derived in the following sub-sections. Based on the model, the necessary condition for stability in the presence of virtual resistance is derived in the subsequent discussion. Further, the effect of communication delay on the steady-state performance of the system is also discussed in this section.

A. Modelling

1) Inverter Output Characteristics: The reference voltage depends on the output of the droop controller, the value of virtual resistance and the emulated harmonic voltages. Considering the fast response of inner voltage and current controllers, the output voltage of the inverter is therefore assumed to be equal to the reference harmonic voltage. For any source i, $v_{i,inv}^h$ is written as,

$$v_i^h(t) = \Delta v_{i,ref}^h(t) - R_{inv} i_i^{0,h}(t). \tag{6}$$

Combining harmonic voltage references of all the inverters in matrix form, and linearising gives,

$$\tilde{\mathbf{v}} = \mathbf{\Delta \tilde{v}_{ref}} - \mathbf{R_{inv}} \tilde{\mathbf{i}}^{\mathbf{0}} \tag{7}$$

where, $\tilde{()}$ represents small signal perturbation around equilibrium point, $\tilde{\mathbf{v}}$, $\mathbf{\Delta \tilde{v}_{ref}}$ and $\tilde{\mathbf{i}}^{\mathbf{0}}$ are the column vectors of inverter output voltage, emulated harmonic voltage and inverter current respectively and $\mathbf{R_{inv}}$ is the diagonal matrix consist of virtual resistances.

2) Modelling of Non-Linear Load: The single phase non-linear load is shown in Fig. 6. It also shows the equivalent circuits, for diode conduction and non-conduction mode. The equations representing the load during diode conduction period is given by,

$$\left.\begin{aligned} \mathbf{L}\frac{\mathbf{d}}{\mathbf{dt}}\tilde{\mathbf{i}}_\mathbf{l} &= (\tilde{\mathbf{v}}_\mathbf{load} - \tilde{\mathbf{v}}_\mathbf{DC}) \\ \mathbf{C}\frac{\mathbf{d}}{\mathbf{dt}}\tilde{\mathbf{v}}_\mathbf{DC} &= \tilde{\mathbf{i}}_\mathbf{l} - \mathbf{G_2}\tilde{\mathbf{v}}_\mathbf{DC} - \tilde{\mathbf{g}}_\mathbf{2}\mathbf{v}_\mathbf{DC} \\ \tilde{\mathbf{v}}_\mathbf{load} &= \mathbf{G_1^{-1}}(\tilde{\mathbf{i}}_\mathbf{load} - \tilde{\mathbf{i}}_\mathbf{l} - \tilde{\mathbf{g}}_\mathbf{1}\mathbf{v}_\mathbf{load}) \end{aligned}\right\} \tag{8}$$

During the diode non-conduction period $\tilde{\mathbf{i}}_\mathbf{l}$ becomes zero. Therefore, the load equation in this duration is written as,

$$\left.\begin{aligned} \mathbf{C}\frac{\mathbf{d}}{\mathbf{dt}}\tilde{\mathbf{v}}_\mathbf{DC} &= -\mathbf{G_2}\tilde{\mathbf{v}}_\mathbf{DC} - \tilde{\mathbf{g}}_\mathbf{2}\mathbf{v}_\mathbf{DC} \\ \tilde{\mathbf{v}}_\mathbf{load} &= \mathbf{G_1^{-1}}(\tilde{\mathbf{i}}_\mathbf{load} - \tilde{\mathbf{g}}_\mathbf{1}\mathbf{v}_\mathbf{load}) \end{aligned}\right\} \tag{9}$$

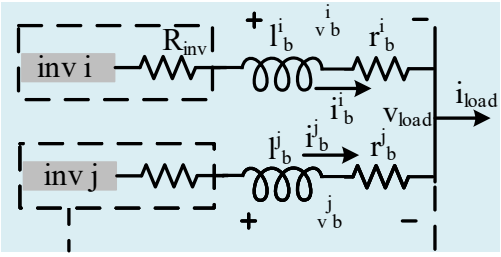

Fig. 7. Power cable network.

3) Combined System: The interconnecting cable network is shown in Fig. 7. The equations for interconnecting cables is given by,

$$\left.\begin{aligned} \tilde{\mathbf{v}}_\mathbf{b} &= \mathbf{M}\tilde{\mathbf{v}} - \mathbf{P}\tilde{\mathbf{v}}_\mathbf{load} \\ \tilde{\mathbf{v}}_\mathbf{b} &= \mathbf{L_b}\frac{\tilde{\mathbf{i}}_\mathbf{b}}{\mathbf{dt}} + \mathbf{r_b}\tilde{\mathbf{i}}_\mathbf{b} \end{aligned}\right\} \tag{10}$$

where, $\mathbf{M}$ is the incidence matrices for sources, connected to the load buses. The dimension of the matrix is $m \times n$, where m is the number of branches/cables and n is the number of source nodes and $\mathbf{P}$ is a matrix whose dimension is $m \times r$, where r is the number of load nodes. r_b and l_b are power cable resistance and inductance.

Kirchoff's Current Law (KCL) at each node gives,

$$\tilde{\mathbf{i}}_\mathbf{load} = \mathbf{P^T}\tilde{\mathbf{i}}_\mathbf{b} \tag{11}$$

Equations (7)–(11), represent small signal linearised models of different components of the system. Out of these, only load and interconnecting cables have differential equations. Hence, $\tilde{\mathbf{i}}_\mathbf{b}$, $\tilde{\mathbf{i}}_\mathbf{l}$ and $\tilde{\mathbf{v}}_\mathbf{DC}$ are chosen to be states of the system. Combining (7)–(11) give the state space linearised model,

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{\mathbf{u}} \tag{12}$$

where,

$$\begin{aligned} \tilde{\mathbf{x}} &= \begin{bmatrix}\tilde{\mathbf{i}}_\mathbf{b} & \tilde{\mathbf{i}}_\mathbf{l} & \tilde{\mathbf{v}}_\mathbf{DC}\end{bmatrix}^\top \\ \tilde{\mathbf{u}} &= \begin{bmatrix}\tilde{\mathbf{g}}_\mathbf{1}\mathbf{v} & \tilde{\mathbf{g}}_\mathbf{2}\mathbf{v}_\mathbf{DC}\end{bmatrix}^\top \\ \mathbf{A}|_\mathbf{cond} &= \begin{bmatrix} \mathbf{a_{11}} & \mathbf{L_b^{-1}}(\mathbf{G_1^{-1}}\mathbf{P}) & \mathbf{0} \\ (-\mathbf{L^{-1}}\mathbf{G_1^{-1}}\mathbf{P^T}) & (-\mathbf{L^{-1}}\mathbf{G_1^{-1}}) & -\mathbf{L^{-1}} \\ \mathbf{0} & \mathbf{C^{-1}} & -\mathbf{G_2}\mathbf{C^{-1}} \end{bmatrix} \end{aligned} \tag{13}$$

where, $\mathbf{a_{11}}$=$-\mathbf{L_b^{-1}}(\mathbf{R_{inv}} + \mathbf{r_b} + \mathbf{P}\mathbf{G_1^{-1}}\mathbf{P}^\top)$. This is the case when the diodes of the non linear load conduct and for this case the state matrix $\mathbf{A}$ is denoted as $\mathbf{A}|_\mathbf{cond}$. When the diodes of the non linear load do not conduct then $\mathbf{i_l}$ becomes zero and the state matrix $\mathbf{A}$ is denoted by $\mathbf{A_{non-cond}}$ for this duration. Therefore, for the non-conduction period of the diodes the states and the state matrix are given as,

$$\begin{aligned} \tilde{\mathbf{x}} &= \begin{bmatrix}\tilde{\mathbf{i}}_\mathbf{b} & \tilde{\mathbf{v}}_\mathbf{DC}\end{bmatrix}^\top \\ \tilde{\mathbf{u}} &= \begin{bmatrix}\tilde{\mathbf{g}}_\mathbf{1}\mathbf{v} & \tilde{\mathbf{g}}_\mathbf{2}\mathbf{v}_\mathbf{DC}\end{bmatrix}^\top \\ \mathbf{A}|_\mathbf{non-cond} &= \begin{bmatrix} \mathbf{a_{11}} & \mathbf{0} \\ \mathbf{0} & -\mathbf{G_2}\mathbf{C^{-1}} \end{bmatrix} \end{aligned} \tag{14}$$

The state matrices in (13) and (14) for diode conduction and non-conduction period are used in the subsequent sections for stability analysis.

B. Stability Analysis

To analyse the stability of the aforementioned model, state matrices $\mathbf{A}|_\mathbf{cond}$ and $\mathbf{A}|_\mathbf{non-cond}$ are considered, as the eigenvalues of the system are determined from state matrices. In this work, multiple inverter and single load configuration is assumed. Hence, in this case, $\mathbf{P}$ is a column matrix with the dimension of $n \times 1$ and $\mathbf{M}$ is a identity matrix of size n.

- For diodes conduction period:
  For this duration, the state matrix $\mathbf{A_{cond}}$ is given in (13). To find the eigenvalues of the matrix $\mathbf{A}|_\mathbf{cond}$, the row echelon form of the $[s\mathbf{I} - \mathbf{A}|_\mathbf{cond}]$ is found, where, s is the eigenvalues of state matrix. From the row echelon form, the characteristic equation is found as,

$$s^{n+2} + A_{n+1}s^{n+1} + A_n s^n + \cdots + A_1 s + A_0 = 0. \tag{15}$$

  The coefficients A_{n+1} to A_0 are given as,

$$\begin{aligned} A_{n+1} &= \sum_{i=1}^{{}^{n+2}C_1} D_1^i, A_n = \sum_{i=1}^{{}^{n+2}C_2} D_2^i, \\ A_{n-1} &= \sum_{i=1}^{{}^{n+2}C_3} D_3^i, \cdots, A_0 = D_{n+2} \end{aligned} \tag{16}$$

  where, $D_1, D_2, D_3, \cdots, D_n$ are the principal minors with one rows, two rows, three rows $\cdots$ complete $\mathbf{A}|_\mathbf{cond}$ matrix, respectively. For any practical system, the line inductance l_b is much lesser than the load inductance L, load capacitance C is greater than L and load conductance G_1 and G_2 are almost equal to or lesser than 1 for high or low power system respectively. With these assumptions, from (16), the relations between A_0, A_1, $\cdots$, A_{n+1} is found as,

$$A_0 > A_1 > A_2 \cdots > A_n > A_{n+1}. \tag{17}$$

  Now, the necessary condition for stability is determined by applying Routh-Hurwitz criteria on (14) and is given by,

$$A_0 > 0; A_1 > 0; \cdots; A_{n+1} > 0 \tag{18}$$

  From the inequality given (17) it is clear that all the other coefficients would be positive if A_{n+1} is positive. Therefore,

$$\begin{aligned} \frac{1}{l_{b1}}(r_{b1} + r_{inv} + \frac{1}{G_1}) + \frac{1}{l_{b2}}(r_{b2} + r_{inv} + \frac{1}{G_1}) \\ + \cdots + \frac{1}{l_{bn}}(r_{bn} + r_{inv} + \frac{1}{G_1}) > 0 \end{aligned} \tag{19}$$

For $l_{b1} = l_{b2} = \cdots = l_{bn} = l_b$ and $r_{b1} = r_{b2} = \cdots = r_{bn} = r_b$, (19) is written as,

$$r_{inv} > -(r_b + \frac{1}{G_1}) \tag{20}$$

- For diodes non-conduction period:
  For this duration, the state matrix $\mathbf{A}|_{\mathbf{non-cond}}$ is given in (14). Same steps as previous is followed here to find the necessary condition for the stability of matrix $\mathbf{A}|_{\mathbf{non-cond}}$. Following the exact same method, the necessary condition for stability in this duration is found to be,

$$r_{inv} > -(r_b + \frac{1}{G_1}) \tag{21}$$

From the condition derived in (20) and (21), it is clear that a significantly large value of negative virtual resistance would result in instability of the system. The condition derived in (20) and (21) is validated for the system under consideration for simulation in section (IV.5).

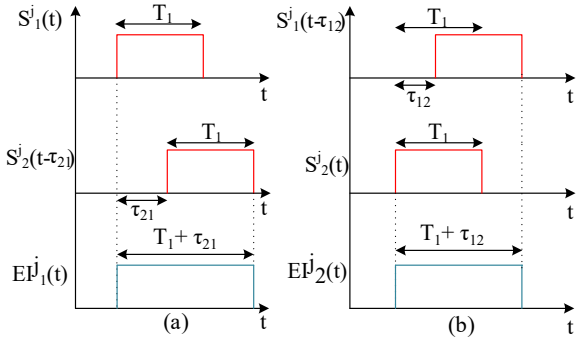

Fig. 8. Effect of equal communication delay on voltage set bit generation for (a) inverter i, (b) inverter j.

C. Effect of communication delay

The proposed scheme uses communication for determining the value of emulated voltages in various inverters. In the case of communication delay, there may be differences in the values of emulated voltages, which would lead to the flow of circulating current. This would deteriorate the current sharing performance. To analyse the effect of communication delay on the steady state performance, the system shown in Fig. 1 is considered.

Consider the time delay of τ_{12} and τ_{21} between data send from inverter-1 to that received by the inverter-2 and vice-versa. Fig. 8 shows the operation in the presence of communication delay. If the j^{th} harmonic voltage at both the inverters exceed their maximum allowed value, set bits S_1^j and S_2^j are generated by inverter-1 and 2 for a duration of T_1 as shown in Fig. 8. Inverter-1 receives S_1^j instantaneously and S_2^j after a delay of τ_{21}. Therefore, EI_1^j (for inverter-1) is set for a duration of $T_1 + \tau_{21}$. In this duration, the RMS value of emulated voltage gets updated $(T_1 + \tau_{21})/T_s$ times, as per (4). Therefore, the RMS values of emulated voltage at end of this duration is,

$$\Delta V_1^j = \frac{\lambda(T_1 + \tau_{21})}{T_s}. \tag{22}$$

TABLE I
SYSTEM SPECIFICATIONS

Parameter	Value
Rating of the Inverters	$S1 = S2$ = 250 kVA
DC link Voltage	$V_{DC1} = V_{DC2}$ = 1000 V
Filter Inductance	$L_{f1} = L_{f2}$ = 0.08 mH
Filter Capacitance	$C_{f1} = C_{f2}$ = 50 μF
Line Impedance 1	$r_{b1} = 5m\Omega$ and $l_{b1} = 3.2\mu H$
Line Impedance 2	$r_{b2} = 2.5m\Omega$ and $l_{b2} = 1.6\mu H$
Nominal ac Voltage	$V_n = 230V_{rms}$
Nominal frequency	$f_o = 50Hz$
Switching Frequency	$f_s = 10kHz$
Rectifier Load	$G_2 = 1.25\mho, C = 250mF$, $L = 0.01mH$
Linear Load	$G_1 = 1\mho$
Droop Parameters	$m = 1.616 \times 10^{-5} rad/s - W$, $n = 8.97 \times 10^{-4} rad/s - VAr$
Emulated Voltage Updating Interval (T_s)	20 ms

Similarly, EI_2^j (for inverter-2) is set for $T + \tau_{12}$ duration, which gives

$$\Delta V_2^j = \frac{\lambda(T_1 + \tau_{12})}{T_s}. \tag{23}$$

Since both the emulated voltages are in the same phase (as discussed in Section II-C-3), the difference in the phase voltages is written using (22) and (23), as

$$\begin{aligned}\Delta\overline{V_1^j} - \Delta\overline{V_2^j} &= \frac{\lambda(T_1 + \tau_{21})}{T_s}\angle\delta_j - \frac{\lambda(T_1 + \tau_{12})}{T_s}\angle\delta_j \\ &= \frac{\lambda(\tau_{21} - \tau_{12})}{T_s}\angle\delta_j.\end{aligned} \tag{24}$$

Applying Kirchoff's voltage and current law on Fig. 2 (c) gives,

$$\overline{I'^j}_1 + \overline{I'^j}_2 = \overline{I^j}_{load} \tag{25}$$

and

$$\Delta\overline{V^j}_1 - \Delta\overline{V^j}_2 = \overline{I'^j}_1(R_{inv} + Z_{line1}) - \overline{I_2'^j}(R_{inv} + Z_{line2}) \tag{26}$$

From (26), the difference in current sharing is found to be,

$$\begin{aligned}\overline{I'^j}_1 - \overline{I'^j}_2 =& \frac{2(\Delta\overline{V^j}_1 - \Delta\overline{V^j}_2)}{Z_{line1} + Z_{line2} + 2R_{inv}} \\ &+ \overline{I^j}_{load}\frac{Z_{line2} - Z_{line1}}{Z_{line1} + Z_{line2} + 2R_{inv}}.\end{aligned} \tag{27}$$

Taking the absolute value of current sharing error from (27) and substituting the expression of $\Delta\overline{V^j}_1 - \Delta\overline{V^j}_2$ from (26),

$$\begin{aligned}\frac{|\overline{I'^j}_1 - \overline{I'^j}|}{I^j_{load}} =& \frac{\lambda|(\tau_{21} - \tau_{12})|/T_s}{I^j_{load}|Z_{line1} + Z_{line2} + 2R_{inv}|} \\ &+ \frac{|Z_{line2} - Z_{line1}|}{|Z_{line1} + Z_{line2} + 2R_{inv}|}.\end{aligned} \tag{28}$$

The first term in (28), shows the effect of communication delay on current sharing error and the second term shows the effect of line impedance mismatch. The current sharing error increases with the increase in difference between τ_{21} and τ_{12}. In case of equal communication delay between the inverters, the first term in (28) becomes zero.

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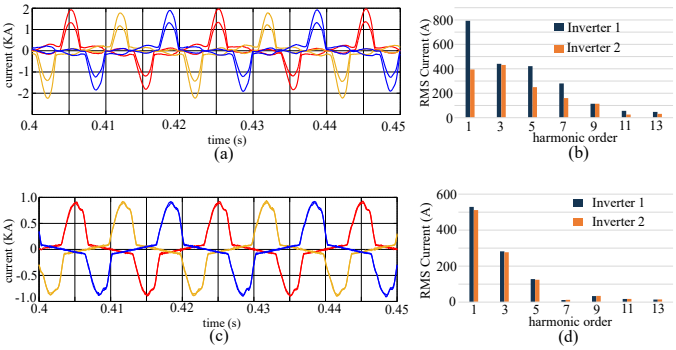


Fig. 9. Simulation result for two inverters connected to a linear and non-linear load: (a) Inverter currents without emulation of virtual impedance (1kA/div), (b) Harmonic spectrum of inverter currents without virtual resistance (c) Inverter currents with emulation of virtual impedance (1kA/div), (d) Harmonic spectrum of inverter currents. Traces (i) R-phase current (red), (ii) Y-phase current (yellow), (iii) B-phase current (blue). X axis:0.01s/div.

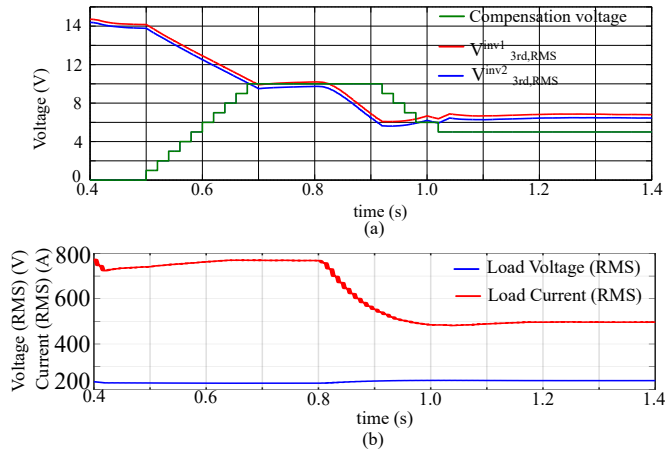


Fig. 10. Simulation results load switching: (a) RMS value of emulated harmonic voltage and inverter output voltage (4V/div) for 3^{rd} harmonic component after load switching. Trace: RMS value of emulated 3^{rd} harmonic compensation voltage (green), rms value of 3^{rd} harmonic component of inverter-1 voltage(red), rms value of 3^{rd} harmonic component of inverter-1 voltage(blue), (b) RMS value of load current and load voltage, Trace: RMS value of load voltage (blue) (200V/div), RMS value of load current (200A/div)(red), X axis: 0.2s/div.

IV. Results

A. Simulation

A detailed simulation study is performed in the MATLAB/Simulink platform to validate the proposed scheme. The system consists of two 3-ϕ 4-wire inverters connected to linear and non-linear loads, as shown in Fig. 1. Table I shows the specifications of the complete system. Each inverter includes inner voltage and current controllers, as shown in Fig. 3.

1) Fundamental Droop Controller: In this case, the inverter is controlled only with fundamental droop control, without virtual resistance and proposed scheme. Fig. 9 (a) shows inverter output currents. It is observed from Fig. 9 (b) that the total current sharing error is 22.19 % and in such a case the THD values of the output voltages of the inverters are 5.53 % and 5.29 % respectively.

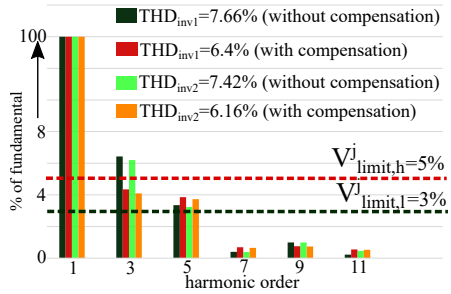


Fig. 11. Harmonic spectrum of output voltage of inverters. Traces: Inverter 1 voltage THD without harmonic voltage compensation (dark green), Inverter 1 voltage THD with harmonic voltage compensation (red), Inverter 2 voltage THD without harmonic voltage compensation (light green) and Inverter 2 voltage THD with harmonic voltage compensation (orange).

TABLE II
Comparison With Existing Techniques

Techniques	Load kVA	% Error in current sharing with 10% estimation error and communication delay		
		0 ms	20 ms	100 ms
[11]	10	20 %	-	-
	100	x	-	-
	500	x	-	-
[17]	10	10 %	12 %	20 %
	100	14.5 %	20 %	30 %
	500	30 %	40 %	56 %
Proposed	10	5 %	9.5 %	15 %
	100	8.2 %	16 %	22 %
	500	13.5 %	25 %	32 %

x=unstable

2) Virtual Resistance: A virtual resistance of value 0.06 Ω is emulated in the individual inverter to restrict the current sharing error less than 10%. The inverter output current waveforms after the emulation of virtual resistance are shown in Fig. 9 (c). It is observed from Fig. 9 (d) that the total current sharing error is reduced to 2.5% after implementation of virtual resistance. In this case, the THD values of the inverter output voltages are 7.66 % and 7.42 % as shown in Fig. 11.

3) Proposed Scheme: To reduce the THD, harmonic voltage is emulated in both the inverters. For demonstrating the operation of the scheme, the RMS value of the 3^{rd} harmonic emulated voltage and 3^{rd} harmonic component of the inverter output voltages are shown in Fig. 10. The voltage emulation starts at 0.5 s. It is seen that with the increase in the emulated 3^{rd} harmonic voltage, the 3^{rd} harmonic component of the output voltage reduces and finally settles at 10 V at 0.7 s. The harmonic spectrum of the inverter output voltages are shown in Fig. 11. It is noted from Fig. 11 that only the third harmonic voltage component is more than $V^3_{limit,h}$, which is set at 5% of the fundamental voltage. Hence, only the third harmonic voltage is emulated to reduce the harmonic distortion. Third harmonic voltage reduces to 4.2 % and 4.1 % in inverter 1 and 2 respectively, after the emulation of third harmonic voltage as shown in Fig. 11. This reduced value of the 3^{rd} harmonic voltage distortion stays within the range as

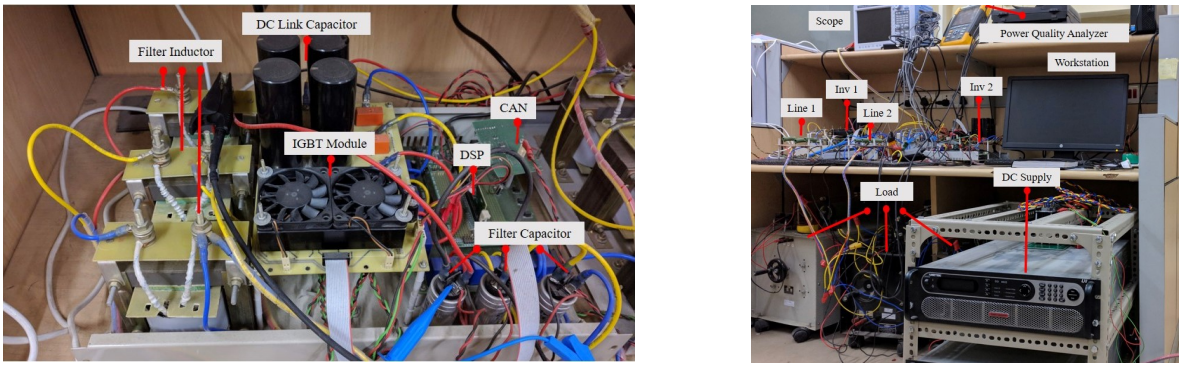


Fig. 12. Developed laboratory prototype of : (a) Single inverter, (b) Two inverter AC microgrid system.

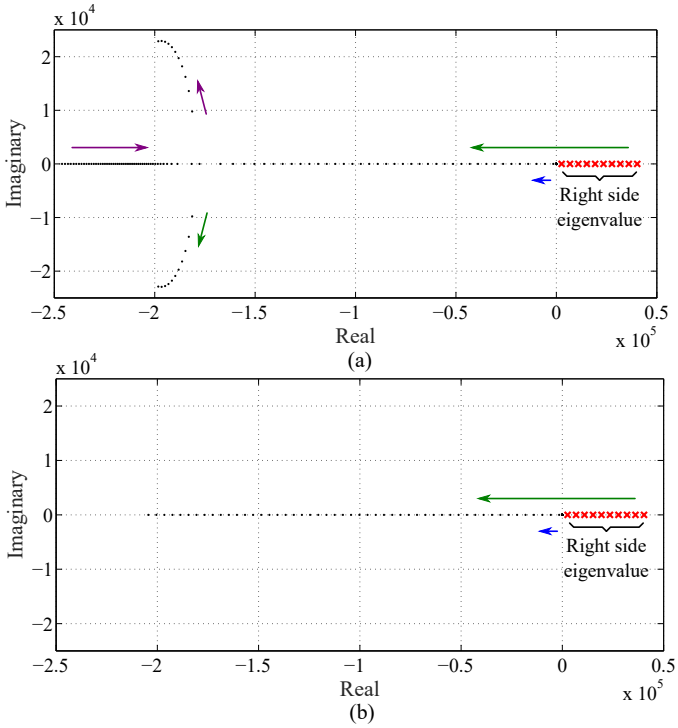


Fig. 13. Locus of eigenvalues for (a) $\mathbf{A}|_{\mathbf{cond}}$, (b) $\mathbf{A}|_{\mathbf{non-cond}}$ for R_{inv} varying from $-0.1\ \Omega$ to $0.5\ \Omega$ in steps of $0.01\ \Omega$.

defined in [20]. However, because of inter harmonics coupling in non-linear load, fifth and seventh harmonic components of the voltage increase slightly after the emulation of third harmonic compensation voltage (which is still below the 5% of the fundamental voltage [21]).

4) Effect of Load Switching: In order to investigate the efficacy of the proposed scheme, the non-linear load resistance R_{dc} is increased from 0.8 Ω to 1.6 Ω at 0.8 s. As a result, the harmonic current drawn by the load reduces, and subsequently, the harmonic distortion in inverter voltages also reduces which is shown in Fig. 10. It is observed from Fig. 10 (a) that the 3^{rd} harmonic component of the inverter voltages reach below $V^3_{limit,l}$ (3% of the fundamental voltage) at 0.92 s. Hence, as per the proposed scheme, the emulated voltage starts to decrease from 0.92 s in the step of 1 V until the RMS voltages finally settle at 1.02 s. In Fig. 10 (b) the RMS value of load voltage and load current are shown.

TABLE III
SPECIFICATIONS FOR EXPERIMENTAL PROTOTYPE

Parameter	Value
Rating of the Inverters	$S1 = S2$ = 800 VA
DC link Voltage	$V_{DC1} = V_{DC2}$ = 270 V
Filter Inductance	$L_{f1} = L_{f2}$ = 3.5 mH
Filter Capacitance	$C_{f1} = C_{f2}$ = 10 μF
Switching Frequency	$f_s = 10kHz$
Line Impedance 1	r_{b1} = 0.25Ω, l_{b1}=120 μH
Line Impedance 2	r_{b2} = 0.5Ω, l_{b2}=230 μH
Rectifier Load	G_2 =0.1 ℧, $L = 500\mu H$, C=1 mF
Linear Load	G_1 = 0.04℧
Nominal frequency	$f_o = 50Hz$

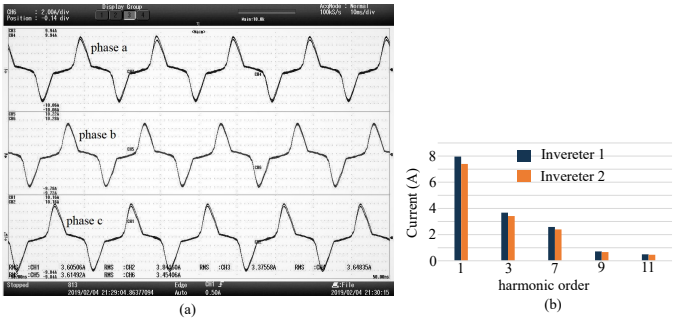
5) Stability Analysis: The stability of the system under consideration is checked using Routh-Hurwitz criteria. The Routh-Hurwitz table for the diode conduction period is given by,

$$\begin{array}{c|ccc} s^4 & 1 & 2.19\times10^{11} & 3.5577\times10^{16} \\ s^3 & 1.09\times10^{6} & 5.0163\times10^{11} & \\ s^2 & 2.142\times10^{11} & 0 & \\ s^1 & 5.0611\times10^{15} & & \\ s^0 & 3.577\times10^{16} & & \end{array} \tag{29}$$

For the diode non-conduction period, as $\tilde{i_l}$ is not present, the characteristic equation of the system is one order less compared to diode conduction period. Therefore the Routh-Hurwitz table for this duration is given as,

$$\begin{array}{c|cc} s^3 & 1 & 2.57\times10^{10} \\ s^2 & 9.968\times10^{5} & 1.2874\times10^{11} \\ s^1 & 2.57\times10^{10} & 0 \\ s^0 & 1.2847\times10^{11} & \end{array} \tag{30}$$

From (29) and (30) all the first elements in every rows of the Routh's table is positive thus ensuring the stability of the system. The effect of R_{inv} on the location of the eigenvalues is shown Fig. 13 (a) and (b) for diode conduction and non-conduction period respectively. Two inverter based microgrid system has four eigenvalues in the diode conduction period. One of the pole is located far negative than the other poles and thus it is not shown in 13 (a). For the same reason two



(a) (b)

Fig. 14. Experimental results for (a) three phase current supplied by inverter-1 and 2 in the presence of virtual resistance, (2A/div) (b) harmonic spectrum of current supplied by the two inverters.

out of three eigenvalues of the system is shown in 13 (b) for diode non-conduction period. It is observed for both the diode conduction and non-conduction period, the system becomes unstable for $\mathrm{R_{inv}}$ equal to -0.0038Ω and the eigenvalues shift to the negative half of the s plane with the increasing value of R_{inv}.

It should be noted that the current $\mathrm{i_l}$ is zero just before and after the diode conduction period and remains zero for the diode non-conduction period for a half cycle of $\mathrm{v_{load}}$. In both the diode conduction and non-conduction periods the dc link voltage $\mathrm{v_{DC}}$ cannot be more than the peak value of $\mathrm{v_{load}}$. Furthermore, it is shown that the system is stable for both the periods, which guarantees the stability of the system.

6) Comparison With Existing Techniques: The proposed control technique is compared with the techniques discussed in [11] and [17] for two cases as,

- *For a 10 % error in the estimation of line parameters*: The current sharing performance of the three techniques for three different load kVA are compared for a case of 10% error in the estimation of line parameters. As shown in Table II, the proposed scheme offers less current sharing compared to the techniques [11] and [17]. It is also observed from Table II, for higher load kVA rating, the scheme discussed in [11] the system becomes unstable.
- *For a delay in the communication channel with the 10 % error in the estimation of line parameters*: The proposed scheme is compared with the technique in [17] in the presence of communication delay of 20 ms and 100 ms. 10% error in the estimation of line parameters is also considered in this case. A communication rate of 200 samples/s is taken for the proposed scheme and [17]. It is evident from Table II that the current sharing error is less with the proposed scheme in case of delay in communication channel compared to the scheme in [17]. It is observed that the % current sharing error increase with the increase in the load kVA rating for both the techniques.

B. Experimental Results

To validate the proposed technique, a scaled-down hardware prototype of the 3-ϕ 4-wire microgrid system of Fig. 1 is developed. Each of the inverters is realized using IGBT module FNA22512A, and a signal attenuation board. Texas Instruments made TMS320F28335 Delfino controllers are used in each of the inverters to implement the control loops. Controller area network (CAN) is used for communication between the two inverters. Fig. 12 shows the developed prototype, and its parameters are given in Table III.

1) Virtual Resistance: A virtual resistance of value 2 Ω is emulated in each of the inverters to restrict the current sharing error within 5% of the load current. The current shared by the inverters after the emulation of virtual impedance is shown in Fig. 14. It is seen from the figure that the current sharing error is 3.77 %. However, due to emulation of virtual impedance, THD values of inverter- 1 and 2 voltages are 10.3% and 9.9%, respectively. Harmonic spectrum is shown in Fig. 15 (a) and (c). It is observed from in Fig. 15 (a) and (c), that the 3^{rd} harmonic component of the inverter voltage is primarily contributing to the THD of the inverter voltage. The 3^{rd} harmonic voltage distortion due to emulation of virtual resistance is 9.1% and 9% in inverter-1 and 2 respectively, which is higher than that of the limit in [20].

2) Proposed Scheme: To reduce the 3^{rd} harmonic voltage component within $V^3_{limit,h}$ (5% of the fundamental voltage) the proposed scheme for voltage emulation is activated at 50 s. Due to the emulation of 3^{rd} harmonic voltage both in inverter-1 and 2, the 3^{rd} harmonic voltage distortion is reduced to 2% and 2.2% in inverter-1 and 2 respectively. Therefore, the THD values of inverter-1 and 2 voltages are also reduced to 6 % and 5.3 % respectively, as shown in Fig. 15 (b) and (d).

3) Effect of Communication Delay: The communication delay is emulated in the communication channel between inverters. The bits, to be delayed are stored in an array and are accessed in the first-in-first-out basis.

- *Equal communication delay between inverter-1 and 2*: The current sharing performance of the proposed scheme is shown in Fig. 16 (orange curve) for an equal communication delay (τ) between inverter-1 and 2. It is seen from the figure that in the presence of equal communication delay, the current sharing error is restricted to 4 %. It is seen from the graph that with the proposed scheme, current sharing performance does not get affected if the equal value of communication delay exists between inverter-1 and 2.
- *Unequal communication delay between inverter-1 and 2*: Unequal communication delay of value τ_{12} and τ_{21} is emulated in the communication link between inverter-1 to 2 and vice versa. To observe the effect of unequal communication delay, τ_{21} is set to 0 and τ_{12} is varied. The current sharing performance is highly dependent on the difference between τ_{12} and τ_{21}. The trend of current sharing error and THD of inverter output voltage with $\tau_{12}-\tau_{21}$ is shown in Fig. 16 (blue curve). As shown in the figure, the current sharing error increases with increase in the value of $\tau_{12}-\tau_{21}$, which is in close agreement with the mathematical model derived in section IIIC. Furthermore, with a larger value of τ_{12}, the duration of voltage emulation in inverter-2 increases. Hence, the THD of the output voltage of inverter-2 reduces with the

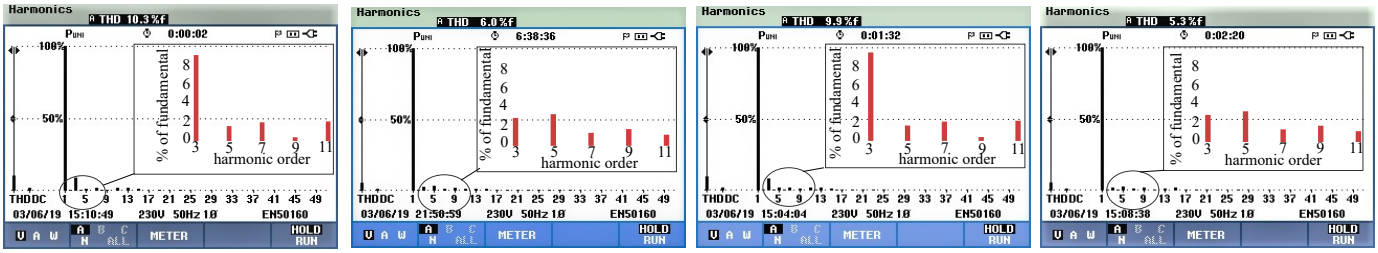


Fig. 15. Harmonic spectrum of output voltage Inverter-1 and 2. (a) Inverter-1 without harmonic voltage emulation and, (b) Inverter-1 with harmonic voltage emulation, (c) Inverter-2 without harmonic voltage and, (d) Inverter-2 with harmonic voltage emulation.

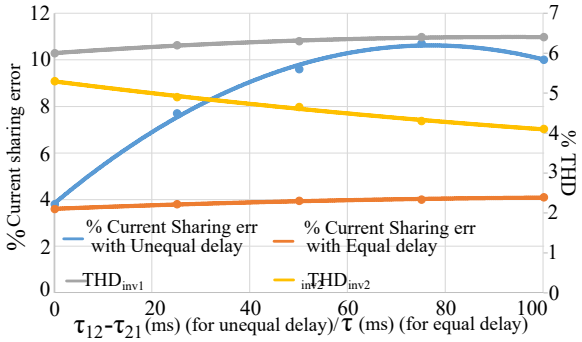


Fig. 16. Trend of current sharing performance and voltage THD in the presence of communication delay. Traces: current sharing error in case of unequal communication delay between the inverters (blue), current sharing error in case of equal communication delay between the inverters (orange), THD of inverter 1 output voltage in case of unequal communication delay (grey), THD of inverter 2 output voltage in case of unequal communication delay (yellow).

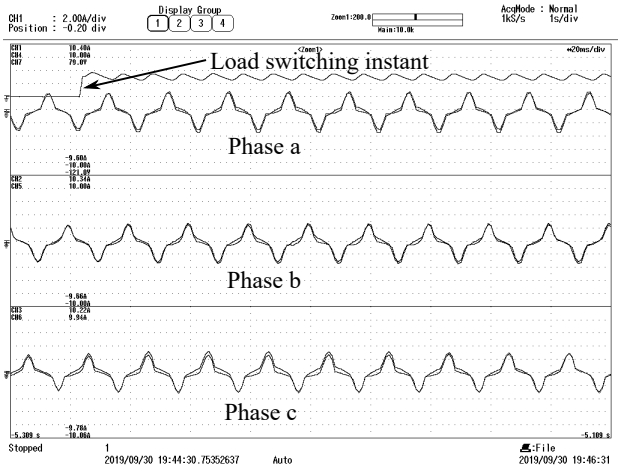


Fig. 17. Experimental result for the proposed method with load switching, current (2 A/div), Voltage (50V/div).

increase in the value of τ_{12}, whereas the THD of inv1 is almost constant which is observed in Fig. 15 (yellow and grey curves).

4) Effect of Load Switching: In order to investigate the performance of the proposed technique during load switching, the dc load R_{DC} is switched from 33 Ω to 20 Ω. The current sharing performance of the proposed technique during load switching is shown in Fig. 17. It is observed that, for R_{DC}=33

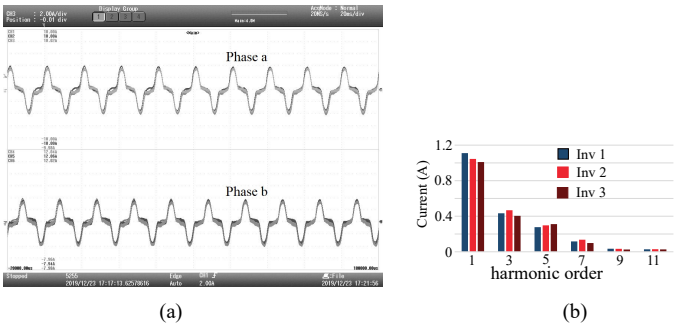


Fig. 18. Experimental results for (a) current supplied by inverter-1, 2 and 3 in the presence of virtual resistance, (2A/div), (b) harmonic spectrum of current supplied by the three inverters.

Ω, the THD of the output voltages of inverter-1 and 2 are 7 % and 6.2 % with all the voltage harmonic components less than $V^{j}_{limit,h}$ (5 % of fundamental). In case of reduced value of R_{DC} (20 Ω), it is observed that without the harmonic voltage emulation the THD of the output voltages of inverter-1 and 2 becomes 8.3% and 7.9% respectively out of which the 3^{rd} harmonic voltage distortion is 6% and 5.8 % in inverter-1 and 2 respectively. After the emulation of the 3^{rd} harmonic voltage, the 3^{rd} harmonic voltage distortion reduce to 3.4% and 3.6%, thus the THD of the output of voltages of inverter-1 and 2 also reduce to 6.5% and 5.8% respectively. It is further observed from Fig. 17 that the current sharing error between the two inverters remains within 10% in case of load switching.

5) With Reduced Communication: To validate the proposed modified control technique with reduced communication, a scaled-down laboratory prototype of a 3-ϕ 4-wire microgrid system with three inverters is developed. A virtual impedance of value 2 Ω is emulated in individual inverters for ensuring current sharing error among the inverters is not more than 5 %. The inverter output currents after the emulation of virtual resistance is shown in Fig. 18. As shown in Fig. 19, the THD of the output voltages become 8 %, 8.3 %, and 7.5 % in inverter 1, 2, and 3, respectively. It is observed that the 3^{rd} harmonic component of the inverter voltage is primarily contributing to the THD of the harmonic voltage.

To reduce the 3^{rd} harmonic component of the voltage, 3^{rd} harmonic compensation voltage is emulated at 50 s. No direct communication between inverter 1 and 3 is implemented. Only neighbors (1,2) and (2,3) have communication among themselves. Due to the emulation of 3^{rd} harmonic compensation

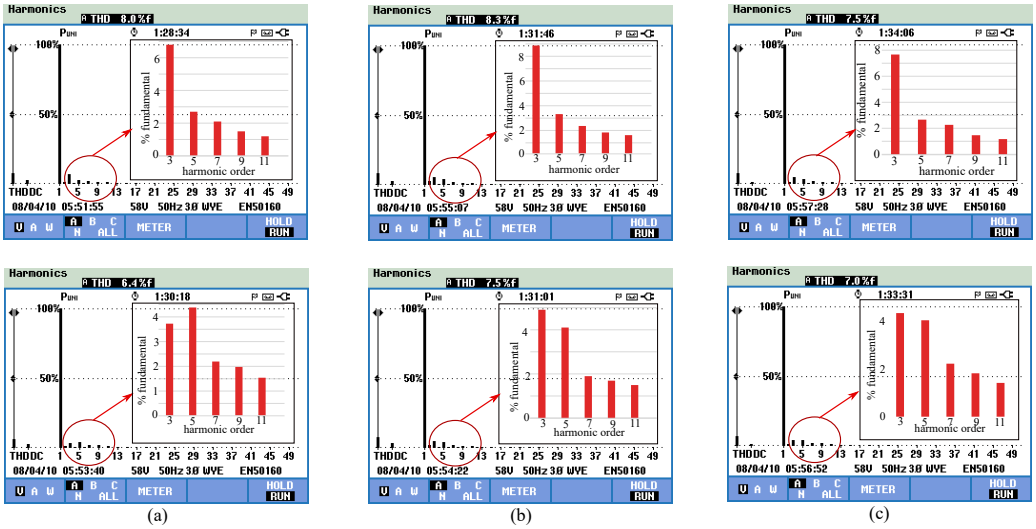


Fig. 19. Harmonic spectrum of output voltage of Inverter-1, 2 and 3 with reduced communication. (a) Inverter-1 without harmonic voltage emulation (top), with harmonic voltage emulation (bottom), (b) Inverter-2 without harmonic voltage emulation (top), with harmonic voltage emulation (bottom) and (c) Inverter-3 without harmonic voltage emulation (top), with harmonic voltage emulation (bottom)

voltage, the 3 rd harmonic voltage distortion reduces to 3.4 %, 4.9 % and 4.3 % in inverter 1, 2 and 3 respectively. Therefore, the THD if inverter-1, 2, and 3 also reduce to 6.4 %, 7.5 %, and 7 % respectively, as shown in Fig. 19 (a), (b) and (c) respectively.

V. Conclusion

The proposed scheme achieves the objective of proportional harmonic current sharing and lower harmonic voltage distortion at the output of the inverters. The control technique is distributed in nature, thus ensures increased reliability. Furthermore, communication of two bits per harmonic frequencies reduces data congestion in the communication channel. A mathematical analysis is carried out to find the condition on virtual resistance for the stable operation of the system. Furthermore, the effect of communication delay steady state current sharing error is explored in this paper. A detailed simulation study is carried out for two inverters and remote load system. A scaled-down laboratory prototype is developed to validate the proposed technique. It is observed from experimentation that voltage harmonic distortion is reduced to 6.3 % from 9.8 %, thereby meeting the IEEE 519 standard. Furthermore, the effect of equal and unequal communication delay in the communication channel between the inverters is experimentally verified in this paper. The experimental results are in close agreement with the mathematically obtained solutions.

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