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On Converter Fault Tolerance in MMC-HVDC Systems: A Comprehensive Survey

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***Abstract*—Since they were first proposed, modular multilevel converters have been strongly studied in literature. Due to their high component count, some concerns regarding their reliability arise, and several fault-tolerance schemes have been proposed in recent years. This paper presents a comprehensive survey on the converter fault-tolerance strategies for MMC-HVDC systems based on the available technical literature. Some MMC-HVDC solutions adopted in industry are reviewed. This work proposes analytical expressions to determine the maximum number of submodule failures in the MMC-HVDC system. Thereafter, the limitations of the main converter fault-tolerance schemes under submodule failures are described and critically compared. A case study is conducted based on 1000 MVA Xiamen MMC-HVDC project with $\pm$ 320 kV dc-link voltage, aiming to evaluate the effect of the faulty submodules on the reliability and power losses of the converter. Finally, the remaining challenges and opportunities in the converter fault tolerance in MMC-HVDC systems are stated as well as the future directions of this field.**

***Index Terms*—Submodule failures, converter fault-tolerance schemes, high-voltage direct current, modular multilevel converter, reliability.**

I. Introduction

MODULAR multilevel converter (MMC) is a breakthrough solution which brought the advantages of the cascaded multilevel converters to the dc/ac conversion systems [1]. Since its introduction by Professor Marquardt, in 2001 [2], the interest in MMC and its application has increased considerably. Many research centers and companies have developed submodule topologies, control algorithms and modulation strategies for MMCs [3], [4]. The wide adoption of MMCs in the high-voltage direct current (HVDC) industry is mainly due to their modularity, scalability and inherent fault tolerance. The novelty in comparison with the early cascaded multilevel topologies is the presence of dc-link, which is very attractive for HVDC systems.

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Siemens was the first manufacturer which employed MMC for HVDC transmission in the Trans Bay Cable link, in 2010. Thenceforward, modular multilevel converters have been implemented in many commercial projects (e.g., Nemo link, Nan'ao three-terminal project, Zhoushan five-terminal project, etc) [5]. Nowadays, all leading companies in HVDC market offer solutions based on MMC.

Usually, MMC-HVDC systems employ hundreds to thousands of submodules. Due to the high number of components, concerns regarding reliability arise. MMC-HVDC systems are usually subjected to high availability requirements. In practice, the HVDC system must operate from one to three years without interruption to replace damaged submodules. During the planned maintenance period, the damaged submodules are replaced. In view of this fact, the converter must be designed considering some redundancy strategy [6]. However, this approach increases the MMC total cost.

MMC fault-tolerance schemes have been investigated in many publications in recent years. For example, the search "fault tolerance in modular multilevel converter" in IEEE Xplore database leads to more than 100 results. The MMC fault tolerance is based on 3 steps. The first step is the fault detection and localization of the damaged submodule. The second step is the fault isolation, which is usually based on a bypass structure included in the converter submodule. The third step is the postfault control scheme.

Debnath et al. provide a general overview of the basics of the MMC operation as well as its control challenges in [3]. A review on aspects of converter technologies, control strategies and network topologies for MMC-based multi-terminal HVDC systems is presented in [7]. Dekka et al. present the development of MMC circuit topologies and the future trends of MMC applications in [4]. The evolution and technical challenges of the main control methods are also discussed. However, these works do not present details of the MMC fault-tolerance schemes. A review on the most relevant fault diagnosis methods and fault-tolerance strategies of MMC-HVDC systems is presented in [8]. Nonetheless, the effect of the faulty submodule on the MMC reliability for different redundant techniques is missing.

Therefore, this work contributes to the field by providing a comprehensive survey on the main proposed converter fault-tolerance schemes for MMC-HVDC based on the available technical literature. The main contributions in MMC fault tolerance are described and critically compared. Some MMC-HVDC solutions adopted by industry are reviewed.

Finally, the effect of the faulty submodules on the reliability and power losses of the converter is evaluated, considering a real MMC-HVDC project.

II. MMC-HVDC SYSTEMS

A. System Configurations

There are some possible configurations for MMC-HVDC systems [9], [10]. A symmetrical monopole is shown in Fig. 1(a), which features two poles with opposite voltage potential. Moreover, both poles need to be fully insulated. Figs. 1(b) and (c) present the asymmetrical monopole configuration. This configuration requires only one high-voltage conductor. The dc current can return through a metallic conductor which is usually grounded at a single end, as shown in Fig. 1(b). This return conductor requires low-voltage insulation compared to the high-voltage conductor. When the dc current returns through the ground, the cost of the metallic return is eliminated and the dc circuit is grounded in two separate places [10], as shown in Fig. 1(c). However, the drawbacks of this solution include corrosion on the metallic pipes in the ground and potential negative environmental effects [11].

The most common bipolar configuration consists of two independently controlled asymmetrical monopoles, where the dc current returns through a metallic return path or through the ground, as observed in Figs. 1(d) and (e). An exception is the rigid bipole configuration, which does not present a dedicated metallic return path [12]. In the bipolar configurations, the loss of any converter leads to a reduction of 50 % in transmission capacity, which ensures higher availability than monopolar configurations [12]. However, dc-line-to-ground short circuits lead to total loss of power transfer in rigid bipole configuration. Moreover, the bipolar MMC-HVDC system is more expensive for the same power rating compared to monopolar configurations [10].

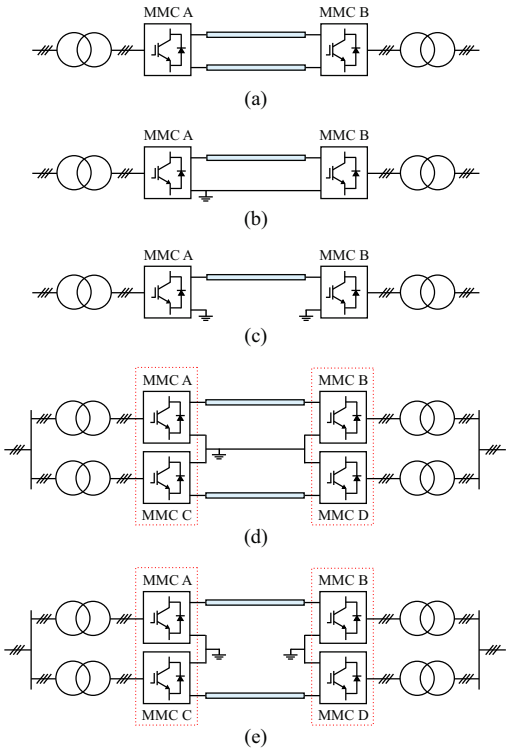

Fig. 1. Configurations of MMC-HVDC transmission systems. (a) Symmetrical monopole. (b) Asymmetrical monopole with metallic return. (c) Asymmetrical monopole with ground return. (d) Bipolar with metallic return. (e) Bipolar with ground return.

The MMCs are commercialized in the form of standard or customized products for high-power applications. According to the configurations shown in Fig. 1, some MMC-HVDC technologies are commercially available under different trade names [10], [13]–[15]. Standard solutions are commercially available for dc-link voltages until $\pm$ 525 kV. In addition, at least one $\pm$ 800 kV MMC-HVDC system is under construction in China [16]. The list of some commercially MMC-HVDC technologies are summarized in Tab. I.

B. MMC Topology

The three-phase MMC is shown in Fig. 2. This topology presents a common dc-link and can be applied to HVDC transmission systems, electric drives and renewable energy conversion systems. The impedance L_g refers to the transformer leakage inductance. The six MMC arms are composed of an inductor L_a, N non-redundant submodules per arm and N_R redundant submodules. Therefore, the total number of submodules per arm is $N + N_R$.

The MMC was originally proposed with both half-bridge and full-bridge submodules. The half-bridge submodule topology reduces converter energy losses and cost. For MMC-HVDC applications, the dc-link short circuit becomes a difficult problem because antiparallel diodes of half-bridge submodules conduct as rectifier bridges, even if the IGBTs are blocked [17]. In this case, the full-bridge submodule topology can be applied, which ensures the dc-link short circuit handling capability. Moreover, this submodule topology can synthesize negative voltage, which can bring some advantages, as mentioned in [4]. However, the great energy losses in normal operation by using twice the number of semiconductors represent a drawback of this submodule structure [18]. Alternatively, some submodule topologies and hybrid MMC have been proposed as possible solutions [3], [19].

Due to its simplicity and cost savings, the half-bridge submodule is commonly applied in commercial MMC solutions. In this case, a bypass structure is usually connected in parallel with each submodule. This structure has two functions: i) protecting the antiparallel diode during the dc-link short circuit and ii) bypassing the submodules in case of submodule failures. The bypass structure is described in details in the next section.

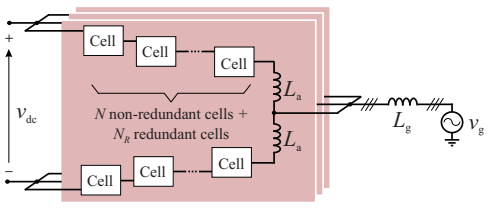

Fig. 2. Schematic of the three-phase MMC-HVDC.

TABLE I
COMMERCIALLY AVAILABLE MMC-HVDC TECHNOLOGIES.

Manufacturer	Product Name	submodule Structure	Semiconductor Technology	Bypass Structure
Siemens	HVDC PLUS	half-bridge/full-bridge	Plastic IGBT Module (PIM)	Fig. 3(a) and (c)
GE/Alstom	HVDC MaxSine	half-bridge/full-bridge	Plastic IGBT Module (PIM)	Fig. 3(a) and (c)
ABB	HVDC Light	half-bridge	Press-pack IGBT (PPI)/IGCT	Fig. 3(d) and (e)
C-EPRI	HVDC Flexible	half-bridge	Press-pack IGBT (PPI)	Fig. 3(e)
RXPE	-	half-bridge	Press-pack IGBT (PPI)	Fig. 3(b)

C. Semiconductor Technology and Bypass

The bypass structure included in the converter submodule is useful to implement the redundancy strategy. Some approaches adopted in industry are presented in Fig. 3. The bypass realization is strongly dependent on the semiconductor technology employed.

When plastic IGBT modules (PIM) are employed, the bypass structure is usually based on a press-pack thyristor connected in parallel with a vacuum contactor, as illustrated in Fig. 3(a). The thyristor provides a fast bypass (turn-on time of few microseconds), compared with the vacuum contactor (turn-on time of tens of milliseconds), which is required during dc-link short circuit [20]. Moreover, the faulty submodules must stay bypassed until the next scheduled maintenance. This bypass structure is adopted in half-bridge submodule realizations by some manufacturers, such as Siemens, GE and Alstom [21]–[23].

If a dc-link short circuit happens, the diodes of PIM devices cannot handle the surge currents. This fact arises from the construction of standard PIM devices, which include the diodes inside the power module. Indeed, PIM devices are mainly designed for motor drive applications, where the current stresses in the diodes are not severe [24]. Therefore, the thyristor is fired to take over the surge currents and protect the diodes during a dc-link short circuit. It is important to remark that the selected thyristor is a high-voltage device, which must present a current rating compatible with the surge currents and forward voltage drop much lower than the diodes [25]. In addition, the selected thyristor must withstand high dv/dt even during normal operation [26].

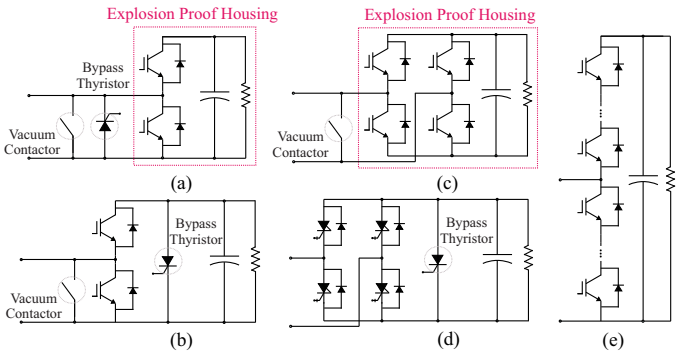

Fig. 3. Different bypass structure realizations for: (a) PIM-based half-bridge submodules; (b) PPI-based half-bridge submodules; (c) PIM-based full-bridge submodules; (d) IGCT-based full-bridge submodules; (e) PPI-based half-bridge submodules without bypass structure.

Moreover, the bypass structure plays an important role during IGBT failures. PIM presents both open circuit failure mode (OCFM) and short circuit failure mode (SCFM). During OCFM, the submodule capacitor voltage cannot be controlled and the monitoring unit must bypass the submodule due to undervoltage or overvoltage [27]. However, SCFM leads to a short circuit in the submodule capacitor. The surge currents can be as high as 500 kA [24]. Although surge-limiting inductors can be present, the current is still high enough to cause the explosion of the device [24]. In addition, this solution leads to an increase in the commutation inductance, which is a drawback. Therefore, when PIM devices are employed, a commonly adopted solution employs an explosion proof housing for the submodules [28]. Under such conditions, the bypass structure is activated to guarantee the submodule current continuity. The vacuum contactor assumes the arm current, since the thyristor cannot handle ac currents. Moreover, the contactor can handle the rated current without any cooling. Siemens, GE and Alstom also presented solutions based on full-bridge submodule topology [21]–[23], as shown in Fig. 3(c). In this case, a thyristor is not required, since the full-bridge topology ensures the dc-link short circuit handling capability. Therefore, only the vacuum contactor is employed in the bypass structure of full-bridge submodules.

When press-pack IGBT (PPI) devices are used, different bypass structures can be employed, as shown in Fig. 3(b) and (d). The use of discrete devices allows selecting diodes that can handle the surge currents during dc-link short circuits. Therefore, no bypass structure is necessary to protect the diodes. Moreover, PPI devices have inherent stable short circuit failure mode [29]. In this case, a thyristor is connected in parallel with the submodule capacitance. If a failure occurs, the thyristor is fired to assume the capacitor discharge current. Thereafter, the thyristor fails in short circuit and the submodule is bypassed due to the conduction of the submodule diodes, as shown in Fig. 3(d) [29]. This approach was proposed by ABB for IGCT-based submodules and its main drawback is the power losses in the diodes of the faulty submodule. RXPE has proposed the use of an additional bypass vacuum contactor, as shown in Figs. 3(b), to solve this issue [25].

Finally, ABB and C-EPRI also employ half-bridge submodules without any bypass structure, as shown in Fig. 3(e) [15], [30]. Series-connected PPI devices are employed in the submodule to avoid the problem of surge currents during SCFM. When one device fails, the other IGBTs handle the submodule capacitor voltage. Additional devices are included to provide redundancy [31]. Therefore, the redundancy is

implemented in device level, instead of submodule level.

Table I summarizes the semiconductor technology employed in the submodules of some commercially available MMC-based products. The use of IGCTs is still limited, since only two companies produce this component (ABB and Mitsubishi). As noted, since the PIM technology is mature and widespread in the industry, many manufacturers adopt this technology.

Regarding the submodule power supply scheme, the most popular approach is to take the power from the submodule capacitor [6]. When the submodule is bypassed, the submodule bleeder resistors are expected to discharge the capacitor. Under such conditions, some scheme must be employed to ensure the operation of the bypass structure. One possible approach is based on irreversible mechanical switch, which ensures the submodule current continuity even when the submodule capacitor discharges [20].

III. Faults in Modular Multilevel Converters

In MMC-HVDC applications, a large number of power semiconductor devices are used and each of these devices may be considered as a potential failure point [32]. Failures in power semiconductor devices cause the MMC to operate displaced from the setting point or even to shut down the converter [33]. Particularly, in the HVDC applications, under no circumstances should it be allowed to shut down the MMC excepting during scheduled maintenance [34]. Therefore, the converter fault tolerance is necessary. It is based on three steps: i) identification of the existence and location of the faulty submodule; ii) bypassing of the faulty submodule; iii) compensation of the faulty component by a redundant one, or reconfiguration of the MMC control.

A. Fault Diagnosis

A submodule can experience faults in different components, such as IGBT modules, capacitors, control system or power supply. In this case, the faulty submodule must be detected and then isolated by the bypass structure, as shown in Fig. 3. The fault detection approaches found in the literature can be divided into two main groups:

1) Hardware-based Methods: employ redundant components or additional sensors. A failure can be detected if the behavior of the components is different from the redundant ones, or the additional sensors detect anomalous signals [33]. Some fault detection methods with an additional sensor for each IGBT device or each half-bridge submodule are presented in [35].

The hardware-based methods require additional sensors and signals, which increases the cost and the implementation complexity for MMC-HVDC, due to the high numbers of submodules. Therefore, the fault detection methods based on the existing measured variables in the original controllers are becoming a trend [18], [33]. In this view, the application of analytical methods is increased by the great advances in computational technology in recent decades [33].

2) Analytical Methods: these methods check the consistency between the actual system behavior and its estimated behavior [36]. Some authors propose solutions based on existing voltage and/or current measurements. A fault detection method for multilevel converter based on voltage switching frequency analysis is presented in [37]. A fault locating based on state-observer-based fault detection and capacitor voltage comparison are introduced in [36], [38]. A fault diagnosis method using artificial intelligence-based techniques is presented in [39]. Fault detection based on the sliding mode observer are proposed in [40], [41]. The Kalman filter is adopted to detect open-circuit faults and the faulty submodule is then located by comparing the capacitor voltages in the same arm in [42].

Although the analytical methods are more sophisticated, the cost and hardware complexity are smaller than those required by the hardware-based methods.

B. Converter Fault-Tolerance Schemes

The objective of the converter fault-tolerance control system is to overcome the presence of faulty submodule and restoring the stability of the power converter with acceptable performance level [43]. In general, there are two bypass schemes for the MMC under submodule failure conditions [44]. In this first solution, the faulty submodules are bypassed as well as an equal number of submodules in other MMC arms, to keep the MMC symmetrical operation. The second approach is carried out bypassing only the faulty submodules and then the MMC operates in asymmetric state. A notable advantage of the asymmetric operation is the use of all healthy submodules in the MMC operation. However, this approach results in asymmetry in the synthesized voltage of the faulty phase. In this case, some MMC fault-tolerance method must be employed:

1) Adaptive Reference Voltage: The main adaptive reference voltage approaches can be divided into: capacitor voltage increasing (CVI) [43], [45] and zero-sequence voltage injection (ZSVI) [46]–[50].

a) Capacitor Voltage Increasing: the CVI method is one of the most straightforward MMC fault-tolerance methods. This approach is based on the voltage increase of one or more healthy submodules in the faulty arm to compensate the missed voltage capacity [43], [45]. The number of levels at the converter voltage output is reduced while the overmodulation is avoided [51]. Since MMC-HVDC systems has been built with hundreds or thousands of submodules, reducing the output voltage levels would be an economic solution. Nevertheless, in practical applications, the safe operating area of the submodules is generally 50-60 % of the semiconductors blocking voltages [52]. Therefore, the CVI is limited by the maximum voltage stresses at the semiconductor devices and submodule capacitors.

b) Zero-Sequence Voltage Injection: among all methods injecting zero-sequence voltage to balance output voltages, the third-order harmonic voltage injection (THVI) and the neutral-shift (NS) methods deserve to be highlighted. The THVI is an attractive approach for MMC control, due to

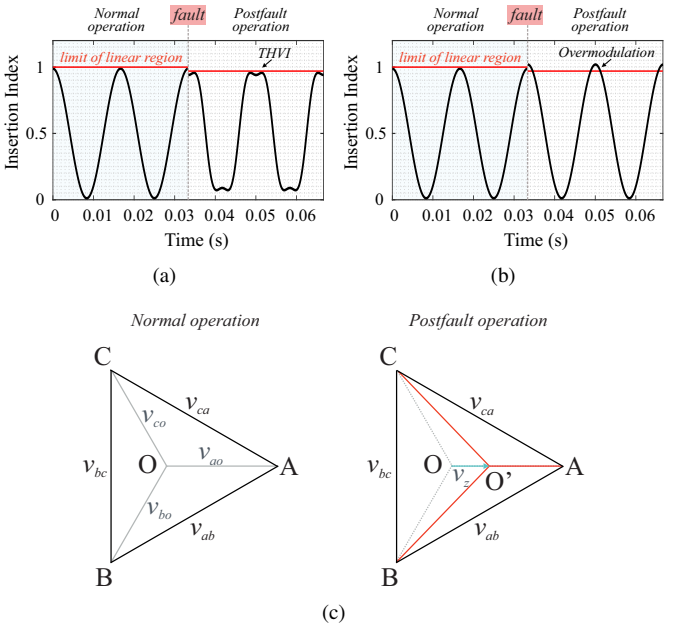

Fig. 4. Operating principle of fault-tolerance methods: (a) THVI; (b) Overmodulation; (c) Neutral-shift.

the high dc-link voltage utilization ratio [46]. However, the THVI approach can only be considered a MMC fault-tolerance scheme if the converter is initially designed to operate with sinusoidal PWM modulation. Additionally, the challenge is to obtain the optimal magnitude and phase of the THVI [47], [48]. Moreover, THVI has a significant impact on the submodule voltage fluctuations of the MMC [48]. Its principle is presented in Fig. 4(a).

The NS method adjusts the angles between the phase voltages in such a way that all the healthy submodules are utilized, the line-to-line voltages are balanced, and the amplitude of line voltages is maximized [49], [50]. The essence of the NS method is to inject a fundamental zero-sequence voltage (FZSV) based on phasorial calculation. The ac-side voltages of the converter with respect to the midpoint of its dc side are regulated to be unbalanced. However, the three-phase line-to-line voltages of the converter are maintained as a balanced set, as shown in Fig. 4(c). Thus, the amplitude of three-phase voltages of the converter should be proportional to the number of the remaining operating submodules in corresponding phases, which limits the converter output voltage [50]. The NS approach can be applied as MMC fault-tolerance method by reference modification, as described by the Siemens patent in [53].

2) Modulation-Based Methods: another alternative to operate the converter under faulty submodule condition is modifying the converter modulation scheme [54]. These approaches can be sorted into space-vector modulation (SVM) and overmodulation methods [54]–[58].

a) Space-vector modulation: the presence of redundant switching states is a well-known characteristic of multilevel converters. Through space-vector modulation, these states can be optimized. Zang et al. propose a fast SVM algorithm to control the converter under faulty conditions, which can produce a three-phase balanced line-to-line voltage, as described in [55]. SVM methods able to insert an external dc offset to the faulty converter phases are presented in [54]. These studies are performed for five- and seven-level cascaded H-bridge (CHB), which can be extended to low-level MMC application [54]. However, the SVM techniques are quite complex for a high number of submodules in MMC-HVDC applications.

b) Overmodulation: MMC-HVDC are usually designed to operate in the converter linear region, which implies that the peak-to-peak voltage in the ac port should be lower than the dc port voltage [56]. However, the ac fundamental component of the voltage can be increased beyond this limit through overmodulation strategies, as shown in Fig. 4(b). Since this voltage command is permanently beyond the limits (e.g. postfault operation), it cannot be physically produced by the MMC. Therefore, operation in the overmodulation region can increase the total harmonic distortion (THD) in the output current [56]. However, the THD in MMC-HVDC system might not be an issue, due to the large number of series-connected submodules [57]. Additionally, Cupertino et al. demonstrate that the MMC operating as STATCOM presents a notable inherent fault tolerance in the overmodulation region, as presented in reference [58].

3) Redundancy-Based Methods: when MMC submodule failures are identified, the corresponding submodule should be bypassed [59]. Under such conditions, a redundancy strategy might be used to ensure that the converter remains operating without affecting the overall performance [21], [60]. Redundancy strategies can be implemented through N_R additional submodules in the converter structure, as illustrated in Fig. 2. In general, the redundant submodules are usually operated in active mode or standby mode [21], [59], [60]:

a) Active Strategy: the redundant submodules operate "actively". Essentially, there is no difference between the redundant submodules and non-redundant submodules. The MMC arm continues to operate upon submodule failures as long as the number of healthy submodules is higher than N. This redundant mode can operate on active redundancy without load-sharing (AR) or active redundancy with load-sharing (ALR) [59]. A load-sharing rule dictates how stress or load is redistributed to the surviving components after a component fails or degrades within the system. Active redundant submodule schemes are preferred in converter fault-tolerance operation for medium or low-voltage application [61]. The advantages of these active reserve methods are higher submodule utilization ratio, no additional charging time for reserve submodule and improved dynamic performance [61], [62]. All these factors lead to the broad acceptance of active reserve methods in medium and low-voltage applications.

b) Standby Strategy: the redundant submodules are bypassed and initially discharged. When failures occur, the corresponding faulty submodules are bypassed from the MMC arm, and redundant submodules are inserted [60]. Therefore, the standby redundant (SR) method presents low converter power losses, which is an interesting feature for HVDC applications. However, an extra power supply is required

for the redundant submodule, since the capacitor is initially discharged in standby submodules [8]. Another issue arises when a standby submodule fails, since the failure can only be detected if the submodule is operating. Moreover, this strategy results in the worst performance for dynamic behavior, since the charging process of the standby submodules affects the submodule voltage and grid current [51].

To overcome the charging process of the standby submodules, warm redundant submodules work in voltage balance state under normal operation is presented in reference [44]. Therefore, the redundant submodules can quickly replace the faulty submodules without significant transients. Moreover, the power losses of the redundant submodules are lower than those in active redundancy.

Theoretical analysis of the redundant sharing among the converter arms is described in [63]. As advantages, for the same reliability requirements, this strategy requires less redundant submodules. However, reconfiguration switches are required, which increases the implementation complexity.

All the redundancy techniques have advantages in relation to converter reliability, besides ensuring symmetrical operation in postfault condition. In addition, redundancy results in an inherent extra power that might be used in emergency situations [64].

C. MMC control under faulty submodules

Unlike many other converter topologies, the control of MMC is quite challenging and involves multiple control objectives [4], as shown in Fig. 5. Some control methods for the MMC, such as direct modulation, closed- and open-loop control are investigated in [65]. The complexity of the control system can be an issue, due to the high number of submodules in MMC-HVDC. In such cases, the open-loop control reduces the use of communication and computational resources, as described in [65].

Usually, the HVDC systems are composed of two ac stations. One station regulates the total transmitted active power while the other controls the total dc-link voltage. The output current is typically used to control the active power or the MMC total stored energy (proportional to the dc-link voltage) [66]. Some control techniques are well established and implemented in the stationary-abc, stationary-$\alpha\beta$ or synchronous-dq reference frames [66].

When submodule failure occurs, upper and lower arm voltages can differ in terms of number of levels, and even-order harmonics can appear in the output current. This issue is solved in the literature through several modulation strategies [61], [62]. An improved level-shifted carrier PWM based on the concept of virtual voltage is proposed in [61]. In [62], the period and phase registers of the phase-shifted carrier PWM in converter fault-tolerance operation are properly adjusted, according to the information of bypassed submodules. However, the change in the number of operating submodules adds complexity to the carrier arrangement in the modulation scheme [4]. On the other hand, the staircase modulation schemes provide a flexible algorithm, able to adapt to faulty submodule conditions. In [67], the nearest level control (NLC) is proposed as optimized control strategy, based on the dynamic redundancy. It is important to remark that harmonic distortion will be an issue only in systems with few SMs, which is not the case of the state-of-art MMC-HVDC systems.

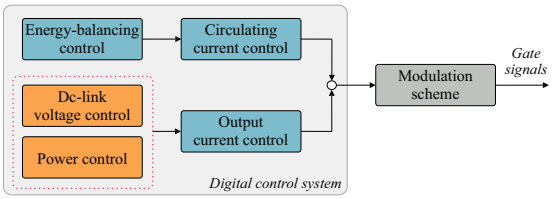

Fig. 5. Block diagram of the MMC classical control.

According to [66], the MMC operates with two ideally independent currents (i.e., the output current and the circulating current). Since a faulty submodule affects the energy balance of the MMC, this effect is usually treated in the circulating current control. The circulating current control has been used to balance and equally distribute the MMC total energy between each arm and suppress the harmonics of the circulating current during asymmetric operation [68].

Yang et al. propose a circulating current-suppressing (CCS) control method based on synchronous-dq reference frames, as described in [49]. It can achieve only the suppression of the second-order frequency ac components of the circulating current. In [69], the adjustment of submodule capacitor voltages on the faulty arms is proposed to ensure the energy equalization of each arm. A CCS control that can suppress the multi-different frequency components of the circulating current under different submodule failure types is proposed in [70]. Further, this method can help fast-limiting the transient fault current caused at the faulty submodule bypassed moment.

IV. Comparison of MMC Fault-Tolerance Schemes

This section intends to analyzes the limitations of each MMC fault-tolerance scheme in the occurrence of submodule failures. Therefore, the following consideration is assumed:

$$V_{dc} = NV_{SM}, \tag{1}$$

where V_{dc} is the MMC dc-link voltage and V_{SM} is the submodule capacitor voltage. Moreover, the submodule capacitor voltage can be described by:

$$V_{SM} = \delta V_{SM,FIT}, \tag{2}$$

where δ is the margin of the submodule utilization ratio and $V_{SM,FIT}$ is the maximum continuous dc voltage of the semiconductor devices for a specified failure rate, due to cosmic radiation [52]. A typical failure rates for one IGBT module is 100 FIT (failure in time) [52].

Alternatively, the dc-link voltage can be described by the maximum number of submodule failures N_f allowed in the MMC:

$$V_{dc,f} = (N - N_f)V_{SM}. \tag{3}$$

If the MMC is designed to operate with sinusoidal PWM modulation in steady state, the phase-to-neutral voltage synthesized by the converter is $V_s = V_{dc}/2$. On the other hand, if the MMC operates with a THVI scheme under postfault condition, $V_s = V_{dc,f}/\sqrt{3}$ can be reached [71]. Therefore:

$$\frac{V_{dc,f}}{V_{dc}} = \frac{(N - N_f)V_{SM}}{NV_{SM}} = \frac{\sqrt{3}}{2}. \tag{4}$$

Thus, the maximum number of submodule failures is:

$$N_{f,THVI} = \left(1 - \frac{\sqrt{3}}{2}\right) N. \tag{5}$$

According to Eq. (5), the THVI method allows about 13 % of submodule failures in postfault operation. However, it is noteworthy that the initial design of the converter operating with the THVI method is more interesting. Therefore, the submodule capacitances can be reduced, since the energy storage requirements are reduced when 1/6 of third-harmonic injection is employed [71].

According to [72], the number of failures allowed by NS method is given by:

$$N_{f,NS} \leq N \left[1 - (1 + \delta_m)\left(\frac{1}{2} + \frac{\widehat{V}_g}{V_{dc}}\right)\right], \tag{6}$$

where δ_m is the modulation margin in practical application and $\widehat{V}_g$ is the amplitude of the grid voltage. As noted, the converter fault tolerance of the NS method is related to the modulation margin. Therefore, the same argument described for the THVI methods is applied to the NS schemes.

The SVM schemes have an interesting feature for HVDC systems by reducing converter switching loss. Nevertheless, the reduced output voltage in postfault condition is the common drawback for these schemes [73]. Moreover, in an MMC with a large number of submodules (N $>$ 20), it is difficult to implement the SVM schemes [4].

The operation in the region of overmodulation is not desired under normal conditions. However, there are exceptional cases in which MMC could be forced to operate in this mode. These would include transient conditions or quasi-permanent conditions, such as the failure of one or more submodules of the MMC [56]. Regarding HVDC systems, long periods of operation in the overmodulation region should be avoided due to reduced power quality.

In the CVI method, the utilization ratio of the submodule is improved effectively [8]. The synthesized voltage remains unchanged and the submodule capacitor voltages of the operating submodules are increased. Therefore, the following relation is obtained $(N - N_f)V_{SM,f} = NV_{SM}$. The operating voltage can be increased until reaching $V_{SM,FIT}$, thus:

$$V_{SM,f} = \frac{N}{N - N_f}\delta V_{SM,FIT} \leq V_{SM,FIT}. \tag{7}$$

Therefore, for the CVI method:

$$N_{f,CVI} = (1 - \delta)\, N. \tag{8}$$

It is worth to remark that the maximum redundancy in this method is dependent on the voltage margin. Therefore, the operating voltage of the submodules must be reduced, while additional submodules must be included in the initial design phase. Thus, the initial cost of the CVI method is expected to be similar to that of redundant schemes.

The redundant configurations increase the converter reliability at the cost of increased component investment and control complexity [74]. The maximum allowed number of failures in these methods depends only on the cost related to the implementation of redundant submodules. According to [51], the AR strategy is less efficient than the ALR method. Furthermore, the SR method achieves higher efficiency, since there are fewer operating submodules. However, the required activation time by the redundant submodule is relatively longer [74]. Thus, the SR strategy results in the worst performance for dynamic behavior.

Due to the described limitations of the THVI, NS, SVM and overmodulation schemes in MMC-HVDC applications under faulty submodule conditions, the next sections aim to evaluate the effect of the faulty submodules on the reliability and power losses of MMC, considering the CVI, AR, ALR and SR methods.

V. Case Study

A real MMC-HVDC system is employed in this case study. The Xiamen transmission project has the delivery capacity of 1000 MVA with $\pm$ 320 kV dc-link voltage. It is the first bipolar MMC-HVDC system in the world. This configuration has two converter stations, and each converter station is composed of two MMCs, as observed in Figs. 1(d) and (e). The case study evaluates the reliability at both converter level and system level. Moreover, since the loss of a pole in the bipolar configuration ensures 50 % of the transmission capacity, the bipolar MMC-HVDC system-level reliability is evaluated based on the probability that at least 1 pole is under operation. The main parameters used in the Xiamen project are summarized in Tab. II [75].

Fig. 6 illustrates the reliability block diagram (RBD) of a bipolar MMC-HVDC system. As noted, the RBD can be divided into four hierarchies: submodule level, arm level,

TABLE II
Main parameters used in Xiamen MMC-HVDC project.

Parameters	Values
Rated power (per pole)	500 MVA
Dc-link voltage (V_{dc})	320 kV
Grid voltage (V_g)	220 kV
IGBT ratings	3.3 kV/1.5 kA
Nominal submodule voltage (V_{SM})	1.6 kV
Maximum submodule voltage ($V_{SM,FIT}$)	1.8 kV
Submodule switching frequency	150 Hz
Submodule capacitance (C_{SM})	10 mF
Arm inductance (L_a)	60 mH
Arm resistance	1.6 Ω
Non-redundant submodules (N)	200
Redundant submodules (N_R)	16

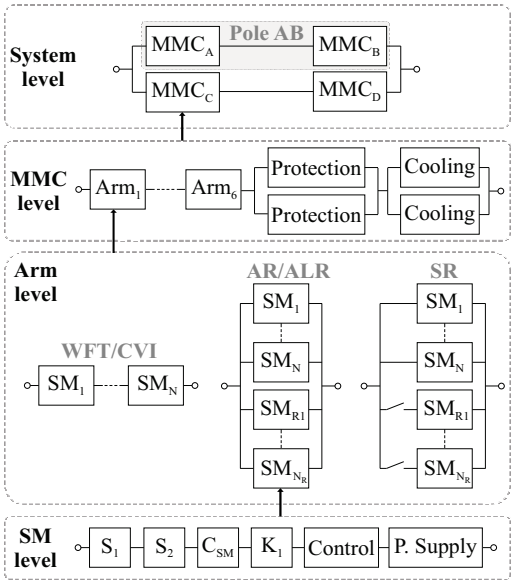

Fig. 6. Hierarchical reliability modeling of a bipolar MMC-HVDC.

converter level and system level. In each hierarchical level, the RBD is used to represent the reliability relationship of system components [60]. An active redundancy of both cooling and protection systems is included, which is a common practice in real HVDC projects [63]. Since the failure rate (λ) of arm inductor is generally negligible when compared with the submodule components [63], the reliability model of arms focuses on submodules. Furthermore, the failure rate of other HVDC components such as dc cables, transformers and dc switchgears are not considered in the present analysis. These components can be included in the analysis when the objective is to compute the energy availability of the whole HVDC system. However, this analysis requires failure rates and repair times for each component, as described in [76].

Voltage stress factors (η) for IGBT modules and power supply are assumed as 2.43, while the value of 7.5 is chosen for capacitors, as described in [63]. When the voltage stress in the component increases, its failure rate also increases. The increase of failure rate can be expressed by:

$$\lambda_{b^*} = \lambda_b v_s^{\eta}, \tag{9}$$

where λ_b is the base failure rate and v_s is the ratio of the applied voltage to the nominal voltage. The failure rate of an operating submodule (λ_{SM}) is obtained by summing the failure rates of its components, as presented in Fig. 6. The standby redundant submodule is unable to enter into operation by the bypass switch, since the bypass switch is assumed to fail in short circuit mode [77]. Therefore, the failure rate of the standby redundant submodules is assumed equal to the failure rate of the bypass switch [77]. All component failure rates employed in this work are presented in Table III. These values were based on statistical data and information from State Grid Corporation of China [63], [77], [78].

Besides the converter operation without fault tolerance (WFT), four MMC fault-tolerance schemes are selected: AR, ALR, SR and CVI methods. The figures of merit selected are

TABLE III
COMPONENT FAILURE RATE DATA.

System	Component	λ_b (occ/year)	No.
Submodule	IGBT module ($S_{1,2}$)	0.0008	2
	Capacitor (C_{SM})	0.001752	1
	Control system	0.00318	1
	Power supply	0.03504	1
	Thyristor (K_1)	0.00041	1
	Bypass switch (K_2)	0.00876	1
MMC	Protection system	0.03	1+1
	Cooling system	0.04	1+1

the reliability function and the power losses under normal and faulty conditions. The MMC reliability is evaluated through the models proposed by [63]. This reference considers the AR, ALR and SR schemes. The MMC reliability is evaluated based on Markov Chain-based approach. The MMC reliability model for the CVI strategy is obtained by adapting the model to the ALR proposed by [63], since both strategies present a similar concept. To ensure the operation of at least one pole, the system-level reliability is evaluated through the *one-out-of-two* model [60].

The power losses in semiconductor devices are evaluated based on look-up tables of the conduction and switching loss information provided in the datasheet. The part number 5SNA 1500E330305 of 3.3 kV - 1.5 kA is considered in the analysis. The temperature dependence of the power losses is included in the evaluation. The hybrid thermal model is employed to estimate the junction and case temperature of each power device, as described in [79]. The heatsink value of 20 K/kW ensures the maximum junction temperature around 110 °C for the most stressed power device at rated operating conditions. An ambient temperature of 40 °C is assumed. All calculations are conducted using PLECS and MATLAB.

VI. RESULTS

The effect of faulty submodules on MMC power losses operating at rated power is illustrated in Fig. 7(a). As observed,

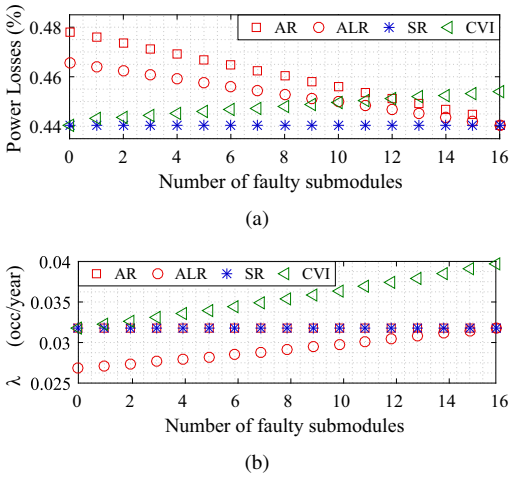

Fig. 7. Effect of faulty submodules on: (a) MMC power losses operating at rated power; (b) failure rate of remaining operating submodules.

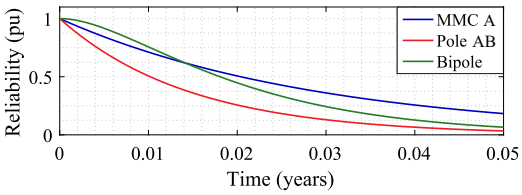

Fig. 8. Reliability function for different hierarchical levels. *Remark*: Reliability of the bipolar MMC-HVDC ensuring at least one operation pole.

the SR and CVI methods present the lowest MMC power losses for normal operating conditions, around 0.441 %. The ALR and AR methods start with a greater number of operating submodules, reaching MMC power losses of 0.465 % and 0.478 %, respectively. The ALR method presents lower MMC power losses than the AR method due to lower initial blocking voltage in the submodules. Considering the active redundancy, the MMC power losses decrease if the number of operating submodules decreases. When the maximum number of failures occurs, AR and ALR have the same MMC power losses compared to the SR method. However, the CVI method presents an increase in the converter power losses of approximately 0.014 % in the fault limit operation when compared to the other MMC fault-tolerance methods.

Fig. 7(b) shows the failure rate of the remaining operating submodules under faulty submodule condition. The AR and SR schemes present the similar submodule failure rate for all conditions. The ALR method presents approximately 15 % reduction in the submodule failure rate, reaching the same failure rate of about 0.032 (occ/year) in the failure limit operation. Moreover, the CVI method has a submodule failure rate about 25 % higher under the same condition.

Fig. 8 shows the reliability function for different hierarchical levels. The system-level reliability function is calculated as the probability that at least one pole is operating. As noted, the system-level reliability is higher than the reliability of a single pole. A low reliability is observed, since no MMC fault-tolerance method is applied. In this way, Fig. 9(a) presents the MMC reliability for different MMC fault-tolerance schemes in comparison to the WFT scheme.

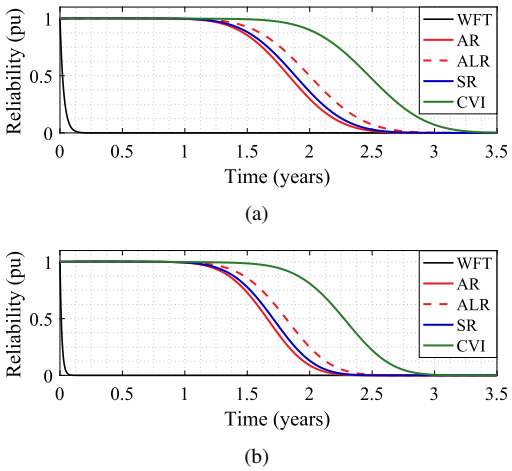

Fig. 9. Reliability function for different MMC fault-tolerance schemes. (a) Converter level; (b) System level with at least one operating pole.

As observed in Fig. 9(a), the WFT solution gives a converter reliability less than 1 % within 2 months of operation. Considering that the scheduled maintenance is performed annually, the AR scheme has a converter reliability of 99.6 % within 1 year of operation. The SR and ALR schemes present a converter reliability of 99.7 %. and 99.8 %, respectively. Due to the submodule voltage margin adopted in the project, the CVI scheme can admit 22 faulty submodules (6 more than the redundant techniques). Thus, the CVI method has the highest MMC reliability, which reaches more than 99.9 % for 1 year of operation.

A similar analysis is performed at the level of the bipolar MMC-HVDC system. Fig. 9(b) illustrates the system-level reliability that ensures at least one operational pole. The CVI method present the highest system-level reliability, since it reaches more than 99.9 % for 1 year of operation, against 99.3 % of the AR scheme.

VII. Conclusion

This work presented a comprehensive survey on the converter fault-tolerance strategies for the MMC-HVDC systems introduced in past literature. Some MMC-HVDC solutions adopted by industry were reviewed. The main approaches related to fault diagnosis, converter fault-tolerance methods and MMC control under fault conditions were discussed. The limitations of each MMC fault-tolerance schemes under submodule failures are described and critically compared. It is important to remark that this survey is based on the available technical literature, since not all manufacturers have published their topologies and control strategies. A case study is conducted based on a real MMC-HVDC project, aiming to evaluate the effect of the faulty submodules on reliability and power losses. The following conclusions are highlighted, based on past research and the results obtained in this work:

1) PIM devices are currently preferred due to their commercial availability. This fact is observed because the electric drive market is broader than the HVDC market. In addition, PPI technology is relatively new, and is still maturing. This technology provides advantages in terms of short-circuit handling and guaranteed short-circuit failure mode. Therefore, the authors consider that the PPI device can be increasingly adopted in the future.
2) The bypass structure is essential in MMC-HVDC systems based on half-bridge submodules during dc-link short circuits. However, it is not recommended to neglect the bypass structure from submodules with dc-short circuit handling capability (e.g. full-bridge submodules), because it plays a fundamental role in the converter fault tolerance. In addition, the vacuum contactor is interesting to reduce power losses in the faulty submodules.
3) The fault detection based on the analytical methods provides lower cost, using existing measured variables in the controllers. Future developments in computational intelligence and machine learning are promising, since simple fault detection algorithms are still a demand from the HVDC industry.

4) The ZSV and overmodulation methods present a limited potential and cannot be the main converter fault-tolerance strategy for MMC-HVDC systems. However, they can be interesting solutions in emergency situations.
5) The CVI scheme is relatively simple to be implemented. However, it requires a design margin to be employed. The results for the adopted case study indicate higher power losses under faulty submodule conditions, since the operating voltage of the remaining submodules increases. In addition, when the number of failures increases, the number of levels in the converter output decreases, which leads to higher harmonic distortion. It is important to remark that MMC-HVDC systems present hundreds to thousands of submodules, and harmonic distortion will hardly be an issue.
6) The SR method presents the lowest power losses among the studied schemes, which is a clear advantage for high-power converters. However, the charging process of the standby submodules is a drawback of this technique. Moreover, an extra power supply is required for the redundant submodule, since the capacitor is initially discharged in standby submodules. Another issue arises when a standby submodule fails, since the failure can only be detected if the submodule is operating.
7) The Xiamen MMC-HVDC project has 16 redundant submodules per arm. The results indicated that the ALR scheme leads to higher reliability, compared to the AR and SR approaches, due to the reduced submodule voltage stress. The CVI method can reach 22 submodule failures, due to the voltage margin adopted in this project. Thus, the CVI method presented the highest reliability.
8) Strategies to reduce the cost of redundancy are still required by the MMC-HVDC industry. Therefore, the redundancy sharing among the converter arms and the optimum combination of converter fault-tolerance schemes are possible approaches to reduce the requirement of redundant submodules and may be investigated in further research.
9) The conclusions stated for the Xiamen MMC-HVDC project are dependent on the adopted failure rates, which were based on statistical data and information from the State Grid Corporation of China. Indeed, the approach adopted for reliability evaluation did not consider the wear-out of the components, which directly affects the failure rates. The authors consider that more accurate estimation of the component failure rate and its effect on the redundancy design are topics which must be investigated in further research.

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