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Optimization of Centralized Equalization Systems Based on an Integrated Cascade Bidirectional DC-DC Converter

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Abstract—This paper presents a novel integrated cascade bidirectional dc-dc converter for optimizing a centralized charge equalization system. Through the integrated cascade structure, the polarity switches and the bidirectional dc-dc converter in the traditional centralized system are integrated, and the cells with different voltage polarities are equalized by controlling the operating state of the converter. Compared with the conventional methods, the number of active switches is significantly reduced, leading to a more compact size and a higher reliability. Moreover, with a phase-shifted PWM modulation strategy, the peak value of the transformer current is reduced and the soft-switching operation is realized, thus greatly reducing the transformer and switching losses. Finally, the experimental results on 13 series-connected battery cells show that the proposed scheme exhibits the excellent performance in terms of equalizing efficiency and speed. The performance improvement of the proposed equalizer is further validated by a systematic comparison with the conventional centralized equalization methods.

Index Terms—Bidirectional dc-dc converter, integrated cascade, battery equalizers, zero-voltage switching (ZVS).

I. INTRODUCTION

DUE to the limited voltage and capacity of a single lithium-ion battery, multiple cells are typically packed in series and parallel to meet the requirements of high-power applications [1]. However, there are often inconsistencies in terms of performance among the cells in a battery pack, and such inconsistencies tend to grow over time. This will reduce the available capacity and accelerate the degradation of battery packs, and even cause fire and explosion accidents. Therefore, battery equalization technology should be adopted to achieve safe and reliable operation of battery packs [2], [3].

According to the energy consumption in the equalization process, equalization technologies are composed of passive type [4] and active type [5]–[26]. The active methods including capacitor equalization, transformer equalization, and dc-dc converter equalization, etc., have obvious advantages such as

high efficiency and low energy consumption, which have been frequently applied as effective solutions in recent years.

The equalization technology based on switched-capacitors is widely used in practical systems because of its simple structure and easy implementation. In [5]–[6], equalization methods based on a double-layer switched-capacitor and chain structure are proposed. Compared with the classical switched-capacitor scheme in [7], the equalization path between cells in these two methods is shortened, and the equalizing efficiency and speed of long series-connected battery strings are improved. Several primary improvements are presented in [8]–[11] such as delta structure, star structure and coupling capacitor structure. These structures provide a direct balancing path between any two cells, and achieve global equalization of the entire battery pack. However, the balancing current in the capacitor-based methods depends on the voltage gap between the cells, which tend to cause an uncontrollable equalization current and a low equalization accuracy.

Transformer equalization technology requires a large number of switches and transformer windings, which has the disadvantages of large volume and difficult expansion. Based on these problems, the intensive attentions about improving the transformer equalization method have been given in [12]–[15]. An equalization circuit based on a forward-flyback converter is proposed in [12], where a multi-winding transformer merges the forward and flyback converters to achieve the automatic balance of the battery packs. Compared with the traditional multi-winding scheme in [13], the additional demagnetizing circuit is neglected so as to improve the applicability of this method in practical operation. In [14], an equalizer based on coupled half-bridge converters is adopted. By sharing a transformer winding between two cells to form a half-bridge converter, the quantity of the transformer windings and circuit volume are effectively reduced.

According to the structure and distribution of converters, the dc-dc converter equalization technology can be divided into distributed [16]–[20] and centralized [21]–[26] methods, which have evident advantages such as high equalization accuracy, high equalization current and high efficiency. In distributed system, each cell is connected with an individual equalizer, where the classical distributed circuits include buck-boost converters [16], LC resonant converters [17], Cuk converters [18] and quasi-resonant converters [19]. Also, a multiphase interleaved converter is presented in [20], which can provide a real-time balance with high efficiency. However, the increase of cell number also causes the increase of volume, cost and control complexity of the distributed method, which reduces the practicability of this method in large capacity battery packs.

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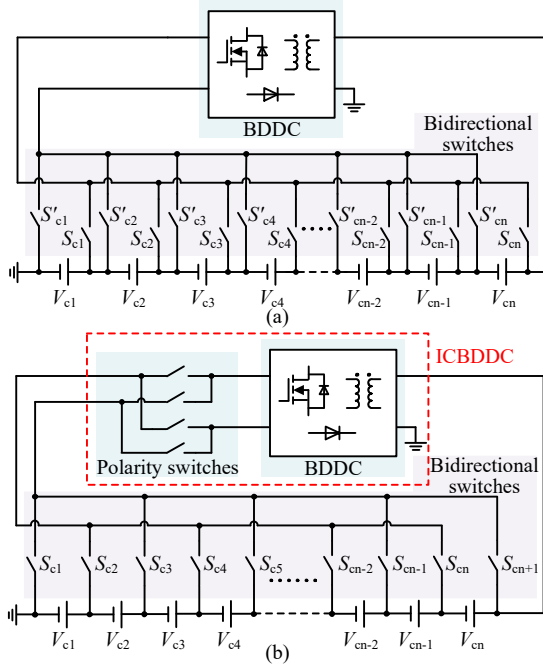


Fig. 1. Architectures of centralized charge equalization systems. (a) Traditional architecture without polarity switches. [21]-[22] (b) Traditional architecture with polarity switches [23]-[26] and its optimization process.

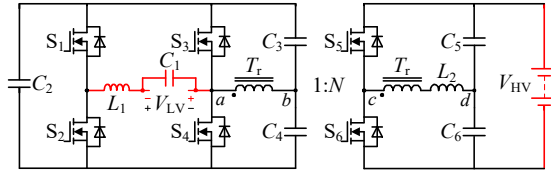


Fig. 2. Proposed integrated cascade bidirectional DC-DC converter.

Compared with the distributed dc-dc converter equalization method, the centralized method has the attractive advantages such as easy expansion, low control complexity, and compact structure, which is more suitable for systems with a large number of cells. As shown in Fig. 1, for systems with n cells, there are two traditional centralized equalization architectures. The first architecture in Fig. 1(a) includes $2n$ bidirectional switches, and the voltage polarity of the cells connected to the bidirectional dc-dc converter (BDDC) is fixed [21], [22]. The second architecture shown in Fig. 1(b) consists of $n+1$ bidirectional switches and 4 polarity switches, which adjust the voltage polarity of the unbalanced cells connected to the BDDC via the polarity switches [23]-[26]. When the number of cells is large, compared with the first architecture, the second equalization architecture significantly reduces the total number of active switches and improves the integration of the equalization system. However, the conduction of polarity switches and bidirectional switches should be coordinated to ensure the system efficiency and avoid the risk of short circuit.

Fig. 1(b) shows the optimization process of the centralized charge equalization architecture, where the polarity switches are integrated with BDDC to build a novel integrated cascaded bidirectional DC-DC converter (ICBDDC). Compared with a series of conventional BDDCs proposed in [21]-[26], the most contribution of the ICBDDC is to optimize the centralized equalization system to have fewer switches, resulting in a more compact size and a higher integration. Moreover, the optimized

architecture is able to avoid the coordination problem of bidirectional switches and polarity switches, further improve the reliability and modularity of the equalization system, and address the dilemma of achieving equalization with low cost and high efficiency for a long series-connected battery string.

II. OPERATION AND ANALYSIS OF THE CONVERTER

Fig. 2 shows the topology of the proposed ICBDDC, where the turn ratio of transformer T_r is $1:N$. In the proposed converter, the low-voltage side V_{LV} is connected to a cell selected by the switch array, and the high-voltage side V_{HV} is connected to the battery string. L_1 is the filter inductance on the low-voltage side, and L_2 is the energy transfer inductance, which consists of the transformer leakage inductance L_r and the external inductor.

This converter can equalize the cells with different voltage polarities selected by the switch array, where the voltage polarities of the odd-numbered and even-numbered cells connected to V_{LV} are left-positive/right-negative and right-positive/left-negative, respectively. To achieve bidirectional controllable power transmission, a phase-shifted PWM control strategy is developed for the proposed converter. As illustrated in Fig. 3, T_s is the switching period of S_1 - S_6 , and ϕ is the phase-shift duty cycle between the primary side and secondary side of the transformer. The optimization characteristics of the centralized equalization system based on the proposed ICBDDC are summarized as follows.

- 1) *Volume and structure*: The proposed converter greatly reduces the number of active switches, so that the centralized equalization system has a more compact structure, lower cost and better scalability.
- 2) *Efficiency*: The phase-shifted PWM modulation reduces the peak value of the transformer current and realizes zero-voltage switching (ZVS) operation of switches, which thus reduces the transformer loss and switching loss.
- 3) *Reliability and security*: The integrated cascade structure avoids the risk of short circuit caused by poor coordination of bidirectional switches and polarity switches, and also enables the equalization current work in a controllable and continuous state to prevent potential damage to the cell.
- 4) *Equalization performance*: The proposed converter obtains a high voltage conversion ratio and enhances the equalization voltage gap, which can not only increase the balancing current to improve the equalization speed, but also equalize a battery string containing more cells.

A. Boost Mode

When a single cell is overcharged, the converter is operated in boost mode to release the energy stored in the cell to the entire battery string. Fig. 3 (a)-(b) are equalization switching waveforms of overcharged odd-numbered and even-numbered cells, respectively. The only difference is the switching sequence of several switches. Since cells with different voltage polarities have the same equalization principle, to simplify the length, the equalization of odd-numbered cells is taken as an example for analysis. As shown in Fig. 3 (a), there are two control variables D_2 and ϕ , when an odd-numbered cell is equalized. With the proposed control strategy, adjusting D_2 can match the primary and secondary voltages of the transformer, and adjusting ϕ can control the power flow of the converter.

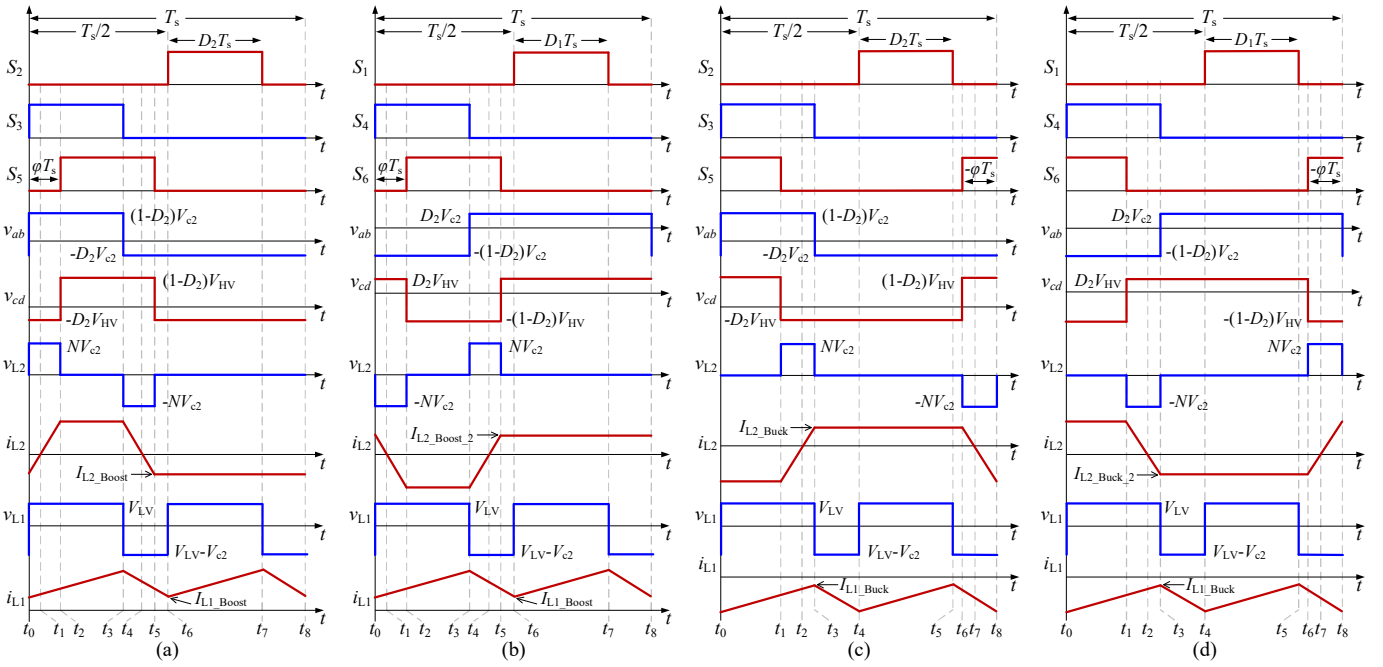


Fig. 3. Switching sequence diagrams of the proposed converter. (a) Equalization of an overcharged odd-numbered cell. (b) Equalization of an overcharged even-numbered cell. (c) Equalization of an undercharged odd-numbered cell. (d) Equalization of an undercharged even-numbered cell.

According to Fig. 3 (a), when the converter is operated in boost mode with $\varphi > 0$, the voltage relation between the primary and secondary side of the converter and the volt-second balance relation of inductor L_1 can be respectively written by

$$\begin{cases} V_{LV} D_2 T_s = (V_{C2} - V_{LV})(1 - 2D_2) \frac{T_s}{2} \\ NV_{C2} = V_{HV} \end{cases} \quad (1)$$

Thus, the voltage gain in boost mode can be calculated:

$$M_{\text{Boost}} = \frac{V_{HV}}{V_{LV}} = \frac{N}{1 - 2D_2} \quad (2)$$

In addition, under a phase-shifted PWM control, the voltage on capacitors C_3 - C_6 can be expressed as

$$\begin{cases} V_{C3} = (1 - D_2)V_{C2} \\ V_{C4} = D_2 V_{C2} \\ V_{C5} = (1 - D_2)V_{HV} \\ V_{C6} = D_2 V_{HV} \end{cases} \quad (3)$$

By combining (3) and the switching waveforms in Fig. 3 (a), and assuming that I_{L2_Boost} is the initial value of the current i_{L2} , then, the current flowing into L_2 on the high-voltage side in a switching cycle can be expressed as follows:

$$i_{L2} = \begin{cases} I_{L2_Boost} + \frac{NV_{C2}}{L_2} t & (t_0 < t < t_2) \\ I_{L2_Boost} + \frac{\varphi T_s NV_{C2}}{L_2} & (t_2 < t < t_3) \\ I_{L2_Boost} + \frac{(D_2 + \varphi)T_s NV_{C2}}{L_2} - \frac{NV_{C2}}{L_2} t & (t_3 < t < t_5) \\ I_{L2_Boost} & (t_5 < t < t_8) \end{cases} \quad (4)$$

From (4) and the voltage v_{ab} on the primary-side of the transformer, the power transmitted from the low-voltage side to the high-voltage side can be calculated by

$$P_{\text{Boost1}} = \frac{1}{T_s} \int_0^{T_s} N i_{L2} v_{ab} dt = \frac{\varphi N^2 V_{LV}^2 [2D_2(1 - D_2) - \varphi]}{2L_2 f_s (1 - 2D_2)^2} \quad (5)$$

It should be noted that the converter works in boost mode with $\varphi > 0$, so the transmitted power P_{Boost} is positive.

Likewise, assuming I_{L1_Boost} is the initial value of the current i_{L1} , the current flowing into the low-voltage side inductor L_1 in a switching cycle can be expressed as

$$i_{L1} = \begin{cases} I_{L1_Boost} + \frac{V_{LV}}{L_1} t & (t_0 < t < t_3) \\ I_{L1_Boost} + \frac{D_2 T_s V_{C2}}{L_1} + \frac{V_{LV} - V_{C2}}{L_1} t & (t_3 < t < t_6) \\ I_{L1_Boost} + \frac{V_{LV}}{L_1} (t - \frac{T_s}{2}) & (t_6 < t < t_7) \\ I_{L1_Boost} + \frac{D_2 T_s V_{C2}}{L_1} + \frac{V_{LV} - V_{C2}}{L_1} (t - \frac{T_s}{2}) & (t_7 < t < t_8) \end{cases} \quad (6)$$

Subsequently, the output power of the overcharged cell on the low-voltage side can be obtained:

$$P_{\text{Boost2}} = \frac{1}{T_s} \int_0^{T_s} V_{LV} i_{L1} dt = \frac{V_{LV} [2L_1 f_s I_{L1_Boost} + V_{LV} D_2]}{2L_1 f_s} \quad (7)$$

Ignoring the power loss during the power conversion, by substituting (5) into (7), the initial value of i_{L1} can be given by

$$I_{L1_Boost} = \frac{\varphi N^2 V_{LV} [2D_2(1 - D_2) - \varphi]}{2L_2 f_s (1 - 2D_2)^2} - \frac{V_{LV} D_2}{2L_1 f_s} \quad (8)$$

In addition, the ampere-second balance relations of C_5 and C_6 in a switching cycle can be obtained by the following:

$$\int_{t_0}^{t_2} -i_o dt + \int_{t_2}^{t_5} (i_{L2} - i_o) dt + \int_{t_5}^{t_8} -i_o dt = 0 \quad (9)$$

$$\int_{t_0}^{t_2} -(i_{L2} + i_o) dt + \int_{t_2}^{t_5} -i_o dt + \int_{t_5}^{t_8} -(i_{L2} + i_o) dt = 0 \quad (10)$$

where i_o is the equivalent load current in boost mode.

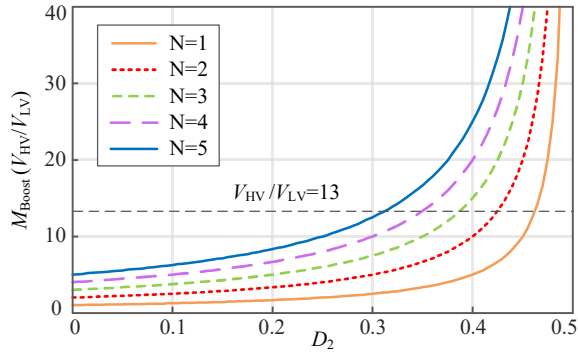


Fig. 4. Voltage gain in boost mode under different turn ratios N .

Thus, the initial value of current i_{L2} can be calculated by

$$I_{L2_Boost} = \frac{-NV_{LV}D_2\varphi}{L_2f_s(1-2D_2)} \quad (11)$$

In boost mode, the voltage gain versus the duty cycle D_2 under different transformer turn ratios N are shown in Fig. 4. It can be seen that the voltage gain of the converter is only related to the transformer ratio N and the duty cycle D_2 , but not to the phase-shift duty cycle φ . When N is small, a high boost gain can be achieved by adjusting D_2 , which provides the ability to balance a battery pack with more batteries.

B. Buck Mode

When a single cell is undercharged, the converter is operated in buck mode to release the energy stored in the entire battery string to the cell. Fig. 3 (c) and (d) show the equalization switching waveforms of the undercharged odd-numbered and even-numbered cells, respectively, and the difference is also the switching sequence of the switches. As previously mentioned, the equalization of odd-numbered cells is analyzed as an example. Additionally, to ensure consistency of the derivation analysis, the positive direction of the voltage and the current of each inductor are defined as being the same as the boost mode.

According to Fig. 3 (c), when the converter works in buck mode with $\varphi < 0$, the derivation analysis of the converter is the same as that in boost mode. Thus, the derivation results are given directly to save space.

The voltage gain in buck mode can be given as (12), and the capacitor voltages V_{C3} - V_{C6} also can be represented in (3).

$$M_{Buck} = \frac{V_{LV}}{V_{HV}} = \frac{1-2D_2}{N} \quad (12)$$

The power transmitted from the low-voltage side to the high-voltage side can be calculated by

$$P_{Buck1} = \frac{1}{T_s} \int_0^{T_s} N i_{L2} v_{ab} dt = \frac{\varphi N^2 V_{LV}^2 [2D_2(1-D_2) + \varphi]}{2L_2 f_s (1-2D_2)^2} \quad (13)$$

The output power of the undercharged cell on the low-voltage side V_{LV} can be obtained:

$$P_{Buck2} = \frac{1}{T_s} \int_0^{T_s} v_{L1} i_{L1} dt = -\frac{V_{LV} [V_{LV} D_2 - 2L_1 f_s I_{L1_Buck}]}{2L_1 f_s} \quad (14)$$

Note that the battery string releases energy to the undercharged cell in buck mode. Therefore, the transmission powers P_{Buck1} and P_{Buck2} are both negative.

Ignoring the power loss during the power conversion, by combining (13) and (14), the initial value of i_{L1} can be given by

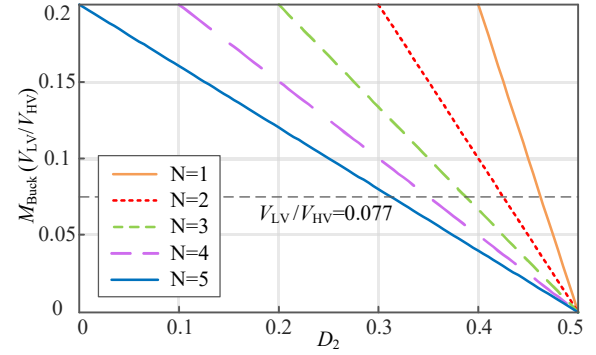


Fig. 5. Voltage gain in buck mode under different turn ratios N .

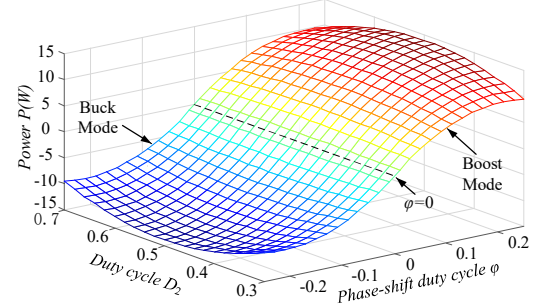


Fig. 6. Power curve versus D_2 and phase-shift duty cycle φ .

$$I_{L1_Buck} = \frac{\varphi N^2 V_{LV} [2D_2(1-D_2) + \varphi]}{2L_2 f_s (1-2D_2)^2} + \frac{V_{LV} D_2}{2L_1 f_s} \quad (15)$$

Similarly, according to the ampere-second balance relations of capacitors C_5 and C_6 , the initial value of i_{L2} can be derived as

$$I_{L2_Buck} = \frac{-NV_{LV}D_2\varphi}{L_2 f_s (1-2D_2)} \quad (16)$$

As illustrated in Fig.5, the voltage gain curves under different transformer turn ratios N can be obtained according to (12). As seen, the proposed converter has a high buck gain when N is small, which not only prevents D_2 from working in the limit state, but also reduces the volume and loss of the transformer.

According to the above analysis, the positive direction of the voltage and current of each inductor in boost mode is consistent with the buck mode, which directly causes different polarities in the transmission powers P_{Boost} and P_{Buck} . By substituting the parameters in Table I into (5) and (13), the power curve versus D_2 and φ can be obtained in Fig. 6. It can be seen that when $\varphi > 0$, the low-voltage side releases energy to the high-voltage side, which can equalize the overcharged cell. In contrast, the undercharged cell can be equalized when $\varphi < 0$. After the duty cycle D_2 is determined, the output power can be increased monotonously as φ increases, and the maximum and minimum power values are at $\varphi = D_2(1-D_2)$ and $\varphi = D_2(D_2-1)$.

III. PARAMETER DESIGN AND ZVS ANALYSIS

As previously mentioned, due to the symmetry of the converter, the equalization of cells with different voltage polarities has the same parameter design principles and soft-switching analysis. Therefore, only the equalization of odd-numbered cells is analyzed here and the conclusions are also applicable to the equalization of even-numbered cells.

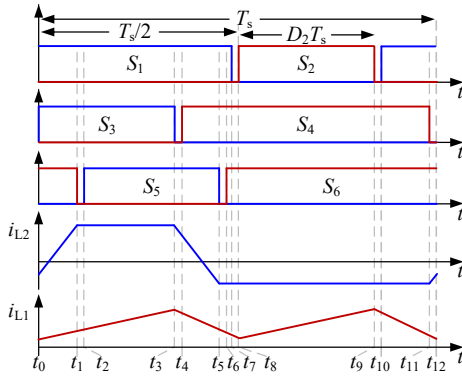


Fig. 7 Switching sequence diagrams with dead time in boost mode.

A. Circuit Parameter Design

Since the V_{LV} terminal is connected to an unbalanced cell, to avoid potential damage to the lithium-ion battery, L_1 should be operated in CCM mode to achieve a small current ripple. Therefore, the selection of L_1 depends on the ripple demand of the equalization current. It is assumed that the ripple coefficient α of i_{L1} is 0.15, which means $\Delta i_{L1} = \alpha I_{L1}$, and the equalization current is set to 3A. By substituting the parameters in Table I into (2) and (12), the duty cycle $D_2=0.308$ can be calculated. Then, the required inductance L_1 can be calculated by

$$L_1 > \frac{V_{LV} D_2}{\alpha I_{L1} f_s} = \frac{3.7 \times 0.308}{0.15 \times 3 \times 40 \times 10^3} = 63 \mu\text{H} \quad (17)$$

Hence, the filter inductance L_1 can be taken as 70 μH to achieve the ripple demand of the equalization current.

The value of inductance L_2 can be derived by substituting the parameters in Table I into (5) and (13). Assuming that only the size of each parameter is considered, it can be concluded that L_2 first increases and then decreases with an increase in $|\varphi|$, and has a maximum value at $|\varphi|=D_2(1-D_2)$. To make assure the operation of the converter, L_2 should be less than the maximum value within its range. This condition can be represented as (18)

$$L_2 < \frac{|\varphi| N^2 V_{LV}^2 [2D_2(1-D_2) - |\varphi|]}{2f_s P(1-2D_2)^2} = 118 \mu\text{H} \quad (18)$$

From (11) and (16), it can be seen that the peak value of the current flowing into the transformer is inversely proportional to L_2 , while a smaller peak current can improve the efficiency of the transformer. Therefore, in combination with (18), the energy transfer inductance L_2 can be selected as 115 μH .

B. ZVS Analysis

Since the ZVS implementations in boost mode and buck mode have the same principle, the boost mode is selected as an example to perform the following analysis. In practice, there is a dead time between the two switches above and below the bridge arm, which should be considered in the analysis of ZVS.

1) *ZVS of S_1 and S_4* : As shown in Fig. 7, after S_2 and S_3 are turned OFF at t_9 and t_3 , respectively, S_1 and S_4 will not be turned ON immediately due to the dead time. During $[t_9-t_{10}]$, the current i_{L1} freewheels through the body diode of S_1 to create the ZVS condition of S_1 at t_{10} . A similar case occurs within $[t_3-t_4]$, where the currents i_{L1} and i_{L2} freewheel through the body diode of S_4 at the same time. Hence, the ZVS condition is that the energy stored in L_1 and L_2 must charge and discharge the junction capacitors of the switches within the dead time.

TABLE I
COMPONENTS AND PARAMETERS OF THE PROTOTYPE

Parameters	Values/Ratings
Rated voltage of V_{LV}	3.7 V
Rated voltage of V_{HV}	48.1 V
Switching frequency (f_s)	40 kHz
Inductors L_1	70 μH ; Core:MS-090125-2; 28 turns
Inductors L_2	115 μH ; Core:MS-090125-2; 35 turns
Capacitors C_1	100 μF /16 V; multilayer ceramic capacitor
Capacitors C_2 - C_4	100 μF /35 V; solid-state capacitor
Capacitors C_5 - C_6	100 μF /100 V; aluminum electrolytic capacitor
Transformer T_r	Core: PQ2620-PC44; Primary turns $N_1 = 5$; Secondary turns $N_2 = 25$; Turns ratio 1:5; Leakage inductance $L_{s2} = 5 \mu\text{H}$; Magnetizing inductance $L_{m1} = 22.5 \mu\text{H}$;
MOSFETs S_1 - S_4	IRF1010Z; $V_{DSS}=55\text{V}$, $I_D=75\text{A}$; $R_{DS(on)}=7.5\text{m}\Omega$
MOSFETs S_5 , S_6	IRF540Z; $V_{DSS}=100\text{V}$, $I_D=36\text{A}$; $R_{DS(on)}=26.5\text{m}\Omega$
MOSFETs S_{c1} - S_{c14}	IRF7862PbF; $V_{DSS}=30\text{V}$, $I_D=21\text{A}$; $R_{DS(on)}=3.3\text{m}\Omega$

$$\begin{cases} \frac{1}{2} L_1 [i_{L1}(t_9)]^2 > \frac{1}{2} (C_{oss1} + C_{oss2}) V_{C1}^2 \\ \frac{1}{2} L_1 [i_{L1}(t_3)]^2 + \frac{1}{2} L_2 [i_{L2}(t_3)]^2 > \frac{1}{2} (C_{oss3} + C_{oss4}) V_{C1}^2 \end{cases} \quad (19)$$

where C_{oss1} - C_{oss4} are the junction capacitors of S_1 - S_4 .

$i_{L1}(t_3)$, $i_{L1}(t_9)$ and $i_{L2}(t_3)$ are the peak currents of L_1 and L_2 , and the junction capacitors of the switches are commonly small. Therefore, the conditions in (19) are always satisfied, and S_1 and S_4 can achieve ZVS in the full load range.

2) *ZVS of S_5 and S_6* : Similarly, after S_6 is turned OFF, S_5 will not be turned on immediately. During $[t_1-t_2]$, i_{L2} freewheels through the body diode of S_5 , thereby achieving the ZVS of S_5 at t_2 . The operation principle during $[t_5-t_6]$ is the same as that during $[t_1-t_2]$, where the ZVS operation of S_6 can be realized. Therefore, the ZVS conditions of S_5 and S_6 in boost mode are:

$$\begin{cases} i_{L2}(t_5) = I_{L2_Boost} = \frac{-NV_{LV} D_2 \varphi}{L_2 f_s (1-2D_2)} < 0 \\ i_{L2}(t_1) = I_{L2_Boost} + \frac{\varphi T_s N V_{C2}}{L_2} = \frac{(1-D_2) N V_{LV} \varphi}{L_2 f_s (1-2D_2)} > 0 \end{cases} \quad (20)$$

Since the value of φ is commonly positive during boost mode, the ZVS conditions in (20) are always satisfied. Thus, both S_5 and S_6 can achieve ZVS operation from no load to full load.

3) *ZVS of S_3* : When S_4 is turned OFF at t_{11} , i_{L2} freewheels through the body diode of S_3 during the dead time. However, when S_3 is turned ON, i_{L1} flows through S_3 in the opposite direction to i_{L2} . To fully realize the ZVS of S_3 and prevent its junction capacitor from recharging, it is necessary to ensure that the discharge current of C_{oss3} at t_{12} is greater than the charge current. This condition can be expressed as

$$-N i_{L2}(t_{12}) - i_{L1}(t_{12}) > 0 \quad (21)$$

By combining (8), (11) and (21) and assuming K_{ZVS} is the equivalent ZVS coefficient, the ZVS condition of S_3 in boost mode can be calculated by

$$K_{ZVS} = \frac{V_{LV} [\varphi L_1 N^2 (\varphi - 2D_2^2) + L_2 D_2 (1-2D_2)^2]}{2L_1 L_2 f_s (1-2D_2)^2} > 0 \quad (22)$$

By substituting the parameters in Table I into (22), the ZVS range of S_3 can be obtained. The results show that S_3 can achieve ZVS from no load to 8% load and 80.7% load to full load.

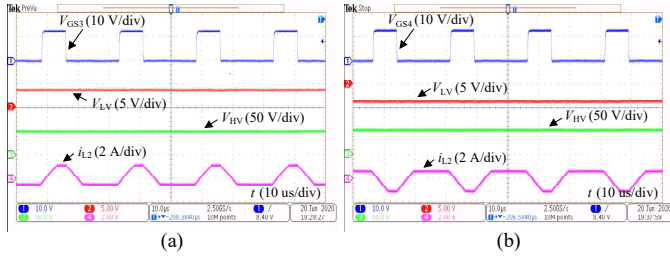


Fig. 8 Equalization waveforms of overcharged cells. (a) odd-numbered cell. (b) even-numbered cell.

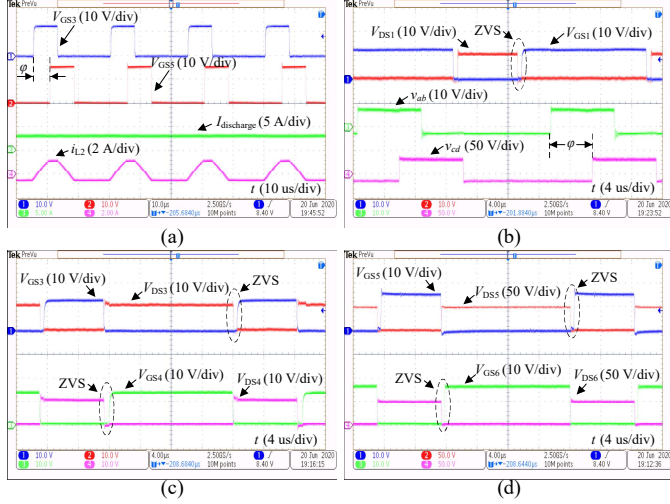


Fig. 9 Experimental waveforms of the proposed ICBDDC in boost mode. (a) V_{GS3} , V_{GS5} , $I_{discharge}$ and i_{L2} . (b) ZVS waveforms of S_1 and the transformer voltage waveforms. (c) ZVS waveforms of S_3 and S_4 . (d) ZVS waveforms of S_5 and S_6 .

IV. EXPERIMENT EVALUATION

To verify the operation principle and equalizing performance, an equalization experiment is performed on a battery string consisting of 13 series-connected 3.5 Ah cells, and the voltage ranges of the single battery and battery string are 3V-4.2V and 39V-54.6V, respectively. The cell voltages are monitored in real time by the battery stack monitor LTC6812 and transmitted to the controller TMS320F28335 through data communication. In addition, the switch matrix gate driver EMB1428Q is required to expand the PWM ports of the controller, and each port is connected with an opt-coupler to increase the driving force of the PWM signals. Moreover, according to the working principle described above, the proposed converter has two control variables D_2 and ϕ . With the proposed modulation strategy, setting a voltage closed-loop to adjust the control variable D_2 can achieve the required voltage gain, and then setting a current closed-loop to adjust the phase-shift duty cycle ϕ can control the power flow of the converter.

A. Experimental Waveforms of the Proposed ICBDDC

When a single cell is overcharged, the converter is operated in boost mode to release the energy stored in the unbalanced cell to the entire battery string. Fig. 8 (a)-(b) show the equalization waveforms of overcharged odd-numbered and even-numbered cells, respectively, which exactly correspond to the operating waveforms in Fig. 3 (a)-(b). As seen, the proposed converter achieves the equalization of cells with different voltage polarities, and realizes a 13-times voltage conversion.

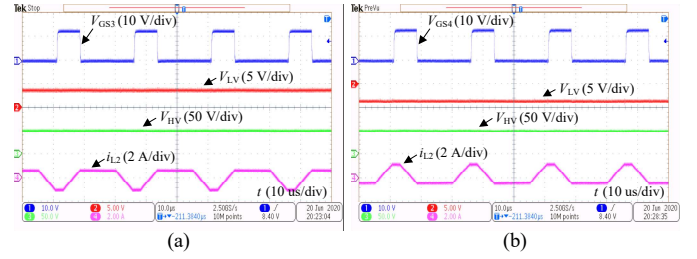


Fig. 10 Equalization waveforms of undercharged cells. (a) odd-numbered cell. (b) even-numbered cell.

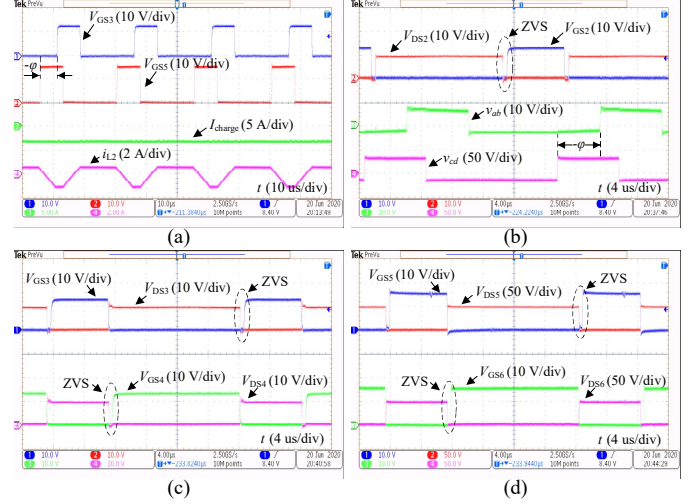


Fig. 11 Experimental waveforms of the proposed ICBDDC in buck mode. (a) V_{GS3} , V_{GS5} , I_{charge} and i_{L2} . (b) ZVS waveforms of S_2 and the transformer voltage waveforms. (c) ZVS waveforms of S_3 and S_4 . (d) ZVS waveforms of S_5 and S_6 .

To be unified with the previous description, the equalization of odd-numbered cells is also analyzed as an example. Combined with Fig. 9 (a)-(b), under the phase-shifted PWM modulation strategy, the phase-shift duty cycle ϕ between V_{GS3} and V_{GS5} is approximately 0.21. At this time, the equalizing discharging current $I_{discharge}$ is 3A, and the converter is operated in a state close to full load. The voltages v_{ab} and v_{cd} on the primary and secondary sides, respectively, are shown in Fig. 9(b), and their voltages correspond to a transformer turn ratio of 1:5. According to the ZVS conditions and Fig. 9 (b), it can be seen that before S_1 is turned on, the current i_{L1} freewheels through the body diode of S_1 to reduce its terminal voltage V_{DS1} to zero so as to realize the ZVS of S_1 . Moreover, several similar processes occur in Fig. 9 (c)-(d), which means that before the switches S_3 - S_6 are turned on, their corresponding terminal voltages V_{DS3} - V_{DS6} have all dropped to zero, so that the ZVS of S_3 - S_6 can be successfully realized.

When a cell is undercharged, the converter is operated in buck mode to release the energy stored in the entire battery string to the unbalanced cell. Fig. 10 (a)-(b) show the equalization waveforms of undercharged odd-numbered and even-numbered cells, respectively, which completely correspond to the operating waveforms in Fig. 3 (c)-(d). The experimental results show that the converter implements the equalization of cells with different voltage polarities, and realizes the required buck conversion gain according to the set duty cycle. The experimental waveforms are consistent with the theoretical analysis in buck mode.

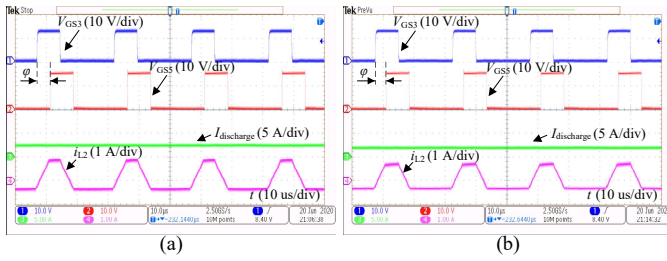


Fig. 12 Experimental waveforms with different equalizing discharging current in boost mode. (a) $I_{\text{discharge}}$ is 2.5A. (b) $I_{\text{discharge}}$ is 2A.

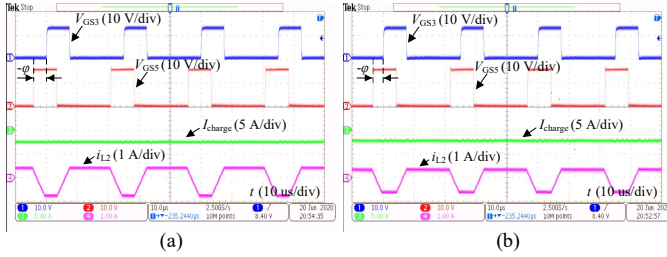


Fig. 13 Experimental waveforms with different equalizing charging current in buck mode. (a) I_{charge} is 2.5A. (b) I_{charge} is 2A.

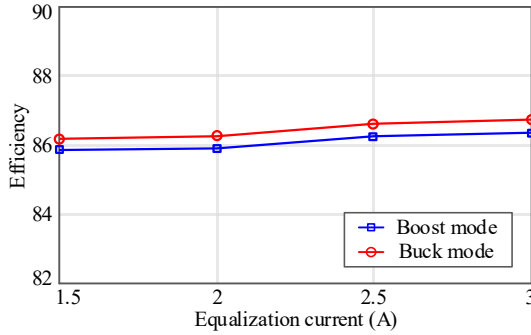


Fig. 14 Efficiency curves with different equalization current.

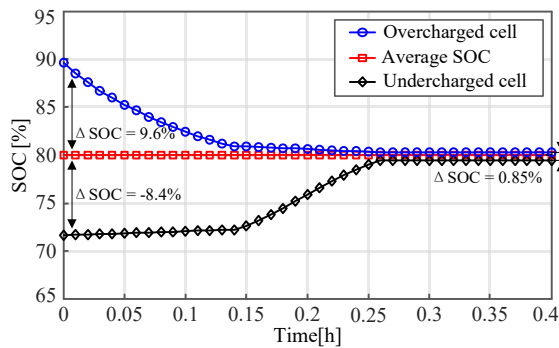


Fig. 15 Results of equalization for lithium-ion battery cells.

It can be seen from Fig. 11 (a)-(b) that the gate drive signal V_{GS5} leads V_{GS3} . At this time, the phase-shift duty cycle ϕ between V_{GS3} and V_{GS5} is close to -0.21, the equalizing charging current I_{charge} is 3A, and the converter works in a state close to full load. According to the waveform of the current i_{L2} , under the phase-shifted PWM control, the peak value of the transformer current is small, so that the transformer loss is accordingly reduced. Fig. 11(b)-(d) shows the ZVS waveforms of the switches, which validates the theoretical analysis of ZVS in buck mode.

In the late stage of the equalization process, the equalizing current should be decreased to prevent overcharging or

undercharging of the equalized battery. Fig. 12 shows the experimental waveforms with different equalizing discharging currents in boost mode. With a decrease in the phase-shift duty cycle ϕ , the output power and the discharging current $I_{\text{discharge}}$ of the overcharged cell decrease gradually. Fig. 13 shows the experimental waveforms with different equalizing charging currents in buck mode. Since $\phi < 0$ in this mode, with an increase in ϕ , the equalizing charging current I_{charge} of the undercharged cell decreases accordingly. The experimental results validate the feasibility and effectiveness of the phase-shifted PWM modulation strategy, and the relationship between the equalization current and the phase-shift duty cycle ϕ is consistent with the theoretical analysis.

Furthermore, Fig. 14 shows the efficiency curves of boost mode and buck mode when the equalization current is 1.5A to 3A. It can be seen that the conversion efficiency at full load measured in the experiment is 86.3% in boost mode and 86.8% in buck mode. Note that the ZVS range of S_3 in boost mode and S_4 in buck mode is 80.7% load to full load. Therefore, the efficiency when the equalization current is 2A is lower than that when the equalization current is 2.5A, which also verifies the correctness of the soft-switching analysis.

B. Equalization Experimental Results

When equalizing a battery string, the controller estimates the state of charge (SOC) value of each cell based on the battery voltage monitored by LTC6812 and the current monitored by the current sensor, and calculates the difference between the SOC of each cell and the average SOC of the battery string. According to the SOC difference value (ΔSOC), the cells that need to be balanced are arranged. When $\Delta\text{SOC} > 2\%$, the overcharged cell will release energy with a preset discharging current. When $\Delta\text{SOC} < -2\%$, the undercharged cell will receive energy with a preset charging current. Note that overcharged cells should be prioritized for equalization, because overcharging tends to cause damage of battery pack.

To validate the performance of the equalizer under the condition of a serious unbalance, a cell is charged to 9.6% higher than the average SOC and another cell is discharged to 8.4% lower than the average SOC before the experiment began. According to the equalization principle, the maximum equalizing charging current and discharging current are both set to 3A, and the overcharged cell starts to be equalized first. As shown in Fig. 15, the equalization of the overcharged cell is completed after 8.4 minutes, and the equalization of the undercharged battery is completed after 7.2 minutes. However, the SOC difference in a practical system is not large. When the SOC difference is reduced, the equalization time will be reduced. The results indicate that the proposed method has an excellent individual equalizing performance with a fast time and can quickly and accurately equalize an unbalanced cell.

C. Comparison and Analysis

To validate the obvious performance enhancement of the proposed equalizer, a comprehensive and systematic evaluation is conducted between the proposed method and other conventional centralized equalization methods. As described in Table II, the performances are evaluated in terms of component count, costs, size/weight, impact on state-of-health (SOH), modularity, conversion efficiency and control complexity.

TABLE II
PERFORMANCE COMPARISON OF CENTRALIZED CHARGE EQUALIZATION SYSTEMS FOR BATTERY STRING CONSISTING OF N CELLS

Topology		Proposed equalizer	Reference [26]	Reference [25]	Reference [23], [24]	Reference [21], [22]
No. of	MOSFETs	$2(N+1)+6$	$2(N+1)+8$	$2(N+1)+8$	$2(N+1)+12$	$4N+2$
	Gate driver ICs	$N+7$	$N+9$	$N+9$	$N+13$	$2N+2$
	Transformers	1	1	1	1	2
	Inductors	2	2	1	1	0
	Capacitors	6	5	3	2	2
	Diodes	0	2	0	0	2
Costs (\$) when the number of cells is 13	MOSFETs	68	72	72	80	108
	Gate driver ICs	30	33	33	39	42
	Transformers	5	5	5	5	10
	Inductors	4	4	2	2	0
	Capacitors	9	7.5	4.5	3	3
	Diodes	0	4	0	0	4
Total		116	125.5	116.5	129	167
ZVS operation in Boost mode		Yes	Yes	No	No	No
ZVS operation in Buck mode		Yes	Yes	Yes	No	No
Voltage spike caused by leakage inductance		No	No	Yes	Yes	Yes
Size / weight		Low	Medium	Low	Medium	High
Impact on state-of-health (SOH)		Excellent	Good	Excellent	Excellent	Satisfactory
Modularity		Excellent	Good	Good	Good	Satisfactory
Control complexity		Good	Satisfactory	Excellent	Satisfactory	Satisfactory
Conversion efficiency		High	High	Medium	Medium	Low

Component cost per unit (\$): MOSFET (2), Gate driver ICs (1.5), Transformer (5), Inductor (2), Capacitor (1.5), Diode (2) [27]-[29].

The components in the centralized equalization system include switches, driver ICs, transformers, inductors, capacitors, and diodes. Compared with other centralized equalizers, the proposed method has the least number of switches and driver ICs, which significantly reduces the number of components. In addition, the costs of each equalizer can be quantitatively compared by calculating the sum of prices of all components [27]-[29], and the size/weight can also be determined according to the number and volume of components.

“Impact on state-of-health” is evaluated by the influence of the equalizer on the battery lifetime and SOH. The equalization current of the equalizer proposed in [21], [22] is discontinuous and the peak value is large, which may cause potential damage to the cell. The equalizer in [26] makes the equalization current continuous by setting an additional filter circuit, but this will increase the costs and losses. Furthermore, other equalizers can make the equalization current work in a continuous and controllable state, so that the negative influence of the equalizer on the battery is minimized.

The equalization architecture used in [21], [22] contains a large number of bidirectional switches in the switch array. In [23]-[26], the number of bidirectional switches is reduced by setting polarity switches. However, the coordination between these two parts of switches is an issue that cannot be ignored. The proposed method significantly reduces the number of switches in the switch array through the integrated cascade equalization architecture. Moreover, due to the high-voltage conversion ratio of the converter, the number of cells that can

be contained in each module is greater when modularized. Therefore, this method is more suitable for the equalization of long battery strings and has the advantage of modularity.

“Control complexity” is evaluated by the complexity of control circuit and control strategy. Each cell of the equalizer in [21], [22] contains two separate bidirectional switches, which leads to an increase in the number of driving circuits and increases the control complexity. Likewise, the bidirectional full-bridge converter used in [23], [24] has a large number of power switches, which also increases the demand for driving circuits. The design and implementation of the quasi-resonant operation in [26] is complicated, thereby the control strategy of this method is more complicated. The proposed equalizer significantly reduces the number of switches and driving circuits in the centralized equalization system. Combined with the proposed phase-shifted PWM control strategy, this method has lower control complexity and higher practicability.

The conversion efficiency is determined by the loss of the switch array and the converter. According to the loss model in [29]-[30], the losses of the entire equalization system mainly include switching loss, conduction loss, transformer loss, inductance loss and diode loss. To compare the efficiency fairly, a prototype of each equalizer is designed according to the same specifications in Table I, so that the loss numerical values of various equalizers at full load can be listed in Table III and the losses distribution and comparison of them can be plotted in Fig. 16. As seen, the ZVS implementation of the converters in [21]-[25] has limitations, and these converters cannot avoid

TABLE III
LOSS NUMERICAL VALUES OF VARIOUS EQUALIZERS IN BOOST MODE AND BUCK MODE

Topology	Proposed equalizer	Reference [26]	Reference [25]	Reference [23], [24]	Reference [21], [22]
Losses in Boost mode SOC = 89.6% $I_{\text{discharge}} = 3\text{A}$	Switching	0.179	0.055	0.321	0.408
	Conduction	0.199	0.365	0.188	0.279
	Transformer	0.492	0.651	1.005	1.097
	Inductor	0.782	0.527	0.484	0
	Diode	0	0.263	0	0.199
Total (W)	1.652	1.861	1.998	1.926	1.983
Losses in Buck mode SOC = 71.6% $I_{\text{charge}} = 3\text{A}$	Switching	0.178	0.087	0.156	0.158
	Conduction	0.202	0.273	0.198	0.202
	Transformer	0.516	0.664	1.013	1.112
	Inductor	0.817	0.534	0.485	0
	Diode	0	0.275	0	0.899
Total (W)	1.713	1.833	1.852	1.913	2.371

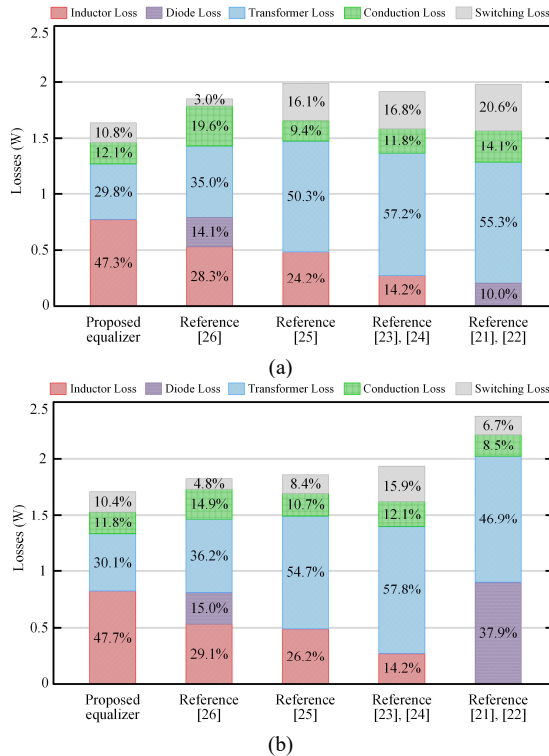


Fig. 16 Losses distribution and comparison of various equalizers. (a) Equalization in boost mode. (b) Equalization in buck mode.

voltage spikes caused by leakage inductance, so the switching loss of these equalizers are relatively large. In addition, the converters in [21]–[26] require a large transformer volume and turn ratio to achieve a high voltage gain, which increases the transformer loss. The proposed converter reduces the number of switches in the entire equalization system and realize ZVS in both boost mode and buck mode. Thus, the conduction loss and switching loss of these two equalizers are both small. Furthermore, the integrated cascaded structure also enables the converter to obtain a high voltage gain, thus greatly reducing the transformer loss.

V. CONCLUSION

This paper presents a novel ICBDDC for optimizing a centralized charge equalization system. The operation principle, the parameter design and ZVS analysis, the experimental evaluation, and the comparative studies with conventional methods are introduced. For the proposed ICBDDC, a simple and practical phase-shifted PWM modulation strategy is proposed, which not only ensures bidirectional controllable power transmission but also improves the conversion efficiency. In addition, the converter also avoids voltage spikes caused by leakage inductance and saturation of the transformer core caused by magnetic bias. Finally, equalization experiments on 13 series-connected battery cells are conducted, and the performances of various equalizers are comprehensively compared. The comparative analysis and experimental results show that the proposed novel ICBDDC obtains outstanding performance in terms of equalization efficiency, modularity, impact on SOH and control complexity, and addresses the dilemma of achieving equalization with low cost and small size for a long series battery string.

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