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Source-Side Virtual *RC* Damper-Based Stabilization Technique for Cascaded Systems in DC Microgrids

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***Abstract*—Cascaded connection of power converters is a dominant connection form in DC microgrids. In such systems, despite the possible instability caused by the impedance interactions between the individually designed converters, tightly regulated load converters acting as constant power loads (CPLs) tend to destabilize the system owing to their negative resistance characteristics. Hence, this paper proposes a new virtual series *RC* damper in parallel with the source-side converter's capacitor without compromising the load's dynamic performance. Using this design-oriented active damping method, which utilizes a simple control structure with a more straightforward tuning of the control parameter, the stability and performance of the system are guaranteed. The feasibility and robustness of the suggested active stabilization idea against unanticipated variations in input voltage amplitude, and CPL power rating (load changes) as well as step changes in output voltage reference, are also authenticated. The control and operation principles, as well as the circuit physical meaning realized by the presented technique for three cascaded systems comprising the basic DC/DC converters feeding CPLs, are theoretically analyzed. Simulation and experimental results are provided to validate the effectiveness of the proposed active stabilizer.**

***Index Terms*—Active damping, constant power load (CPL), cascaded DC systems, virtual series *RC* damper, stability.**

I. Introduction

NOWADAYS, multi-converter DC distributed power system without connecting to the utility grid is widely used in such applications as more electric aircraft, electric vehicles, marine, and stand-alone DC microgrids (MGs), thanks to the high efficiency, high power transfer capacity, modularity, and simple control structures [1], [2]. As seen in Fig. 1, in DC MGs, from the source-side, the power sources inject energy into the intermediate DC bus via their respective converters to maintain a regulated voltage on it; on the other, from the load-side, besides the resistive loads, some loads draw tightly regulated outputs from the DC bus via the load converters. Hence, the cascaded interconnection of the converters is the most basic configuration for such a system [3]–[6]. A basic model of such structure in DC MGs is shown in Fig. 2.

Though in such a system, each converter is individually well-designed to be stable, the instability problem in the system level is still a great concern due to the interactions between the converters as well as the inherent nonlinearity of the self converter [7]. The impedance interactions issue was first addressed by the Middlebrook stability criterion [8], which is also known as impedance-based stability analysis and is suitable for small-signal analysis. However, this impedance-ratio-based stability analysis has a conservative attitude because of the variety of options for how to apply it to the design of subsystems in DC MGs, though it is well accepted by the industrial and academic societies. Moreover, in such cascaded systems, when the control loop gain and bandwidth of the load converter is sufficiently higher than that of the

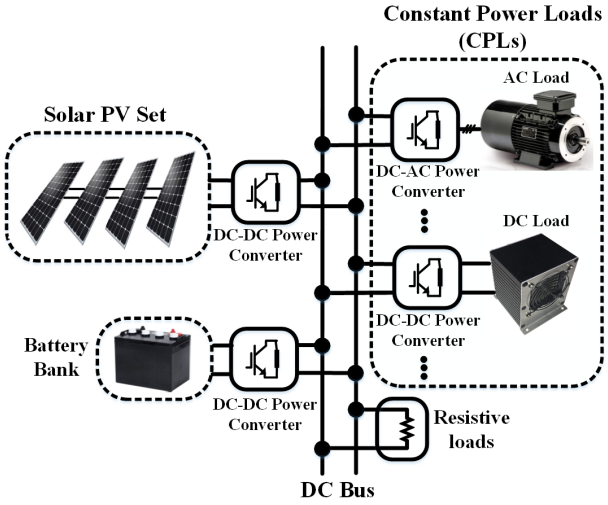

Fig. 1. Typical structure of DC MGs.

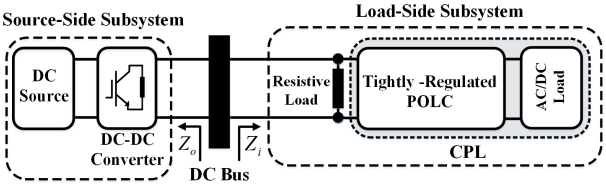

Fig. 2. A basic model of a cascaded system.

source converter, it is tightly controlled in a way as to maintain constant power for the load [9]. Accordingly, it behaves like a constant power load (CPL) for its upstream circuit. CPLs tend to destabilize system due to their negative resistance feature that results in reduced system damping, degraded stability margins, and significant voltage oscillations or even voltage collapse on the DC bus [9]. Thus, overcoming the CPL instabilities in the structure shown in Fig. 2 is one of the most important issues in achieving a stable DC MG. Hence, the adopted control method should be robust enough to ensure system stability and performance.

Many techniques have been performed to eliminate CPL instability in cascading systems based on the different stability criteria [2], [4], [5], [10]–[14]. The underlying idea behind these techniques is to improve the system damping by some modifications that can be generally classified into three compensation regions of system-level, namely, source-level, load-level, or using additional circuits in the intermediate-level. These modifications can be done in system hardware as passive damping (PD) methods and in their control loops as active damping (AD) approaches. PD solutions can be implemented by adding passive elements to the system, including resistance, resistance-inductance, and resistance-capacitance. The weaknesses of these approaches include increasing size, cost, weight, power losses, and reducing the system bandwidth,

which are detrimental to system efficiency. In contrast, the AD techniques introduce sufficient damping into the system by the dynamic modifications in the control structure of the source- or load-side [4]–[6], [15]–[20] [21], [22]. Furthermore, an ancillary circuit can also be embedded in the intermediate bus to emulate an adaptive variable virtual impedance or to inject a compensating current [3], [23]. The ultimate goal of these methods is to modify Z_i or/and Z_o for satisfying the stability criteria and consequently, stabilizing the DC cascaded systems. In source-side compensators, Z_o is remedial shaped by the increasing control loop bandwidth of the source-converter [4], or by applying an auxiliary damping loop [5], [15]–[19]. However, when the CPL's upstream circuit is uncontrollable, compensation at the load- and intermediate-levels is suggested as two alternative solutions. In load-side compensation methods [6], [20], Z_i can be modified by injection of power or current stabilizer signal into the CPL control loops. Nevertheless, the additional stabilizer loop dynamics may adversely impact the CPL control loops and thereby jeopardize the load performance [9], [24]. Accordingly, source-side stabilization methods are usually more preferred over the load-side AD techniques [19]. In auxiliary circuit-based approaches [3], [23], a shunt active damper is connected between the source and load subsystems to reshape Z_i or/and Z_o. Although these methods maintain modularity of the system, they result in increased costs, power losses, and system complexity. Generally speaking, many of the impedance stability-based contributions have sophisticated corrective control structure with different levels of conservatism in the design and realization of the stability criterion, as well as their effectiveness versus unforeseen events has not been assessed holistically.

Prompted by these challenges, a new stabilizer control approach based on a virtual series *RC* damper is proposed in parallel with the source-side converter's capacitor for overcoming CPL instability. This stabilizing branch is actively inserted into the output of the source-side circuit by feeding back the related converter's capacitor current through a well-designed proportional coefficient. Accordingly, practical constraints such as weight saving and low power dissipation are preserved, which are critical factors for on-board DC MGs. Using this design-oriented technique, the stability and performance of the DC/DC power converter systems loaded by CPLs in DC MGs are guaranteed. The intuitive circuit physical meaning realized by the proposed scheme is also theoretically proved. The effectiveness and robustness of the presented method have been verified by laboratory tests and simulation results. The main advantages and novel contributions of the presented active stabilization technique are outlined in the following, which comprehensively cover the shortcomings of the existing methods and exhibit more excellent performance in comparison with them.

1) Simple Control Strategy with Ease in Setting the Control Parameter: The active stabilizer technique is implemented for the DC cascaded conversion systems comprising a source converter loaded by a resistive load and multiple CPLs based on the simple control scheme with an easy adjustment of a control parameter. By taking advantage of these merits, the feasibility of developing this control approach for more complex DC MGs with multiple sources can be easily explored.

2) Operational Capability with High Flexibility: This outstanding performance feature can be clearly understood since the proposed control approach is applicable for the three main DC/DC converter systems loaded by CPLs with a similar control realization and only with different analytical concepts.

3) Without Affecting the Dynamic Performance of the Load Converter: It is an important and vital factor to authenticate the effectiveness of a control method in compensating exclusively for the undesirable effect without adversely affecting other favorable conditions of the system. Since this stabilizer control scheme is realized by modifying the source converter's voltage control signal (direct control of the converter's switch duty cycle), the CPL destabilizing effect is eliminated without affecting the dynamic performance of the load converter.

4) High Robustness Against input Voltage Variation, CPL Power Rating Change (Equivalent Load Variation), and Step Change in Output Voltage Reference: The active stabilizer scheme exhibits high robustness with the acceptable transients and fast dynamic responses against possible unpredictable variations in the network without requiring new information of them.

The rest of the paper is organized as follows. The stability of the cascaded systems comprising the basic DC/DC converters powering CPLs is separately analyzed based on their small-signal averaged equivalent circuits in section II. In section III, first, the proposed stabilizer for a buck converter with CPLs is explained in detail. Second, to verify its effectiveness, simulation and experimental results are presented. Subsequently, the presented AD scheme is performed on the boost and buck-boost converters feeding CPLs along with complete descriptions of their control performance theory in Sections IV, individually. Then, simulation and experimental results are included in the same section to validate the theoretical findings and efficiency of the active stabilization idea on these cascaded systems. Finally, this paper is concluded in Section V.

II. Modeling and Stability Analysis of DC/DC Power Converter Systems Loaded by CPLs

In this section, by considering the system dynamics, the stability of the cascaded systems consisting of the basic DC/DC converters loaded with CPLs is separately analyzed. Toward this end, the small-signal averaged equivalent circuit of the mentioned systems is derived via the averaged switch modeling technique, wherein the averaging and linearization are executed directly on the converter circuit rather than its state equations [25]. It should be noted that all the closed-loop controlled basic DC/DC converters feeding CPL and operating in continuous conduction mode (CCM) are unstable under both voltage mode control (VMC) and current mode control (CMC) [9]. Hence, due to the simplicity in design and implementation as well as the evaluation of the proposed stabilizer in the worst operating conditions from the stability perspective, the considered source-side converters operate in CCM and under VMC. However, the presented stabilization scheme can also be implemented for DC/DC converters operating in CMC.

A. Buck Converter Feeding CPL Under VMC

Fig. 3 shows a buck converter loaded by CPL. The CPL has been replaced by its small-signal model comprising a negative

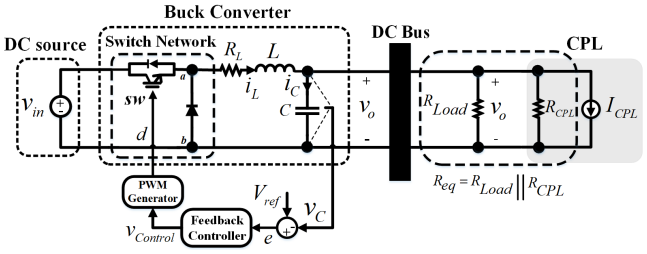

Fig. 3. A DC/DC buck converter loaded by CPL under VMC.

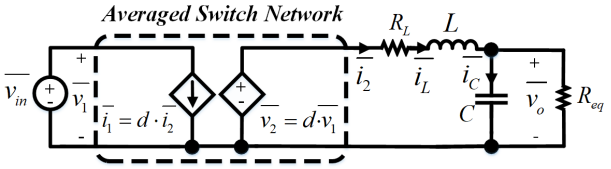

Fig. 4. The averaged time-invariant network of Fig. 3 (Step 1).

resistance ($R_{CPL} = -V^2/P$) in parallel with an independent current source ($I_{CPL} = 2P/V$), where P and V are the rated power and the terminal voltage of the CPL for a given operating point, respectively. I_{CPL} does not affect the system stability, however, R_{CPL} attenuates the system damping and tends to destabilize the system. L and C are the inductor and capacitor of the source-side converter, R_L is the inductor's intrinsic resistance, V_{in} is the input voltage, R_{eq} is the small-signal equivalent load resistance. The linearized circuit-averaged model of the cascaded system is firstly extracted. For this purpose, averaged switch modeling technique is applied to the system shown in Fig. 3, with two subintervals during each switching period, T_{sw}:, ($d.T_{sw}$: (*SW*: ON and Diode: OFF)) and (($(1-d).T_{sw}$: (*SW*: OFF and Diode: ON)), where d is defined as the switch duty cycle. The implementation procedure of this technique is summarized below.

Step 1,: The switch network considered in Fig. 3 is defined as a two-port network with four terminal variables, namely, v_1, i_1, v_2, and i_2. Two of them can be arbitrarily selected as the independent inputs (v_1, i_2) and the remaining two quantities are then accounted for as dependent outputs (i_1, v_2). The only task required in this step is to compute the average values of the dependent sources in terms of the independent quantities by following the switching status of two subintervals during each T_{sw}, where they are exhibited with $\overline{x}$ (see Fig. 4).

Step 2,: Assuming that the averaged system parameters are equal to the respective dc values, X, plus small ac variations, $\hat{x}$, where the magnitude of the ac terms is much smaller than the dc terms. As seen in Fig. 5, by inserting these perturbed signals in the network represented in Fig. 4, and discarding the second-order terms derived by multiplication of ac quantities, small-signal averaged equivalent circuit is eventually obtained. Finally, by neglecting the dependent current source effect and transfer of the input voltage source to the right-side of the ideal transformer, the simplified small-signal equivalent circuit of a buck converter with CPL can be achieved (see Fig. 5).

As a result, the small-signal control-to-output transfer function and its associated poles can be derived as (1) and (2), respectively. Given that $R_{eq} < 0$ and $|R_{eq}| > R_L$ (actual circumstances), the system will become unstable due to the existence of a complex-conjugate pole pair in the right half-plane (RHP). Therefore, in this case, system stability can be achieved through the realization of inequality (3) derived by applying the Routh's stability criterion for (1).

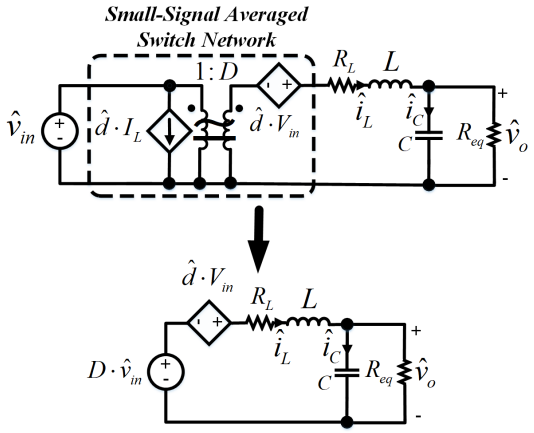

Fig. 5. Simplified small-signal averaged equivalent circuit of Fig. 3. (Step 2).

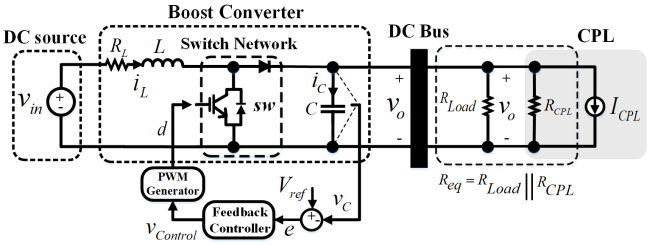

Fig. 6. A DC/DC boost converter loaded by CPL under VMC.

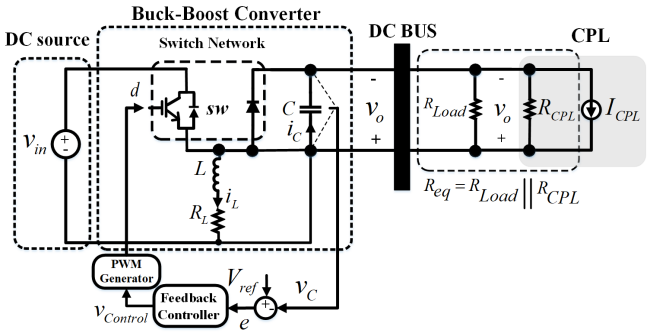

Fig. 7. A DC/DC buck-boost converter with CPL under VMC.

$$\frac{\hat{v_o}}{\hat{d}} = \frac{V_{in}}{LC\cdot s^2+\left(R_LC+\frac{L}{R_{eq}}\right)\cdot s+\left(1+\frac{R_L}{R_{eq}}\right)}. \quad (1)$$

$$P_1, P_2 = \frac{-\left(\frac{L}{R_{eq}}+R_LC\right)\pm\sqrt{\left(\frac{L}{R_{eq}}+R_LC\right)^2-4LC\left(1+\frac{R_L}{R_{eq}}\right)}}{2LC}. \quad (2)$$

$$R_LC > \frac{L}{|R_{eq}|}. \quad (3)$$

B. Boost and Buck-Boost Converters Feeding CPL Under VMC

Figs. 6 and 7 illustrate the boost and buck-boost converters loaded with CPL, respectively. A similar implementation procedure of the averaged switch modeling technique is performed like steps 1 and 2 for achieving their simplified small-signal averaged equivalent circuits (see Figs. 8(a) and 8(b)). Their control-to-output transfer functions can be obtained as (4) and (5), respectively, and the poles are also gained by (6). By examining the poles' location, given that $R_L < |R_{eq}| \cdot D'^2$

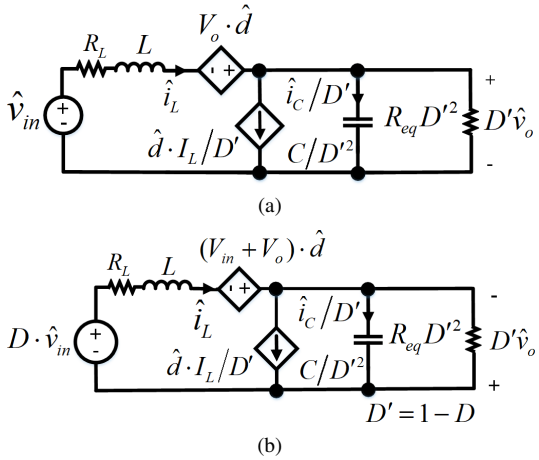

Fig. 8. Simplified small-signal averaged equivalent circuit. (a) Boost converter. (b) Buck-boost converter.

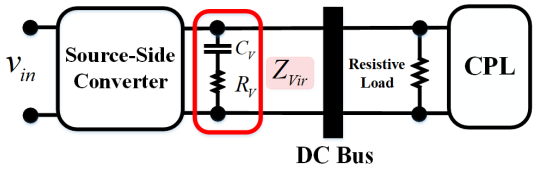

Fig. 9. Concept of the proposed AD control strategy.

and $R_{eq} < 0$; similar to the buck converter, the stability condition for these systems can be fulfilled by satisfying (3).

$$\frac{\hat{v_o}}{\hat{d}} = \frac{D^{'}V_o - I_L(R_L+sL)}{LC\cdot s^2+\left(R_LC+\frac{L}{R_{eq}}\right)\cdot s+\left(D'^2+\frac{R_L}{R_{eq}}\right)}. \quad (4)$$

$$\frac{\hat{v_o}}{\hat{d}} = \frac{D^{'}(V_{in}+V_o) - I_L(R_L+sL)}{LC\cdot s^2+\left(R_LC+\frac{L}{R_{eq}}\right)\cdot s+\left(D'^2+\frac{R_L}{R_{eq}}\right)}. \quad (5)$$

$$P_1, P_2 = \frac{-\left(\frac{L}{R_{eq}}+R_LC\right)\pm\sqrt{\left(\frac{L}{R_{eq}}+R_LC\right)^2-4LC\left(D'^2+\frac{R_L}{R_{eq}}\right)}}{2LC}. \quad (6)$$

Obviously, for a specific CPL and restriction on the R_{Load} control, R_{eq} cannot be changed flexibly. Therefore, it can be concluded that to meet (3), one of the LC filter parameters should be properly set, that is, either increasing R_L, or decreasing L, and or increasing C. Usually, L is selected to satisfy other design requirements such as CCM, and desired inductor current ripple amplitude [25], which does not coincide with the stability condition mentioned for the inductor value (see (3)). Besides, the actively increasing R_L cannot be a suitable solution for suppressing CPL instabilities in various loading conditions [15]. As a general outcome, the parameter that can be set more freely is C. However, increasing C alone ensures system stability at the expense of slowing down the system dynamic response. Accordingly, as shown in Fig. 9, to guarantee the system stability, improved dynamic response, and increased damping, the virtual insertion of a series *RC* damper at the source's converter output will be an excellent choice.

III. Proposed Virtual Series *RC* Damper for Buck Converters Loaded by CPLs

In this section, firstly, how to influence and design the proposed AD technique for stabilizing buck converter system feeding CPL is described in detail. After that, the effectiveness of the presented method is validated by the simulation and

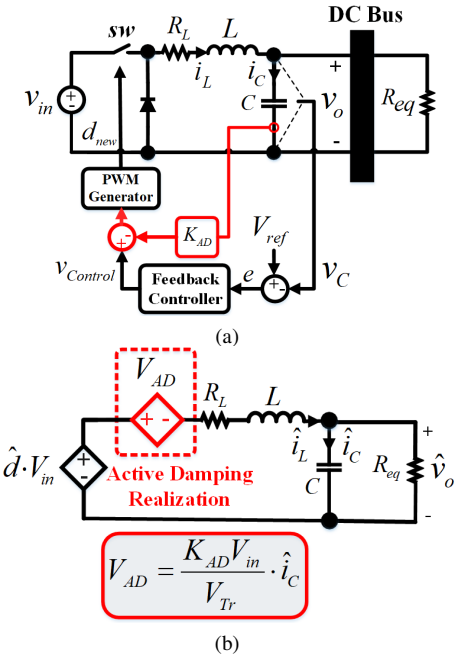

Fig. 10. AD applied to the buck converter system loaded by CPL. (a) Circuit schematic. (b) Modified small-signal averaged equivalent circuit.

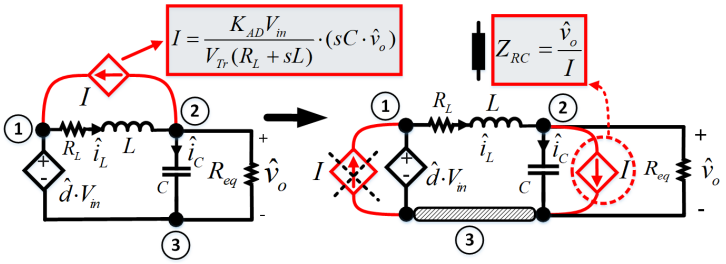

Fig. 11. Another analytical interpretation of Fig. 10(b).

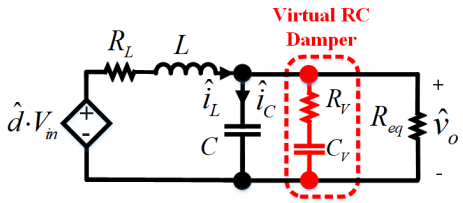

Fig. 12. The circuit physical meaning of the proposed AD applied to the buck converter loaded by CPL.

experimental results comprehensively, in which, its robustness against sudden changes in input voltage amplitude and CPL value is also evaluated. Meanwhile, to show the superiority of our contributions, comparisons have been performed with the AD scheme offered by [15] and PI + designed D-based control method, whose are close to ours.

A. Description of the Circuit Physical Meaning Realized by the Proposed AD Control Scheme

Fig. 10(a) depicts the circuit schematic of the system shown in Fig. 3 considering the presented AD method. This achieved by the proportional feedback of the source converter's capacitor current and subtracting it from the voltage control signal. Whereby, by replacing $\hat{d}-(K_{AD}.\hat{i_c}/V_{Tr})$ instead of $\hat{d}$ in Fig. 5, the simplified small-signal averaged equivalent circuit is modified as Fig. 10(b) by ignoring the ac term of input voltage, where V_{Tr} is the triangular carrier signal amplitude. It can be understood that the applied AD scheme acts as a dependent

voltage source V_{AD} to dynamically modify the converter output voltage for overcoming the CPL's instability effect. It is quite evident from Fig. 10(b), this technique has an interesting circuit physical meaning, which its result is graphically has been illustrated in Fig. 11. This outcome is achieved based on the circuit analysis, which has been summarized step-by-step as follows:

1) *Converting the Thevenin circuit consisting of the voltage source V_{AD} and the impedance $R_L - L$ to the corresponding Norton equivalent circuit.*

2) *Removing the dependent current source, I, between nodes 1 and 2 and moving it from node 2 toward node 3 and finally to node 1.*

At this step, the dependent current source in parallel to the voltage source can be ignored (see Fig. 11).

3) *Converting the dependent current source to an impedance.*

According to one of the efficiently used rules in circuit analysis, which implies that: " *each dependent current source that depends on its voltage can be modeled as an impedance* ", the proposed AD stabilizer scheme introduces a virtual series *RC* damper in parallel with the capacitor (see Fig. 12).

In line with this, R_V and C_V can be readily derived as

$$\frac{\hat{v_o}}{I} = \frac{LV_{Tr}}{K_{AD}CV_{in}} + \frac{1}{s}\left(\frac{R_L V_{Tr}}{K_{AD}CV_{in}}\right) = R_V + \frac{1}{sC_V} \quad (7)$$

B. Selecting an Effective AD Term (K_{AD})

Considering (7), since the effect of C_V is dominant than R_V at around DC frequency, the system's equivalent capacitance can be regarded with a good approximation as $C + C_V$. In this way, as was specified in Section II, by further increasing the system equivalent capacitor (increasing C_V), the damping effect to stabilize the system can be significantly enhanced. It is important to note that for avoiding system response slow down due to increased capacitance alone, the presence of a resistive term is vital. As previously mentioned and is evident from (3), to compensate the CPL instability, the minimum required capacitor is determined as

$$C_{\min} = \frac{L}{R_L|R_{eq}|}. \quad (8)$$

Therefore, K_{AD}, must be selected effectively so that C_V is much larger than $C_{V,min} = (C_{min} - C)$. Hence, given the importance of choosing a proper K_{AD} to eliminate the CPL instability, the design process algorithm is presented below:

Step 1) *Computation of C_{min}.*

Considering the value of $|R_{eq}|$ at the desired output voltage, the needed C_{min} for fulfilling the system stabilizing condition is calculated by (8).

Step 2) *Computation of $C_{V,min}$.*

The minimum value of the desirable virtual capacitor, $C_{V,min}$, is obtained by $C_{min} - C$.

Step 3) *Computation of $K_{AD,min}$.*

$K_{AD,min}$ is then achieved by (9), which incorporates a virtual series *RC* damper ($C_{V,min}$ and $R_{V,max}$) into the system.

Step 4) *Selecting a suitable K_{AD}.*

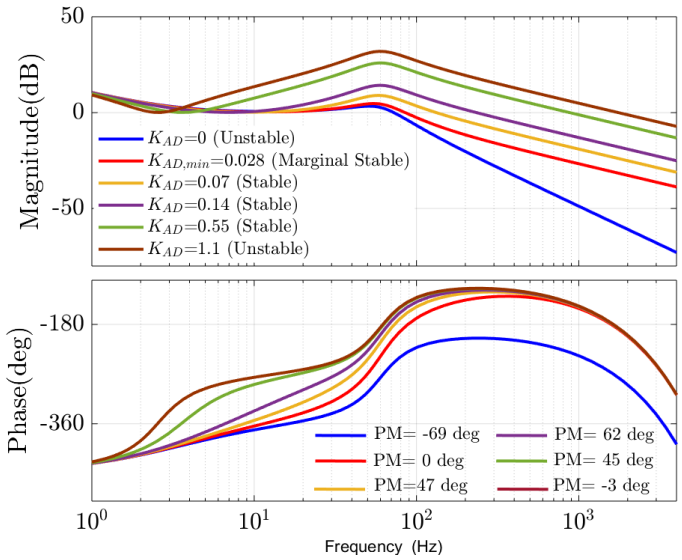

Fig. 13. Bode plot of the open-loop gain of $\hat{v_o}/\hat{d}$ related to the buck converter feeding CPL. Red line: $C_{V,min}$ = 43.2 mF, $R_{V,max}$ = 10.2 Ω; Yellow line: $C_V = 2.5\ C_{V,min}$, $R_V = 0.4\ R_{V,max}$; Purple line: $C_V = 5\ C_{V,min}$, $R_V = 0.2\ R_{V,max}$; Green line: $C_V = 20\ C_{V,min}$, $R_V = 0.05\ R_{V,max}$.

TABLE I
THE PARAMETERS OF THE DC/DC CASCADED CONVERTER SYSTEMS WITH CPL

Source-Side Converter	L	C	R_L	R_{Load}	P_{CPL}	V_{in}	V_o	D
Buck	20 mH	350 μF	45 mΩ	470 Ω	2250 W	200 V	150 V	0.75
Boost	2.4 mH	750 μF	5 mΩ	200 Ω	2250 W	100 V	150 V	0.33
Buck-Boost	2.4 mH	750 μF	5 mΩ	200 Ω	1800 W	120 V	150 V	0.55

The proper choice will be made by a designer to achieve a robust system with effective damping and favorable dynamic performance, as well as keeping the system at a safe phase margin. This shows high flexibility in selecting K_{AD} with an acceptable stable band in accordance with the design requirements.

It should be noted since K_{AD} is inversely dependent on the values of the $|R_{eq}|$ and V_{in}, it must be adjusted much larger than $K_{AD,min}$ to achieve high robustness against descending variations of those factors. This means that only in the initial K_{AD} setting requires to know $|R_{eq}|$ and the input voltage level. Accordingly, with unexpected changes in these factors, the stability can be well ensured only by the effective initial selection of K_{AD} without knowing the new values of them.

$$K_{AD,min} = \frac{C_{V,min}R_L V_{Tr}}{CV_{in}}. \quad (9)$$

It is worth mentioning that the implementation of the proposed method by a digital control system is an important practical issue that must be investigated. In fact, in the digitally-controlled systems, there are two types of delay: the computation delay and the pulse width modulation (PWM) delay [26]. Since the synchronous sampling scheme is commonly used in digitally-controlled systems, the computation delay is considered as one sampling period T_s. On the other hand, the PWM delay is caused by the zero-order-hold *ZOH* effect, which can account for about half of the sampling period. These delay effects are implemented in the control loop model of the digitally-controlled converter at the output corresponding to

the difference between the proposed AD feedback term and the output of the digital PI controller by the cascaded connection of Z^{-1} and *ZOH* blocks. Also, in s-domain, the digital control system delay can be regarded as $e^{-s1.5T_s}$. The delay-induced phase lag effect leads to reduce the phase margin in the high-frequency range. Hence, it should be noted that in the low-frequency range and due to the small amount of T_s, the delay does not affect the virtual *RC* damper introduced by the AD technique, and only can lead to limiting the upper band of K_{AD} to a certain value. Therefore, considering the computational and modulation delays, the Bode diagram of the open-loop gain related to the control-to output of Fig. 10(a) is plotted in Fig. 13, with the parameters given in Table I. For $K_{AD,min}$, the system approaches the marginal stability situation. As seen, with increased K_{AD}, the system's phase margin is enhanced, which indicates an increase in system damping. Whereby, the stability of the closed-loop control system is also ensured. When computational and modulation delays are considered, increasing K_{AD} from a certain amount gradually reduces the system's phase margin, and ultimately, the system becomes unstable. This means that there is a specified band for K_{AD}, [$K_{AD,min}$, $K_{AD,max}$]. $K_{AD,min}$ was achieved through (9) and $K_{AD,max}$ is also defined as the maximum value of the allowable damping gain which can be easily achieved by solving (10) and (11). By substituting the parameters of Table I in the mentioned equations and satisfying them simultaneously, $K_{AD,max} \cong 0.98$ is achieved. As a result, the allowable stable range is determined as [0.028 , 0.98], which well-authenticated the results obtained in Fig.13. It should be noted that the purpose of an efficient design is to achieve a robust system with an effective damping and appropriate dynamic performance, as well as a safe phase margin. In light of this, it is important to select an efficient K_{AD} based on these goals. This indicates high flexibility in choosing an acceptable damping gain rate that can vary depending on the designer's point of view. Since the efficient K_{AD} is definitely much higher than $K_{AD,min}$, the system robustness against sudden changes in input voltage and load will be guaranteed. It can be also found that by decreasing T_s, the stable band of K_{AD} can be extended.

$$\angle\left[e^{-jTsw}G(s)\right] = -\pi, \tag{10}$$

$$\left|e^{-jTsw}G(s)\right| = 1, \tag{11}$$

where

- $G(s) = \frac{\hat{v_o}}{\hat{d}}(s)\,|_{open-loop} = e^{-jT_sw} \cdot [Eq.(1)] \cdot (G_{AD}(s) + G_{PI}(s))$,
- $G_{AD}(s) = s \cdot K_{AD,max} \cdot C$: (The resulting AD gain),
- $G_{PI}(s) = K_P + \frac{K_I}{s}$: (PI controller).

It is worth mentioning that given the relationship between the capacitor current and voltage, the reader's mind may be oriented in the direction that the presented AD control feedback can also be implemented by using the derivative feedback of the output voltage with an adjusting gain CK_{AD}. In fact, with this attitude, first, we are dealing with a PID controller that has a design-oriented derivative term, not a conventional PID controller. Second, the capacitor current feedback that incorporates information of the load current and

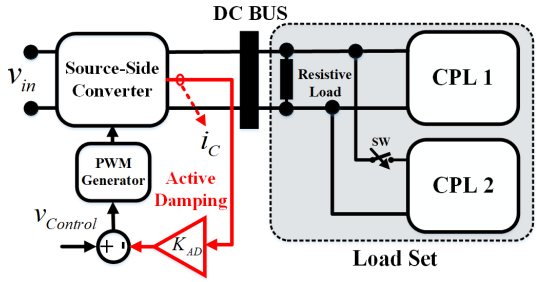

Fig. 14. Structure of DC MG considered in simulation and experimental tests.

current dynamics of the source converter's inductor, has a different nature of dynamic and performance than the output voltage (capacitor voltage) derivative term. Third, the output voltage derivative term corresponding to the PID controller injects significant noise into the closed-loop system of DC/DC converters compared with other AD control approaches that use capacitor current information. This negative effect is mainly due to the parasitic inductance and resistance of the output capacitor, which are respectively defined as the equivalent series inductance (ESL) and equivalent series resistance (ESR) [25], [27]. Besides, it will impose adverse effects on the system during large-signal and small-signal transients or even at steady-state by making impulse responses with large overshoots and undershoots, as well as discrete jumps at switching transitions [9], [27], [28]. These undesirable reactions significantly degraded phase margin, and thereby the system stability is jeopardized [29], [30]. Although the noise and phase margin can be improved by reducing the cut-off frequency of the low-pass filter associated with the derivative term, it leads to degradation of the closed-loop control bandwidth and slows down the system's dynamic performance. Therefore, in this case, there would always be a compromise between the closed-loop damping performance and the filter bandwidth. Accordingly, by further reducing the filter bandwidth, the stable range of K_{AD} is strongly restricted and as a result, the benefits of derivative gain cannot be fully exploited. As a general conclusion, it can be found that for robust stabilization of DC cascaded systems with CPLs, the proposed AD control approach exhibits reliable performance in different operating conditions with minimum recovery time and insignificant output voltage deviation for various transients in comparison with PI + designed D control strategy. These outcomes will also be verified in the next section by comparative experimental results.

C. Simulation and Experimental Verifications

To confirm the correctness and robustness of the proposed control method, a simulation was conducted on a typical DC MG depicted in Fig. 14 using Matlab/Simulink in the discrete-time domain with the parameters listed in Table I. Meanwhile, to further correspond with the actual conditions and to demonstrate the feasibility of the presented stabilizer technique, the control system delays including computation and PWM delays are also taken into account in the simulated model. Moreover, to ensure the applicability of the stabilization method in real-life, separate hardware prototypes of the cascaded systems consisting of three basic DC/DC converters with the structure shown in Fig. 14 was also built and tested

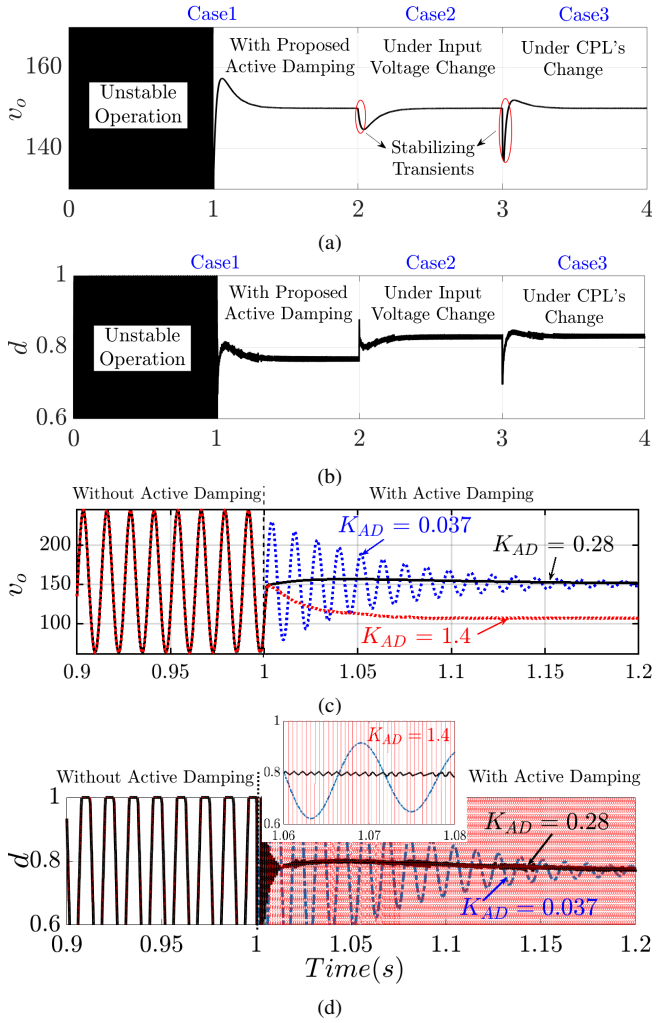

Fig. 15. Simulation results of the buck converter system with CPLs. (a) Output voltage under three operation cases. (b) Switch duty cycle under three operation cases. (c) The dynamic performance of the proposed stabilizer for different K_{AD}. (d) Switch duty cycle variations for different K_{AD}.

(see Fig. 16). The control part is realized by a dSPACE real-time 1202 (Microlab Box), whose sampling rate is 10 kHz. The switching frequency is equal to the sampling rate of the control part. It is worth noting that to overcome the distortion effect induced by the switching noise on the capacitor's current sampling, a low-pass filter has been installed between the current sensor and the analog to digital converter with a cut-off frequency of around 50 kHz [31]. This cut-off frequency will be appropriate considering that the switching noise frequency is usually higher than 1 MHz [32]. The parameters considered for the experimental setup are similar to the simulation model parameters. In both simulation and laboratory tests, three operational cases have been considered:

- ***Case 1***: The performance of the system without and with the proposed AD method.
- ***Case 2***: The evaluation of transient stability and system's dynamic performance under input voltage change.
- ***Case 3***: The evaluation of transient stability and system's dynamic performance under CPL power rating changes.

Before describing the results, how to select the effective K_{AD} based on the previous subsection is brought numerically. For a given desired output voltage, the negative equivalent load

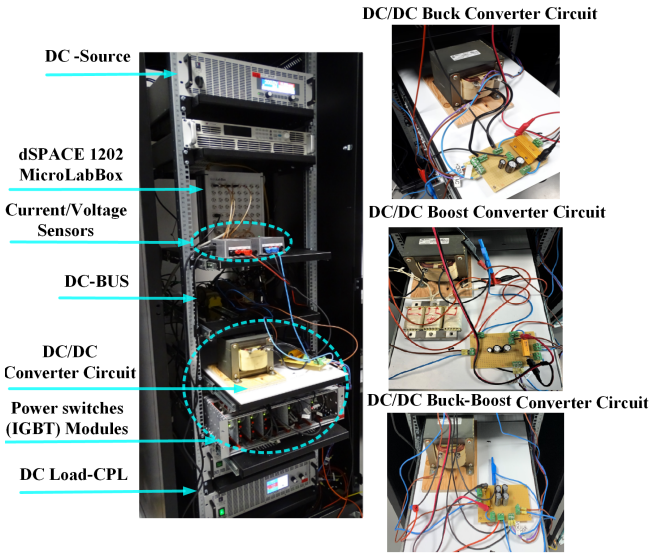

Fig. 16. Experimental setup.

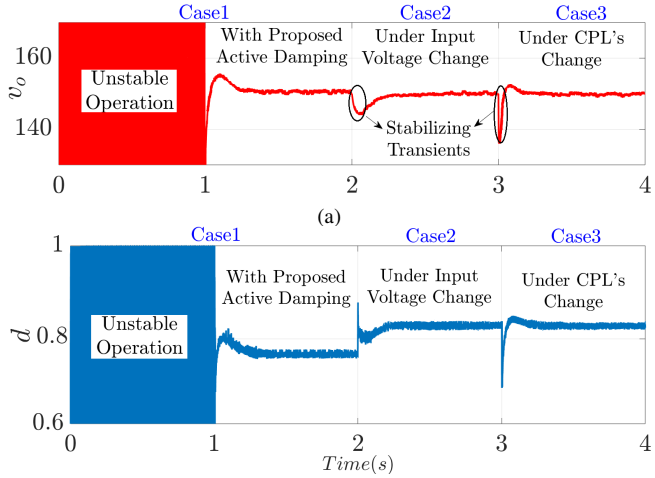

Fig. 17. Experimental results of the buck converter with CPLs under three operation cases. (a) Output voltage. (b) Switch duty cycle.

resistance of the system is

$$R_{eq} = R_{CPL} \| R_{Load} = -\frac{150^2}{2250} \| 470 = -10.2\,\Omega. \quad (12)$$

The minimum required virtual capacitor for system stability is

$$C_{V,min} = \frac{L}{R_L |R_{eq}|} - C = 43.2\,\text{mF}. \quad (13)$$

Then, according to (11), the minimum K_{AD} is achieved as

$$K_{AD,min} = \frac{C_{V,min} R_L V_{Tr}}{C V_{in}} = 28 \times 10^{-3}\Omega. \quad (14)$$

As outlined earlier, to attain an effective damping rate with the desirable phase margin (see Fig. 13) and high robustness against unforeseen changes in input voltage and CPL as well as to avoid slowing system response, $K_{AD} = 0.55$ ($C_V = 855.5\,\text{mF}$ and $R_V = 519.5\,\text{m}\Omega$) has been selected, which is approximately 20 times larger than $K_{AD,min}$. In Case 1, as can be observed from Figs. 15(a) and 17(a), when the AD controller is switched off, ($0 \le t \le 1\,\text{s}$), unstable oscillations occur on the DC bus voltage of the cascaded system due to the CPL effect. Once the suggested damping controller is

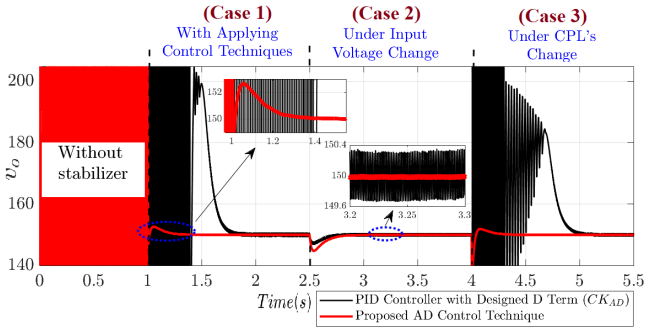

Fig. 18. Comparative experimental results between the proposed AD control method and the PI + designed D (CK_{AD}) controller with a similar damping gain rate ($K_{AD} = 0.55$) for the buck converter loaded by CPLs.

switched on, ($1 \leq t \leq 2\,\mathrm{s}$), the severe oscillations in DC bus voltage are rapidly damped and it makes the system stable. Effective damping performance and system stability can also be confirmed by Figs. 15(b) and 17(b), due to the desirable duty cycle achieved by deploying the proposed method. To investigate the robustness of the presented active stabilizer, transient stability and the system's dynamic performance have been evaluated in Cases 2 and 3. For this purpose, in Case 2, a 12.5% reduction in the input voltage value has been applied at $t = 2\,\mathrm{s}$. Also, in Case 3, CPL 750 W has been plugged into the system in parallel with the present CPL 2250 W at $t = 3\,\mathrm{s}$. As specified, after these abrupt variations, without causing unstable oscillations, the DC bus voltage reaches the desired value with the stable transients and very rapid dynamic responses. Admissible results have also been achieved for the switch duty cycle in accordance with the operational cases (see Figs. 15(b) and 17(b)). These results clearly show the robustness of the proposed damping method against unexpected changes. Another simulation result has been given to show the dynamic performance of the proposed active stabilizer for different K_{AD}. As seen in Fig. 15(c), by increasing K_{AD} in the allowable stable range ($K_{AD} = 0.28$), the DC bus voltage oscillations are damped rapidly in comparison with $K_{AD} = 0.037$. However, as also approved in Fig.13, with further increased K_{AD} and goes beyond its permissible band ($K_{AD} = 1.4$), the performance of the proposed AD scheme cannot properly track the output voltage reference and leads to system instability. These results can also be confirmed by Fig.15(d) which indicates the switch duty cycle variations for different K_{AD}. According to the resultant outcomes, it can be concluded that the CPL instability can be effectively resolved using the presented AD method, provided that K_{AD} fulfills the stability condition through virtually inserting a suitable series *RC* damper in parallel with the source's converter capacitor.

D. Experimental Comparison with the PI + Designed D (CK_{AD}) Control method

As shown in Fig.18, to demonstrate and validate the superiority of the proposed AD technique over the PI + designed D control method, their performance has been experimentally compared for a same damping term ($K_{AD} = 0.55$) under three operational cases. The performance results for both control methods are also summarized in Table II. Dynamic performance, reference voltage tracking, and transient recovery time of the system have been evaluated under changes in

TABLE II
A PERFORMANCE COMPARISON BETWEEN THE PROPOSED AD CONTROL SCHEME AND PI+DESIGNED D CONTROL METHOD UNDER A SIMILAR DAMPING GAIN ($K_{AD} = 0.55$) FOR THE BUCK CONVERTER SYSTEM LOADED BY CPLS.

Proposed AD Control Strategy			
Evaluation of Transient and Dynamic Performance			
Response Characteristics	**Case 1**	**Case 2**	**Case 3**
Dynamic Response Time	Very Fast	Very Fast	Very Fast
Maximum Overshoot or Undershoot	2.8%	3.2%	2.6%
Settling Time (Transient Recovery Time)	185 ms	220 ms	208 ms
PI + Designed D Control Strategy			
Evaluation of Transient and Dynamic Performance			
Response Characteristics	**Case 1**	**Case 2**	**Case 3**
Dynamic Response Time	Very Slow	Very Fast	Very Slow
Maximum Overshoot or Undershoot	230%	2.1%	285%
Settling Time (Transient Recovery Time)	785 ms	205 ms	1.05 s

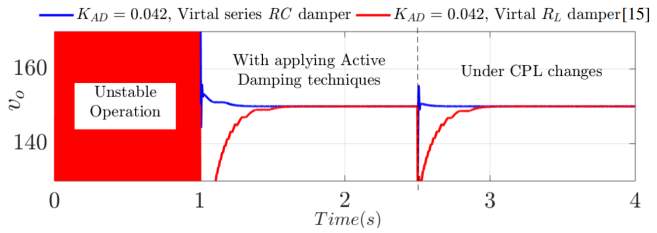

Fig. 19. Comparison of dynamic and transient performance of the proposed AD method with the AD approach provided by [15].

the input voltage and CPL power rating. The level of these changes is similar to the cases considered in the subsection *C* from Section III. The cut-off frequency of the low-pass filter corresponding to the derivative term, 10 kHz has been selected. As seen, once applying the proposed AD control technique at $t = 1\,\mathrm{s}$, the severe oscillations in DC bus voltage are rapidly damped and a desirable dynamic response is achieved with minimum transient recovery time (See Fig.18, and Table II). In contrast, the control method based on the PI + designed D controller exhibits a poor and sluggish dynamic response with significant fluctuations in transient performance. These superiorities are also clearly evident when the CPL's power rating variation (load change) is applied. Furthermore, in the PI + designed D control method, both the small output voltage deviation and the fast transient recovery time cannot be realized at the same time. Therefore, it can be concluded that in stabilization of DC cascaded systems consisting of DC/DC power converters loaded by CPLs, the proposed method has a more effective and robust performance than the PI + designed D control technique.

E. Comparison with the Virtual R_L Damper-Based Stabilization Strategy Offered by [15]

To demonstrate the superiority of our contributions, we also have done a comparison with the AD proposed by [15], whose is close to ours. In [15], to stabilize the DC/DC converters feeding CPLs, system damping has improved by emulating a resistance in series with the source-side converter inductor. This achieved by feeding back a proportional coefficient of the inductor current and subtracting it from the voltage control signal. However, the presented virtual R_L damper-based stabilization method cannot be suitable for different performance conditions due to its inherent limitations and

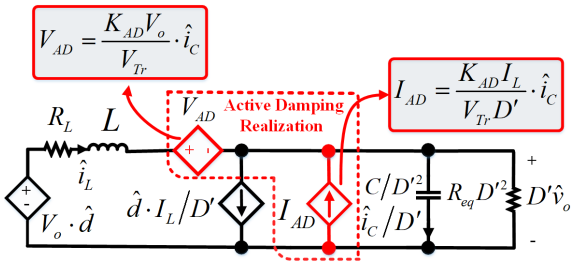

Fig. 20. Modified small-signal averaged equivalent circuit of the boost converter loaded by CPL with applying the proposed AD.

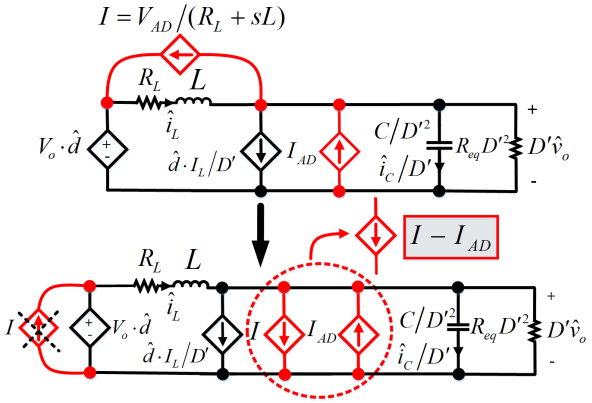

Fig. 21. Another analytical interpretation of Fig. 20.

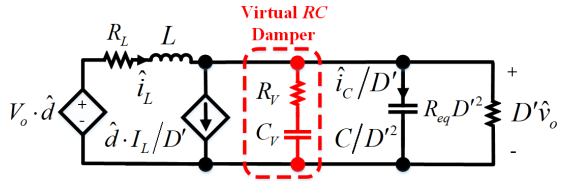

Fig. 22. The circuit physical meaning of the proposed AD applied to the boost power converter system loaded by CPL.

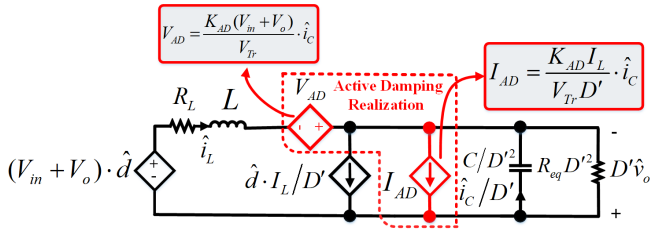

Fig. 23. Modified small-signal averaged equivalent circuit of the buck-boost converter feeding CPL with the proposed AD.

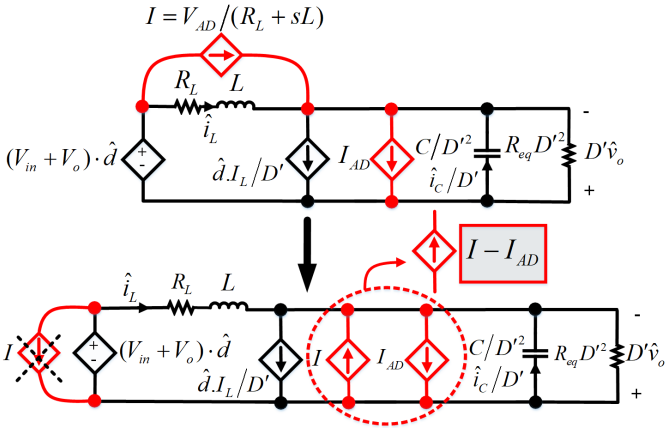

Fig. 24. Another analytical interpretation of Fig. 23.

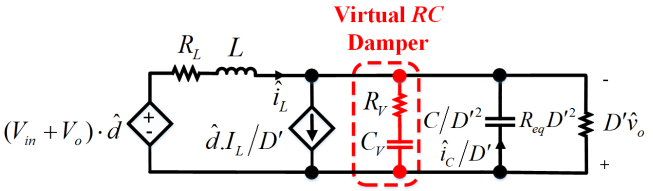

Fig. 25. The circuit physical meaning of the proposed AD applied to the buck-boost power converter system loaded by CPL.

shortcomings. First, the stable range of K_{AD} is very limited, which the lack of control flexibility of the proposed method. As a typical example, by applying the AD scheme suggested by [15] to a buck converter system shown in Fig. 3 with the parameters given in Table I, the stable band for K_{AD} is limited to $(0.027, 0.051)$ which is equivalent to $(R_{L,min}=\frac{L}{C|R_{eq}|}=5.51\,\Omega, R_{L,max}=|R_{eq}|=10.2)$. It is clear that in this case, the maximum damping gain is only 1.5 times its minimum value. In contrast, as explained in detail in the subsection B, for having a safe phase margin and desirable damping effect, the maximum damping gain obtained by our proposed AD technique is approximately 20 times its minimum value. Second, since the allowed value of the virtual $R_{L,max}$ is limited to $|R_{eq}|$, for a severe descending change in CPL power rating, the system stability may not be maintained. Hence, it can be found that the AD technique provided by [15] is not robust against CPL power rating changes. Third, as shown in Fig. 19, for a similar $K_{AD}=0.042$, the proposed active stabilizer applied to the system indicated in Fig. 3 has a rapid dynamic response with a reduction of about 75% in settling time. In addition, the results demonstrate that using the proposed AD stabilizer technique, the rise time has been reduced from 0.45 s to 30 ms.

IV. Proposed Virtual Series *RC* Damper for Boost and Buck-Boost Converters Loaded by CPLs

A. Description of the circuit physical meaning realized by the proposed AD scheme

Like the buck converter system, after applying the proposed AD, Fig. 8(a) is modified as Fig. 20 by replacing $\hat{d}-(K_{AD}.\hat{i}_c/V_{Tr})$ instead of $\hat{d}$. As seen, the added AD term can be well modeled as two dependent voltage and current sources, namely V_{AD} and I_{AD}. Consequently, it has an interesting circuit physical meaning as shown in Fig. 21. Using DC relations and given that in practical conditions $R_L << |R_{eq}|\cdot D'^2$, I-I_{AD} can be simplified as

$$I-I_{AD}=\frac{K_{AD}\hat{i}_C}{V_{Tr}}\left[\frac{V_o}{R_L+sL}-\frac{V_o}{D'^2|R_{eq}|}\right]\cong\frac{K_{AD}V_o\hat{i}_C}{V_{Tr}(R_L+sL)}. \quad (15)$$

It leads to the remedial shaping of the boost converter equivalent circuit virtually, as shown in Fig. 22. In this case, based on the circuit analysis,R_V and C_V are achieved as

$$\frac{D'\hat{v}_o}{I-I_{AD}}=\frac{LD'V_{Tr}}{K_{AD}CV_o}+\frac{1}{s}\left(\frac{D'R_LV_{Tr}}{K_{AD}CV_o}\right)=R_V+\frac{1}{sC_V}. \quad (16)$$

The process of the proposed damping performance on the buck-boost converter feeding CPL is also illustrated in Figs. 23 to 25. In accordance with the same conditions aforementioned, I-I_{AD} can be simplified as

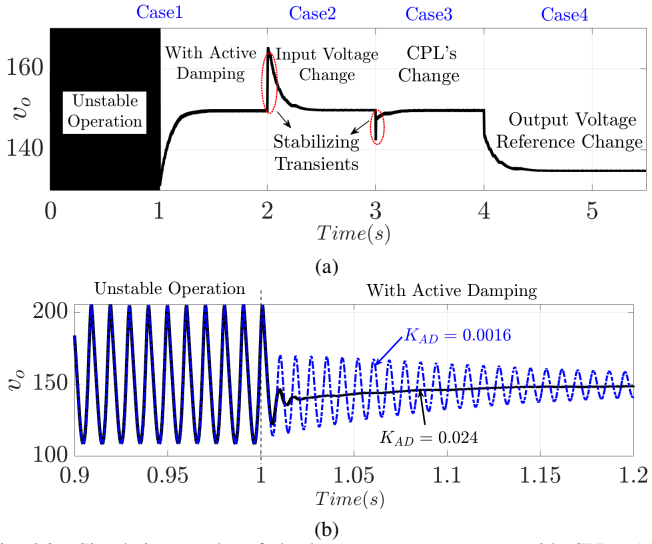

Fig. 26. Simulation results of the boost converter system with CPLs. (a) Output voltage under four operation cases. (b) Dynamic performance of the proposed stabilizer for different K_{AD}.

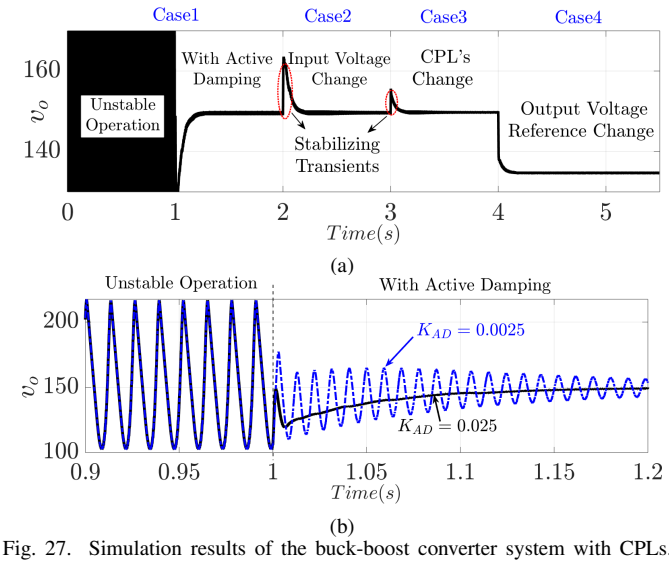

Fig. 27. Simulation results of the buck-boost converter system with CPLs. (a) Output voltage under four operation cases. (b) Dynamic performance of the proposed stabilizer for different K_{AD}.

$$I - I_{AD} = \frac{K_{AD}\hat{i}_C}{V_{Tr}}\left[\frac{(V_{in}+V_o)}{R_L+sL} - \frac{V_o}{D'^2|R_{eq}|}\right] \cong \frac{K_{AD}(V_{in}+V_o)\hat{i}_C}{V_{Tr}(R_L+sL)}. \quad (17)$$

This can lead to the virtual insertion of a series *RC* branch as depicted in Fig. 25, which R_V and C_V are obtained as

$$\frac{D'\hat{v}_o}{I-I_{AD}} = \frac{LD'V_{Tr}}{K_{AD}C(V_{in}+V_o)} + \frac{1}{s}\left(\frac{D'R_LV_{Tr}}{K_{AD}C(V_{in}+V_o)}\right) = R_V + \frac{1}{sC_V}. \quad (18)$$

B. Selecting an Effective AD Term (K_{AD})

The procedure of determining the acceptable range of K_{AD} for boost and buck-boost converters loaded by CPLs is similar to the method described for the buck converter. Consequently, the effective damping terms of these systems are respectively determined by (19) and (20). To increase the system damping and to achieve high robustness against unexpected variations in the influential factors, namely the input voltage, CPL power rating, as well as step changes in output voltage reference, without knowing the new values of them, the effective K_{AD} should be selected sufficiently larger than the relevant $K_{AD,min}$, provided that the system response speed is not affected and also a safe phase margin for the system is attained.

$$K_{AD} > \frac{D'C_{V,Crit}R_LV_{Tr}}{CV_o} = K_{AD,min}. \quad (19)$$

$$K_{AD} > \frac{D'C_{V,Crit}R_LV_{Tr}}{C(V_{in}+V_o)} = K_{AD,min}. \quad (20)$$

C. Simulation and Experimental Verifications

To verify the effectiveness of the proposed stabilization method on the boost and buck-boost converters feeding CPLs, simulations in the discrete-time domain were carried out in Matlab/Simulink for the model shown in Fig. 14 taking into account computation and PWM delays. Besides, considering the built experimental setup, the applicability of the presented technique in real conditions has been also tested (see Fig. 16). The parameters considered in the simulation models and the experimental setups are given in Table I. Since V_o and D' are the affecting factors in adjusting K_{AD} (see (19) and (20)), in addition to three operational cases investigated in both simulation and experimental tests, evaluation of transient

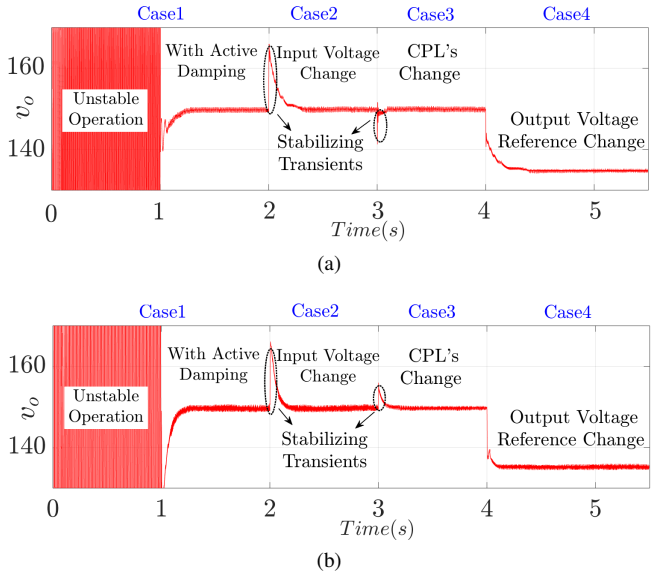

Fig. 28. Experimental verifications of the boost and buck-boost converters loaded by CPLs under four operation cases. (a) Output voltage of the boost circuit. (b) Output voltage of the buck-boost circuit.

stability and system's dynamic performance under descending changes of the output voltage reference is also considered in case 4. To enhance the system damping with the desired phase margin and to ensure robustness in the face of unexpected changes aforementioned, as well as to prevent the system response from slowing down, $K_{AD} = 0.026$ ($C_V = 886.3\,\text{mF}$ and $R_V = 541.5\,\text{m}\Omega$) and $K_{AD} = 0.0078$ ($C_V = 706\,\text{mF}$ and $R_V = 679.8\,\text{m}\Omega$) have been selected, respectively, for the boost and buck-boost converters loaded by CPLs, which are 20 times larger than their corresponding $K_{AD,min}$. In case 1, as seen from Figs. 26(a), 27(a), 28(a), and 28(b), without AD, fluctuations occur on the DC bus voltage of the cascaded systems due to the CPL instability. Once applied proposed technique at $t = 1\,\text{s}$, the severe fluctuations in DC bus voltage are rapidly damped and it leads to the system stable. To show the robustness of the presented active stabilizer, transient stability and the system's dynamic performance have been also evaluated in Cases 2 to 4. For the boost converter, in

case 2, a 20% increase in the input voltage has been applied at $t = 2\,\mathrm{s}$. Also, in Case 3, CPL $750\,\mathrm{W}$ has been linked into the system in parallel with the available CPL $2250\,\mathrm{W}$ at $t = 3\,\mathrm{s}$. Moreover, a 10% reduction has been applied to the output voltage reference at $4\,\mathrm{s}$. As seen, after these sudden changes, without causing unstable oscillations, the DC bus voltage reaches the desired value with the stable transients and very rapid dynamic responses. Likewise, for the buck-boost converter, in case 2, a 42% ($V_{in} = 170\,\mathrm{V}$) increase in the input voltage has been applied at $t = 2\,\mathrm{s}$ (functional mode change from boost to buck). In Case 3, CPL $600\,\mathrm{W}$ has been paralleled into the available CPL $1800\,\mathrm{W}$ at $t = 3\,\mathrm{s}$. Besides, a 10% reduction has been applied to the output voltage reference at $t = 4\,\mathrm{s}$. These outcomes illustrate how the proposed stabilization technique handles the transient response in a robust way. To show the dynamic performance of the proposed stabilizer for different K_{AD}, another results from the simulations have been brought as Figs. 26(b) and 27(b). As specified, by increasing K_{AD}, the DC bus voltage fluctuations are damped rapidly.

As a consequence, the proposed novel AD technique can be considered as an acceptable precondition stabilization control scheme for a more complex DC network. Accordingly, how to generalize the proposed control approach to the dc-bus-based multiple source converters system application will be the future work for the authors. However, in this case, we will face some challenges. The big challenge is due to the interactions among the source converter's control loops, where each of the converters cannot include the virtual series *RC* damper adapted for a specific load. Other challenges can arise from load sharing and interleaving issues among the source converters. Our future work is to resolve these challenges.

V. Conclusions

In this paper, we have introduced a new AD stabilizer technique by inserting a virtual series *RC* damper at the source-side for stabilizing the cascaded structures consisting of the basic DC/DC converters with single or multiple CPLs in DC MGs. Using this design-oriented approach, which takes advantage of a simple control structure with an easy setting of the control parameters, the system stability and performance are ensured without compromising the load dynamic performance while preserving the practical constraints such as weight saving and low power dissipation. In addition, the flexibility of the presented technique in choosing a desirable AD term to achieve a stable cascaded system with high robustness and proper dynamic performance against transient unanticipated variations occurring in the system has been demonstrated. The validity and effectiveness of the proposed active stabilizer on the three cascaded systems were also verified through both simulation and experimental results, which are in good agreement with the theoretical findings.

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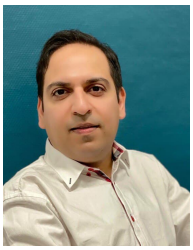

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