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Enhanced Fault Ride-through of Power Converters Using Hybrid Grid Synchronization

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***Abstract*—Inaccurate phase-angle jump estimation of the grid voltage during faults is one of the major causes for poor fault ride-through performance of converters. To overcome this issue and make the converter's current controller robust, this paper proposes a hybrid grid synchronization transition technique. In this concept, a synchronous reference frame based phase-locked loop (SRFPLL) grid synchronization method is used during normal grid operation and switched to an arctangent based phase-angle estimation during grid faults. Simultaneously frequency estimation is switched to the arctangent derived frequency. A common transition method, which depends on the phase-angle error between the two phase estimation techniques, is proposed to ensure a smooth transition between the hybrid phase-angle and frequencies. The transition technique is implemented using the current control of a three-phase voltage source converter in the synchronous reference frame. The performance of the converter during both symmetrical and asymmetrical grid faults along with the fault ride-through strategies is tested using real-time experiments. It is observed that the transition based hybrid grid synchronization technique reduces the loss of synchronism duration. Additionally, it offers a more robust converter current control performance compared to the SRFPLL technique over a wide range of voltage sags and phase-angle jumps.**

***Index Terms*-Voltage source converters, grid faults, phase-angle jumps, phase-locked loop, hybrid grid synchronization, fault ride-through.**

I. Introduction

Voltage source converters (VSCs), unlike the synchronous generators, are unable to maintain their phase shift and phase sequencing during grid transients [1]. Hence, most VSCs are equipped with phase-locked loop (PLL) based grid synchronization [2]. The use of the PLL technique for synchronization purpose suffer from transient stability issues (for instance loss of synchronization (LOS)) mainly in a weak grid, where the equivalent grid impedance is high enough to be influenced by the PLL dynamics [3], [4]. Moreover, during events like grid faults, phase-angle jumps (PAJs) at the grid voltage negatively impacts the converter's operation as the PLL wrongly estimates the grid voltage phase-angle which results in LOS for a longer time. PAJs occur mainly due to the unequal X/R ratio of the fault impedance and the equivalent grid impedance. Recently grid fault as a result of LOS is reported by the North American Electric Reliability Corporation (NERC). According to the report, the LOS of the PLL with the grid during fault triggered the trip of a 900 MW solar PV plant in southern California [5]. Other records from industries illustrate that voltage sags of 20-100 ms duration contribute to 46% of all types of other voltage transients [6]. During such adverse grid scenarios, it has always been a challenge to design an immune, fast, simple and yet robust PLL for grid synchronization.

From the simplicity in implementation point of view, most industrial converters employ the conventional synchronous reference frame based phase-locked loop (SRFPLL) technique for grid synchronization [7]. SRFPLL estimates the frequency and phase-angle in a single-loop and hence suffers during PAJs [8]. Also, the proportional and integral (PI) gain parameters (K_{PPLL}, K_{IPLL}) of the PLL are designed based on the bandwidth selection, which provides a settling time of almost 5-10 fundamental time periods (100-200 ms) [9] to achieve the stability margin. From the perspective of the fault ride-through operation, such settling time is quite large. Additionally, the assumption to equate sine of phase-angle error to absolute value (i.e. $\sin\theta_e \approx \theta_e$) as in SRFPLL based grid synchronization technique, holds well for small PAJs (up to $\pm 7^0$) [10]. Higher PAJs make this assumption invalid and result in wrong phase-angle estimation with SRFPLL and create LOS situations for the converters. On the other hand during asymmetrical grid faults and harmonics in the grid voltage, SRFPLL includes low bandwidth pre/in-loop filters to eliminate the negative sequence components at the cost of slower dynamics [11], [12]. Several advanced PLLs have been investigated by researchers, which have not yet been implemented by leading companies in their commercial products due to several factors [13]-[15]. It is worth noting that even advanced PLL techniques consider the usual in-loop design trade-off and hence may result in a slow dynamic response. They also suffer from LOS risk during large grid perturbations [16].

On the other hand, open-loop grid synchronization techniques are well accepted for their faster dynamics and unconditional stability. A handful of work on open-loop grid synchronization techniques can be found in [17]. However, during off-nominal grid frequency variations, such techniques create additional phase-angle error which can only be solved by making them frequency adaptive. Thus an additional frequency detector will be needed in a feedback or feedforward manner. If frequency is fed in a feedback path

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(for instance using SRFPLL), the open-loop features of these techniques do not hold any more and accordingly stability of the synchronization techniques needs to be addressed. On the other hand frequency information can be provided in a feedforward way using additional filters and advanced frequency detectors at the cost of degrading the dynamic response.

Attempts have been made to design an adaptive/hybrid SRFPLL technique to avoid the issue of the LOS, for example, using a freezing PLL concept [18]. In this case, non-availability of the information of phase-angle, results in the flow of uncontrolled current to the grid and the grid code is violated [19]. Other solutions to avoid LOS during fault include zero current injection [20], grid impedance and X/R ratio dependent current injection [21], and PLL estimated frequency adaptive current injection [22]. All these techniques either require 1 p.u. reactive current rating requirement during severe grid fault or the prior knowledge of grid impedance, which make them unrealistic. The use of first-order SRFPLL during faults is implemented as a solution in [23]-[24] to avoid LOS for longer time. In this technique, the proportional gain of the SRFPLL needs to be tuned carefully as a higher value might reduce the settling time at the cost of affecting the stability margin.

Moreover, adding voltage (at the point of common coupling (PCC)) feedforward compensation terms to the output of the current controller can overcome the negative impact of the PLL dynamics during grid faults. Nevertheless, such feedforward compensation acts as a positive feedback to the control systems of the current-controlled converters and decreases the system stability margin especially in a weak grid where the grid impedance is of utmost concern [25]-[27]. Additionally, such voltage feedforward compensation adds harmonics to the current to be injected to the grid as a result of large grid impedance seen at the PCC [28].

Among the adaptive PLL techniques as discussed above, either freezing PLL [18] or first-order PLL [23] can be considered as a simple and reliable synchronization technique to provide robust fault ride-through (FRT)/ low voltage ride-through (LVRT) for converters. The freeze PLL proposes to disable its closed-loop control during the fault. With this technique, the converter can ride-through more severe faults; e.g. even zero voltage ride-through. However, disabling the PLL loop during non-severe fault does not help the converter to accurately track the grid voltage phase-angle as a result of PAJ. With the inaccurate phase-angle information, the converter fails to provide the required amount of active and reactive power during the fault as demanded by the grid code. On the other hand, resetting the integrator during the fault time as suggested in [23] provide infinite damping to the PLL in case of severe faults that improves the LOS issue. Nevertheless, it does not discuss any adaptive design to tune the proportional gain and hence its value is proposed to follow the conventional PLL design. The selection of proportional gain is a trade-off between the faster synchronization (lower settling time) and good in-loop filtering (lower bandwidth). The settling time in [23] is chosen as 100 ms which can be considered as a delayed response to ride-through short duration grid faults. Additionally, discussion on the impact of PAJ on the current controller dynamics during the fault inception and recovery is missing in the scope of the work. Moreover, it does not take into account the frequency adaptive behavior of the pre-filter used for extracting the positive sequence phase-angle during asymmetrical faults. In a nutshell, both [18] and [23] provide emphasize on the more severe grid fault and hence provide space to investigate the impact of PAJ on the LVRT of the converter during non-severe grid faults.

To fulfil the research gap as discussed above and achieve improved grid synchronization performance along with robust FRT / LVRT operation for grid-connected converters, a hybrid grid synchronization technique is proposed in this paper. In this method, the grid voltage phase-angle is estimated using a combination of low bandwidth SRFPLL and arctangent in the stationary reference frame ($\alpha\beta$-frame). This is named as "transition phase-locked loop" (TPLL) (as hybrid phase-angle estimator). The proposed TPLL is used for the improved ride-through operation for 3-ph dq-current controlled converter during symmetrical faults having both voltage sag and PAJs. Additionally, the frequency is estimated using a combination of SRFPLL technique and the arctangent derived frequency. This is referred as "transition frequency-locked loop" (TFLL) (as hybrid frequency estimator) in this work. During asymmetrical faults, the hybrid frequency estimator (as TFLL) is used in the frequency adaptive pre-filter (dual second-order generalized integrator in this work) during the extraction of both positive and negative sequence voltage components and frequency adaptive current controller. A smooth transition scheme is proposed for the above mentioned hybrid frequency and phase-angle estimators. The transition is controlled by two pre-defined ramp functions (called as weight functions). The ramp functions are enabled depending on the phase-angle error (as a result of any PAJ due to grid fault) between the fast estimated arctangent and slow estimated SRFPLL. The design of the transition scheme is analyzed in regards to the selection of the transition time. Further its impact on the dynamics of the weight functions is investigated. The grid synchronization and current controller performance during the LVRT operation are tested using experiments. It is further compared with conventional and other adaptive SRFPLL techniques. Comparisons are also made with the SRFPLL technique having voltage feedforward compensation during the faults with PAJs.

The advantages of the proposed hybrid grid synchronization transition technique over [18] and [23] are:

- It avoids PLL gain tuning issues during grid faults like in [18]. Simultaneously, it provides fast and accurate phase-angle information for the converter controller during PAJ.
- Unlike [23], it reduces the grid synchronization delay and helps the converter to ride-through the PAJ faster during faults. Additionally, it takes into account the frequency adaptability of the pre-filter and current controller.

The paper is organized as follows to address the aforementioned contributions; in Section II, the proposed hybrid grid synchronization strategy is detailed along with the transition algorithm framework, Section III explains the implementation of the proposed hybrid grid synchronization in the current controller of a three-phase grid-connected converter during both symmetrical and asymmetrical faults along with the LVRT strategy. Section IV provides experimental validation and comparison of the proposed TPLL and TFLL versus conventional SRFPLL during grid faults (sag and PAJs) along with the activation of LVRT mode. Section V discusses the obtained results. The findings of the current research work are concluded in Section VI.

II. Proposed Hybrid Grid Synchronization Technique

The proposed hybrid grid synchronization technique includes frequency and phase-angle estimation using both a classical second-order SRFPLL and an Arctangent method as shown in Fig. 1. It also provides a transition scheme between the two synchronization techniques that depends on the grid voltage conditions. The parameters used for the proposed techniques are discussed in the following sub-sections step by step.

A. Grid Synchronization Using SRFPLL during Normal Grid Condition

The parameters of the SRFPLL used in the hybrid grid synchronization are designed based on the linearized model as discussed in [1]. The PLL model is represented by a second-order closed-loop control structure. The transfer function of the linearized second-order SRFPLL is given by

$$\frac{\theta_{PLL}(s)}{\theta_e(s)} = \frac{K_{PPLL}s + K_{IPLL}}{s^2 + 2\zeta\omega_{bw}s + {\omega_{bw}}^2} \tag{1}$$

where θ_{PLL} represents the phase-angle estimated by the PLL and θ_e is the steady-state phase-angle error between the actual and estimated value i.e., ($\theta_e = \Delta\theta = \theta_g - \theta_{PLL}$). In the right hand side of (1), ζ and ω_{bw} are the damping ratio and bandwidth respectively for the PLL, which are decided by the designer. The set values of ζ and ω_{bw} provide the proportional and integral gain parameters (K_{PPLL} and K_{IPLL}) that form the closed-loop structure of the PLL.

In this work, it is proposed to design the PLL to provide accurate grid voltage parameter estimation during normal grid voltage conditions, i.e., the steady-state operating conditions. In the steady-state, maintaining a good power quality of the injected grid current is given priority for the power converter. To achieve this, a low bandwidth (= 8.5 Hz) is suggested for the SRFPLL, which sets $\omega_{bw} = 2 \times \pi \times 8.5$. The ζ value is chosen to be 0.707 to provide optimum damping during the frequency and phase-angle estimations. Based on ω_{bw}, the settling time (T_{set}) for the PLL is calculated as

$$T_{set} = 4.6\tau \cong \frac{4.6}{\zeta\omega_{bw}} \tag{2}$$

where τ represents the rise time. T_{set} is considered nearly equal to 120 ms. Upon the selections of ω_{bw}, ζ and T_{set}, the values for K_{PPLL} and K_{IPLL} are calculated as

$$K_{PPLL} = 2\zeta\omega_{bw} = \frac{9.2}{T_{set}}, K_{IPLL} = {\omega_{bw}}^2 = \frac{4.6^2}{(\zeta T_{set})^2} \tag{3}$$

It is to be noted here that grid synchronization using the conventional SRFPLL as discussed above requires both Clarke and Park transformation of the measured voltage signal. After the Park transform, the estimated q-axis voltage (V_q), is considered as the phase-angle error (represented as in (1)). In fact the actual expression for V_q can be derived as $V_q = \sin(\theta_e)$. The linearized approximation leads to the assumption as $\sin(\theta_e) \cong \theta_e$. The approximation of the 'sin' of the phase-angle error as its absolute value holds good for smaller magnitudes. In case of larger magnitude of phase-angle error for instance, the PAJ during grid faults, such approximation results in poor tuning of the PLL gain parameters. Hence inaccurate grid voltage frequency and phase-angle error tracking highly affect the converter current controller during the faults. This issue is mitigated in this paper, as discussed below.

B. Grid Synchronization Using Arctangent during Grid Faults with Phase-angle Jumps

To avoid this issue of erroneous phase-angle estimation with SRFPLL during large PAJ, this paper proposes to switch to the phase-angle estimation in the $\alpha\beta$-frame using the arctangent function. Undoubtedly, such technique speeds up the grid synchronization process as (i) there are no tuning issues and hence it is independent of PLL settling time, (ii) it is decoupled from the estimated frequency (frequency variations generally do not occur during faults), and (iii) it requires only Clarke transformation ($abc/\alpha\beta$) for estimation. However, the implementation of arctan function adds complexity for low cost digital signal processors. Additionally, such phase-angle estimation suffers from large oscillations during an unbalanced grid. In this paper, the computational burden of 'arctan' is reduced by carefully implementing its third-order polynomial approximation as

$$\theta_{arctan} = \frac{\pi}{2} \times \frac{0.6404V_\beta {V_\alpha}^2 + {V_\beta}^2 V_\alpha + {V_\beta}^3}{{V_\alpha}^3 + 1.6404V_\beta {V_\alpha}^2 + 1.6404{V_\beta}^2 V_\alpha + {V_\beta}^3} \tag{4}$$

which provides an approximation error of 0.0008°, and hence is considered negligible. A proper phase unwrapping has been achieved using four quadrant approximations. During grid unbalance an additional frequency adaptive pre-filter is added to the proposed technique which will be discussed in the following section. To avoid sudden switch between SRFPLL and arctan phase while implementing hybrid grid synchronization in real time, a smooth transition from one phase estimator to the other is proposed in the name of TPLL.

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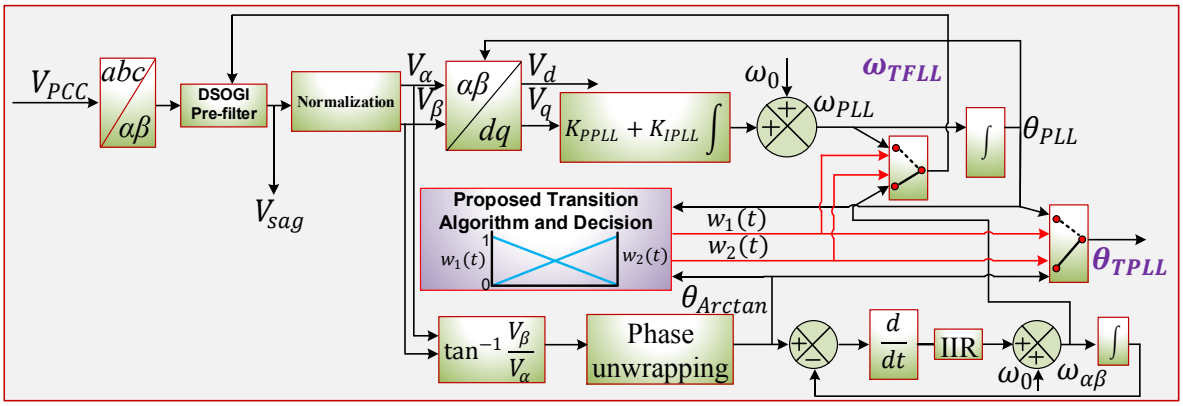

Fig. 1. Hybrid grid synchronization scheme for the grid connected VSC.

C. Proposed Transition Framework for TPLL

The flow chart of the proposed TPLL is shown in Fig 2.

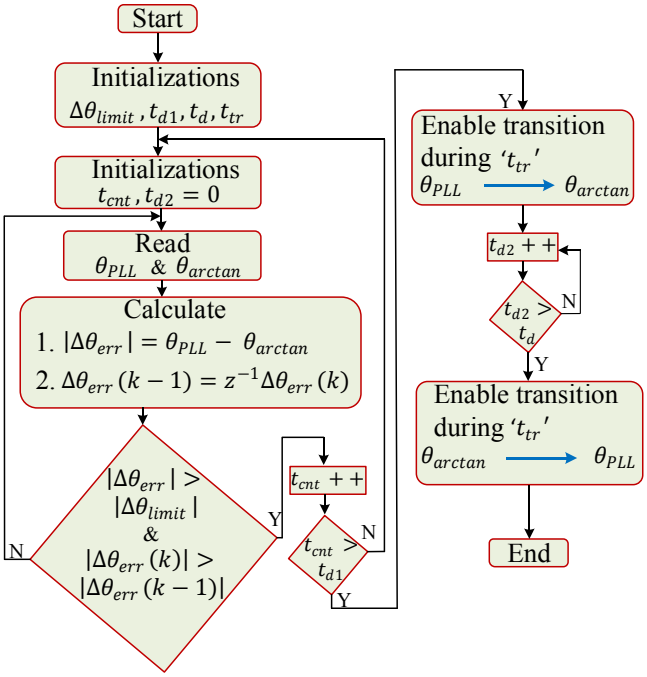

Fig. 2. Flow-chart for the proposed transition framework between two synchronization methods.

The phase-angle error limit ($\Delta\theta_{limit}$), t_{d1}, t_d are initialized at first. The phase-angle difference between the SRFPLL estimated phase (θ_{PLL}) in the dq-frame and arctangent estimated phase (θ_{arctan}) in the $\alpha\beta$-frame is calculated. The phase error ($\Delta\theta_{err}$) is compared with the $\Delta\theta_{limit}$, which is set as $\pm 7^0$ [10]. As soon as PAJ occurs due to the grid faults and $\Delta\theta_{err}$ exceeds $\Delta\theta_{limit}$ in the rising slope, the counter (t_{cnt}) counts for 10 samples (i.e. $t_{d1} = 10T_s$). If the error still exits, then the first transition process is enabled. During this transition, the phase-angle required for the frame transformation and current controller will switch from SRFPLL to the arctangent based phase estimation. Once the fault is cleared, and $\Delta\theta_{err} \approx 0^0$, the second transition is activated. Before switching back to SRFPLL during second transition, the counter $t_{d2} = t_d$ is delayed for at least the settling time of the SRFPLL to ensure smooth recovery of the phase estimation from arctangent to the SRFPLL in the steady-state.

During the transition, instead of directly switching between the phase estimation techniques, two weight functions (w_1 and w_2) are defined to act as gains for the two estimated phase-angles i.e. SRFPLL and arctangent. w_1 and w_2 are two positive and negative ramp functions ranging from 0 to 1, which decide the transition time for the TPLL technique. The control diagram along with the graphical representation of the hybrid grid synchronization transition framework used for proposed TPLL during a PAJ related fault is provided in Fig. 3. During the occurrence of grid fault, the converter is switched to the LVRT mode following the TPLL based synchronization.

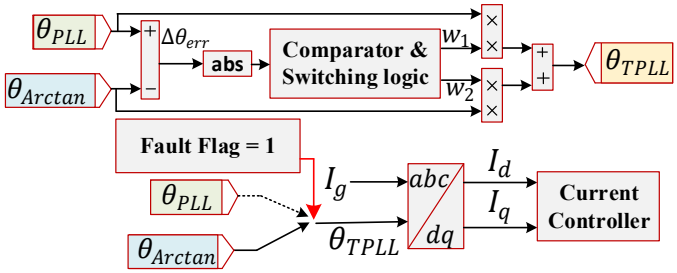

Fig. 3. Transition framework for the proposed TPLL and phase-locking of the grid current.

The mathematical expression for the phase-angle required for frame transformation as well as current controller operation (θ_{TPLL}) as a function of weighted θ_{PLL} and θ_{arctan} is given by

$$\theta_{TPLL} = w_1(kT_s)\theta_{PLL} + w_2(kT_s)\theta_{arctan} \quad (5)$$

The relation between the two weight functions is, $w_2(kT_s) = 1\text{-}w_1(kT_s)$. The value of k can be decided depending on the transition time set for the proposed technique. The value of T_s is kept the same as sampling time, i.e., 0.1 ms. The value for k

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is varied between 1 to 20, which implies a variation in the transition time (t_{tr}) from 0.1 ms to 2 ms respectively as shown in Fig. 4. All the tests are performed with a transition time t_{tr} = 2 ms to ensure a smooth transition. Higher transition time is not suitable for the current controller to respond during grid voltage PAJs. Such transition between the two phase estimation techniques (SRFPLL and arctangent) can help the converters to operate robustly during grid faults as compared to the SRFPLL technique, which delays the phase estimation for more than 100 ms.

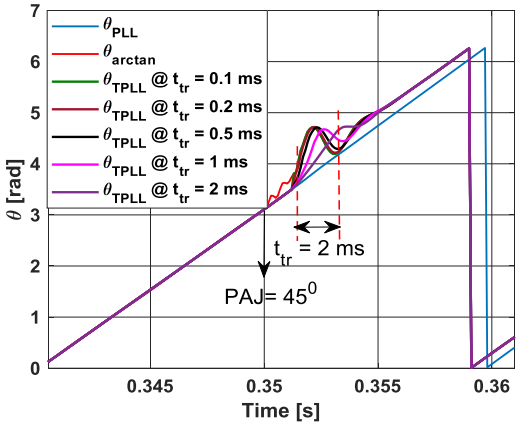

Fig. 4. Transition phase-locked loop with varying transition times (t_{tr}).

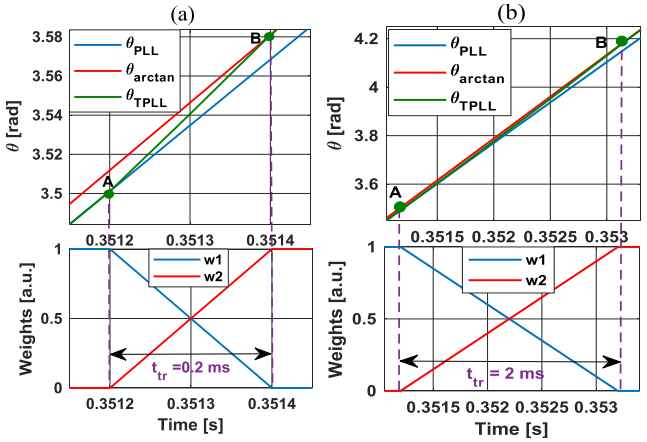

Fig. 5. Impact of transition time (t_{tr}) on weight functions $w1$ and $w2$: a) with t_{tr} = 0.2 ms and b) t_{tr} = 2 ms.

Further, the impact of t_{tr} of the TPLL on the dynamics of weight functions ($w1$ and $w2$) is analyzed. Two values of t_{tr} are considered such as 0.2 ms and 2 ms to represent fast and slow transition respectively. The lower and upper boundary for both $w1$ and $w2$ are kept as 0 and 1 respectively. It can be observed that with the lower value t_{tr} i.e., 0.2 ms, both $w1$ and $w2$ reach their final state from the initial state at a faster rate. On the other hand with higher t_{tr}, both the weight functions follow comparatively a lower ramp rate. It is worth noting that the lower transition time helps in a faster phase-angle switch from SRFPLL to arctangent estimation on the occurrence of PAJ. This can be depicted from Fig. 5(a). The points 'A' and 'B' are referred to the start and end points of the transition process. However, with a transition time of 0.2 ms there is an overshoot during the transition as shown in Fig. 4. In contrast, the higher transition time provides a bump-less transition and hence results in a smooth phase-angle switching between the two estimators as shown in Fig. 5(b). The impact of different t_{tr} on the current controller dynamics of the power converter during the FRT will be investigated later in the experimental section. Furthermore, the impact of both positive and negative PAJs on the proposed transition scheme is demonstrated as shown in Fig. 6. The t_{tr} is kept as 2 ms. It is observed that with the same transition period, point B moves to point C due to a higher PAJ (from ±45° to ±60° in Fig. 6).

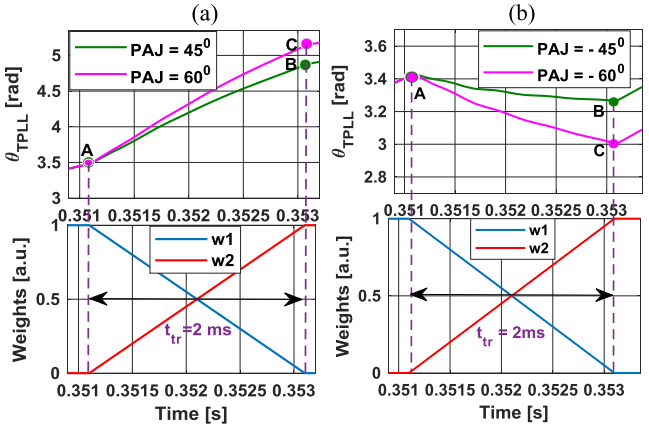

Fig. 6. Impact of various PAJs (positive and negative) on the proposed TPLL with t_{tr} = 2 ms: (a) +ve PAJs and (b) –ve PAJs.

D. Simultaneous Frequency and Phase-angle Transition

In case of unbalanced grid voltage, phase-angle estimation using arctangent function suffers from double power frequency oscillations. This is avoided by using frequency adaptive dual second-order generalized integrator (DSOGI) based pre-filter for the grid voltage. Unlike the conventional DSOGI based phase-locked loop concept, the frequency adaptability of the DSOGI pre-filter is enhanced using transition based frequency estimations. In addition to phase-angle transition as discussed above during a phase-angle jump based grid fault, the frequency estimation is switched from SRFPLL technique to the rate of change of arctangent phase-angle estimation as given by

$$\begin{aligned} f_{\alpha\beta} &= \frac{1}{2\pi}\frac{d(\theta_{arctan}{}^{+})}{dt} \\ &= \frac{1}{2\pi}\frac{d[\tan^{-1}(V_\beta{}^{+}(t)/V_\alpha{}^{+}(t))]}{dt} \\ &= \frac{V_\beta{}^{+}(t)V_\alpha{}^{+}(t) - V_\alpha{}^{+}(t)\dot{V}_\beta{}^{+}(t)}{[V_\alpha{}^{+}]^2 + [V_\beta{}^{+}]^2} \end{aligned} \quad (6)$$

where '+' represents the positive sequence phase-angle. A first-order infinite impulse response (IIR) based digital filter is used at the output of the frequency estimation to generate the filtered frequency ($f_{\alpha\beta(f)}$) as given by

$$f_{\alpha\beta(f)}(n) = f_{\alpha\beta(f)}(n-1) + c(f_{\alpha\beta} - f_{\alpha\beta(f)}(n-1)) \quad (7)$$

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where 'c' is called the forget factor which is related to the filter cut off frequency (f_c) and sampling frequency (f_s) as $c = 1 - e^{-2\pi f_c/f_s}$. For a sampling frequency of 10 kHz, the cut-off frequency is chosen to be 25 Hz, which is much faster than the PI gains of the SRFPLL. However such frequency estimation provides error at steady-state at low sampling frequency and off-nominal grid frequency. To avoid this issue the proposed hybrid grid synchronization switches back to the SRFPLL frequency estimation after the grid fault recovery. In real time, frequency variations are much slower as compared to an abrupt change is phase-angle during fault. The mathematical expression for the transition frequency locking (TFLL) is given by

$$f_{TFLL} = w_1(kT_s)f_{PLL} + w_2(kT_s)f_{\alpha\beta(f)} \tag{8}$$

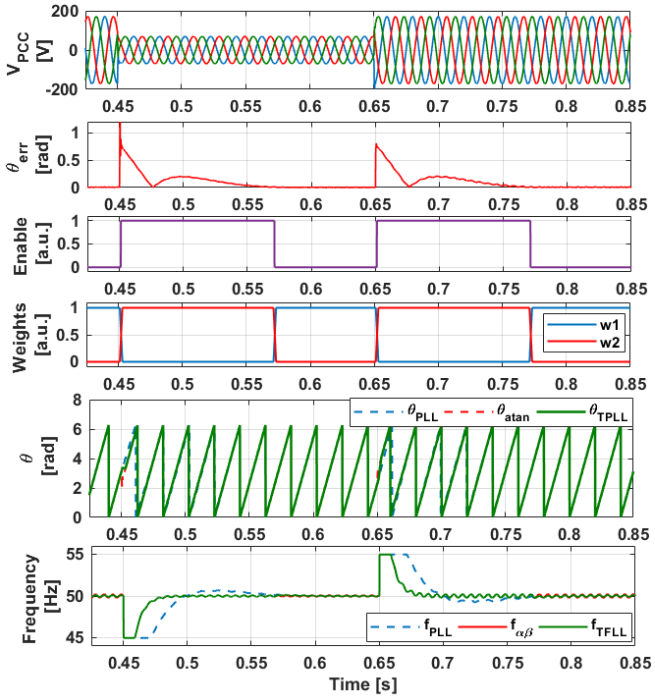

Fig. 7. Simultaneous frequency and phase-angle transition using the prposed hybrid grid synchronization duirng the grid fault inception and recovery.

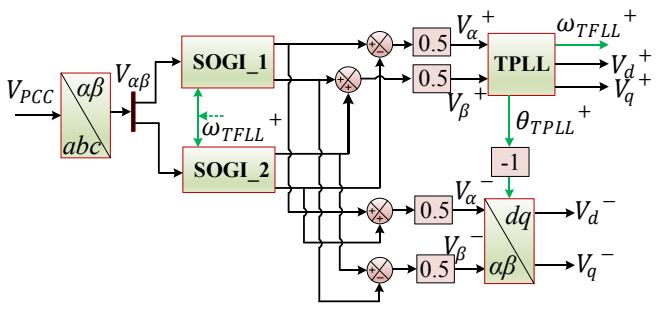

Fig. 8. Positive and Negative Sequence voltage component extraction using simultaneous frequency and phase-angle transition.

An instance of simultaneous phase-angle and frequency transition during a phase-angle jump at t = 0.45s is shown in Fig. 7. During unbalanced grid voltage, positive and negative sequence voltage extraction using simultaneous frequency and phase-angle transition is shown in Fig. 8.

E. Dynamic Analysis of Frequency-error Due to Phase-angle Jump

The relationship between the estimated phase-angle and frequency, which will be used during fault in this paper (as given by (4) and (7)), can be presented in the Laplace domain as

$$H(s) = \frac{\Delta\omega(s)}{\Delta\theta(s)} = \frac{k}{\tau}\frac{s}{[1/\tau + s]} \tag{9}$$

where $\tau = \frac{1}{\omega_c} = \frac{1}{2\pi f_c}$ and k is the gain. The inverse-Laplace relationship considering phase-angle $\Delta\theta(s)$ as a step function (e.g., a phase-angle jump) can be obtained as

$$\Delta\omega(t) = \frac{k}{\tau}e^{-\frac{t}{\tau}}[\Delta\theta(t)] \tag{10}$$

The rate of change of frequency deviation will be given by

$$\frac{d[\Delta\omega(t)]}{dt} = -\frac{k}{\tau^2}e^{-\frac{t}{\tau}}[\Delta\theta(t)] + \frac{k}{\tau}e^{-\frac{t}{\tau}}\frac{d[\Delta\theta(t)]}{dt} \tag{11}$$

At steady-state, $\lim_{t\to\infty}\frac{d[\Delta\omega(t)]}{dt} = 0$ for any value of k and τ. This illustrates the bounded behavior of $\Delta\omega(t)$ due to step change in $\Delta\theta(t)$. However, in case of SRFPLL, (10) can be modified and given as

$$\Delta\omega(t) = K_{PPLL} + K_{IPLL}\int V_q\, dt \tag{12}$$

Similarly (11) will be modified and given as

$$\frac{d[\Delta\omega(t)]}{dt} = K_{PPLL}\dot{V_q} + K_{IPLL}V_q \tag{13}$$

where $V_q = a - b\sin(\Delta\theta)$.

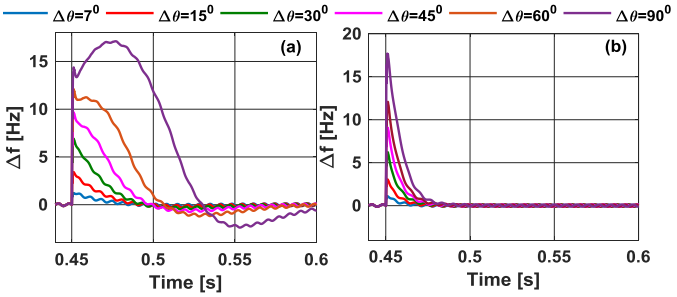

Fig. 9. Impact of phase-angle jumps on the estimated frequency error (a) SRFPLL and (b) proposed TFLL.

It can be observed that the sensitivity of $\Delta\omega(t)$ due to a PAJ ($\Delta\theta$) varies in a non-linear fashion, where term 'a' is related to the voltage drop in the line impedance and 'b' is voltage magnitude at the grid point [23]. At higher PAJ, the linear

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approximation based phase-angle estimation in case of SRFPLL pose a risk of LOS and will affect the current controller that uses such phase-angle estimation during the fault-ride through operation.

However, by using the proposed hybrid grid synchronization, the frequency sensitivity due to a PAJ can be improved as shown in (11). An example of estimated frequency error dynamics by SRFPLL and proposed TFLL in relation to various phase-angle jumps (7° to 90°) are shown in Figs. 9(a) and (b) respectively. The frequency error in case of SRFPLL is observed to experience increased oscillations due to phase-angle jumps even after 150 ms which is typically considered as low voltage ride-through duration. On the other hand, in case of proposed TFLL scheme, oscillations die out within 60-70 ms after the fault inception. However, the overshoots observed in both the cases are band limited (between ±5 Hz) to maintain the estimated frequency between 45-55 Hz in the rest of the analysis.

III. Current Control Model of Voltage Source Converter using Hybrid Grid Synchronization

The proposed hybrid grid synchronization transition scheme is implemented in this section with the grid-connected three-phase voltage source converter. The synchronization technique is applied in the closed-loop current control to enhance the frequency and phase-angle tracking capability of the converter during grid faults with PAJ. The details of the model description along with LVRT strategies are provided below.

A. System Description

The schematic of the system configuration of a grid-connected three-phase VSC along with its local controller is shown in Fig. 10.

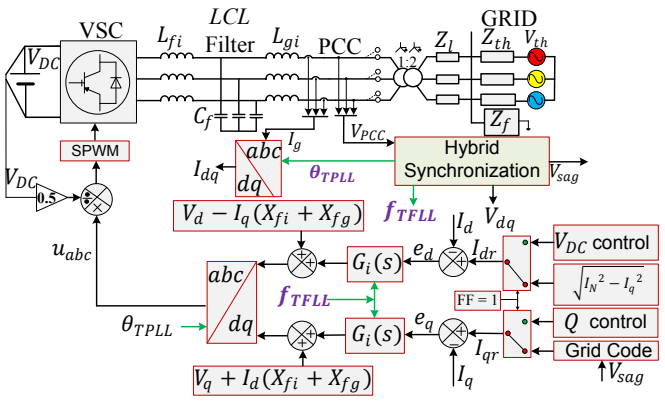

Fig. 10. Grid-connected three-phase voltage source converter (VSC) with its control structure in *dq*-frame using hybrid grid synchronization.

The closed-loop control system consists of the plant (*LCL* filter), grid synchronization unit, the current controller, and the pulse width modulation (PWM) unit. The current controllers are implemented in the synchronous reference frame (SRF). The three-phase voltages and currents at the PCC (V_{abc}, I_g) are measured and sampled using analog-to-digital converters (ADCs). V_{abc} is fed into the synchronization unit to obtain the phase-angle to be used for frame transformation (abc/dq) of the instantaneous sampled voltage and current signals. The synchronization is done using the hybrid technique discussed in Section II. During fault (i.e. FF=1 in Fig. 10), d and q-axis current references (I_{dr} and I_{qr}) are decided by the grid code. PI controllers are used for current regulation to achieve zero steady-state tracking error (i.e. $e_d = e_q = 0$). The outputs of the PI controller are transferred to the abc-frame and then fed to the sinusoidal pulse width modulation (SPWM) to generate the gate signals for the inverter switches.

B. Current Control during Asymmetrical Faults

During asymmetrical grid faults, a combination of PI and resonant controller (PI+R) is used to regulate the unbalance current as shown in Fig. 11 [29]. The purpose is to supply positive sequence balanced grid current during the fault and thus the negative sequence current references are set to zero. The resonant controller (RES) center frequency is tuned at twice the power frequency (100 Hz) in order to mitigate the ripples in the *dq*-axes current components and hence eliminate the need for sequence components extraction for current. Moreover the resonant part of the current controller is made frequency adaptive and fed by the proposed transition frequency ($\omega_{TFLL}{}^{+}$). This is done to avoid large frequency oscillations as a result of PAJ which is observed in the case of the SRFPLL estimations during grid fault. The positive sequence phase-angle ($\theta_{TFLL}{}^{+}$) is derived using the proposed frequency adaptive DSOGI filter as shown in Fig. 8.

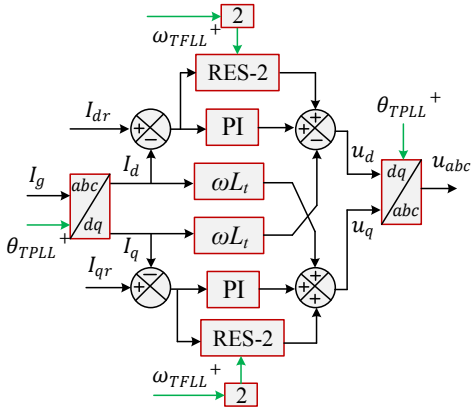

Fig. 11. Current control using proposed hybrid frequency adaptive PI+R controller to inject positive sequence current during asymmetrical faults.

The inner current controller expressions in the corresponding d and q-axis are given by

$$u_d(s) = -\omega L_t I_q + G_i(s)[I_{dr}(s) - I_d(s)] \quad (14)$$

$$u_q(s) = \omega L_t I_d + G_i(s)[I_{qr}(s) - I_q(s)] \quad (15)$$

where the current gain $G_i(s)$ is a combination of PI (K_{pi}/K_{ii}) and RES (K_{ir}) gains which is expressed as

$$G_i(s) = K_{pi} + \frac{K_{ii}}{s} + \frac{K_{ir}s}{s^2 + (2\omega_{TFLL}{}^{+})^2} \quad (16)$$

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C. Low Voltage Ride-through Operation Following Grid Code

In this work, the LVRT operation is tested with the proposed hybrid synchronization scheme during grid faults. To test the technique and current controller dynamics for grid code compliance, Danish grid code is chosen [30]. Out of several current controller strategies, constant peak current technique is implemented [31] to inject reduced active power and increased reactive power during the fault period. In this technique, the converter's d-axis current is reduced and the q-axis current is increased to provide reactive current support during the fault. Once the fault is cleared, the q-axis current is set to zero and d-axis current is set to the rated value to achieve unit power factor operation. The voltage magnitude and reactive current injection profile during the fault is shown in Fig. 12(a) and Fig. 12(b) respectively.

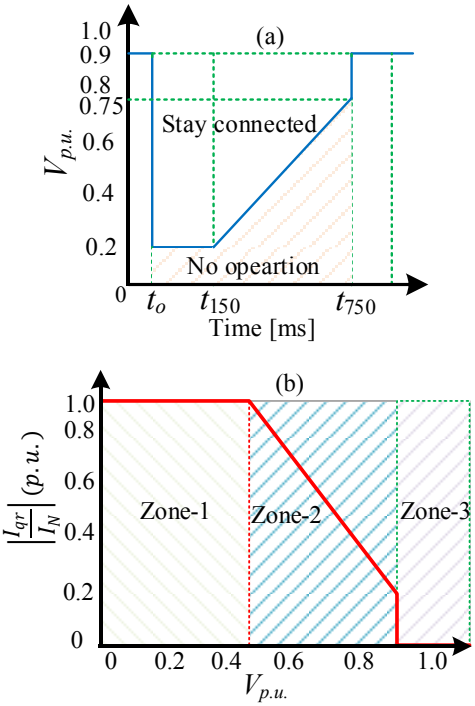

Fig. 12. (a) Voltage profile and (b) reactive current injection following low voltage ride-through (LVRT) operation.

The amount of reactive current injection is decided based on the amount of voltage drop as given by

$$\left|\frac{I_{qr}}{I_N}\right| = \begin{cases} 0, & if\ \ 0.9 < V_{p.u.} \le 1.0, \quad Zone-3 \\ 2\left(1-V_{p.u.}\right), if\ \ 0.5 < V_{p.u.} \le 0.9, Zone-2 \\ 1.0, & if\ \ 0.0 \le V_{p.u.} \le 0.5, \quad Zone-1 \end{cases} \quad (17)$$

where I_{qr}, I_N, and $V_{p.u.}$ are the reactive current, nominal current and grid voltage magnitude in p.u. respectively.

IV. Experimental Results

The performance of the current controller using the proposed hybrid grid synchronization technique is compared with the SRFPLL technique using laboratory experiments. The setup used is shown in Fig. 13. The grid voltage sag (60%) and PAJ ($\pm 45^0$) are programmed in real time using a programmable ac power supply (Regatron TC.ACS 4-quadrant grid simulator). The software model for the current controller in the SRF is interfaced with the Danfoss three-phase converter of 2.2 kW rating with *LCL* filter using a dSPACE1103 (DS1103) control board and a personal computer (PC).

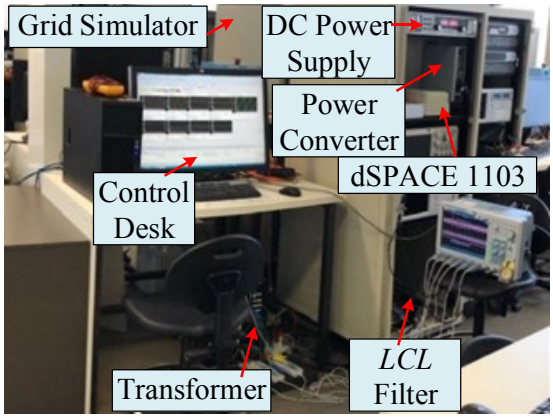

Fig. 13. Experimental setup used to test the proposed technique during faults.

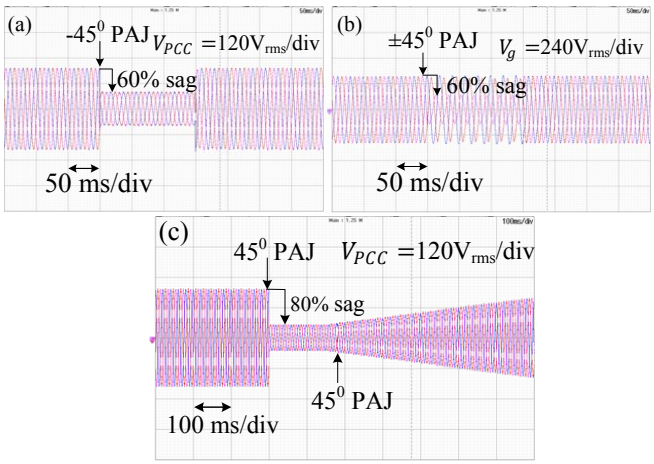

Fig. 14. Voltage profiles for (a) symmetrical, (b) asymmetrical and (c) Danish grid code generated using grid simulator.

TABLE I
CONVERTER AND CONTROLLER PARAMETERS

Parameters and Symbols	Values
Rated Power (P_{rated})	760 W
DC voltage (V_{DC})	480 V
Grid voltage (V_g)	240 V_{rms}
PCC voltage (V_{PCC})	120 V_{rms}
Nominal current (I_N)	3 A
Grid Frequency (f_g)	50 Hz
Proportional gain of the current control (k_{pi})	7
Integral/Resonant gain of the current control (k_{ii}/k_{ir})	7000
Settling time of the SRFPLL (T_{set})	120 ms
Transition time for TPLL (t_{tr})	2 ms
Grid side filter inductance (L_{fg})	0.5 mH
Converter side filter inductance (L_{fi})	1.8 mH
Filter Capacitance (C_f)	4.7 µF
Sampling frequency (f_{sam}) and Switching frequency (f_{sw})	10 kHz

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The parameters for the converters, filters, and controllers are provided in Table I. The grid voltage is reduced to 50% of the rated voltage using an isolation transformer (i.e. 120 V_{rms}). The converter output is connected to the secondary of the transformer. The voltage profiles generated for symmetrical, asymmetrical and Danish LVRT grid code using the grid simulator for tests are shown in Fig. 14. Experimental results obtained with the setup are discussed below.

A. Comparisons of Grid Synchronization Performance

The grid synchronization performance of the proposed technique is compared with the first-order SRFPLL and freezing PLL in addition to the conventional SRFPLL during the symmetrical fault. The dynamics of the estimated grid parameters are shown in Fig. 15(a), (b), (c) and (d). The first-order SRFPLL reduces the frequency oscillations as compared to the second-order. With the freezing PLL, the frequency and phase-angle become uncontrolled during the fault with a steady-state frequency error. The grid synchronization performance with the proposed hybrid technique is observed to be superior to the other techniques.

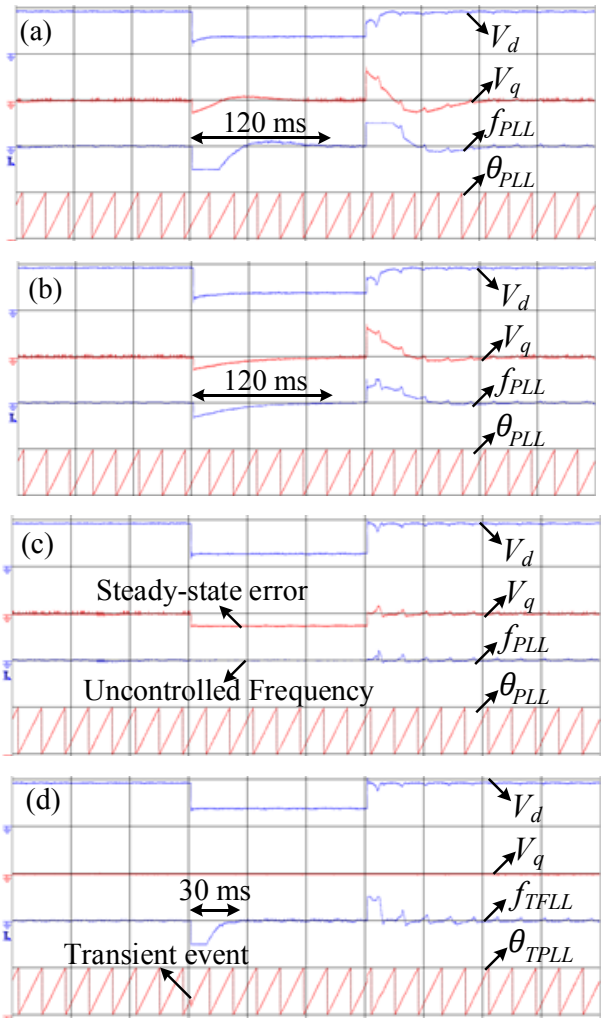

Fig. 15. Grid synchronization performance during grid fault (60% voltage sag and -45° PAJ): Response with (a) the Second-order SRFPLL (b) the First-order SRFPLL [23]. (c) Freezing-PLL [18] and (d) with the Proposed TPLL+TFLL. Ch-1: V_d [120 V/div], Ch-2: V_q [50 V/div], Ch-3: f [10 Hz/div], Ch-4: θ [2Π rad/div].

B. LVRT with Varying Transition Time of TPLL

The impact of various transition times of the TPLL on the current controller during the LVRT is explored and the responses are shown in Fig. 16.

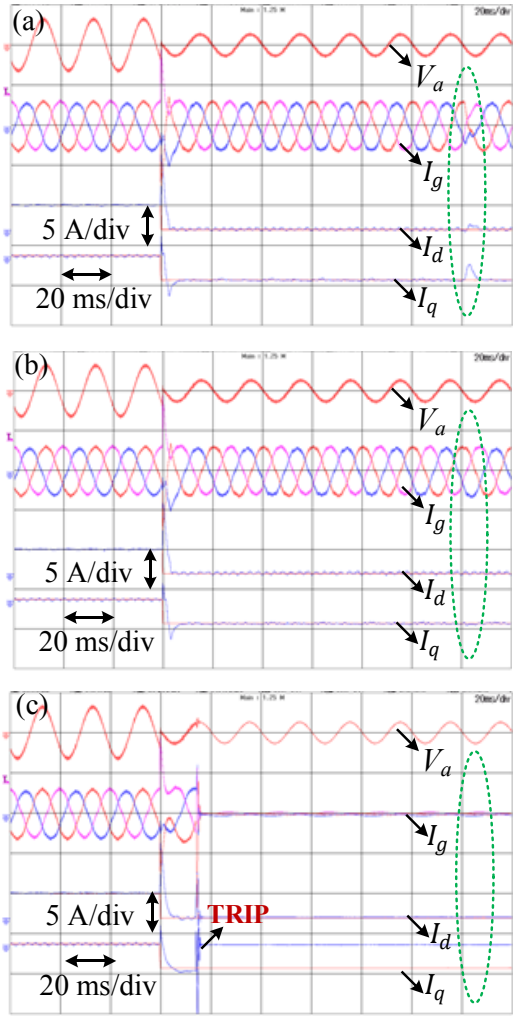

Fig. 16. Impact of varying the transition time (t_{tr}) of TPLL on current controller during LVRT: a) t_{tr} = 0.2 ms, b) t_{tr} = 2 ms, and c) t_{tr} = 20 ms.

The transition times selected for comparisons are 0.2 ms, 2 ms, and 20 ms. The current control dynamics with 0.2 ms transition time is shown in Fig. 16(a). It can be observed that it provides an overshoot in the *dq*-axes current components during the transition between SRFPLL and arctangent while following the LVRT. The overshoot is more significant during the second transition i.e. when the phase-angle used by the current controller switches from arctangent to SRFPLL. This event is highlighted using the green color circle. The impact of the overshoot is reflected in the grid current as well. Further by choosing the transition time as 2 ms, the issue of the overshoot in the grid current (especially the *q*-axis current) is resolved. The phase-angle transition dynamics with both 0.2 ms and 2 ms transition have been shown previously. It is

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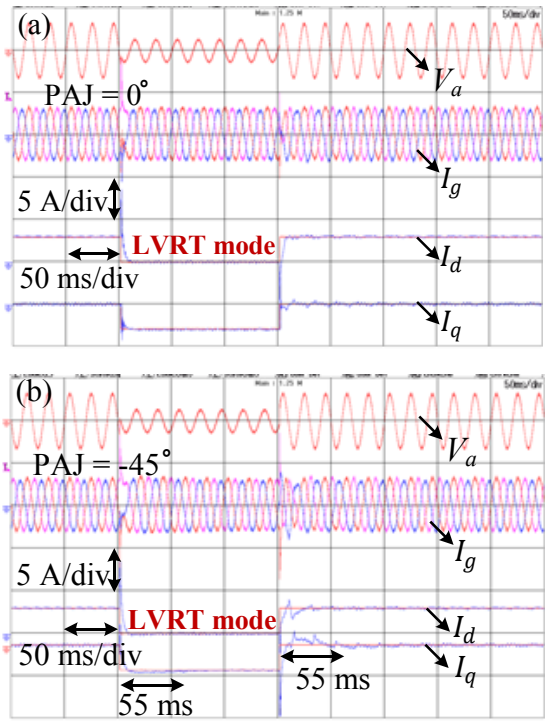
evident that the smooth phase-angle transition of TPLL with 2 ms transition time results in an improved LVRT operation as shown in Fig. 16(b). Further, a higher transition time (20 ms) is also selected to observe the current control dynamics. The response is shown in Fig. 16(c). It is noticed that choosing the transition time to such high value provides the converter with wrong phase-angle information. Hence, it leads to the tripping during the first transition event itself as highlighted in Fig. 16(c) as 'TRIP'. Therefore, the transition time for the proposed TPLL is chosen to be 2 ms in all the further experimental analysis.

C. LVRT during Symmetrical Faults

The effect of the PAJ on the current controller response can be observed from the dynamics of the dq -axis current components. Without any PAJ the SRFPLL provides smooth LVRT response as can be noticed from Fig. 17(a). In case of the occurrence of PAJ in addition to the voltage sag, I_q takes more than 2 fundamental periods corresponding to 50 Hz, to reach to the steady-state current magnitude as set for the LVRT mode i.e., 3 A as shown in Fig. 17(b). It is to be noted that, this response time for SRFPLL is dependent on the amount of PAJ. The value provided in the figure is for -45° PAJ. On the other hand, the response time of dq-axis current components of the TPLL synchronized VSC is much faster. The I_q settles within 8 ms as shown in Fig. 17(c). The TPLL is activated as soon as the phase-angle error exceeds the threshold value. During fault recovery, the performance of the SRFPLL (I_q) worsens further, while with TPLL the recovery is quite smooth. The net current magnitude remains almost the same for both techniques during faults.



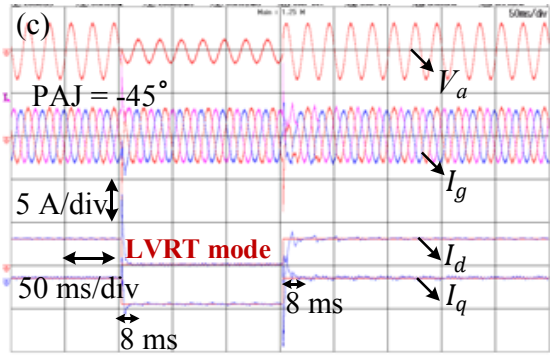
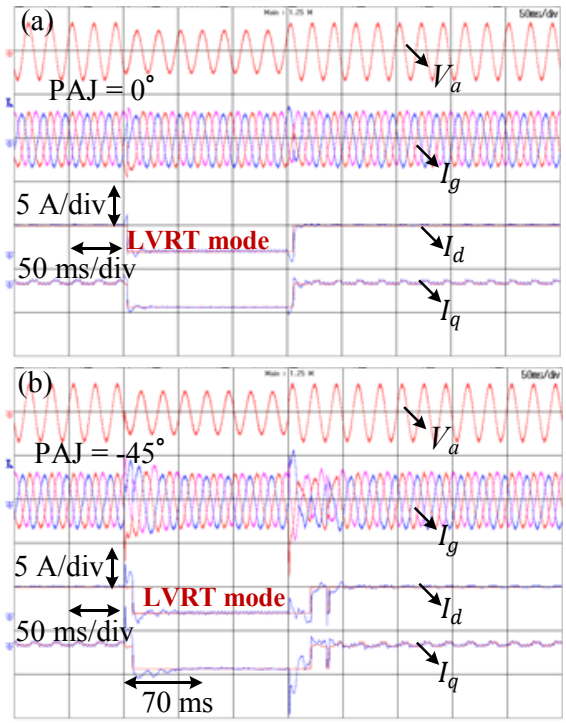


Fig. 17. Response of I_g, I_d and I_q during symmetrical faults and -45° PAJ (a) SRFPLL with no PAJ (b) SRFPLL with -45° PAJ and (c) with the proposed TPLL.

D. LVRT during Asymmetrical Faults

The current controller performance is further tested with the addition of -45° and +45° PAJ during asymmetrical sag as shown in Fig. 18 and Fig. 19 respectively. As mentioned earlier, DSOGI is used as common pre-filter to extract the positive sequence voltages. It is observed from Fig. 18(a) that with no PAJ there is smooth operation by SRFPLL technique during LVRT mode. However as seen in Fig. 18(b) and Fig. 19(a) that when a PAJ is associated during the fault, the SRFPLL suffers during the resynchronization process at the end of the LVRT mode.

In contrast, with the proposed simultaneous frequency and phase-angle transition during PAJ, the frequency adaptability of the DSOGI is enhanced and also a robust current controller dynamics is achieved during both fault inception and the recovery point as shown in Fig. 18(c) and Fig. 19(b). The resynchronization in case of +45° PAJ is observed to be smoother for SRFPLL as compared to -45° PAJ.



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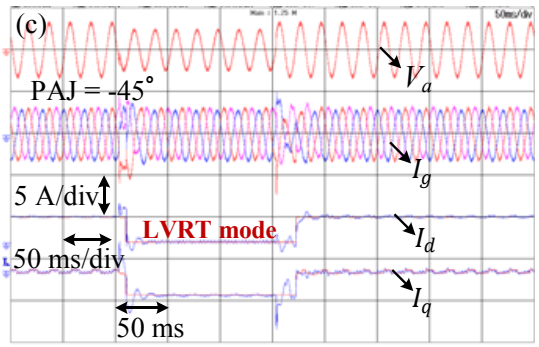

Fig. 18. Response of I_g, I_d and I_q during asymmetrical faults (fault in phase A) with (a) SRFPLL and No PAJ, (b) SRFPLL with -45° PAJ and, (c) proposed hybrid synchronization technique.

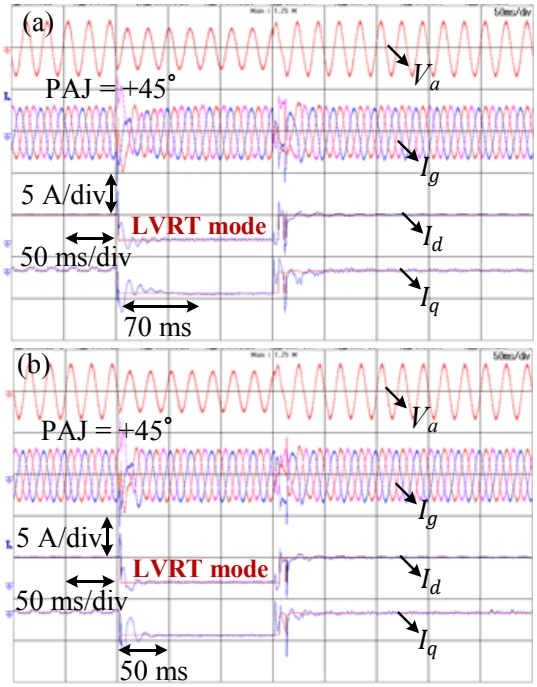

Fig. 19. Response of I_g, I_d and I_q during asymmetrical faults (fault in phase A) and +45° PAJ with (a) SRFPLL and (b) proposed hybrid synchronization technique.

E. Comparison with Voltage Feedforward Compensation

It is evident that the addition of grid voltage feedforward compensation can improve the disturbance rejection capability of the grid-connected converter. Hence its impact on the current controller during LVRT as a result of grid fault with PAJ is tested. The addition of the voltage feedforward is considered in two ways. In the first, the three-phase grid voltage measured at the PCC is added directly at the output of the current controller without its frame transformation i.e. in *abc*-frame. The response of the current controller is shown in Fig. 20(a). The second one is the filtered grid voltage feedforward compensation. In this case, the measured signal is pre-filtered and estimated *dq*-axes components are fed at the current controller output. LVRT response of the converter with this mode of compensation is shown in Fig. 20(b). It is noticed that the disturbance rejection speed (resulting from the PAJ) using voltage feedforward compensation is almost similar to the proposed hybrid grid synchronization technique. Moreover, both the techniques show improved response as compared to SRFPLL synchronization and without voltage feedforward compensation during PAJ.

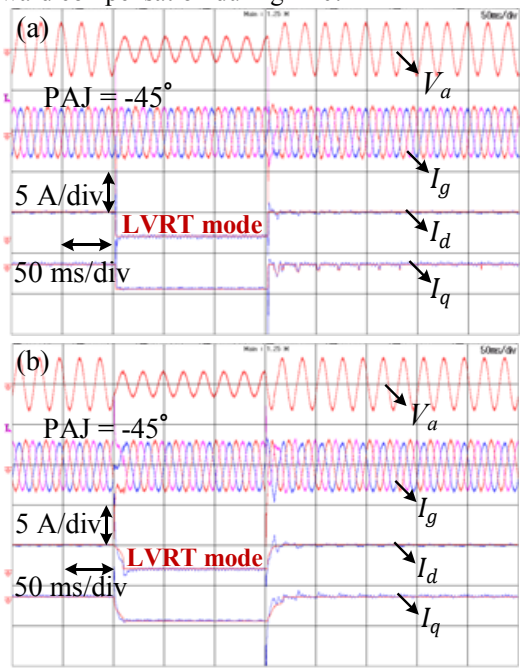

Fig. 20. Response of I_g, I_d and I_q during symmetrical faults with (a) SRFPLL with direct voltage feedforward compensation, and (b) SRFPLL with filtered voltage feedforward compensation.

F. Comparison with Other Adaptive PLL

The impact of grid fault with PAJ on the converter's LVRT operation is investigated with the adaptive SRFPLL technique. The technique proposes the switch from the second-order SRFPLL to the first-order by resetting its integral gain (K_{IPLL} = 0) on the occurrence and recovery of the fault [23].

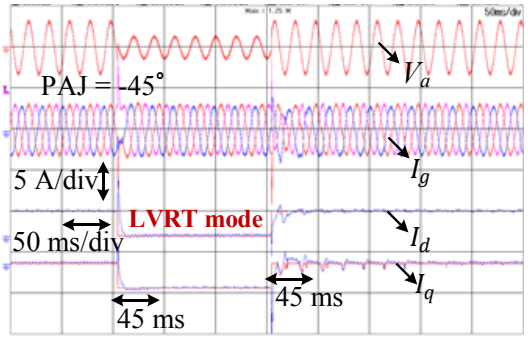

Fig. 21. Response of I_g, I_d and I_q during symmetrical faults and -45° PAJ with adaptive SRFPLL.

The considered fault is a symmetrical fault with -45° PAJ as shown in the test scenario C. The response of the current controller is shown in Fig. 21. In comparison to the response of second-order SRFPLL as shown in Fig. 17(b), adaptive SRFPLL provides a better damping to ride-through the PAJ. It reduces the current tracking time during LVRT from 55 ms to 45 ms. In contrast, when compared to the proposed technique; the improvement in the response time is not significant. As

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observed from Fig. 17(c), the proposed TPLL only takes around 8 ms to ride-through PAJ and it is independent of PLL settling time.

G. LVRT Operation during Grid Voltage Harmonics

The LVRT operation of the proposed hybrid synchronization scheme is tested with grid voltage harmonics. 3% 3rd and 3% 5th harmonics are considered. The response of the current controller is shown in Fig. 22. It is noticed that the transition scheme is not affected with the grid voltage harmonics. The tracking time is observed to be same as observed with grid voltage with no harmonics in Fig. 17(c).

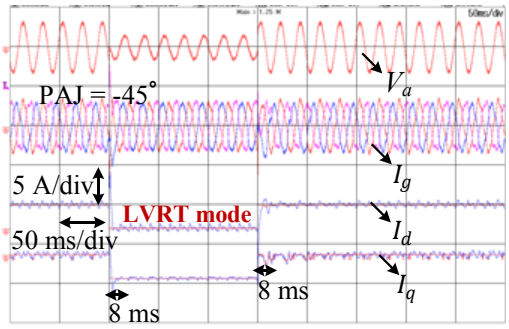

Fig. 22. Response of I_g, I_d and I_q during symmetrical faults and -45° PAJ with proposed TPLL during 3% 3rd and 3% 5th grid voltage harmonics.

H. LVRT Operation with Danish Grid Code

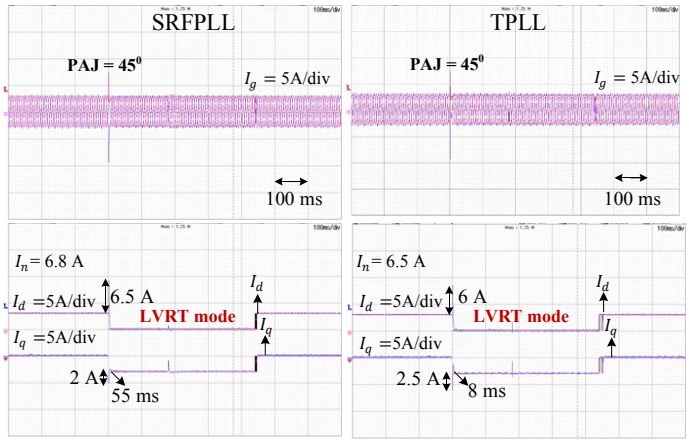

Fig. 23. Response of I_g, I_d and I_q during Danish grid code profile with 45° PAJ with conventional SRFPLL and proposed TPLL.

A performance comparison between the SRFPLL and the TPLL is done following the Danish grid code compliance. In addition to the voltage profile, PAJ of 45° is added. The current controller performance with and without PAJ is tested as shown Fig. 23. The responses of the SRFPLL and TPLL are observed to follow the same trend as discussed for the symmetrical sag and PAJ during the voltage profile. During the PAJs, the TPLL is observed to ride-through faster as compared to the SRFPLL during the LVRT operation.

V. Discussion

Grid synchronization performance of the proposed technique is compared with the conventional and other adaptive PLL techniques in Fig. 15. It is observed that, the PLL techniques are highly influenced by the PAJ during the grid fault. The classical second-order SRFPLL provides the poorest performance due to its higher settling time and insufficient damping. The damping of the PLL is improved by adaptively resetting its integral gain during the fault inception and recovery and thus called the first-order SRFPLL. However it hardly improves the settling time of the PLL, which is decided by its proportional gain. Similarly by freezing the PLL loop during the fault with PAJ results in inaccurate phase-angle tracking. The steady-state error observed in the *q*-axis voltage in this case will violate the grid code requirement while injecting active and reactive power during LVRT. In contrast, the proposed hybrid synchronization transition is seen to provide a fast and accurate phase-angle and frequency tracking as it features the independency from PLL gain tuning issue during the PAJ. The hybrid grid synchronization is dependent on the selection of the suitable transition time. From Fig. 16, it is evident that lower transition time leads to an overshoot in the *dq*-axis current of the converter during LVRT. On the other hand, higher transition time provides a bump-less current control response of the converter. It is also observed that the selection of the transition time to a very high value leads to the tripping of the converter. Therefore, much higher transition time is not recommended to allow smooth and faster current tracking during the LVRT.

Further, the impact of grid synchronization on the current control of the converter is explored during several grid faults. It is noticed that as long as the PCC voltage experiences only voltage sag, the conventional SRFPLL provides a robust LVRT. In case of the occurrence of PAJ during either symmetrical or asymmetrical faults, the proposed technique can improve the current controller dynamics much better than the SRFPLL. This is illustrated in Fig. 18 and Fig. 19. On the other hand, by adaptively switching from a second-order PLL to first-order PLL during fault, the grid current tracking time is reduced as shown in Fig. 21. However, it is higher than the proposed hybrid technique. Lastly, the proposed technique is compared with the voltage feedforward compensation control as shown in Fig. 20. Both methods have almost identical transient disturbance rejection capabilities to ride-through the PAJ. It is to be noted that the voltage feedforward compensation in a weak grid-connected converter affects the stability of its closed-loop control [25]-[27]. In contrast, the proposed technique does not consider the voltage feedforward compensation and hence can be used in a weak grid. Several adaptive voltage feedforward compensation methods can be investigated to improve the stability of the converter and simultaneously ride-through the PAJ in weak grid but it has not been in the scope of this paper.

VI. Conclusion and Future Work

This paper presents a simple and reliable hybrid grid synchronization technique for a three-phase voltage source converter. Depending on the grid voltage conditions such as normal operation or fault occurrence, it switches simultaneously between the synchronous reference frame

phase-locked loop and arctangent (in the $\alpha\beta$-frame) based phase-angle estimation and its derived frequency estimation respectively. A common transition algorithm relying on the phase-angle error between the two phase estimators is proposed to ensure a smooth transfer between them. The hybrid grid synchronization transition technique is implemented in the dq-current controller of the grid connected converter. Its performance is explored and compared with the conventional synchronous reference frame phase-locked loop with and without voltage feedforward compensation using real-time experimental findings. It is revealed that using the proposed technique, the loss of grid synchronization duration is reduced. Additionally, a more robust current controller dynamics during both fault inception and recovery is achieved in the case of both symmetrical and asymmetrical faults including voltage sag and phase-angle jumps ensuring an improved low voltage ride-through operation. The detailed simulation of the proposed transition scheme at higher voltage and higher power level grid-connected converter system will be done as future research work.

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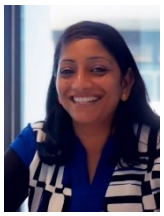

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