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Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2021.3070038

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Citation for published version (APA):
Guo, J., Chen, Y., Wang, L., Wu, W., Wang, X., Shuai, Z., & Guerrero, J. M. (2021). Impedance Analysis and Stabilization of Virtual Synchronous Generators with Different DC-Link Voltage Controllers Under Weak Grid. *IEEE Transactions on Power Electronics* , *36*(10), 11397-11408. Article 9392261. https://doi.org/10.1109/TPEL.2021.3070038

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2021.3070038, IEEE Transactions on Power Electronics

Impedance Analysis and Stabilization of Virtual Synchronous Generators with Different DC-Link Voltage Controllers Under Weak Grid

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Abstract—In recent years, the virtual synchronous generator (VSG) concept has been widely studied to integrate renewable energy sources. However, instability occurs due to the implementation of the dc-link voltage controllers under the weak grid, and its mechanism remains unclear, which is investigated in this paper. At first, the wideband *dq*-frame impedance models of the VSGs with the dc-link voltage controllers for two cases are established. Then, the stability analyses of the VSGs are compared based on these impedance models. It is revealed that the interaction dynamics between the dc-link voltage loop and the active loop lead to the negative resistor behavior of the q-q channel impedances for both VSGs, which induces the emerging oscillations of the system in a weak grid. Besides, as a useful design guideline, the parameter design of the VSGs is proposed to enhance the system stability. Finally, experimental results obtained from a 100kW prototype system show good agreement with simulated results, validating the impedance models and theoretical analysis.

***Index Terms*—virtual synchronous generator; *dq* small-signal impedance modeling; stability analyses; dc-link voltage dynamics**

I. Introduction

Voltage source converters (VSCs) have been widely utilized to integrate renewable energy sources in remote areas into the power grid. However, the emerging oscillations easily occur due to the interactions between the VSCs and the weak grid, resulting from the VSC's multiple-timescale dynamics contributed by the dc-link voltage control [1], the reactive power control [2], the phase-locked loop (PLL) [3], etc. Fortunately, the researchers have continuously improved the stability analysis methods and control methods in the literature [4]-[27].

Manuscript received Aug 3, 2020; revised Oct 30, 2020 and Jan 21, 2020; accepted Mar 19, 2021. This work was supported by the National Natural Science Foundation of China under Grant (52077070), the Zhuhai City Industrial University Research Colloboration Project (ZH22017001200019PWC), the China postdoctoral Science Foundation under Grant (2020M682551), and the State Grid Science and Technology Project (SGXJ0000KXJS1700841). *(Corresponding author: Yandong Chen.)*

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The virtual synchronous generator [5]-[6], which controls the inverter to generate an output voltage via embedding the mathematical model of synchronous generators into the controller of the inverter, has been generally studied. Due to the excellent performances, it has been applied to enhance the inertia and damping of the system [7]-[8] and provide the seamless transition between off-grid and grid-interfaced modes of the inverter [9]. The parameter design of power loops is proposed in [10] to ensure the stability and dynamic performance of the VSG. Furthermore, the potential advantages of the VSG operating under the different grid conditions are revealed in recent studies [11]-[12]. Since the VSG can replace the DQ-frame PLL with the power balanced synchronization, the possible instability issues caused by the PLL can be eliminated. The study in [11] reveals that the impedance of the VSG without the inner loop and the dc-link voltage loop behaves as the inductor that is similar to the impedance of the weak grid. To satisfy the demands of voltage and current limitation, the VSG cascaded with the voltage and current loop is studied in [13]-[14]. Besides, to enhance the stability and improve the control flexibility, the virtual impedance is added to the VSG in [15]. Its design considerations are provided in [16] for the VSG in the weak grid. The above studies do not need to consider the dc-link voltage control since the energy storage is connected to the dc side to keep the dc-link voltage constant. However, when the VSG is used to integrate renewable energy sources such as photovoltaic systems and wind power generations, the dc-link voltage needs to be regulated. In these cases, the VSG instability may occur in the weak grid due to the implementation of the dc-link voltage controllers, which needs to be further explored.

Two tools are widely used for small-signal stability analysis: the state-space method and the impedance-based method. However, the state-space method needs full knowledge of the hardware and control design of the converter, which is very difficult to obtain and validate. By contrast, the impedance that can be measured, validated, and visualized is suitable for the stability analysis of the VSG in the weak grid.

The principle of the impedance-based method is to divide the system into two independent subsystems according to the source and load parts, and then apply the Nyquist stability criterion to the impedance ratio of two subsystems [17]-[20]. At present, many small-signal impedance modeling methods are proposed in [17]-[32]. Among them, the sequence impedance and *dq*-frame impedance are widely utilized. Besides, It is believed that the sequence impedance and the *dq* impedance are the same after considering the frequency coupling [21]-[22]. Thus, *dq*-frame impedance modeling is used in this paper since it is more convenient.

The impedance-based analysis method requires a very high precision of the impedance model. At present, the *dq*-frame impedance models of single-phase[27]-[28] or three-phase converters considering many factors are gradually developed [27], such as the PLL [23]-[25], the dead-time [32], the dc-link voltage [26], the AC voltage and current loops, the controllers in the static coordinate [29], and LCL filters. Specifically, the *dq*-frame impedance model of the VSG without the dc-link voltage controller is established in [31]. Including the dc-link voltage controller, the *dq*-frame impedance model of the PLL-based VSG used for the rectifier station of the VSC-HVDC system is also studied in [12]. However, the PLL dynamics can lead to q-q channel negative resistor behavior and easily induce the oscillation when it is used for the inverter in the weak grid [23]. On the one hand, the VSGs in this paper are used to integrate renewable energy resources, which are different from those of [12], [31]. On the other hand, the differences between the dq-frame models and the abc-frame models of the control delay and sampling filters are ignored in [12], [31].

Thus, this paper focuses on the wideband *dq*-frame impedance modeling and stability analyses of the no PLL-based VSGs with different dc-link voltage controllers in the weak grid. The contributions are summarized as follows:

1) Considering the control delay, the sampling filters, and the different dc-link voltage controllers, the wideband dq-frame impedance models of the VSGs are established and verified by the impedance measurement.

2) The stability analyses of the VSG with the different dc-link voltage controllers in the weak grid are compared.

3) The parameter design is proposed for the VSGs to enhance the system stability, which can be considered as a useful design guideline.

The rest of the paper is organized as follows: Section II presents the control of the VSGs with different dc-link controllers. Section III builds and compares the wideband *dq*-frame impedance models of the VSGs with different dc voltage controllers. Section IV compares the stability analyses of the different VSGs in the weak grid. Section V shows the experimental results. Section VI draws the conclusions.

II. The Topology and Control of The VSGs

The three-phase converter connected to the ac weak grid via an *L* filter is shown in Fig. 1, where Z_g is the grid impedance; R_f is the parasitic resistance of the filter inductor L_f; C_{dc} is the dc-link regulator capacitor; u_{ga}, u_{gb}, and u_{gc} are the three-phase grid voltages; u_a, u_b, and u_c are the three-phase voltages at the point of common coupling (PCC); i_a, i_b, and i_c are the output currents; e_a, e_b, and e_c are the converter voltages; u_{dc} is the dc-

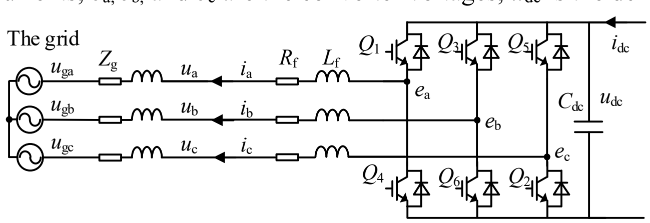

Fig. 1 The main circuit

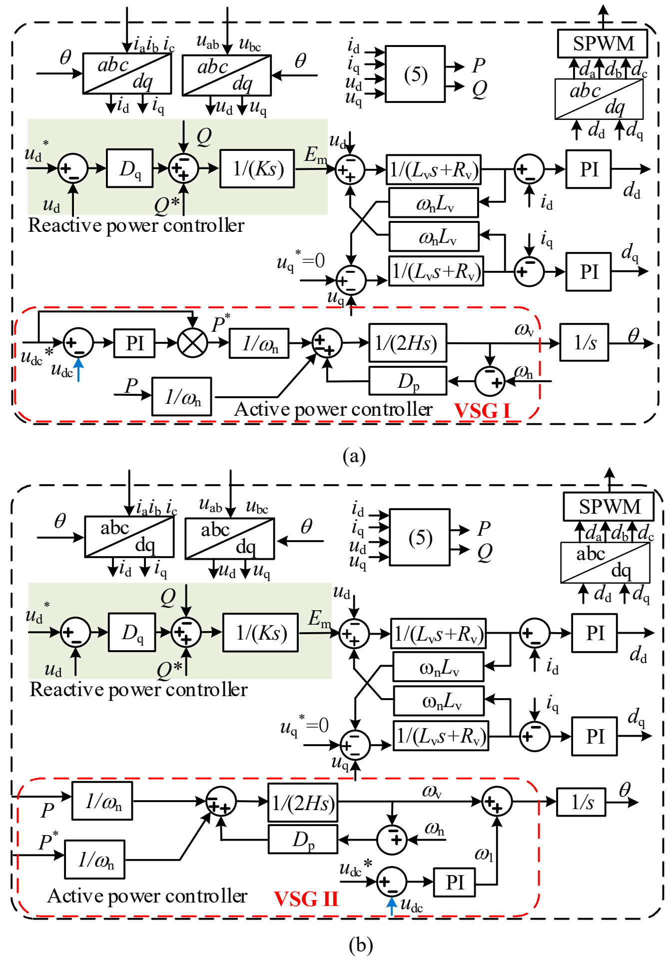

Fig. 2 The control of the VSGs (a) VSG I; (b) VSG II.

link voltage. i_{dc} is the dc-link current that flows from the renewable energy resource to the converter.

Fig. 2 shows the controls of the VSGs, where variables with an asterisk (*) correspond to reference signals; subscript d means variables in the d- channel, and subscript q means variables in the q- channel. Except for the dc-link voltage controllers, the control of the VSG I and VSG II are the same.

The dc-link voltage controller of the VSG I [8], [35] is expressed as follows:

$$P^* = -(u_{dc}^* - u_{dc})(k_{pu1} + k_{iu1}/s)u_{dc}^* \tag{1}$$

where k_{pu1} and k_{iu1} are the proportional and integral gains of the dc-link voltage proportion-integral (PI) controller of VSG I.

Besides, the dc-link voltage controller used for the droop control-based inverter [1] is introduced into the VSG II. Compared with the VSG I, the only difference is the position of the dc-link voltage controller.

$$\omega_1 = (u_{dc}^* - u_{dc})(k_{pu2} + k_{iu2}/s) \tag{2}$$

where k_{pu2} and k_{iu2} are the proportional and integral gains of the dc-link voltage PI controller of the VSG II, respectively; ω_1 is the output of the dc-link voltage PI controller of the VSG II.

The reactive power controller simulates primary voltage regulations of synchronous machines, and the active power controller of the VSG emulates the inertia and primary frequency regulation of synchronous machines [11].

$$\omega_n - \omega_v = \frac{P^* - P}{(2Hs + D_p)\omega_n} \tag{3}$$

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$$E_m = (D_q(u_d^* - u_d) + Q^* - Q)/(Ks) \tag{4}$$

where ω_v and ω_n are the output angular frequency of the VSG and the rated angular frequency of the grid, respectively; θ is the phase angle of the inner electric potential of the VSG; H is the virtual inertia constant; D_p and D_q are the damping coefficient and the voltage-drooping coefficient, respectively; K is the inertia coefficient of reactive power loop; u_d* is the rated PCC voltage in the d-axis.

The active power P and reactive power Q are given as

$$\begin{cases} P = 3/2(u_d i_d + u_q i_q) \\ Q = 3/2(u_q i_d - u_d i_q) \end{cases} \tag{5}$$

The ac voltage controllers adopt the virtual impedance to emulate the synchronous machines' electrical part [14], and the current controllers adopt PI regulators in the dq frame. L_v and R_v are the virtual resistor and inductor, respectively.

III. Wideband *DQ* Impedance Modeling of The VSGs with Different dc-Link Voltage Controllers

A. The dq-Frame Small-Signal Model of the Main Circuit

The average model of the VSC in the dq frame is given as

$$\begin{cases} L_f \dfrac{di_d}{dt} = \dfrac{1}{2} d_d u_{dc} - u_{gd} - R_f i_d \\ L_f \dfrac{di_q}{dt} = \dfrac{1}{2} d_q u_{dc} - u_{gq} - R_f i_q \end{cases} \tag{6}$$

$$C_{dc} \frac{du_{dc}}{dt} + i_{dc} = \frac{3}{4}(d_d i_d + d_q i_q) \tag{7}$$

The *dq*-frame model of the main circuit by adding the *dq*-frame small-signal perturbations to (4) and (5) is obtained as:

$$\Delta u_{dc} = \mathbf{G_1} \begin{bmatrix} \Delta i_d^s \\ \Delta i_q^s \end{bmatrix} + \mathbf{G_2} \begin{bmatrix} \Delta d_d^s \\ \Delta d_q^s \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} \Delta i_d^s \\ \Delta i_q^s \end{bmatrix} = \mathbf{Z_L}^{-1}(\mathbf{G_3}\Delta u_{dc} + \mathbf{G_4} \begin{bmatrix} \Delta d_d^s \\ \Delta d_q^s \end{bmatrix} - \begin{bmatrix} \Delta u_d^s \\ \Delta u_q^s \end{bmatrix}) \tag{9}$$

where "Δ" denotes the small-signal perturbation of a variable; I_{d0} and I_{q0} are steady-state values of the output currents; U_{dc0} is the steady-state value of the dc-link voltage; D_{d0} and D_{q0} are the steady-state values of duty cycles; $\mathbf{G_1}$=-3/(4$C_{dc}s$)[D_{d0} D_{q0}]; $\mathbf{G_2}$=-3/(4$C_{dc}s$)[I_{d0} I_{q0}]; $\mathbf{G_3}$=[D_{d0}/2 0; 0 D_{q0}/2]; $\mathbf{G_4}$=[U_{dc0}/2 0; 0 U_{dc0}/2].

Since U_{d0} can be obtained by measuring the PCC voltage and U_{q0}=0, the other values need to be calculated as

$$\begin{cases} I_{q0} = -Q_0/(1.5U_{d0}) \\ I_{d0} = \sqrt{\dfrac{2}{3}P^*/R_f + \dfrac{1}{4}U_{d0}^2/R_f - I_{q0}^2} - \dfrac{1}{2}U_{d0}/R_f \\ D_{d0} = 2(U_{d0} + I_{d0}R_f - I_{q0}\omega_n L_f)/U_{dc0} \\ D_{q0} = 2(I_{d0}\omega_n L_f - I_{q0}R_f)/U_{dc0} \end{cases} \tag{10}$$

where Q_0=D_p(U_n-U_{d0})+Q* for the VSG; Q_0= Q* for the VSI.

B. The dq Dynamics Related to the Park Transformation

One remarkable feature of the VSG is that the rotor swing equation is used for the synchronization. The phases of the VSG and the PCC voltage are not consistent at the steady-state, which is different from the PLL-based inverter. The variables in the controlled *dq* frame and the system *dq* frame for the VSG can be interconnected by [19]

$$\begin{bmatrix} \Delta f_d^c \\ \Delta f_q^c \end{bmatrix} = \mathbf{T_1} \begin{bmatrix} \Delta f_d^s \\ \Delta f_q^s \end{bmatrix} + \mathbf{T_2} \begin{bmatrix} f_{d0}^s \\ f_{q0}^s \end{bmatrix} \Delta\delta \tag{11}$$

where Δδ=Δθ; (c) represents the control variables; (s) represents the control variables.

Besides, $\mathbf{T_1}$ and $\mathbf{T_2}$ are defined as follows:

$$\mathbf{T_1} = \begin{bmatrix} \cos(\delta_0) & \sin(\delta_0) \\ -\sin(\delta_0) & \cos(\delta_0) \end{bmatrix} \tag{12}$$

$$\mathbf{T_2} = \begin{bmatrix} -\sin(\delta_0) & \cos(\delta_0) \\ -\cos(\delta_0) & -\sin(\delta_0) \end{bmatrix} \tag{13}$$

where δ_0 is the steady-state phase deviation between the system and controlled *dq* frame of the VSG;

The *dq*-frame dynamics related to the Park transformation are derived according to (9) as follows:

$$\begin{bmatrix} \Delta d_d^s \\ \Delta d_q^s \end{bmatrix} = \mathbf{T_1}^{-1} \begin{bmatrix} \Delta d_d^c \\ \Delta d_q^c \end{bmatrix} - \mathbf{G_{d1}} \begin{bmatrix} \Delta\theta \\ \Delta E_{m1} \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} \Delta i_d^c \\ \Delta i_q^c \end{bmatrix} = \mathbf{T_1} \begin{bmatrix} \Delta i_d^s \\ \Delta i_q^s \end{bmatrix} + \mathbf{G_{i1}} \begin{bmatrix} \Delta\theta \\ \Delta E_{m1} \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} \Delta u_d^c \\ \Delta u_q^c \end{bmatrix} = \mathbf{T_1} \begin{bmatrix} \Delta u_d^s \\ \Delta u_q^s \end{bmatrix} + \mathbf{G_{v1}} \begin{bmatrix} \Delta\theta \\ \Delta E_{m1} \end{bmatrix} \tag{16}$$

where ΔE_{m1} is the intermediate variable used for calculation.

From (14)-(16), $\mathbf{G_{d1}}$ models the small-signal perturbation path from Δθ to the duty cycle in the system dq frame. $\mathbf{G_{i1}}$ models the small-signal perturbation path from Δθ to the current in the controlled dq frame. $\mathbf{G_{v1}}$ models the small-signal perturbation path from Δθ to the voltage in the controlled dq frame. $\mathbf{G_{d1}}$, $\mathbf{G_{i1}}$, and $\mathbf{G_{v1}}$ are defined as follows:

$$\mathbf{G_{d1}} = \begin{bmatrix} D_{q0} & 0 \\ -D_{d0} & 0 \end{bmatrix} \tag{17}$$

$$\mathbf{G_{i1}} = \mathbf{T_2} \begin{bmatrix} I_{d0} & 0 \\ I_{q0} & 0 \end{bmatrix} \tag{18}$$

$$\mathbf{G_{v1}} = \mathbf{T_2} \begin{bmatrix} U_{d0} & 0 \\ U_{q0} & 0 \end{bmatrix} \tag{19}$$

C. Wideband dq-Frame Impedance Model of the VSG I

The *dq*-frame model of the control delay based on the transformation between *abc*-frame controllers and *dq*-frame controllers in [29]-[30]and Euler's formula is derived as:

$$\mathbf{G_{del}} = e^{-T_{del}s} \begin{bmatrix} \cos(\omega_n T_{del}) & \sin(\omega_n T_{del}) \\ -\sin(\omega_n T_{del}) & \cos(\omega_n T_{del}) \end{bmatrix} \tag{20}$$

where T_{del}=1.5/f_s, and f_s is the switching frequency.

Similarly, the *dq*-frame model of the first-order low-pass filters for voltage or current signals is derived as follows:

$$\mathbf{K_x} = \frac{1}{(1+T_x s)^2 + (\omega_n T_x)^2} \begin{bmatrix} 1+T_x s & \omega_n T_x \\ -\omega_n T_x & 1+T_x s \end{bmatrix} \tag{21}$$

where x indicates current (i) or voltage (v); T_x is the time constant of low-pass filters for the voltage or current signals.

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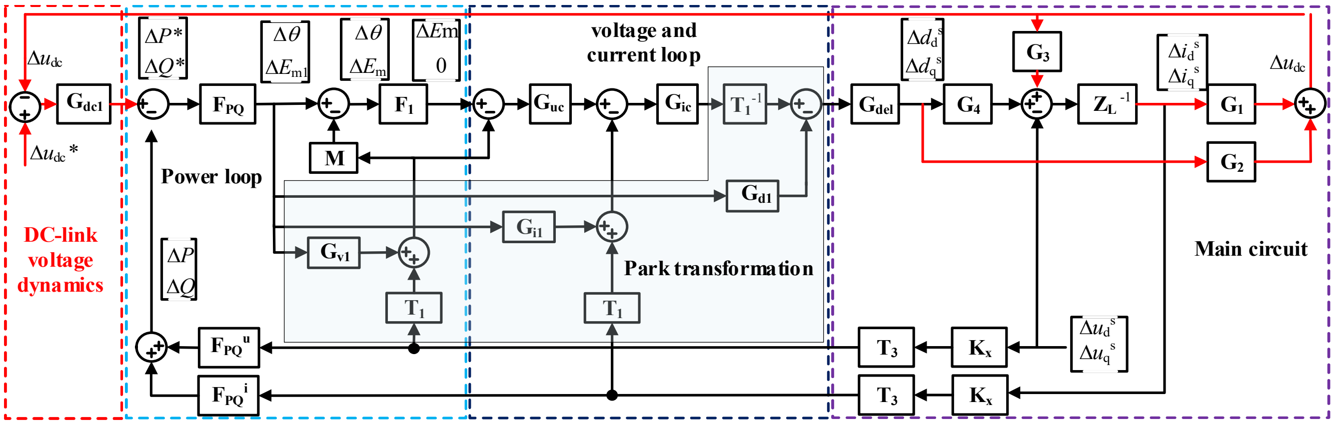

Fig. 3 The wideband *dq*-frame small-signal model of the VSG I.

Besides, the low-pass filters can lead to a phase deviation (β) between the PCC voltage and the sampling voltage, which can be ignored if the cut-off frequency is large. T_3 is defined as:

$$\mathbf{T_3} = \begin{bmatrix} \cos(\beta) & -\sin(\beta) \\ \sin(\beta) & \cos(\beta) \end{bmatrix} \tag{22}$$

The control delay and sampling filters not only enhance the coupling in the dq frame but also lead to the difference betweensteady-state values of the system and the controlled dq frame. When the switching frequency and the cut-off frequency of the low-pass filter is high, the difference can be ignored.

$\mathbf{G_{dc1}}$ represents the dc-link voltage controller of the VSG I, which is denoted by a two-by-one transfer matrix:

$$\mathbf{G_{dc1}} = \left[-(k_{pu1} + k_{iu1}/s)u_{dc}^{*} \quad 0\right]^{T} \tag{23}$$

Adding small-signal disturbances to active power controllers of the VSG I yields:

$$\begin{bmatrix} \Delta\theta \\ \Delta E_m \end{bmatrix} = -\mathbf{F_{PQ}} \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} - \mathbf{M} \begin{bmatrix} \Delta u_d^c \\ \Delta u_q^c \end{bmatrix} \tag{24}$$

where $\mathbf{F_{PQ}}$ and $\mathbf{M}$ are defined as follows:

$$\mathbf{F_{PQ}} = \begin{bmatrix} 1/(2H\omega_n s^2 + D_p\omega_n s) & 0 \\ 0 & 1/(Ks) \end{bmatrix} \tag{25}$$

$$\mathbf{M} = \begin{bmatrix} 0 & 0 \\ D_q/(Ks) & 0 \end{bmatrix} \tag{26}$$

Especially, the derivations of (24) and (35) are shown in Appendix A. By doing linearization to (5) and eliminating the steady-state values, it yields:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \mathbf{F_{PQ}^i} \begin{bmatrix} \Delta i_d^{\,c} \\ \Delta i_q^{\,c} \end{bmatrix} + \mathbf{F_{PQ}^u} \begin{bmatrix} \Delta u_d^{\,c} \\ \Delta u_q^{\,c} \end{bmatrix} \tag{27}$$

where $\mathbf{F_{PQ}^u}$ and $\mathbf{F_{PQ}^i}$ are defined as follows:

$$\mathbf{F_{PQ}^i} = \frac{3}{2} \begin{bmatrix} I_{d0} & I_{q0} \\ -I_{q0} & I_{d0} \end{bmatrix} \tag{28}$$

$$\mathbf{F_{PQ}^u} = \frac{3}{2} \begin{bmatrix} U_{d0} & U_{q0} \\ -U_{q0} & U_{d0} \end{bmatrix} \tag{29}$$

Besides, $\mathbf{F_1}$ used for the matrix transformation is defined as:

$$\mathbf{F_1} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \tag{30}$$

$\mathbf{G_{uc}}$ and $\mathbf{G_{ic}}$ represent the voltage controller matrix and the current controller matrix, respectively, which are expressed as:

$$\mathbf{G_{uc}} = \begin{bmatrix} L_v s + R_v & \omega_n L_v \\ -\omega_n L_v & L_v s + R_v \end{bmatrix}^{-1} \tag{31}$$

$$\mathbf{G_{ic}} = \begin{bmatrix} k_{pi} + k_{ii}/s & 0 \\ 0 & k_{pi} + k_{ii}/s \end{bmatrix} \tag{32}$$

According to (8), (9), (14)-(16), (24), (27), the voltage and current loops ($\mathbf{G_{uc}}$, $\mathbf{G_{ic}}$), the dc-link voltage loop ($\mathbf{G_{dc1}}$), the control delay ($\mathbf{G_{del}}$), sampling filters ($\mathbf{T_3}$, $\boldsymbol{K_x}$) and the transformation matrix ($\mathbf{F_1}$), the dq-frame small-signal model of the VSG I is shown in Fig. 3. From Fig. 3, the *dq*-frame impedance model of the VSG I is derived as:

$$\begin{cases} \mathbf{Z_{vsg1}} = \left(\mathbf{B} - \mathbf{A}\mathbf{F_{PQ}^{i}}\mathbf{K_x} + \mathbf{G_{del}}\mathbf{T_1^{-1}}\mathbf{G_{ic}}\mathbf{G_{uc}}\left(\mathbf{T_1}\mathbf{K_x} + \mathbf{F_1}\mathbf{M}\mathbf{T_1}\mathbf{K_x}\right)\right)^{-1} \cdot \\ \left(\mathbf{A}\left(\mathbf{F_{PQ}^{u}}\mathbf{K_x} + \mathbf{G_{dc}}\mathbf{G_1}\right) - \mathbf{G_{del}}\mathbf{T_1^{-1}}\mathbf{G_{ic}}\mathbf{T_1}\mathbf{K_x} - \mathbf{B}\left(\mathbf{Z_L} - \mathbf{G_3}\mathbf{G_1}\right)\right) \\ \mathbf{A} = \mathbf{G_{del}}\left(\mathbf{G_{d1}} + \mathbf{T_1^{-1}}\mathbf{G_{ic}}\left(\mathbf{G_{i1}} + \mathbf{G_{uc}}\mathbf{G_{v1}} + \mathbf{G_{uc}}\mathbf{F_1}\left(\mathbf{M}\mathbf{G_{v1}} - \mathbf{I}\right)\mathbf{F_{PQ}}\right)\right) \\ \mathbf{B} = \left(\mathbf{I} - \mathbf{A}\mathbf{G_{dc}}\mathbf{G_2}\right)\left(\mathbf{G_4} + \mathbf{G_3}\mathbf{G_2}\right)^{-1} \end{cases} \tag{33}$$

where $\mathbf{I}$ is the 2×2 unity matrix.

When the dc-link voltage controller is ignored, the impedance model ($\mathbf{Z_{vsg}}$) is obtained from (33) by setting $\mathbf{G_{dc}}$, $\mathbf{G_3}$, $\mathbf{G_2}$, and $\mathbf{G_1}$ to be zero.

$$\mathbf{Z_{vsg}} = \left(\mathbf{G_4}\left(\mathbf{A}\mathbf{F_{PQ}^{i}}\mathbf{K_x} - \mathbf{G_{del}}\mathbf{T_1^{-1}}\mathbf{G_{ic}}\mathbf{G_{uc}}\left(\left(\mathbf{T_1} - \mathbf{F_1}\mathbf{M}\mathbf{T_1}\right)\mathbf{K_x}\right)\right) - \mathbf{I}\right)^{-1} \cdot \left(\left(-\mathbf{G_4}\mathbf{A}\mathbf{F_{PQ}^{u}} + \mathbf{G_4}\mathbf{G_{del}}\mathbf{T_1^{-1}}\mathbf{G_{ic}}\mathbf{T_1}\right)\mathbf{K_x} + \mathbf{Z_L}\right) \tag{34}$$

D. Wideband dq-Frame Impedance Model of the VSG II

Adding the small-signals disturbance to the active and reactive power controllers of the VSG II yields:

$$\begin{bmatrix} \Delta\theta \\ \Delta E_m \end{bmatrix} = -\mathbf{F_{PQ}} \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} - \mathbf{M} \begin{bmatrix} \Delta u_d^c \\ \Delta u_q^c \end{bmatrix} - \mathbf{G_{dc2}}\Delta u_{dc} \tag{35}$$

where $\mathbf{G_{dc2}}$ is defined as

$$\mathbf{G_{dc2}} = \begin{bmatrix} -(k_{pu2} + k_{iu2}/s)/s \\ 0 \end{bmatrix} \tag{36}$$

Expect for (35), the small-signal models of the VSG II are the same as that of the VSG I. According to (8), (9), (14)-(16), (27), (35), the AC voltage and current loops ($\mathbf{G_{uc}}$, $\mathbf{G_{ic}}$), the dc-link voltage loop ($\mathbf{G_{dc2}}$), the control delay ($\mathbf{G_{del}}$), sampling filters ($\mathbf{T_3}$, $\boldsymbol{K_x}$) and the transformation matrix ($\mathbf{F_1}$), the dq-frame

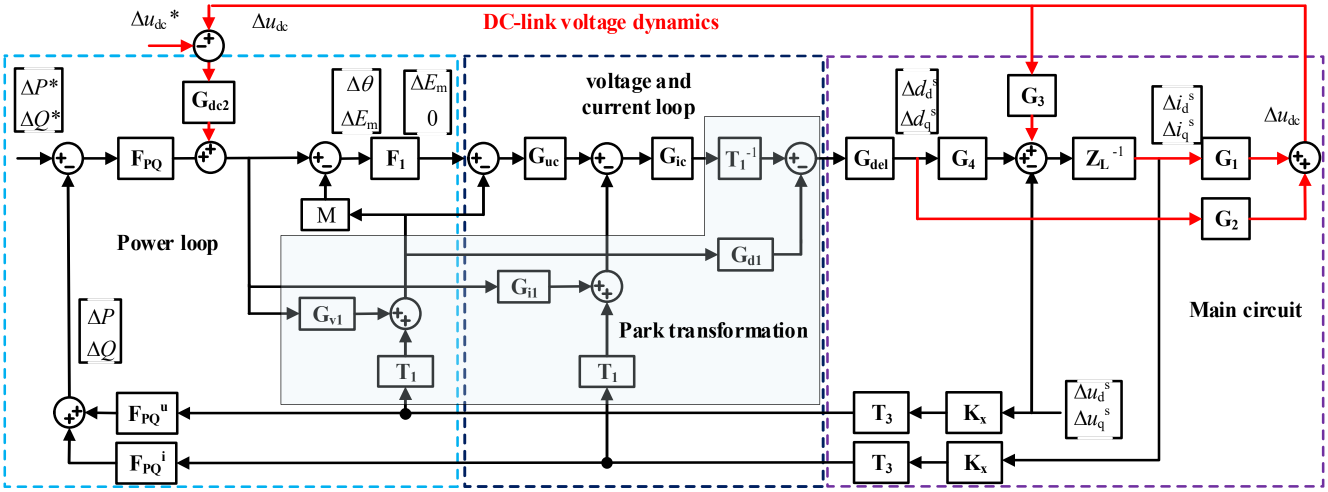

Fig. 4 The wideband *dq*-frame small-signal model of the VSG II.

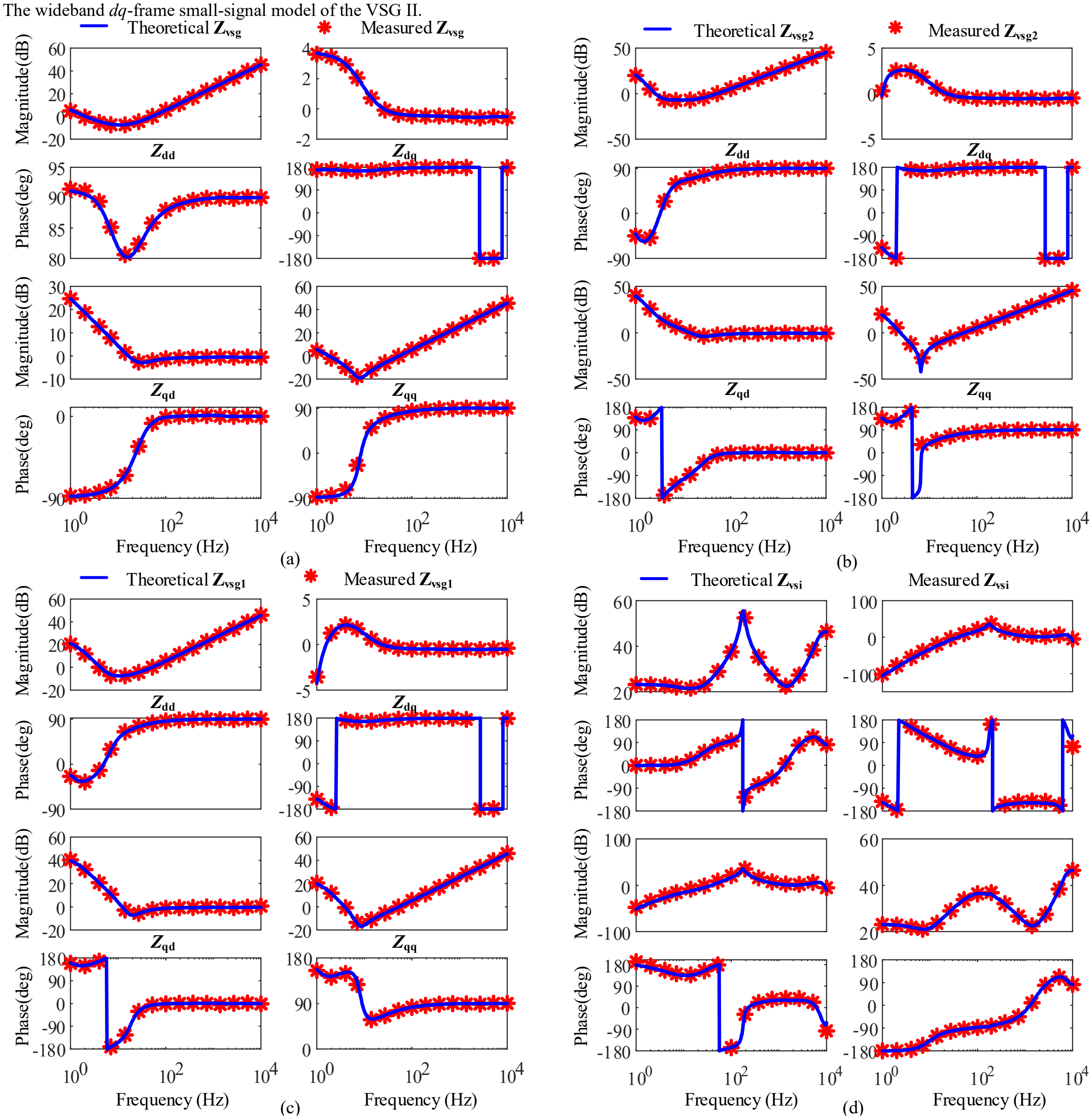

Fig.5 The *dq*-frame impedance of the VSG and VSI (a) $\mathbf{Z}_{vsg}$; (b) $\mathbf{Z}_{vsg2}$; (c) $\mathbf{Z}_{vsg1}$; (d) $\mathbf{Z}_{vsi}$.

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small-signal model of the VSG II is shown in Fig. 4. From Fig. 4, the *dq*-frame impedance model of the VSG II is derived as:

$$\begin{cases} \mathbf{Z}_{\mathbf{vsg2}}=\left(\mathbf{C}\text{-}\mathbf{A}\mathbf{F}_{\mathbf{PQ}}{}^{\mathbf{i}}\mathbf{K}_{\mathbf{x}}+\mathbf{G}_{\mathbf{del}}\mathbf{T}_{\mathbf{1}}{}^{-1}\mathbf{G}_{\mathbf{ic}}\mathbf{G}_{\mathbf{uc}}\left(\mathbf{T}_{\mathbf{1}}\mathbf{K}_{\mathbf{x}}+\mathbf{F}_{\mathbf{1}}\mathbf{M}\mathbf{T}_{\mathbf{1}}\mathbf{K}_{\mathbf{x}}\right)\right)^{-1}\cdot \\ \left(\mathbf{A}\left(\mathbf{F}_{\mathbf{PQ}}{}^{\mathbf{u}}\mathbf{K}_{\mathbf{x}}+\mathbf{F}_{\mathbf{PQ}}{}^{-1}\mathbf{G}_{\mathbf{dc}}\mathbf{G}_{\mathbf{1}}\right)\text{-}\mathbf{G}_{\mathbf{del}}\mathbf{T}_{\mathbf{1}}{}^{-1}\mathbf{G}_{\mathbf{ic}}\mathbf{T}_{\mathbf{1}}\mathbf{K}_{\mathbf{x}}\text{-}\mathbf{C}\left(\mathbf{Z}_{\mathbf{L}}\text{-}\mathbf{G}_{\mathbf{3}}\mathbf{G}_{\mathbf{1}}\right)\right) \\ \mathbf{C}=\left(\mathbf{I}-\mathbf{A}\mathbf{F}_{\mathbf{PQ}}{}^{-1}\mathbf{G}_{\mathbf{dc}}\mathbf{G}_{\mathbf{2}}\right)\left(\mathbf{G}_{\mathbf{4}}+\mathbf{G}_{\mathbf{3}}\mathbf{G}_{\mathbf{2}}\right)^{-1} \end{cases} \tag{37}$$

E. Verification and Comparative Analysis of dq-Frame Impedances of the VSGs and VSI.

TABLE I
SYSTEM PARAMETERS OF THE VSG I AND VSG II

Symbol	Value	Symbol	Value
U_{dc}	700 V	L_v	3mH
V_g	220 V	R_v	0.25Ω
L_f	3mH	D_q	321
R_f	0.0012	K	7.1
ω_n	100π	D_p	4.14
ω_{ic}	4000π(rad/s)	H	0.01 kg.m^2
ω_{vc}	4000π(rad/s)	k_{pu1}	0.4052
C_{dc}	5 mF	k_{iu1}	2.93
f_0	50Hz	k_{pu2}	0.08
P^*	10kW	k_{iu2}	1
Q^*	0	k_{ii2}	0.0395
f_s	20kHz	k_{pi2}	0.158

In Table I, the parameter design of the VSG I refers to [35]. Expect for the dc-link voltage controller parameters, the system parameters of the VSG II is the same as the VSG I. Besides, both the bandwidths of the DC-link voltage loop of the VSG I and VSG II are set as 10 Hz. To verify the impedance models of the VSGs, the impedance measurements are carried out on the MATLAB/SIMULINK. The impact caused by the measured PLL needs to be considered when the impedance measurement is implemented [33]-[34]. Fig. 5(a)-(c) shows that the theoretical models and measured results are consistent. For comparative analysis, Fig. 5(d) shows the *dq*-frame impedance of the VSI ($\mathbf{Z}_{\mathbf{vsi}}$), considering the symmetric PLL [3], the dc-link voltage controller, etc. The control method and the theoretical model of the VSI are given in Appendix B. The comparisons between the VSGs and the VSI are shown below.

1) Comparing Fig. 5(b) (c) with Fig. 5(a), it is found that the impedance of the VSG without the dc-link voltage controller ($\mathbf{Z}_{\mathbf{vsg}}$) behaves as an inductor in the middle and high-frequency range. Besides, there is no negative resistor behavior in the low-frequency range. However, both q-q channel impedances of the VSG I and VSG II behave as negative resistors with a V-type magnitude in the low-frequency range, caused by the dc-link voltage controllers. Besides, both q-d channel impedances of VSG I and VSG II are larger than that of the VSG. It means that the dc-link voltage controllers enhance the d-q channel coupling of both VSGs.

2) Comparing Fig. 5(b) (c) with Fig. 5(d), the main difference between impedances of the VSGs and the VSI is that in the middle- and high- frequency range, the VSGs behave as the inductors, while $\mathbf{Z}_{\mathbf{vsi}}$ has resonance peaks. The resonance peak is caused by the voltage feedforward and dc-link voltage controller, which might lead to high-frequency oscillations. Fortunately, the VSGs can completely avoid the high-frequency oscillations in the weak grid.

IV. COMPARISON BETWEEN STABILITY ANALYSES OF THE VSGS WITH DIFFERENT DC-LINK VOLTAGE CONTROLLERS

The weakness of the grid is distinguished by the short circuit ratio (SCR), which is defined as follows:

$$\mathrm{SCR}=\frac{S_{\mathrm{SC}}}{S_{\mathrm{N}}} \tag{38}$$

where S_{SC} is the short-circuit capacity at the point of common coupling (PCC), and S_{N} is the rated capacity of the grid-connected equipment.

The grid inductance will affect the SCR. Generally, a grid is considered strong for SCR above 20–25, weak for SCR below 6–10, and ultraweak for SCR below 2 [37]-[38].

The generalized Nyquist criterion (GNC) is applied to the ratio between the grid impedance and the impedance of the VSG to analyze the system stability, which is given by

$$L(s)=\mathbf{Z}_{\mathbf{g}}\mathbf{Z}_{\mathbf{vsg}}^{-1} \tag{39}$$

The GNC shows the system is stable if and only if the net sum of anticlockwise encirclement of the critical point (-1, *j*0) by the set of characteristic loci of L(s) equals to the total number of right-half plane poles of $\mathbf{Z}_{\mathbf{g}}$ and $\mathbf{Z}_{\mathbf{vsg}}^{-1}$. The admittance of the VSG does not have the right half-plane poles. Thus, the system is stable when the Nyquist curve of each characteristic root does not encircle (-1, *j*0). The eigenvalues are given as

$$\lambda_{1,2}(\mathrm{s})=(L_{\mathrm{dd}}+L_{\mathrm{qq}}\pm\sqrt{(L_{\mathrm{dd}}-L_{\mathrm{qq}})^2+4L_{\mathrm{qd}}L_{\mathrm{dq}}})/2 \tag{40}$$

The frequency where λ_1(s) or λ_2(s) intersects the unit circle is the predictive oscillation frequency of the system in the *dq* frame. The position where λ_1(s) or λ_2(s) intersects the unit circle determines the phase margin of the system.

Case I: The proportional gain, integral gain, and *H* are changed when SCR=5.8. Comparing Fig. 6 (a) with Fig. 6 (c), the phase margins of both VSGs are maximized when the PI gains and the virtual inertia (*H*) are selected to be the minimum values. The main difference is that the virtual inertia seriously narrows the selected range of PI gains of the VSG I. In contrast, the virtual inertia has less impact on the selected range of PI gains of the VSG II. With a small dc capacitor, the VSGs are difficult to keep stable unless the virtual inertia is very small. Thus, it would again compromise the capability to provide virtual inertia for the ac system [36]. Besides, the large inertia leads to a slow response of the power loop. Since the dc-link voltage controller of the VSG I is cascaded with the power loop, the bandwidth of the dc voltage controller of the VSG I has to be significantly lower than the bandwidth of the power loop. Thus, the PI gains of the VSG I should be decreasing while the virtual inertia is increasing. However, since the dc-link voltage controller of the VSG II is not cascaded with the power loop, the virtual inertia does not obviously limit the bandwidth of the dc-link voltage controller.

Fig. 6(b) shows that k_{pu1} has the greatest impact on the cut-off frequency (COF) from 3 Hz to 9Hz, which indicates that the VSG I may induce oscillations of 3Hz-9Hz in the *dq* frame and the oscillations of 41-47Hz and 53-59Hz in the *abc* frame. Fig. 6(d) shows that k_{pu2} has the greatest impact on the cut-off frequency (COF) from 2 Hz to 14Hz, which indicates that the VSG II may induce oscillations of 2-14Hz in the *dq* frame and the oscillations of 36Hz-48Hz and 52-64 Hz in the *abc* frame. Moreover, Fig. 6 shows that the *H* has little impact on the VSG II, while the *H* has significant effects on the PM of the VSG I.

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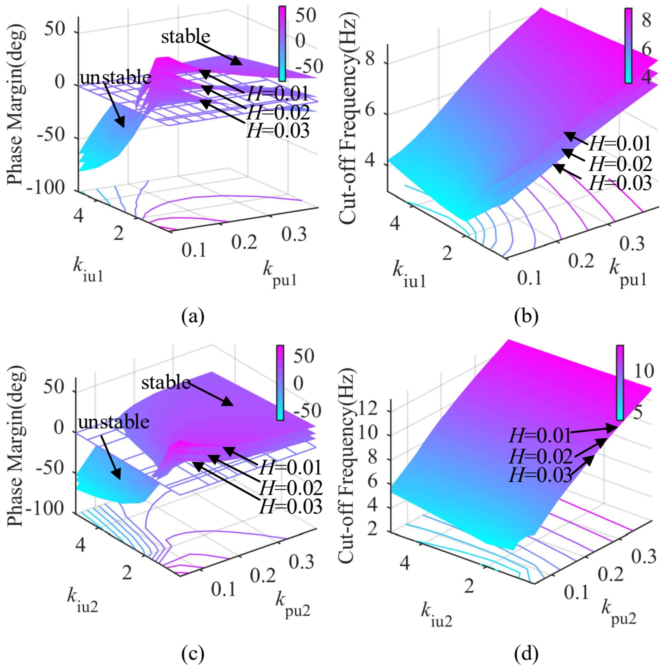

Fig. 6 Phase margin and the cut-off frequency of $\mathbf{Z}_g/\mathbf{Z}_{vsg}$ in case I (a) PM of $\mathbf{Z}_g/\mathbf{Z}_{vsg1}$; (b) COF of $\mathbf{Z}_g/\mathbf{Z}_{vsg1}$; (c) PM of $\mathbf{Z}_g/\mathbf{Z}_{vsg2}$; (d) COF of $\mathbf{Z}_g/\mathbf{Z}_{vsg2}$.

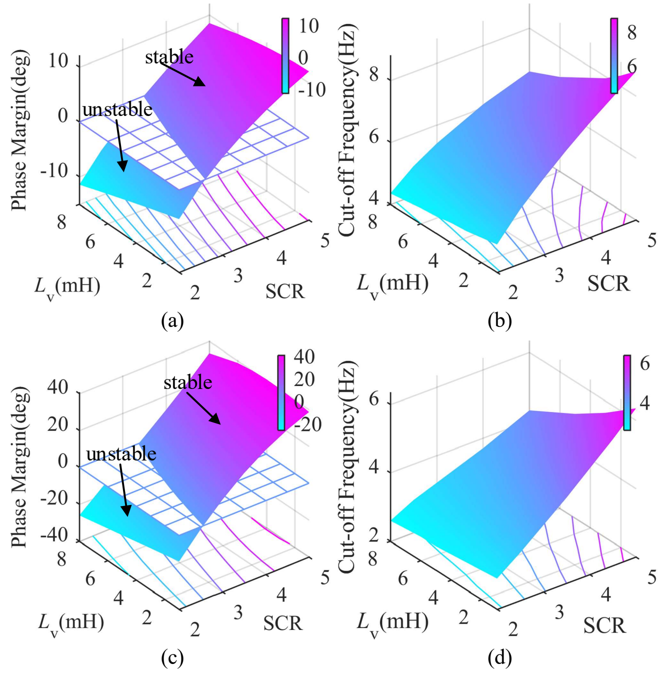

Fig. 7 Phase margin and the cut-off frequency of $\mathbf{Z}_g/\mathbf{Z}_{vsg}$ in case II. (a) PM of $\mathbf{Z}_g/\mathbf{Z}_{vsg1}$; (b) COF of $\mathbf{Z}_g/\mathbf{Z}_{vsg1}$; (c) PM of $\mathbf{Z}_g/\mathbf{Z}_{vsg2}$; (d) COF of $\mathbf{Z}_g/\mathbf{Z}_{vsg2}$.

Case II: The SCR and L_v are changed when the other parameters are fixed. Comparing Fig. 7 (a) with Fig. 7 (c), both PMs of the VSGs in two cases decrease with the SCR decreasing. Interestingly, a smaller L_v leads to a larger PM of both VSGs in two cases, thereby indicating that a smaller L_v needs to be designed to make the VSG more stable in the weak grid. Comparing Fig. 7 (b) with Fig. 7 (d), both COFs of VSGs are rising with increasing the SCR and decreasing the L_v. It is noticed that the COF of the VSG II ranges from 2 Hz to 7 Hz, while the COF of the VSG I ranges from 4Hz to 9 Hz.

Fig. 8 shows the simulation current (I_d) corresponding to Fig. 7. The VSG I is stable when the SCR=3 and L_v=1mH. The oscillation occurs at 5.5Hz in the dq frame of the VSG I when

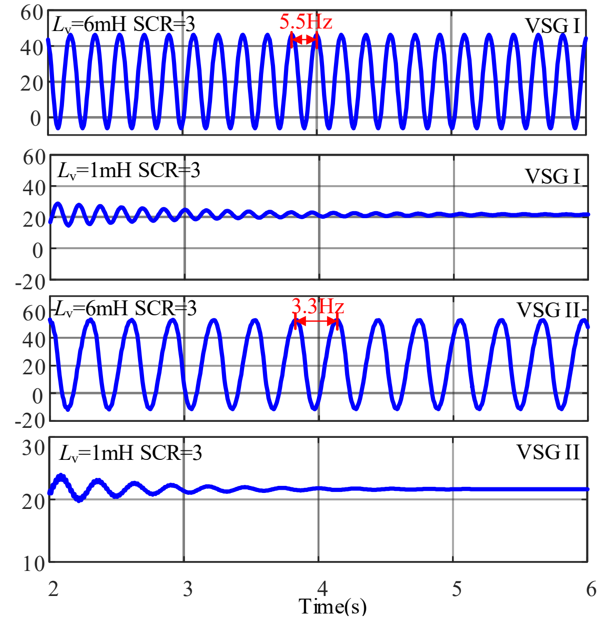

Fig. 8 Simulation current I_d of the VSGs in case II.

SCR=3 and L_v=6mH. It verifies the stability analyses of Fig. 7 (a) (b). The VSG II is stable when the SCR=3 and L_v=1mH. The oscillation occurs at 3.3Hz in the dq frame of the VSG II when the SCR=3 and L_v=6mH. The simulations in Fig. 8 verify the stability analyses in Fig. 7.

V. Experimental Results

To verify the *dq*-frame impedance models, the VSG is measured on the experimental platform as Fig. 9. The control system of the VSG is implemented in the DSP+FPGA. Specifically, the DSP TMS320F2812 is used to realize the control algorithm, and the FPGA EP2C8Q208CN is used to acquire current and voltage signals and transmit data to the DSP. Meanwhile, the high-speed A/D chip ADS8556 is used for sampling current and voltage signals. Besides, the experimental platform is composed of the impedance measurement equipment, the current source, the VSG, and the utility grid. The impedance measurement equipment is mainly composed of the perturbance injection unit, signals sampling units, and industrial personal computer (IPC). Firstly, the IPC is used to control the signals of the voltage amplitude, the phase, and the frequency of the perturbance injection unit. Then the series voltage disturbances are added to the VSG I. Afterwards, the sampling units obtain the voltage and current signals and send them to the IPC. Finally, the IPC calculates the impedances.

Fig. 10 shows the experimental results of the impedance measurement of the VSG I. The measured results are in good agreement with the theoretical model of the VSG I, which verifies the wideband impedance model of the VSG I.

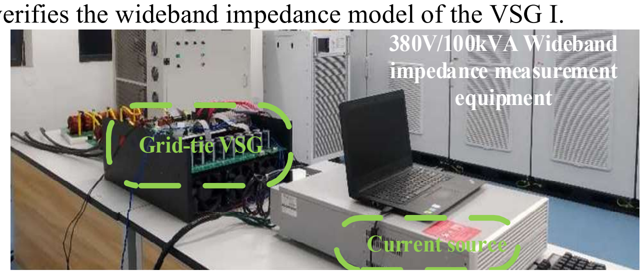

Fig. 9 Experimental platform.

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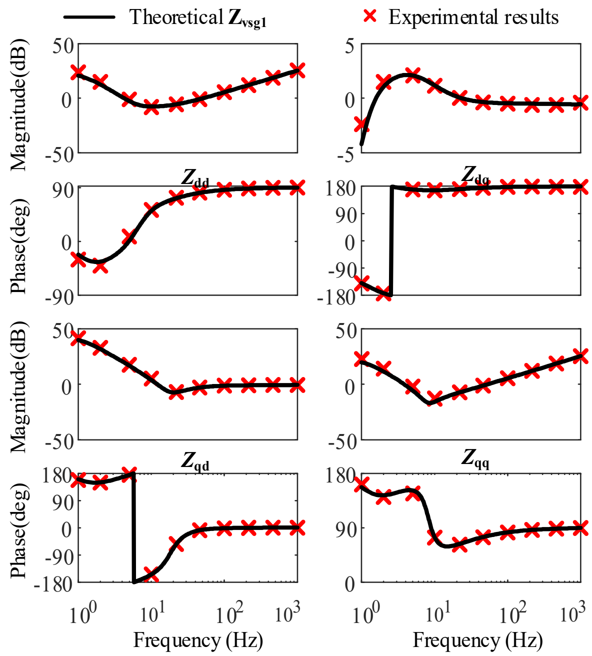

Fig. 10 Experimental results of the VSG I.

Furthermore, the experimental prototype of VSGs in two cases is built in the weak grid to verify the stability analyses presented in the previous sections. The weak grid is emulated by the utility grid in series with the line inductance. Fig. 11 (a) and (b) show that the VSG I becomes unstable when k_{iu1} increases from 0.5 to 2.2 or H increases from 0.01 to 0.03. Fig. 11 (d) shows that the VSG II becomes unstable when k_{iu2} increases from 0.5 to 2. Fig. 11 (e) shows that the VSG II is still stable when H increases from 0.01 to 0.03. The results in Fig. 11 (a), (b), (d), and (e) verify the stability analyses of Fig. 6.

Comparing Fig. 11 (c) with (a), the VSG I becomes stable when only the L_v changes from 3mH to 1mH. Comparing Fig. 11 (f) with (d), the VSG II also becomes stable when only the L_v changes from 3mH to 1mH. Comparing Fig. 11 (g) (h) with (a) (d), both the VSGs in two cases become stable when only the SCR changes from 5.8 to 12. The results in Fig. 11 also verify the stability analyses in Fig. 7.

VI. Conclusion

Based on the GNC, the stability analyses of the VSGs with different dc-link voltage controllers were studied and compared, and the three conclusions were drawn as follows:

1) The wideband dq-frame impedance models of the VSGs were built by considering the two different dc-link voltage controllers. Both proposed models were very accurate, as verified by the experimental results.

2) Both *q-q* channel impedances of the VSG I and VSG II behave as negative resistors with a V-type magnitude in the low-frequency range, caused by the dc-link voltage controllers. Thus, it induces subsynchronous oscillations of the system in the weak grid. Both VSGs are most stable in the weak grid when the PI gains and the virtual inertia are selected to be the minimum values. Besides, the decrease of the virtual stator inductor can enhance the system stability for both VSGs when the SCR is small.

3) The main difference is that the virtual inertia seriously narrows the selected range of PI gains of the VSG I. In contrast, the virtual inertia has fewer impacts on the selected range of PI gains of the VSG II.

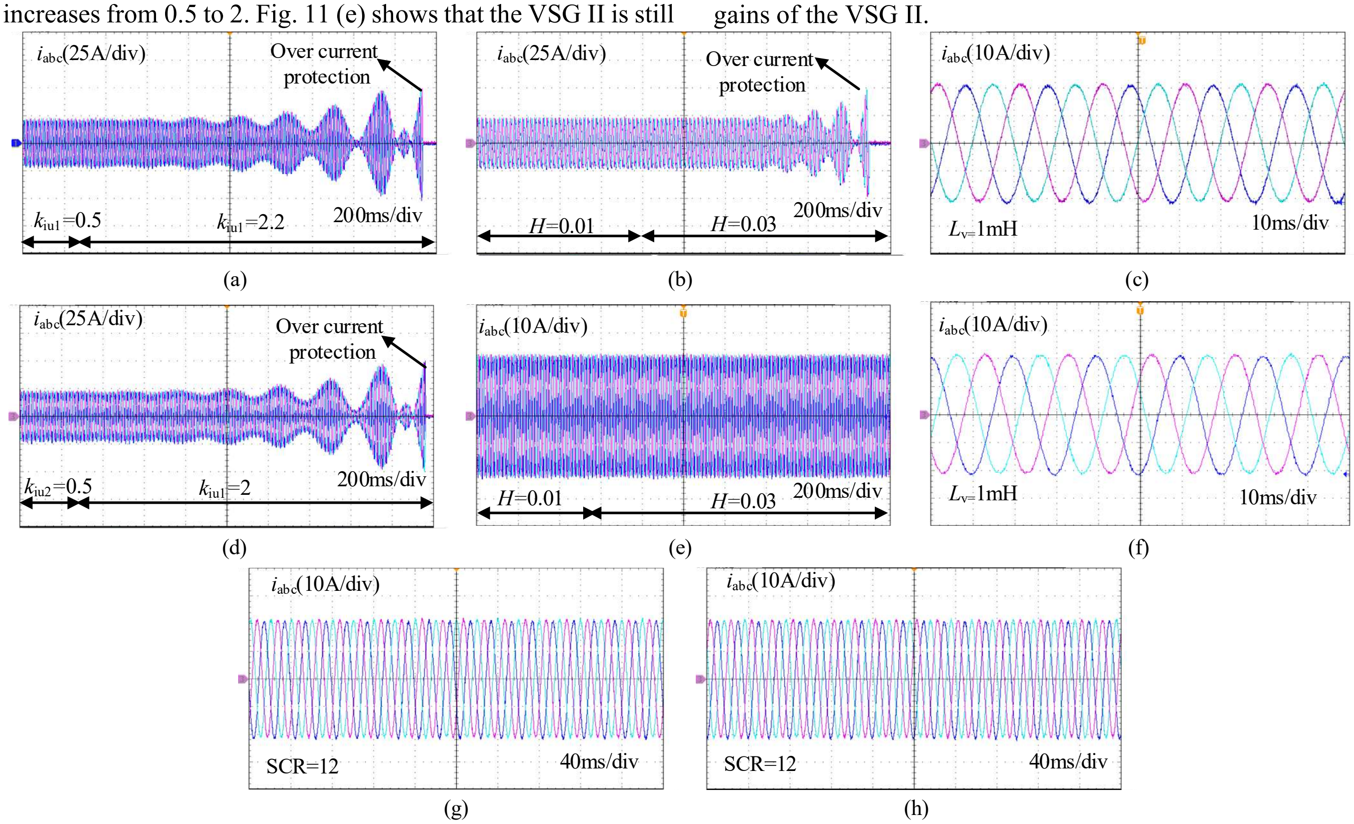

Fig. 11 Experimental waveforms of VSGs (a) VSGI, SCR=5.8, k_{pu1}=0.1, H=0.01, L_v=3mH (b) VSGI, SCR=5.8, k_{pu1}=0.4052, k_{iu1}=2.93, L_v=3mH (c) VSGI, SCR=5.8, k_{pu1}=0.1, k_{iu1}=2.2, H=0.01, L_v=1mH (d) VSGII, SCR=5.8, k_{pu2}=0.05 , H=0.01, L_v=3mH (e) VSGII, SCR=5.8, k_{pu2}=0.08, k_{iu2}=1, L_v=3mH (f) VSGII, SCR=5.8, k_{pu2}=0.05, k_{iu2}=2, L_v=1mH, H=0.01 (g) VSGI, SCR=12, k_{pu1} =0.1, k_{iu1}=2.2, L_v=3mH, H=0.01 (h) VSGII, SCR=12, k_{pu2}=0.05, k_{iu2}=2, L_v=3mH, H=0.01.

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APPENDIX

A. Derivations of (24) and (35)

To order to make Fig.3 and Fig. 4 easy to understand, the small-signal derivation of (24) and (35) are given below.

Based on (2), the small-signal model can be expressed as:

$$\Delta E_{\mathrm{m}}=\frac{-D_{\mathrm{q}}\Delta u_{\mathrm{d}}{}^{\mathrm{c}}-\Delta Q}{Ks} \tag{41}$$

From Fig. 2 (a), the active power loop of the VSG I is given as follows:

$$\theta=\frac{1}{\mathrm{s}}(\omega_{\mathrm{n}}-\frac{P^{*}-P}{(2Hs+D_{\mathrm{p}})\omega_{\mathrm{n}}}) \tag{42}$$

According to (41), the small-signal model can be derived as:

$$\Delta\theta=\frac{\Delta P}{(2Hs+D_{\mathrm{p}})\mathrm{s}\omega_{\mathrm{n}}}) \tag{43}$$

According to (40) and (42), $[\Delta\theta\ \Delta E_{\mathrm{m}}]^{\mathrm{T}}$ can be obtained as:

$$\begin{bmatrix}\Delta\theta\\ \Delta E_{m}\end{bmatrix}=-\begin{bmatrix}\frac{1}{(2Hs^{2}+D_{\mathrm{p}}s)\omega_{\mathrm{n}}} & 0\\ 0 & \frac{1}{Ks}\end{bmatrix}\begin{bmatrix}\Delta P\\ \Delta Q\end{bmatrix}-\begin{bmatrix}0 & 0\\ \frac{D_{\mathrm{q}}}{Ks} & 0\end{bmatrix}\begin{bmatrix}\Delta u_{\mathrm{d}}^{\mathrm{c}}\\ \Delta u_{\mathrm{q}}^{\mathrm{c}}\end{bmatrix} \tag{44}$$

According to the definition of $\mathbf{F}_{\mathbf{PQ}}$ and $\mathbf{M}$, (24) equals (44).

From Fig. 2 (b), the active power loop of VSG II is given as:

$$\theta=\frac{1}{\mathrm{s}}(\omega_{\mathrm{n}}-\frac{P^{*}-P}{(2Hs+D_{\mathrm{p}})\omega_{\mathrm{n}}}+(u_{\mathrm{dc}}^{*}-u_{\mathrm{dc}})(k_{\mathrm{pu2}}+\frac{k_{\mathrm{iu2}}}{s})) \tag{45}$$

According to (45), the small-signal model can be derived as follows:

$$\Delta\theta=\frac{1}{\mathrm{s}}(\frac{\Delta P}{(2Hs+D_{\mathrm{p}})\omega_{\mathrm{n}}}-(k_{\mathrm{pu2}}+\frac{k_{\mathrm{iu2}}}{s})\Delta u_{\mathrm{dc}}) \tag{46}$$

According to (41) and (46), $[\Delta\theta\,\Delta E_{\mathrm{m}}]$ can be obtained as:

$$\begin{bmatrix}\Delta\theta\\ \Delta E_{m}\end{bmatrix}=-\begin{bmatrix}\frac{1}{(2Hs^{2}+D_{\mathrm{p}}s)\omega_{\mathrm{n}}} & 0\\ 0 & \frac{1}{Ks}\end{bmatrix}\begin{bmatrix}\Delta P\\ \Delta Q\end{bmatrix}- \begin{bmatrix}0 & 0\\ \frac{D_{\mathrm{q}}}{Ks} & 0\end{bmatrix}\begin{bmatrix}\Delta u_{\mathrm{d}}^{\mathrm{c}}\\ \Delta u_{\mathrm{q}}^{\mathrm{c}}\end{bmatrix}-\begin{bmatrix}\frac{1}{s}(k_{\mathrm{pu2}}+\frac{k_{\mathrm{iu2}}}{s})\\ 0\end{bmatrix}\Delta u_{\mathrm{dc}} \tag{47}$$

Based on the definition of $\mathbf{F}_{\mathbf{PQ}}$, $\mathbf{M}$, and $\mathbf{G}_{\mathbf{dc2}}$, (35) equals (47).

B. the dq-Frame Impedance Model of the VSI

Fig. 12 shows that the control of the VSI has the symmetric PLL [3], the current loop, the dc-link voltage controller, and the voltage feedforward with the low-pass filters [24], where V_1 is the steady-state PCC voltage aligned to the d-axis.

TABLE II
SYSTEM PARAMETERS OF THE VSI

Symbol	Description	Value
k_{p1}	Proportional gain of VSI current controller	0.046
k_{i1}	Integrator gain of VSI current controller	0.1842
k_{pu1}	Proportional gain of VSI voltage controller	1.8
k_{iu1}	Integrator gain of VSI voltage controller	210
k_{ppll}	Proportional gain of PLL	0.2529
k_{ipll}	Integrator gain of PLL	10.9988

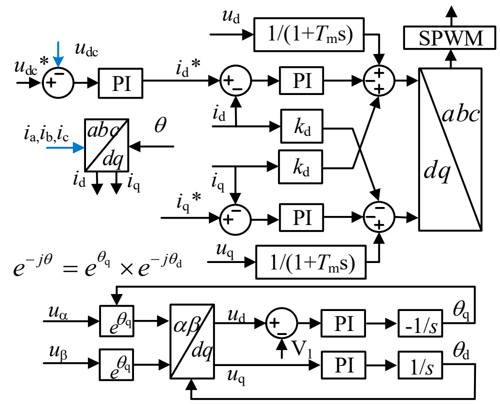

Fig. 12 The control of the VSI.

Based on the small-signal model of the control parts and the main circuits, the dq-frame impedance of the VSI is derived as:

$$\begin{cases}\mathbf{Z}_{\mathbf{vsi}}=\left(\mathbf{D}+\mathbf{G}_{\mathbf{del}}\left(\left(\left(\mathbf{G}_{\mathbf{ci}}-\mathbf{G}_{\mathbf{dei}}\right)\mathbf{G}_{\mathbf{i}}+\mathbf{G}_{\mathbf{4}}\mathbf{G}_{\mathbf{v}}\right)-\mathbf{G}_{\mathbf{d}}\right)\mathbf{T}_{3}\mathbf{K}_{\mathbf{x}}\right)^{-1}\cdot\\ \left(\mathbf{D}\left(\mathbf{Z}_{\mathbf{L}}+\mathbf{G}_{3}\mathbf{G}_{1}\right)-\mathbf{G}_{\mathbf{del}}\left(\mathbf{G}_{\mathbf{ci}}-\mathbf{G}_{\mathbf{dei}}\right)\mathbf{T}_{3}\mathbf{K}_{\mathbf{x}}-\mathbf{G}_{\mathbf{del}}\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{uc}}\mathbf{G}_{1}\right)\\ \mathbf{D}=\left(\mathbf{I}+\mathbf{G}_{\mathbf{del}}\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{uc}}\mathbf{G}_{2}\right)\left(\mathbf{G}_{4}+\mathbf{G}_{3}\mathbf{G}_{2}\right)^{-1}\end{cases} \tag{48}$$

where $\mathbf{G}_{\mathbf{d}}=G_{\mathrm{m}}\begin{bmatrix}D_{\mathrm{d0}} & -D_{\mathrm{q0}}\\ D_{\mathrm{q0}} & D_{\mathrm{d0}}\end{bmatrix}$; $\mathbf{G}_{\mathbf{i}}=G_{\mathrm{m}}\begin{bmatrix}I_{\mathrm{d0}} & -I_{\mathrm{q0}}\\ I_{\mathrm{q0}} & I_{\mathrm{d0}}\end{bmatrix}$;

$$\mathbf{G}_{\mathbf{v}}=I-G_{\mathrm{m}}\begin{bmatrix}U_{\mathrm{d0}} & -U_{\mathrm{q0}}\\ U_{\mathrm{q0}} & U_{\mathrm{d0}}\end{bmatrix};\ G_{\mathrm{m}}=H_{\mathrm{PLL}}/(\mathrm{s}+H_{\mathrm{PLL}}U_{\mathrm{d0}});$$

$$H_{\mathrm{PLL}}=k_{\mathrm{ppll}}+k_{\mathrm{ipll}}/s\ ;\ \mathbf{G}_{\mathbf{uc}}=\begin{bmatrix}k_{\mathrm{pu3}}+k_{\mathrm{iu3}}/s & 0\end{bmatrix}^{\mathrm{T}};$$

$$\mathbf{G}_{\mathbf{dei}}=\begin{bmatrix}0 & 2\omega_{\mathrm{n}}L/U_{\mathrm{dc0}}\\ -2\omega_{\mathrm{n}}L/U_{\mathrm{dc0}} & 0\end{bmatrix};$$

$$\mathbf{G}_{\mathbf{ci}}=\begin{bmatrix}k_{\mathrm{p1}}+k_{\mathrm{p1}}/s & 0\\ 0 & k_{\mathrm{p1}}+k_{\mathrm{p1}}/s\end{bmatrix};$$

$$\mathbf{G}_{\mathbf{5}}=\begin{bmatrix}2/(U_{\mathrm{dc0}}(1+T_{\mathrm{m}}\mathrm{s})) & 0\\ 0 & 2/(U_{\mathrm{dc0}}(1+T_{\mathrm{m}}\mathrm{s}))\end{bmatrix}.$$

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2021.3070038, IEEE Transactions on Power Electronics

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