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A Single-Source Nine-Level Boost Inverter with A Low Switch Count

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***Abstract*—Switched-capacitor-based multilevel inverters for boost-type dc-ac power conversions usually exhibit a trade-off between the switch count and switch-voltage rating, i.e., a reduction of one necessitating an increase of the other. Such a dilemma is well addressed in this paper by proposing a novel single-phase nine-level inverter based on a switched-capacitor network with a single switch. The proposed inverter then reduces the number of switches while generating a boosted dc-link voltage. A unique six-switch full-bridge cooperating with a low-frequency half-bridge further steps-up the output voltage with a quadruple gain. The voltage stresses on the power devices are, however, maintained low even under the boosted high output voltage, as all the switches/diodes can be clamped to any of the low-voltage capacitors. Consequently, low-voltage power devices can be utilized, reducing the overall power loss. Detailed theoretical analysis, calculations, and design considerations of the proposed inverter are provided. Comparisons with the prior-art inverters illustrate its advantages. Simulations and experimental tests on a 1-kVA inverter prototype verify the above-claimed benefits.**

***Index Terms*—Boost multilevel inverter, switched capacitor, low switch count, low voltage stresses.**

I. Introduction

DEVELOPING renewable energies and expanding the adoption of electric vehicles are two main effective approaches for addressing environmental concerns. Both strategies necessarily involve some power conversions from renewable energy sources (e.g., solar) to the electric grids/loads. In such an energy process, one type of commonly-seen power converters is the voltage-source multilevel inverter (MLI) owing to its advantages including a nearly-sinusoidal output voltage, low voltages and thus low *dv/dt* on the semiconductor devices, and a low requirement on the output filter [1].

In general, the traditional MLIs fed by a single dc source can be grouped into two categories: the neutral-point-clamped (NPC) inverter [2], and the flying capacitor (FC) inverter [3]. One common feature shared by both NPC and FC inverters is that the output voltage is always less than the input voltage, which usually requires certain dc-dc boost stages to achieve a high dc-link voltage from the low-voltage energy sources [4]. The numbers of the passive elements and switches are therefore increased, resulting in a high power loss and thus low conversion efficiency [5]. Recently, it has been proven that the voltage boosting can be achieved without additional dc-dc circuits, if boost-type MLIs are utilized [6]–[20].

The attempt to explore voltage boosting for the basic three-level (3L) NPC inverter is initiated by integrating the *Z*-source network [6]. The resultant *Z*-source NPC inverter, however, requires two isolated dc sources, each connected to an "*X*-shape" *LC* network. The volume and complexity of the inverter are thus increased. Modifications are subsequently made with a single dc source. However, the efficiency obtained by the *Z*-source NPC inverter is relatively low [7], due to the high power loss on the *Z*-source network.

Investigation of the step-up MLIs without the inductive component is latterly carried out on a multi-dc-link inverter formed by switched capacitors (SCs) [8]. However, the number of switches required by the SC circuit is relatively large. That is, the reduction of the switch count for SC-based MLIs remains a challenge that has been subsequently addressed in [9]. Nonetheless, a back-end full-bridge (HB) to unfold the stepped dc voltage is required, and it has to use switches withstanding the maximum of the output voltage (V_{omax}). Despite that, the voltage-boost capability achieved by the series/parallel operation makes the SC circuit be increasingly used in boost-type MLIs [10]–[21].

For example, a boosting five-level (5L) inverter with an inherent reversal of its voltage polarity is presented in [10]. However, it still requires nine switches, more than those of the traditional 5L NPC/FC inverter. Another 5L boost inverter with a reduced switch count is presented in [11]. However, the maximum voltage on the switches is equal to V_{omax}, meaning that high-voltage and lossy semiconductor devices are required.

Similarly, a seven-level (7L) boost inverter using a unique SC circuit is developed in [12] (Fig. 1(a)). It utilizes the minimum number of switches to achieve a voltage gain of 3. However, some of the switches must also endure V_{omax}. It may, therefore, be more appealing to use the active (or T-type) NPC structure with bidirectional switches to reduce the voltage stresses, as discussed in [13]−[15], with the one [15] shown in (Fig. 1(b)) . The utilization of bidirectional switches, however, increases the switch count in practice.

Recently, nine-level (9L) SC-based inverters have also demonstrated the capability of achieving higher voltage gains [16]–[21]. One example based on an extendable SC module is presented in [16]. It induces low voltages on its switches compared to inverters from [17] and [18], all of which use no diodes. However, to achieve a 9L output voltage, three SC modules (each using five switches) are required [16], and

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therefore the total switch count increases rapidly. The number of switches can be reduced to a lower level if diodes are used [19]–[21]. Particularly, in [20] and [21], the switch count is significantly reduced based on a symmetrical SC module using two switches and two diodes, although, some switches are required to withstand a high voltage of V_{omax}.

In line with the discussions above, there is a trade-off for the SC-based boost MLIs. That is, using low-voltage switches usually requires a larger number of switches and their associated gate-driver circuits, while having a low switch count requires high-voltage switches. Moreover, the ability to clamp the neutral of the ac output is lost in certain cases, which may limit the applications of the SC-based boost MLIs [22], [23].

To address these issues, this paper proposes a novel 9L boost inverter, as shown in Fig. 1 (c), where an SC network is seen at the input-side circuit and a half-bridge at the output-side circuit of the inverter, with a six-switch full-bridge (6SFB) connecting them in between. In total, the proposed MLI uses nine unidirectional switches, eight (S_1–S_4, and S_6–S_9) of which are connected with anti-parallel diodes. One switch (S_5) is in a series connection with a diode. It can then be realized by an IGBT with the reverse-blocking capability.

Notably, although the 7L inverter in [12] uses a similar SC structure for voltage boosting, it induces the maximum voltage stresses (V_{omax}) on its devices. On the other hand, the 7L inverter in [15] reduces the maximum voltage stresses on switches by cascading a 3L T-type converter with an HB. An additional switch is used to charge the floating capacitor of the HB [15]. Together, both 7L inverters in [12] and [15] again show the aforementioned tradeoff which usually exists in the available SC MLIs.

Differently, the focus of the proposed solution is to develop an SC MLI that reduces the maximum voltage ratings of the components while maintaining a low switch count (or switch-per-level ratio). To achieve this, it is necessary to explore novel SC MLIs. And the 9L inverter proposed features:

1) a high dc-to-ac voltage boosting gain (4 folds), facilitating the use of a single low-voltage dc source;
2) low voltage stresses on the components, avoiding thus high voltage-rating devices;
3) 9L output voltage with a low switch count (9 switches).

In terms of the circuit topology, the derivation of the proposed 9L inverter may have been regarded as a cascaded connection of an SC unit and an HB unit (S_6–S_9, see Fig. 1), assisted by the switch S_5. A similar conception applies to the 9L inverter presented in [16] yet using 19 switches. Therefore, although there are lots of derived topologies using the two units, only with appropriate circuit modifications and/or combinations with innovations, can the proposed 9L derivative achieve the intended performances of a low switch count and low voltage stresses. Such a derivation, however, does not overlay the novelty of the proposed SC-based boost MLI that is not explored in the literature, especially considering the aforementioned advantages and improvements when being compared to its counterparts [10]–[21], to be elaborated in the later sections through a comparative study. Furthermore, the proposed MLI forms a single-phase dc-to-ac common-ground structure since the neutral point that connects to the dc link (middle point) can also serve as the ground, which then suppresses the common-mode ground leakage current, as discussed in [24]–[27].

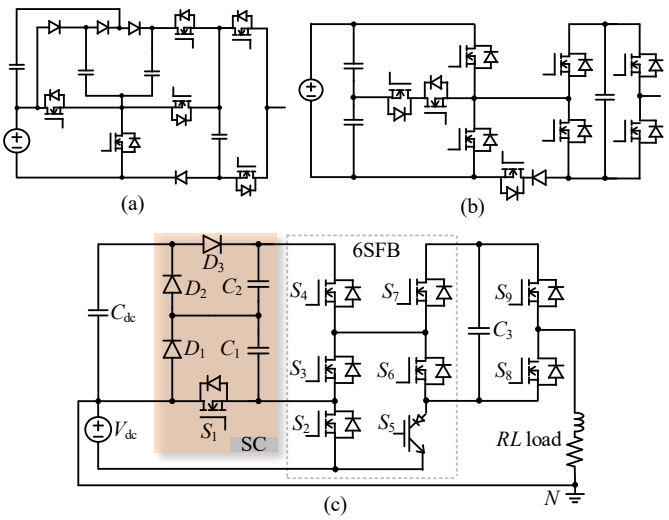

Fig. 1. Circuit structures of the SC-based boost MLIs in (a) [12] for 7L operations with a voltage gain of 3, (b) in [15] for 7L operations with a voltage gain of 1.5, and (c) the proposed inverter for 9L operations with a voltage gain of 4.

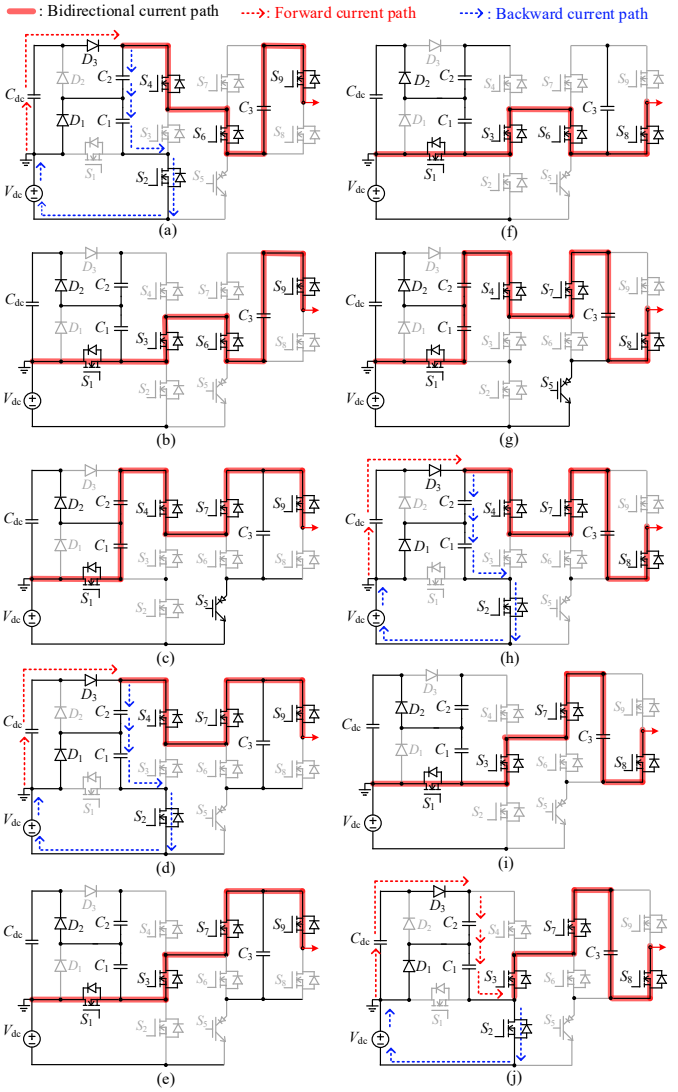

Fig. 2. Operating states (a) to (j): State 1 to 10 of the proposed MLI.

Rest of this paper is organized as follows. Section II describes the operating principles of the proposed MLI and a pulse-width-modulation (PWM) scheme is introduced to create five independent gating signals. Section III presents the detailed calculations of the inverter parameters including voltage ripples of the capacitors, voltage/current stresses of the switches, and power losses, followed with some design considerations. Section IV compares the proposed MLI with selected prior-art SC-based boost MLIs to illustrate the pros and cons. Simulations and experimental results are presented in Section V and a conclusion is drawn in Section VI.

II. Operation and Pulse-Width Modulation

To identify the voltages across the capacitors and subsequently the relationship between the capacitor voltages and the output voltage, the operations of the proposed MLI are depicted in Fig. 2, where there are 10 operating states driven by five independent gating signals as notated in Table I. Assuming that the voltages across the capacitors C_1–C_3 (V_{C1}–V_{C3}) are with negligible ripples, which is usually ensured by large capacitances, the operating states are described as follows.

A. Operating States

During State 1, the switches S_2, S_4, S_6, and S_9 are turned on. Depending on the direction of the output current, the forward and backward currents flow through two different paths. The forward current, i.e., from the dc link to the ac output, is conducted by the diode D_3, while the backward current, i.e., from the ac output to the dc link, flows through the capacitors C_2, C_1, switch S_2, and then V_{dc}, as indicated in Fig. 2(a). In either case, the diode D_1 is forward biased and thus the capacitor C_1 is connected in parallel with the dc source and charged by V_{dc}. Similarly, the capacitor C_2 is charged through the diode D_3. Accordingly, it can be obtained that

$$\begin{cases} V_{C1} = V_{dc} \\ V_{C2} = V_{dc} + V_{Cdc} - V_{C1} \\ v_o{}^1 = V_{Cdc} + V_{C3} \end{cases} \tag{1}$$

where $v_o{}^k$ represents the output voltage in State k (k = 1 to 10).

During State 2, the output voltage is supplied by the capacitor C_3 through a bidirectional current path formed by the conduction of switches S_1, S_3, S_6, and S_9. The diode D_2 is forward biased in this state, and therefore the dc-link capacitor C_{dc} is getting charged by parallelly connecting it to the capacitor C_1, as shown in Fig. 2(b). Its voltage and the output voltage can then be respectively expressed as

$$\begin{cases} V_{C1} = V_{Cdc} \\ v_o{}^2 = V_{C3} \end{cases} \tag{2}$$

During State 3, the conductions of the switches S_1, S_4, S_7, and S_9 form a bidirectional current path from the dc link to the ac output which is now supplied by the series connection of the capacitors C_1 and C_2, as illustrated in Fig. 2(c). In this state, the switch S_5 is turned on and the capacitor C_3 is being charged by the dc input in a series connection with C_1 and C_2. Consequently, the following equation can be written

$$\begin{cases} V_{C3} = V_{dc} + V_{C1} + V_{C2} \\ v_o{}^3 = V_{C1} + V_{C2} \end{cases} \tag{3}$$

TABLE I. Switching States and Key Voltages of the Proposed MLI

State k	S_2 ($\bar{S}_1$)	S_4 ($\bar{S}_3$)	S_6 ($\bar{S}_7$)	S_8 ($\bar{S}_9$)	S_5	$v_o{}^k$	V_{C1}	V_{C2}	V_{C3}
1	1	1	1	0	0	$4V_{dc}$	Inc	Inc	Dec
2	0	0	1	0	0	$3V_{dc}$	Dec	/	Dec
3	0	1	0	0	1	$2V_{dc}$	Dec	Dec	Inc
4	1	1	0	0	0	$1V_{dc}$	Inc	Inc	/
5	0	0	0	0	0	+0	Dec	/	/
6	0	0	1	1	0	–0	Dec	/	/
7	0	1	0	1	1	$-1V_{dc}$	Dec	Dec	Inc
8	1	1	0	1	0	$-2V_{dc}$	Inc	Inc	Dec
9	0	0	0	1	0	$-3V_{dc}$	Dec	/	Dec
10	1	0	0	1	0	$-4V_{dc}$	Inc	Inc	Dec

0: switch-OFF; 1: switch-ON; +0 and –0 mean the zero output voltages in positive, and negative half-cycles, respectively.

Solving the above Eqs. (1)–(3), the voltages across the capacitors C_1–C_3 can then be found as

$$\begin{cases} V_{C1} = V_{dc} \\ V_{C2} = V_{dc} \\ V_{C3} = 3V_{dc} \end{cases} \tag{4}$$

The same analysis can be applied to the other states as presented in Fig. 2(d)–(j). Equation (4) holds and the voltages across the capacitors can be viewed as constants. Therefore, the output voltage can be calculated as listed in Table I. As seen, nine discrete levels including $\pm 4V_{dc}$, $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$, and 0 for the output voltage are guaranteed by the 10 operating states. Moreover, the charge and discharge of the capacitors C_1–C_3 in each state are also indicated by the variations of their voltages including an increase (Inc), decrease (Dec), or no-change (/).

Fig. 2 also depicts that the capacitor C_{dc} is parallelly connected with either the capacitor C_1 or C_2 in any instant, which means its voltage can be maintained at V_{C1} (or V_{C2}), i.e., $V_{Cdc} = V_{C1} = V_{C2} = V_{dc}$. Therefore, each capacitor can be charged or discharged when in the positive/negative half fundamental cycle and their voltages will keep steady. Moreover, a bidirectional current flow between the dc link and the ac output is achieved in all operating states, which supports non-unity power-factor operation, to be demonstrated experimentally in Section V. In the following, a carrier-deposition PWM scheme is presented to generate the gating signals for the nine switches.

B. Multicarrier Pulse-Width Modulation (PWM) Scheme

To generate a 9L output voltage, eight triangular carriers (T_1–T_8) with the same frequency (f_s), phase, and amplitude (E_c) are used to generate five independent gating signals based on the carrier-phase deposition, as shown in Fig. 3(a). The logic circuits for the multicarrier PWM scheme are shown in Fig. 3(b), where the eight triangular signals are compared with a sinusoidal reference that is expressed as

$$V_{ref} = A_m \sin(2\pi f_l t) \tag{5}$$

in which f_l is the fundamental frequency and A_m is the amplitude of the modulation signal. The modulation index is defined as

$$M_a = A_m/(4E_c) \tag{6}$$

Therefore, 10 preliminary logic signals corresponding to the 10 operating states are generated. They are used to determine the gating sequences for switches S_2, S_4, S_6, S_8, and S_5.

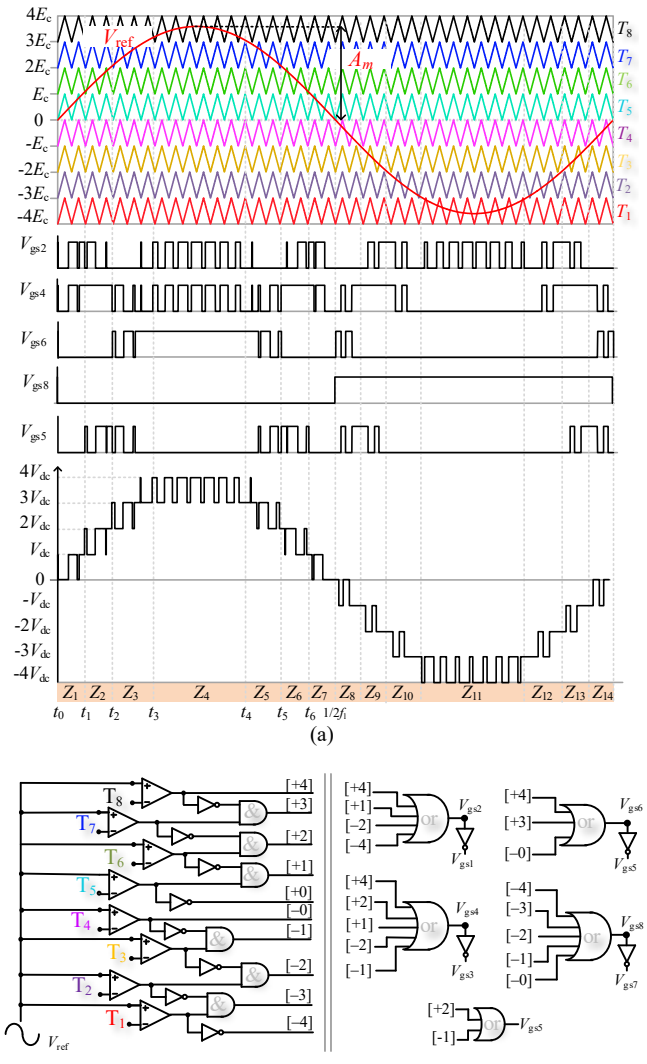

Fig. 3. Multicarrier PWM scheme (a) waveforms and (b) the logic circuits for generating gating signals V_{gs1} to V_{gs9}.

Under the multicarrier PWM scheme, the whole fundamental cycle is then divided into 14 sectors (Z_1–Z_{14}) as shown in Fig. 3(a). Assuming $t_0 = 0$ and letting $V_{ref} = E_c$, the duration of sector Z_1 can be calculated by

$$t_1 = \frac{\arcsin(1/(4M_a))}{2\pi f_l} \tag{7}$$

Similarly, the duration of Z_2 and Z_3 can be found by computing t_2 and t_3 according to

$$t_2 = \frac{\arcsin(1/(2M_a))}{2\pi f_l} \tag{8}$$

$$t_3 = \frac{\arcsin(3/(4M_a))}{2\pi f_l} \tag{9}$$

Furthermore, t_4, t_5, and t_6 can be respectively obtained from

$$t_4 = \frac{\pi - \arcsin(3/(4M_a))}{2\pi f_l} \tag{10}$$

$$t_5 = \frac{\pi - \arcsin(1/(2M_a))}{2\pi f_l} \tag{11}$$

$$t_6 = \frac{\pi - \arcsin(1/(4M_a))}{2\pi f_l} \tag{12}$$

Therefore, the durations of the first seven sectors Z_1–Z_7 can be computed using (7)–(12). Similarly, durations of the other seven sectors in the negative half cycle can also be found due to symmetry.

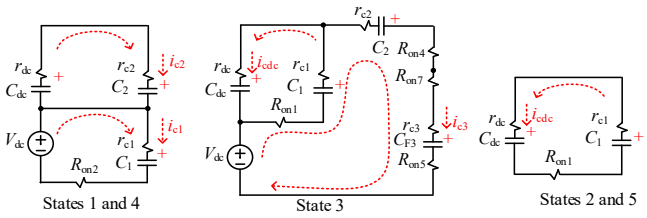

Fig. 4. Equivalents of capacitor-charging circuits in the positive half-cycle.

III. Theoretical Analysis

For the SC network, the peak charging currents of the capacitors depend on their parasitic resistances and the voltage difference between two of them at the starting instant of parallel connection. In principle, the on-state resistances of the switches and the equivalent-series-resistances (ESRs) of the capacitors are very small. To limit the peak charging currents, the voltage ripples of capacitors should be kept at a low level.

A. Capacitor Voltage Ripple and Peak Charging Current

The operating states for charging all the capacitors can be found in Fig. 2. Assuming that the proposed MLI is operating with a unity power factor, the charging currents of the capacitors (i_{C1}, i_{C2}, i_{C3}, and i_{Cdc}) have been extracted from Fig. 2 and reprinted in Fig. 4 considering the parasitic resistances of the non-ideal components. r_{dc}, r_{c1}–r_{c3} in Fig. 4 are the ESRs of the capacitors C_{dc}, C_1–C_3, respectively, and R_{onx} (x = 1 to 9) represents the on-state resistance of the power switch S_x.

The voltages of the capacitors (C_1–C_3) are depicted in Fig. 5 with their microscopic ripples explicitly shown. It can be inferred from Fig. 5 that if one capacitor can be charged and discharged within two consecutive states in each sector, its voltage ripple can be maintained low since the frequency of the carriers is much higher than the fundamental frequency. For example, the voltage of capacitor C_1 keeps steady with a negligible ripple from t_0 to t_2 as it can be replenished during each carrier cycle (see Fig. 5). However, it keeps discharging when in States 2 and 3 (from t_2 to t_3), with its voltage decreasing in sector Z_3. The voltage drop of capacitor C_1 can be calculated by

$$\Delta v_{C1} = \frac{1}{C_1}\int_{t_2}^{t_3} \sqrt{2} I_o \sin(2\pi f_l t) dt \tag{13}$$

where I_o is the root-mean-square (rms) value of the output current (notated as i_o).

Similarly, the voltage drop of capacitor C_2 in sector Z_3 can be estimated by

$$\Delta v_{C2} = \frac{1}{C_2}\int_{t_2}^{t_3} \sqrt{2} I_o \sin(2\pi f_l t) dt \tag{14}$$

Such a voltage drop also applies to the capacitor C_3, which continuously discharges to the output during sector Z_4 (from t_3 to t_4). Its voltage deficiency in this sector is calculated by

$$\Delta v_{C3} = \frac{1}{C_3}\int_{t_3}^{t_4} \sqrt{2} I_o \sin(2\pi f_l t) dt \tag{15}$$

Assuming the capacitors are respectively charged by their nominal voltages defined in (4), the peak charging currents

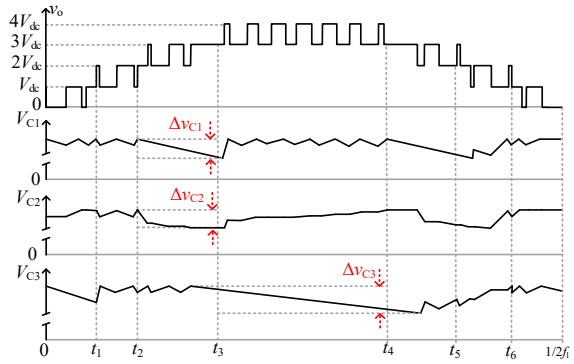

Fig. 5. Sketches (not to scale) of voltages across capacitors C_1–C_3 during the positive half fundamental cycle.

that arise at the beginning of the charging states are calculated as

$$I_{\mathrm{C1pk}} = \frac{\Delta v_{C1}}{R_{\mathrm{on2}}+r_{\mathrm{c1}}} \tag{16}$$

$$I_{\mathrm{C2pk}} = \frac{\Delta v_{C1}+\Delta v_{C2}}{r_{\mathrm{dc}}+r_{\mathrm{c1}}+r_{\mathrm{c2}}+R_{\mathrm{on2}}} \tag{17}$$

$$I_{\mathrm{C3pk}} = \frac{\Delta v_{C3}}{R_{\mathrm{on1}}+R_{\mathrm{on4}}+R_{\mathrm{on5}}+R_{\mathrm{on7}}+r_{\mathrm{c1}}+r_{\mathrm{c2}}+r_{\mathrm{c3}}} \tag{18}$$

Generally, if a small voltage ripple such that: $\Delta v_C < 5\% V_C$ is required to reduce the peak currents, the capacitances C_1–C_3 should fulfill the following requirements

$$C_1 = C_2 \geq \frac{20\sqrt{2}}{V_{dc}} \int_{t_2}^{t_3} I_o \sin(2\pi f_l t)\, dt \tag{19}$$

$$C_3 \geq \frac{20\sqrt{2}}{3V_{dc}} \int_{t_3}^{t_4} I_o \sin(2\pi f_l t) dt \tag{20}$$

B. Switch Voltage and Current Stresses

According to the operating states shown in Fig. 2, the switches S_1–S_9 are clamped by the capacitor(s) when they are off. Their corresponding off-state voltages (V_{ds1}–V_{ds9}) are expressed as

$$V_{\mathrm{ds1}} = V_{\mathrm{ds2}} = V_{\mathrm{dc}} \tag{21}$$

$$V_{\mathrm{ds3}} = V_{\mathrm{ds4}} = 2V_{\mathrm{dc}} \tag{22}$$

$$V_{\mathrm{ds5}} = V_{\mathrm{ds6}} = V_{\mathrm{ds7}} = V_{\mathrm{ds8}} = V_{\mathrm{ds9}} = 3V_{\mathrm{dc}} \tag{23}$$

which implies that the maximum voltage stresses on the switches are $3V_{\mathrm{dc}}$, less than the maximum output voltage $|\pm 4V_{\mathrm{dc}}|$. Similarly, the diodes are all clamped by capacitor C_1 or C_2, with voltage stresses expressed as

$$V_{\mathrm{d1}} = V_{\mathrm{d2}} = V_{\mathrm{d3}} = V_{\mathrm{dc}} \tag{24}$$

It indicates that low-voltage diodes can be utilized.

Although the peaks of the capacitor-charge currents induce the maximum current on some switches/diodes, their average currents must be smaller. Taking the switch S_1 for an example, its average current is the sum of the output current and discharging current of the capacitor C_1 in sector Z_1. Furthermore, the average values of the charging and discharging currents are equal due to a constant capacitor voltage. Therefore, the average current stress of the switch S_1 in Z_1 is given by $(i_o+I_{C1})/2$. The same analysis can be applied to the other switches, and all the average currents of the switches are summarized in Table II.

C. Loss Analysis

TABLE II. THE AVERAGE CURRENT STRESSES OF SWITCHES

Sectors	I_{ds1}	I_{ds2}	I_{ds3}	I_{ds4}	I_{ds5}	I_{ds6}	I_{ds7}	I_{ds8}	I_{ds9}
Z_1 & Z_7	$\frac{i_o+I_{C1}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	$\frac{i_o}{2}$	$\frac{i_o}{2}$	0	0	i_o	0	i_o
Z_2 & Z_6	$\frac{i_o+I_{C1}+I_{C3}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	0	$\frac{2i_o+I_{C3}}{2}$	$\frac{I_{C3}}{2}$	0	$\frac{2i_o+I_{C3}}{2}$	0	i_o
Z_3 & Z_5	$\frac{2i_o+2I_{C1}+I_{C3}}{2}$	0	$\frac{i_o}{2}$	$\frac{i_o+I_{C3}}{2}$	$\frac{I_{C3}}{2}$	$\frac{i_o}{2}$	$\frac{i_o+I_{C3}}{2}$	0	i_o
Z_4	$\frac{i_o+I_{C1}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	$\frac{i_o}{2}$	$\frac{i_o}{2}$	0	i_o	0	0	i_o
Z_8 & Z_{14}	$\frac{2i_o+2I_{C1}+I_{C3}}{2}$	0	$\frac{i_o}{2}$	$\frac{i_o+I_{C3}}{2}$	$\frac{I_{C3}}{2}$	$\frac{i_o}{2}$	$\frac{i_o+I_{C3}}{2}$	i_o	0
Z_9 & Z_{13}	$\frac{i_o+I_{C1}+I_{C3}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	0	$\frac{2i_o+I_{C3}}{2}$	$\frac{I_{C3}}{2}$	0	$\frac{2i_o+I_{C3}}{2}$	i_o	0
Z_{10} & Z_{12}	$\frac{i_o+I_{C1}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	$\frac{i_o}{2}$	$\frac{i_o}{2}$	0	0	i_o	i_o	0
Z_{11}	$\frac{i_o+I_{C1}}{2}$	$\frac{I_{C1}+I_{C2}-i_o}{2}$	i_o	0	0	0	i_o	i_o	0

During a fundamental cycle with 14 sectors, the conduction loss $P_{\mathrm{on}x}$ of a switch S_x (x = 1 to 9) can be calculated as

$$P_{onx} = f_l R_{onx} \sum_{i=1}^{14} \int_{t_{i-1}}^{t_i} {I_{dsx\_zi}}^2\, dt \tag{25}$$

where I_{dsx_zi} is the rms current flowing through the switch S_x in sector Z_i. It can be approximated using the average value in Table II for simplification. Similarly, the average values of the capacitors charging currents are considered for calculating the conduction losses, and a straightforward estimation can be made based on their simulated values [28]. Following (25), the conduction loss of S_1 is calculated by

$$\begin{aligned} P_{on1} = f_l R_{on1} [&2\int_{t_0}^{t_1} \left(\tfrac{I_{C1}+i_o}{2}\right)^2 dt + 2\int_{t_1}^{t_2} \left(\tfrac{I_{C1}+I_{C3}+i_o}{2}\right)^2 dt \\ &+2\int_{t_2}^{t_3} \left(\tfrac{2I_{C1}+2i_o+I_{C3}}{2}\right)^2 dt + \int_{t_3}^{t_4} \left(\tfrac{I_{C1}+i_o}{2}\right)^2 dt \\ &+2\int_{t_7}^{t_8} \left(\tfrac{2I_{C1}+2i_o+I_{C3}}{2}\right)^2 dt + 2\int_{t_8}^{t_9} \left(\tfrac{I_{C1}+i_o+I_{C3}}{2}\right)^2 dt \\ &+2\int_{t_9}^{t_{10}} \left(\tfrac{I_{C1}+i_o}{2}\right)^2 dt + \int_{t_{10}}^{t_{11}} \left(\tfrac{I_{C1}+i_o}{2}\right)^2 dt] \end{aligned} \tag{26}$$

On the other hand, the switching losses $P_{\mathrm{sw}x}$ of the switch S_x are caused by the non-ideal switching-on/-off movements. Assume that t_{r} and t_{f} are the turn-on and -off duty ratios in a switching period. The switching losses of a switch can then be summarized as

$$P_{swx} = V_{dsx} \frac{f_l f_s (t_{\mathrm{r}}+t_{\mathrm{f}})}{2} \sum_{i=1}^{14} \int_{t_{i-1}}^{t_i} I_{dsx\_zi}\, dt \tag{27}$$

Also note that except for the switches S_1 and S_2, all the switches remain off in at least one of the sectors, which reduces the overall switching losses. In particular, for the switches S_8 and S_9 (see Fig. 3(a)), their switching losses are neglected.

The diodes are also stressed by the peak charging currents of the capacitors calculated with (16)–(18) since they are in series connections in the charging paths of the capacitors. The conduction loss of a diode is mainly caused by the forward voltage (V_{F}) when it is conducting. Low voltage-rating diodes usually result in a low V_{F}, and assuming that the three diodes are with the same V_{F}, the total conduction loss of the diodes is thus calculated by

$$P_d = f_l V_{\mathrm{F}} \sum_{i=1}^{14} \int_{t_{i-1}}^{t_i} (I_{\mathrm{d1\_zi}} + I_{\mathrm{d2\_zi}} + I_{\mathrm{d3\_zi}})\, dt \tag{28}$$

where $I_{\mathrm{dy\_zi}}$ (y = 1 to 3) is the average current flowing through the diode D_y in the sector Z_i.

Similarly, the total conduction loss of the capacitors (P_{C}) can be estimated according to

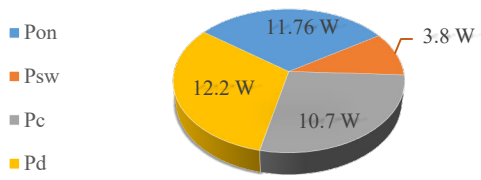

Fig. 6. Calculated losses of the switches (P_{on} and P_{sw}), diodes (P_d), and capacitors (P_C) of the proposed MLI based on the working condition and devices used in the experiment.

$$P_c = f_l r_c \sum_{i=1}^{14} \int_{t_{i-1}}^{t_i} (I_{cdc\_zi} + I_{c1\_zi} + I_{c2\_zi} + I_{c3\_zi})^2 \, dt \quad (29)$$

where I_{cy_zi} is the average current flowing through the capacitor C_y in the sector Z_i, and r_c is the same assumed ESR for each capacitor, i.e., $r_{cdc} = r_{c1} = r_{c2} = r_{c3} = r_c$.

Based on the above analysis, the calculated values of the losses caused by different kinds of components are distributed in Fig. 6. As expected, the conduction losses of the semiconductor devices including switches (P_{on}) and diodes (P_d) caus the highest loss, accounting for more than 60% of the overall loss. Whereas, the switching losses (P_{sw}) of switches evaluated under a 10-kHz switching frequency only take up a small part. Considering the conduction losses of the capacitors (P_c), the overall loss inferred from Fig. 6 is 38.46 W, and therefore the theoretical efficiency of the proposed MLI at its rated power of 1 kW is 96.3%.

D. Design Considerations

The selections of the semiconductor devices are based on their voltage and current ratings. The voltage ratings of the switches are determined according to Eqs. (21)−(23), with their average currents shown in Table II. However, the maximum currents of some switches need to consider the capacitor-charging currents given by (16)−(18). To be specific, the switches S_1, S_2, S_4, S_5, and S_7 conduct at least one capacitor-charge current and the load current. Therefore, their peak currents should be large. Whereas the switches S_3, S_6, S_8, and S_9 only conduct the load current, their maximum currents are relatively small.

Similarly, the voltage ratings of capacitors are determined according to (4). Meanwhile, the selection of the capacitances for C_1−C_3 should fulfill (19) and (20). The same design criterion applies to the dc-link capacitor C_{dc}, which is in a parallel-connection with either the capacitor C_1 or C_2 during all the operating states. If an input capacitor (C_{in}) is required, its value is relatively large to suppress the voltage variation caused by the second-order harmonic. According to [29], the input capacitance should fulfill

$$C_{in} \geq \frac{P_o}{2\pi f_1 V_{dc} \Delta V_{dc}} \quad (30)$$

where ΔV_{dc} is the allowable second-order voltage ripple across the input capacitor, and P_o is the average output power.

Based on the above design considerations, the capacitors used in the experiment are $C_1 = C_2 = C_{dc} = 1$ mF; $C_3 = C_{in} = 3$ mF, which can be implemented with parallel-connected capacitors in practice.

IV. Inverter Performances and Cost Comparisons

A. Comparison of Inverter Performances

Compared to the traditional single-phase 9L NPC/FC inverter, the proposed MLI uses less number of switches and fewer capacitors whose voltages can be self-balanced without auxiliary circuits. But large capacitances are required to reduce the capacitor-voltage ripples and their peak charging currents similar to other SC MLIs as shown in Table III. Both the proposed MLI and the NPC/FC inverter use a single dc source. However, the NPC/FC inverter only achieves a voltage-buck functionality, which requires a high-voltage dc link. Unlike the NPC/FC inverter, however, the proposed MLI requires switches with different voltage/current ratings. Therefore, a careful selection of the switches applies to the proposed MLI, and in fact, other SC-based MLIs, as compared in the following.

To provide a comparative study on the proposed MLI with selected prior-art SC-based MLIs [10]–[21], the numbers of the semiconductor devices including switches (N_S), and diodes (N_D) are summarized in Table III. As seen, most of the MLIs have their switch counts larger than their numbers of voltage levels. That is to say, the switch-per-level ratios (N_S/L) of these

TABLE III. Performances Comparisons with Existing SC-Based Boost MLIs

MLIs	L	N_S	N_D	N_C	V_{dsmax}/V_{omax}	TSV_{sw}	TSV_d	V_{Cmax}/V_{omax}	N_{vb}	NPC or CG?	Reported MLI prototypes					
											S used	D used	C (mF)	f_s (kHz)	$V_{dc}\rightarrow V_{omax}$ (V)	η% @ P_o (W)
[10]	5	9	0	1	0.5	4.5	0	0.5	2	NO	IGBT	-	3.3	2.5	100→200	97.9 @ /
[11]		6	2	2	1	4.5	1.5	1+0.5	2	Yes	Si	Si	1.0+0.47	20	180→360	98.2 @ 600
[12]	7	6	4	3	1	4	2	1+0.67+0.33	3	Yes	SiC	SiC	0.22×2+4.0	25	130→390	96.13 @ 800
[13]		10	0	2	1.33	7.667	0	0.67×2	1.5	Yes	SiC	-	4.7×2	5	100→150	98.3 @ 150
[14]		10	0	1	0.67	6	0	0.67	1.5	Yes	Si	-	0.47	2.5	200→300	96.0 @ 1000
[15]		9	0	1	0.67	5.33	0	0.67	1.5	Yes	Si	Si	4.4	- (ffm)	50→150	96.76 @ 250
[16]	9	19	0	3	0.25	4.725	0	0.25×3	4	No	IGBT	-	4.7×3	2	48→192	88.93 @ /
[17]		12	0	3	1	5.5	0	0.5×2+0.25	4	No	Si	-	4.3×2+2	20	80→320	96.0 @ 1000 *
[18]		11	0	2	0.5	5.5	0	0.25×2	2	No	IGBT	-	4.7×2	2.5	160→320	/ @ 400
[19]		10	1	2	1	6.5	0.25	0.25×2	2	No	Si	Si	1.0×2	/	200→400	95.5 @ 1000
[20]		8	3	3	1	4	1.25	0.5×2+0.25	4	No	Si	Si	3.3×2+3.3	4	80→320	93.0 @ 500
[21]		8	4	4	1	4	1.5	(0.5+0.25)×2	4	No	Si	Si	(2.3+4.7)×2	4	70→280	92.75 @ 1000
Prop-osed		9	3	3	0.75	5.25	0.75	0.25×2+0.75	4	Yes	Si and IGBT	Si	1.0×2+3.3	10	100→400	95.2 @ 1000

Note: "-" means not applicable. "/" means no information. "*" simulated data. "ffm" means fundamental frequency modulation. Bidirectional switches are counted as two switches; dc-link capacitors for all the MLIs are excluded.

inverters are larger than 1. Lesser switches are used by the inverters [12], [20], and [21], whose calculated N_S/L ratios are smaller than that of the proposed MLI. Although they feature a low N_S/L, a high voltage of V_{omax} is withstood by some of its switches ($V_{dsmax}/V_{omax} = 1$). To synthesize both the numbers and voltage stresses of the semiconductor devices, the total standing voltages (TSVs) (in per unit, after being normalized to V_{omax}) of the switches and diodes are respectively calculated by

$$\mathrm{TSV_{sw}}(p.u.) = \frac{1}{V_{\mathrm{omax}}}\sum_{i=1}^{N_S} V_{\mathrm{dsi}} \tag{31}$$

and

$$\mathrm{TSV_{d}}(p.u.) = \frac{1}{V_{\mathrm{omax}}}\sum_{i=1}^{N_D} V_{\mathrm{di}} \tag{32}$$

It can be observed from the 9L inverters that lower TSVs for both switches and diodes are achieved by the inverter [16]. However, since it uses a large number of switches ($N_S = 19$), each driven by an individual gating circuit, the requirement for gate drivers is significantly increased.

Besides the semiconductor devices, the number of capacitors (N_C) and their total voltage V_C are also compared in Table III. The proposed MLI uses three floating capacitors, with a total capacitor voltage of $1.25V_{omax}$, being smaller than or equal to those of the inverters [11]–[13], [17], [20], and [21]. Moreover, the capacitors are not stressed by V_{omax} as their steady-state voltages are $0.25V_{omax}$, $0.25V_{omax}$, and $0.75V_{omax}$, respectively.

The eight indices of the proposed MLI and its 9L counterparts [16]–[21] are consolidated in two radar charts shown in Fig. 7. Low switch count (or low N_S/L) and high voltage gain (or low $1/N_{vb}$) of the proposed MLI are seen compared to the inverters [16]–[18]. Moreover, the two key

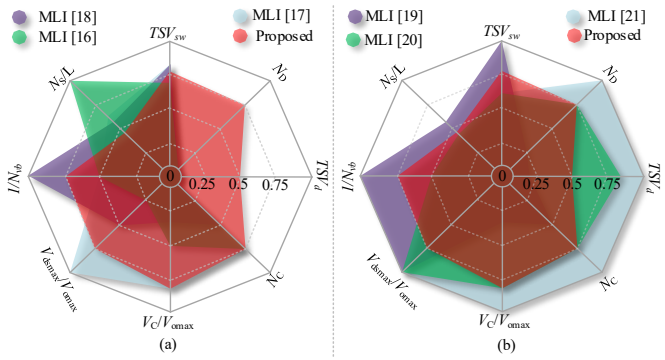

Fig. 7. Performances of the proposed MLI and the SC-based 9L inverters (a) without diodes [16]–[18], or (b) with diodes [19]–[21] (each index is normalized to its maximum value).

features are achieved without using high-voltage (V_{omax}) components (neither switches, diodes, nor capacitors) as compared to inverters [19]–[21]. That is to say, a high step-up output voltage is achieved by the proposed MLI, not necessarily experiencing a tradeoff between the number of the switches and the switch-voltage rating. The superiorities of the proposed MLI are thus justified, which in turn, illustrates the novelty of the proposed solution.

Besides, the proposed MLI provides a single-phase dc-to-ac common-ground (CG) structure similar to inverters presented in [11], [12], [15], and [24]–[27], which, however, is rarely seen in the 9L counterparts [16]–[21]. It should be mentioned that the CG inverters [24], and [26] use the switched-inductor-boost technique, while inverter [25] or [27] features a low

TABLE IV. RECOMMENDED PART NUMBERS FOR THE SI MOSFET, SI DIODE, AND 1-MF CAPACITOR WITH DIFFERENT VOLTAGE RATINGS

Voltage ratings	Si Switches (package)	Unit price	Si Diodes (package)	Unit price	C (1-mF) of different voltages as bases	Unit price($\$_C$)	Other devices	Unit price
600V	IPW60R099 (TO-247)	6.64	DPF30P600HR (TO-247)	4.66	ALF20G102EP500 (500 V)	13.32	Gate driver HCPL-3120	3.82
500V	IRFP31N50LPBF(TO-247)	6.01	/		ESMR401VSN102MA50S (400 V)	9.24		
400V	IRFP360LCPBF (TO-247)	4.62	VS-30EPF04-M3 (TO-247)	3.13	EKMH301VSN102MA60T (300 V)	5.98	Heat sink (TO-220) 6398BG	2.05
300V	IRFB4137PBF (TO-220)	3.81	APT30D30BG (TO-247)	2.09	381LQ102M250A022 (250 V)	4.82		
250V	RCX330N25 (TO-220)	2.94	/		381LX102M200A022 (200 V)	4.07		
200V	IPP320N20N3 (TO-220)	2.72	FFPF30UP20STU (TO-220)	1.37	ESMQ161VSN102MQ30S (160 V)	3.58	Heat sink (TO-247) WA-T247-101E	3.0
150V	IRFB5615PBF (TO-220)	1.59	/					

Notes: RB IGBT (if needed) is implemented by one Si MOSFET and one Si diode; the unit prices (USD) of the components and their manufactural parts are referred to www. digikey.com.

TABLE V. COST OF EACH KIND OF COMPONENT AND THE TOTAL COST OF MLIS IN THIS DESIGN EXAMPLE

MLIs	The cost (USD) of				Total cost (USD)	
	Switches	Drivers	Diodes	Capacitors	excluding heat sink	including heat sink
[10]	26.46	34.38	0	5.31	66.15	84.60
[11]	26.85	22.92	6.75	26.04	82.56	103.70
[12]	26.70	22.92	8.77	56.21	114.60	139.85
[13]	46.44	38.20	0	86.86	171.50	199.60
[14]	42.40	38.20	0	4.34	84.94	113.04
[15]	38.22	34.38	3.13	81.31	157.04	186.09
[16]	30.21	72.58	26.03	50.45	179.30	257.20
[17]	36.02	45.84	0	22.90	104.76	127.16
[18]	29.64	42.02	0	84.13	155.79	178.34
[19]	38.98	38.20	1.37	7.16	85.71	113.96
[20]	26.96	30.56	5.55	87.38	150.45	176.80
[21]	26.00	30.56	6.92	61.87	125.35	153.75
Proposed	32.16	34.38	7.24	37.65	111.43	143.78

Notes: The capacitances are based on their reported values, which are further scaled up/down according to the power levels (if less/larger than 1 kW); the cost of a capacitor (capacitance C_x) with a specific voltage rating is calculated according to $\$_C \times C_x$/1(m F).

TABLE VI. CIRCUIT PARAMETERS OF THE INVERTER PROTOTYPE

Voltage	V_{dc} = 100 V, V_{omax} = 400 V, 50 Hz, 1 kVA
Reactive components	$C_{dc} = C_1 = C_2$ = 1 mF; C_3 = 3.3 mF; C_{in} =3.3 mF and L_{in} = 1 mH (optional)
Switches	S_1–S_4: IXFH72N30X3, V_{gs} = 15V; S_5: FGW85N60RB, V_{gs} = ±15V; S_6–S_9: APT40M70LVR, V_{gs} = 15V;
Diodes	D_1–D_3: APT30S20
Gate driver	HCPL-3120 (voltage range: 15 to 30 V)

voltage level (3L) or a low voltage gain (≤ 1). They are, therefore, not included in Table III for consistency.

Additionally, the reported components used to prototype the MLIs are also included in Table III. Types of semiconductor devices include IGBT and MOSFETs built by silicon (Si) or SiC (silicon carbide). For a high output voltage (> 200 V), prototypes from [11], [14], [18], and [19] are supplied by relatively high dc voltages. While, for the proposed MLI and those of [20] and [21], low-voltage dc sources (< 150 V) are utilized. Under a similar operating condition, the proposed MLI achieves a high and comparable efficiency (η).

B. Case Study on the Inverter Cost

To provide a comparative study on the inverter cost, a general design example is considered assuming that all the compared SC MLIs are prototyped to produce a multilevel output voltage with the maximum V_{omax} = 400 V, nominal power 1 kW. Under such a consideration, the design of an inverter prototype begins with the selection of the semiconductor devices by identifying their voltage ratings. For a fair comparison, the same type of semiconductor devices should be considered (Si MOSFETs and Si diodes are used in this example). Therefore, if a switch requires the reverse-blocking (RB) capability as in [16] and the proposed MLI, it is implemented by one Si MOSFET in series with one Si diode. An appropriate voltage margin of no less than 20% should be left when selecting a switch or diode. For instance, if the peak inverse voltage (PIV) of a switch is 200 V, it is considered to be implemented by a 250-V switch. According to the voltage ratings of the switches/diodes in this case study, the manufacturer part numbers of the semiconductor devices are selected, as given in Table IV. Meanwhile, their current ratings are at a similar level, which is suitable for the compared SC MLIs in the design example.

Similarly, six voltage ratings are identified among the capacitors. The recommended part numbers of the 1-mF capacitors whose voltages are 160 V, 200 V, 250 V, 300 V, 400 V, and 500 V are selected, as given in Table IV. Likewise, a voltage margin of no less than 20% is considered for each capacitor. On the other hand, the selected capacitances are based on their reported values from [10]–[21], which are further scaled up/down according to the power levels (if less/larger than 1 kW). Therefore, the cost of a capacitor with a specific voltage rating is calculated according to $\$_C \times C_x$/1(m F). It should be mentioned that the total cost will unavoidably be increased if the semiconductor devices are accompanied by heat sinks. In this respect and according to the package type listed in Table IV, two recommended heat sinks for the semiconductor devices are also considered.

The monetary cost of each MLI prototype is finally calculated, as shown in the last two columns of Table V.

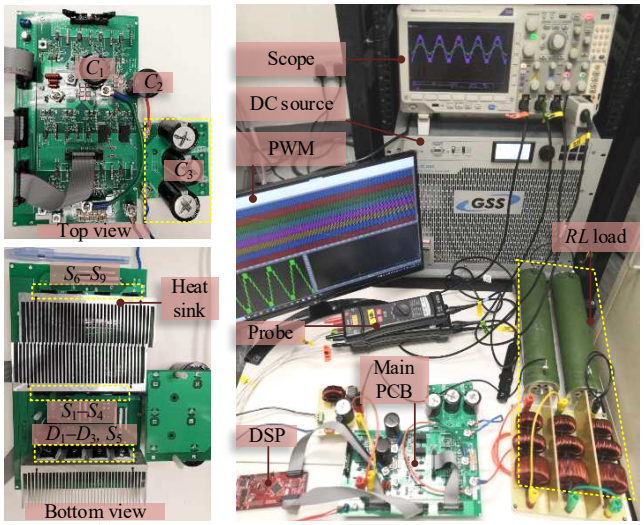

Fig. 8. Photographs of (a) the printed-circuit-board (PCB) of the proposed inverter and (b) experimental setup.

Without accounting for the cost of heat sinks, the total cost of the proposed 9L inverter is higher compared to the 5L inverters [10]–[11], which is expected since more switches and capacitors are required. With the same number of capacitors and a similar structure, the costs of the 7L inverters from [12], [15] are at a similar level to the proposed one. Among the 9L counterparts, the proposed inverter achieves a lower cost than [16], [18], [20], and [21]. However, its cost is slightly higher than those of the MLIs in [17], and [19]. The same conclusion can be drawn when the cost of the heat sink is taken into consideration.

Inferred from the above case study, the use of switches with different PIVs does not increase the overall cost significantly. Instead, it may be more cost-effective since all the switches, diodes, and capacitors need not be burdened by the maximum of the output voltage (400 V in this example).

V. SIMULATION AND EXPERIMENTAL VERIFICATION

To verify the feasibility of the proposed inverter, an experimental prototype with the rated operating power of 1 kW is built using the devices listed in Table VI. An isolated gate-driver capable of providing suitable gating voltages (15 to 30 V) for both MOSFET and IGBT is used (see Table VI). The gating voltage can be negatively biased for fitting the IGBT turn-off.

Since the input current is discontinuous for the proposed SC-based MLIs, an input *LC* filter is considered during the experimental test, which is added between the dc source and

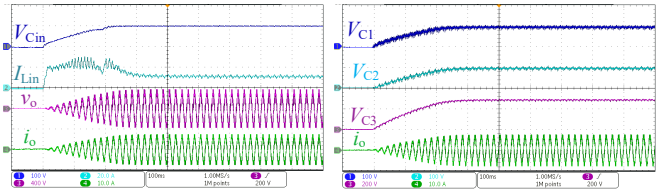

Fig. 9. Experimental waveforms including (a) the capacitor voltage V_{Cin} (100 V/div), input current I_{Lin} (20 A/div), output voltage v_o (400 V/div), output current i_o (10 A/div), and (b) voltages of capacitors C_1, C_2 (100 V/div), and C_3 (200 V/div) during the inverter startup.

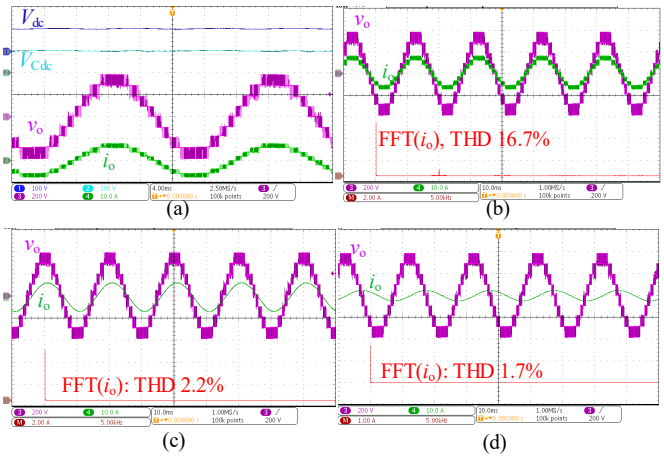

Fig. 10. Steady-state waveforms including (a) V_{dc}, V_{Cdc} (100 V/div) output voltage v_o (200 V/div), and output current i_o (10 A/div); (b) FFT of i_o (2 A/div) under a resistive load; (c) FFT of i_o (2 A/div) under an inductive load with PF = 0.95, or (d) FFT of i_o (1 A/div) under an inductive load with PF = 0.45.

the inverter prototype to maintain a continuous input current drawn from the dc source [30]. It should be noticed that the presence of the input filter is, however, not necessary if the dc source is immune to the pulsating input current, so as to reduce the volume and weight of the overall system [31]–[33]. The ac output is feeding an *RL* load (see Fig. 8), so that both unity and non-unity power-factor operations can be tested. The multicarrier PWM scheme is implemented on a digital signal processor (DSP), and the carrier frequency f_s is 10 kHz.

A. Inverter Soft Start

To limit the inrush current during the start-up process, a soft-start circuit is used, as discussed in [34], and [35]. The dc source is connected to the proposed MLI through a small current-limiting resistor. A relay with a turn-on delay (≈ 0.2s) is used to bypass the resistor when the voltages across the capacitors reach close to their nominal values. Experimental waveforms during the soft-start process are shown in Fig.9. As seen, the input current also the current flowing through the input inductor (I_{Lin}) is confined effectively. Meanwhile, the voltages across the capacitors increase smoothly (Fig. 9(b)). Neglecting the high-frequency voltage ripples, the relationship of the voltages: $V_{C1} = V_{C2} = 1/3V_{C3}$ holds at any instant of the time, which agrees with the theoretical analysis presented in Section II.A.

B. Steady-State Operations

The steady-state output voltage of the proposed MLI is shown in Fig. 10 (a). The input voltage V_{dc} and the voltage across the dc-link capacitor V_{Cdc} keep steady. The ac output voltage is with a sinusoidal staircase of nine discrete voltage levels. The amplitude of each level is 100 V, which together, gives rise to a maximum output voltage of |±400| V, matching with the theoretical analysis. It is worth noting the output voltage when at "$+4V_{dc}$" or "$-4V_{dc}$" decreases/increases slightly, featuring thus a slopy voltage. This is caused by the voltage variations of the capacitor C_3, which continuously discharges to the output during sector Z_4 in (t_3, t_4). Therefore, the output voltage at the "$+4V_{dc}$" level decreases slightly. The same explanation can be applied when the output voltage is at the "$-4V_{dc}$" level.

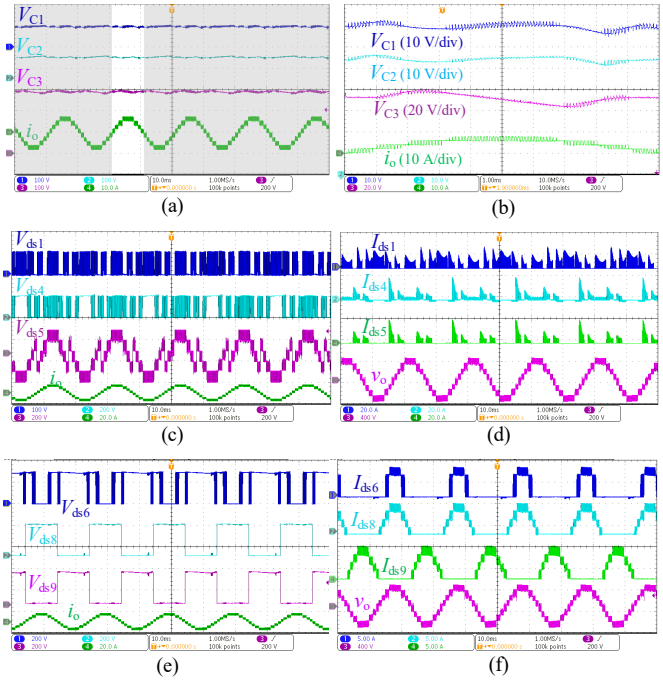

Fig. 11. Experimental waveforms of (a) voltages of capacitors C_1–C_3 (100 V/div) and (b) their zoom-in view; (c) voltages of the switches S_1 (100 V/div), S_4 (200 V/div), and S_5 (200 V/div); (d) currents of the switches S_1, S_4, and S_5 (20 A/div); (e) voltages of the switches S_6, S_8, and S_9 (200 V/div). (f) currents of the switches S_6, S_8, and S_9 (5 A/div).

The fast Fourier transform (FFT) of the output current is tested under different loading conditions. Fig. 10(b) shows that its rms value is 4.5 A under a resistive load, and the total-harmonic-distortion (THD) measured is 16.7%. With an inductive load, the measured THD of the output current is reduced to 2.2% (Fig. 10(c)) due to the filtering effect of the load inductance. A low THD is also tested when the inverter is supplying a low PF load, as shown in Fig. 10(d).

The voltage and current stresses of the capacitors and switches are tested with results shown in Fig. 11. As seen in Fig. 11(a), the voltages across the capacitors V_{C1}–V_{C3} are respectively 100 V, 100 V, and 300 V, confirming again the theoretical analysis. Moreover, a zoom-in view of the capacitor voltages during the positive half cycle is given in Fig. 11(b), which shows that variations of the capacitor voltages match well with the analysis in Section III.A (see Fig. 5). Such a small variation of the capacitor voltage helps to reduce the peak charging current. The voltage and current waveforms of switches are measured and shown in Fig. 11 (c)–(f).

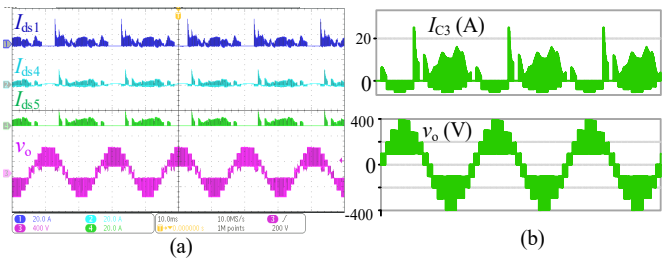

Fig. 12. Illustrations of the (a) experimental currents of I_{ds1}, I_{ds4}, and I_{ds5} (20 A/div) using an alternative PWM scheme [36], and (b) simulated charging current of the capacitor C_3 using a small capacitance (1 mF).

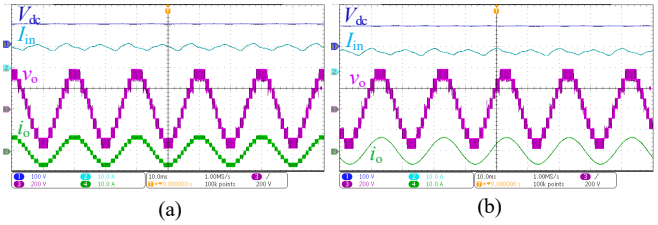

Fig. 13. Experimental waveforms of the input current when the proposed MLI is supplying (a) a resistive load and (b) an inductive load (V_{dc}: 100 V/div, v_o: 200 V/div, I_{in}: 10 A/div, and i_o: 10 A/div).

Specifically, the switch S_1 is stressed by a low voltage (100 V), while it has to conduct the charging currents of the capacitors as summarized in Table II. Therefore, its current has several peaks during a fundamental cycle. Similarly, the currents through switches S_4 and S_5 feature a peak value caused by the charge of capacitor C_3, while their off-state voltages are both 200 V. It can be inferred from the operating states shown in Fig. 2 that the diodes are also stressed by the peak charging currents of the capacitors. Also noticed that the external input *LC* filter is not for limiting the charging current of the SCs which arises internally in the proposed SC MLI (applies to the available SC MLIs).

Note that different from the buck-type NPC/FC inverters, the proposed inverter generates a boosted output voltage, which means the average input current (I_{in}) should be larger than the output current. Moreover, due to the operations of the SC structure, the peak switches currents are larger than the average input current. Despite that, for the rated input current of 10 A (V_{dc} = 100 V and V_{omax} = 400 V), the peak currents of the switches under the rated operating power are around 20 A, which is within the normal operating current range of the selected diodes/switches. Furthermore, their average currents during a fundamental period are smaller than the peak values. For a higher power-level operation, however, the selection of the devices should be reconsidered, since the current ratings of all devices are expected to be increased. To maintain a low charging current during a higher power-level operation, larger capacitances are required.

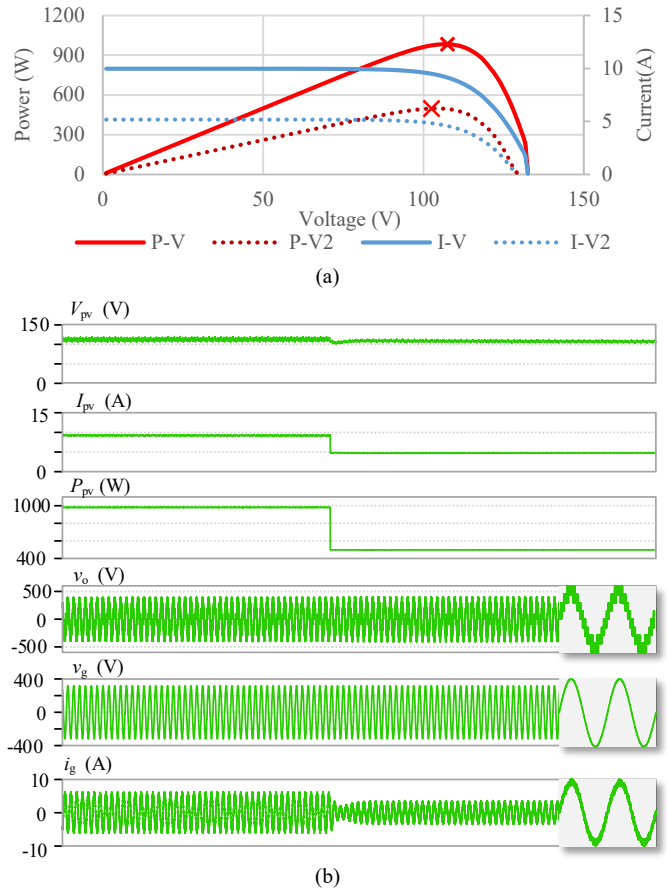

Fig. 14. Illustrations of the (a) output characteristics of the PV source used in the simulation under high irradiance (solid line), and low irradiance (dashed lines) with the two MPPs indicated by "×", and (b) the key waveforms including PV voltage V_{pv}, current I_{pv}, power P_{pv}, output voltage v_o, grid voltage v_g, and grid current i_g with a step-change in the PV irradiance.

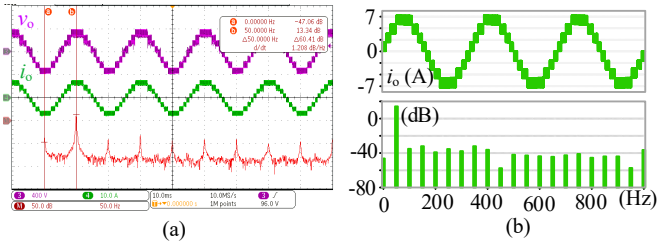

Fig. 15. The spectrum of the load current i_o under a resistive load measured from (a) experiment (-47.06dB at 0 Hz, 13.34dB at 50 Hz) and (b) simulation.

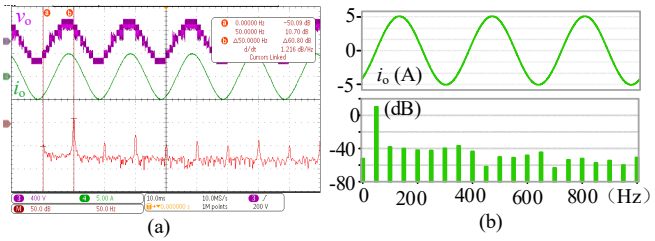

Fig. 16. The spectrum of the load current i_o under an inductive load measured from (a) experiment (-50.09dB at 0 Hz, 10.7dB at 50 Hz) and (b) simulation.

The switches S_6, S_8, and S_9 feature a 300-V off-state voltage, since they are directly clamped by the capacitor C_3. The currents through these three switches are free of the charging currents of the capacitors (Fig. 11(e) and (f)). In particular, the switches S_8 and S_9 are operating at a much lower frequency, and thus free of switching losses.

Also inferred from Fig. 11 is that due to the presence of the SC circuit, large capacitances are usually required to limit the peak charging currents of the capacitors. To avoid using large capacitances, an appropriate selection of the operating states for the 14 sectors may be considered. The experimental test of proposed MLI using an alternative PWM scheme [36] is shown in Fig. 12(a). As can be seen, the maximum current stresses of the switches S_4, and S_5 are reduced to a half. This is because C_3 no longer continuously discharges to the output during sector Z_4 in (t_3, t_4), and its voltage ripple is reduced significantly. In other words, the required capacitance for C_3 can be reduced by using the alternative PWM scheme, which is also simulated with results shown in Fig. 12(b).

The experimental waveform of the input current when the proposed MLI is supplying a resistive load or an inductive load is measured and shown in Fig. 13. In both operations, a continuous and non-pulsating input current is drawn from the dc source although it is coupled with a second-order harmonic

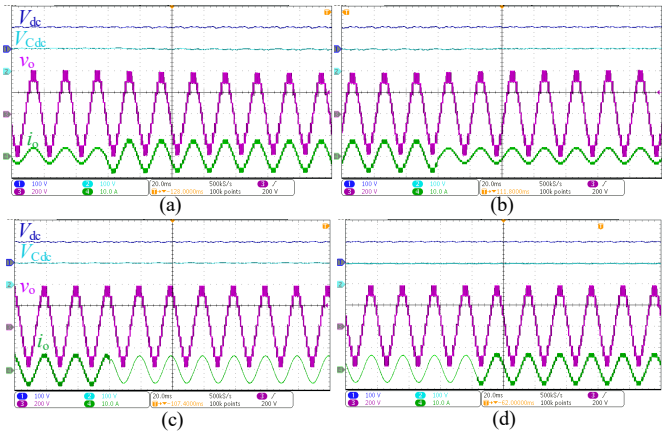

Fig. 17. Responses of the proposed MLI with step-changes in loading condition: (a) from half-load to full-load, and (b) the reverse; (c) from a resistive load to an inductive load, and (d) the reverse (V_{dc} and V_{Cdc}: 100 V/div, v_o: 200 V/div, i_o: 10 A/div).

caused by the single-phase pulsating output power. Therefore, if a PV source is used to feed the proposed MLI, the average output power of the PV source may be reduced. To examine the maximum-power-point-tracking (MPPT) capability of the proposed MLI without using the front-end dc-dc converter, a grid-connected PV power generation is simulated through *Matlab Simulink*. The output characteristics of the PV source used in the simulation are shown in Fig. 14(a). A step-change in the irradiance is tested, causing the output voltage of the PV source to reduce. Similarly, the maximum output power is also reduced as indicated by the two "×" points. It is observed in Fig. 14(b) that the proposed MLI responds quickly, and the MPP is tracked under different irradiance. During the high-irradiance operation, the average output power of the PV source is 980 W out of its maximum value of 982.5 W, which then gives rise to the steady-state MPPT efficiency of 99.7%. It indicates that the proposed MLI is able to track the MPP for PV interfacing. Although the maximum output voltage of the proposed inverter is given by $4V_{in}$, its fundamental component is time-varying with the modulation signal such that $v_{o1} = 4V_{in}A_m\sin(2\pi f_l t)$. A single-stage MPPT operation with a continuous fundamental-voltage gain (dynamic gain) is thus achieved, not necessarily using an additional dc-dc stage [27].

Moreover, to examine the dc component of the output current, the spectrum of the load current is measured and shown in Fig. 15(a). It is observed that the dc component of the output current is not zero but negligibly small at –47.06 dB, as compared to the fundamental component of 13.34 dB at 50 Hz. The difference between them is −60.41 dB, matching with the

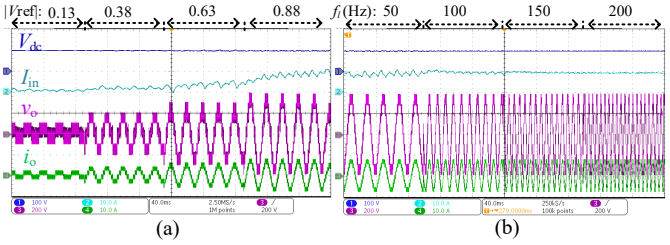

Fig. 18 Responses of the proposed MLI with a variable PWM modulation degree in the (a) amplitude and (b) frequency of the modulation signal V_{ref} (V_{dc}: 100 V/div, v_o: 200 V/div, I_{in}, and i_o: 10 A/div).

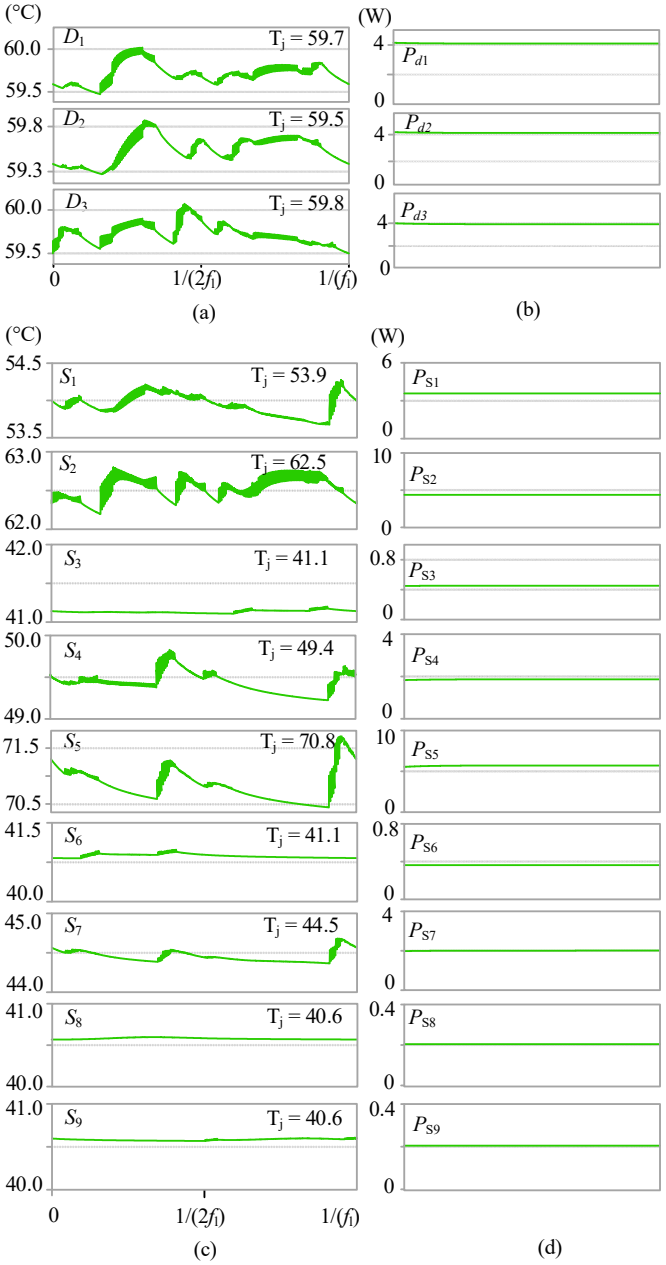

Fig. 19. Simulation results of junction temperatures (T_j/°C) of the (a) diodes and (c) switches during steady-state operation, with their (b), (d) average losses (W).

simulated result shown in Fig. 15(b). A similar observation can be made when the proposed MLI is supplying an inductive load (see Fig. 16).

C. Experimental Dynamic Responses

Dynamic responses of the inverter prototype from full-load to half-load and then back to full-load condition are tested. Both transients are quite smooth without disrupting operations of the proposed MLI as demonstrated in Fig. 17(a)–(b). In addition, the sudden changes from a resistive load to an inductive load, and an inductive load to a resistive load further confirm the stable operations of the proposed MLI under a variable loading condition as shown in Fig. 17(c)–(d).

Besides, the dynamic responses of the proposed MLI under a varied modulation degree are tested and shown in Fig. 18.

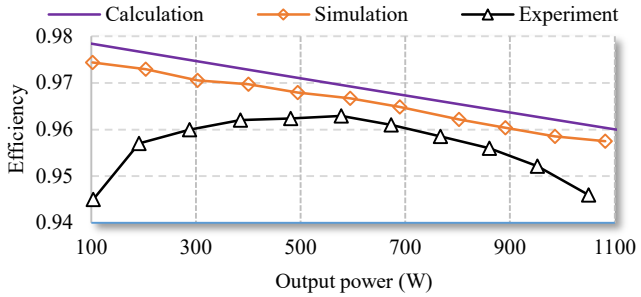

Fig. 20. The calculated, simulated, and experimental (driver included) efficiencies of the proposed inverter supplied by 100 V dc input.

During the experiment, the amplitude of the modulation signal is stepped from 0.13 to 0.38, 0.63, and then 0.88. Accordingly, the proposed MLI operates with a 3L, 5L, 7L, and 9L output voltage, as shown in Fig. 18(a). Similarly, the frequency (f_l) of the modulation signal is changed from 50 Hz to 100 Hz, 150 Hz, and then 200 Hz. The responses of the proposed MLI are shown in Fig. 18(b). Notice from the experimental results is that the ripple of the input current becomes smaller as the fundamental frequency increases. Both dynamic responses with stepped-changes in the modulation degree (amplitude /frequency) illustrate the feasibility of the proposed MLI in applications requiring an adjustable-amplitude/frequency output voltage.

D. Loss and Thermal Behaviors

The thermal behaviors of the diodes and switches are simulated. A small heat sink with a thermal resistance (from junction to ambient) of 5 °C/W is considered for each device. The ambient temperature is set as 40 °C which is assumed uniformly distributed across the heat sink. Under the nominal output power, the thermal behaviors of the diodes are tested and shown in Fig. 19(a). Since the currents through the diodes are different in each sector, it is found that the junction temperatures of the diodes vary slightly within a fundamental cycle. The average junction temperature (T_j) of each diode at steady-state operation reaches a similar level. Their values are 59.7, 59.5, and 59.8 °C, respectively. Similarly, the junction temperatures of the nine switches are tested and shown in Fig. 19(c), where it can be seen that the average steady-state junction temperatures of the switches (S_1 to S_9) are 53.9, 62.5, 41.1, 49.4, 70.8, 41.1, 44.5, 40.6, and 40.6 °C, respectively. Note that, for the switches S_1, S_2, S_4, and S_7, they conduct both the capacitor-charging currents and the output current, their losses are thus higher. For S_5, its junction temperature is the highest among all the switches, since, in addition to the switches, its RB diode induces a proportion of power losses, without which, the junction temperature of switch S_5 reduces to 62.8 °C. Nevertheless, under such a thermal setup, the highest junction temperature at about 70 °C (ambient temperature 40 °C) falls in the normal operating junction temperature of the selected devices (maximum 150 °C), which justifies the heat arrangements of the prototype [37], [38]. Furthermore, the thermal behavior of each semiconductor device is in accordance with its loss behavior (Fig. 19(b) and (d)).

The power conversion efficiency of the proposed MLI under different power levels is tested and compared to its simulated and calculated results in Fig. 20. The simulated result suggests that the efficiency drops with an increase of output power. The

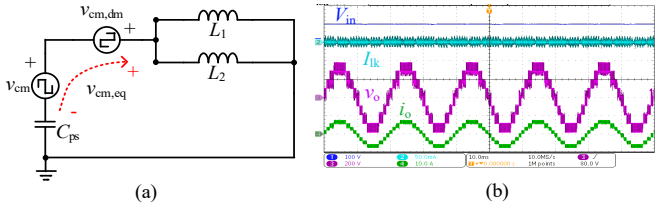

Fig. 21. Illustrations of (a) equivalent common-mode circuit of the proposed MLI, and (b) the key tested waveforms including input voltage V_{in} (100 V/div), output voltage v_o (200 V/div), leakage current I_{lk} (50 mA/div), and output current i_o (10 A/div).

simulated values are slightly lower than their theoretical values, which were previously calculated based on the average currents. Nonetheless, the two curves are close to each other, examining the feasibility of the theoretical analysis of the power losses in Section III.C. For the experimental efficiency, it drops rather than increases at a low power range (e.g., P_o< 300 W), due to the additional losses caused by the driver circuits. The maximum value of the efficiency measured at 600 W is 96.3%, being very close to the calculated and simulated values. However, it deviates slightly from its calculated and simulated values and reduces to 95.2% at the rated power of 1 kW. This is attributed to the IGBT with reverse blocking, which may induce higher losses due to the reverse recovery problem of its internal diode. Therefore, operating the proposed MLI with a lower switching frequency mitigates the effect caused by the RB diode. Despite the discrepancy, the measured efficiency over a wide load range is well above 94.5%, which indeed provides a high-efficiency boost dc-ac power conversion with a low number of switches and low voltage-rating devices.

E. Ground Leakage Current

The common-mode modeling of the proposed single-phase MLI can be simplified as shown in Fig. 21(a), where C_{ps} is the parasitic capacitance between the negative terminal of the dc source and the ground [39], [40]; L_1 and L_2 are the equivalent line inductors connected to the two output terminals 1 (dc-link mid-point), and 2 (connecting point of switches S_8, S_9, see Fig. 1), respectively. According to [39], the equivalent common-mode voltage $v_{cm,eq}$ of the proposed single-phase MLI is thus expressed as

$$v_{\mathrm{cm,eq}} = \frac{1}{2}(v_{1\mathrm{n}} + v_{2\mathrm{n}}) + \frac{(L_2 - L_1)}{2(L_2 + L_1)}(v_{1\mathrm{n}} - v_{2\mathrm{n}}) \quad (33)$$

in which, v_{1n} is the voltage of terminal 1 with respect to the negative terminal of the dc source (notated as n), and v_{2n} is the voltage of terminal 2 with respect to n.

With an asymmetrical line inductor considered in this paper, which means $L_1 = 0$ and $L_2 = L_f$, Eq. (33) can be simplified and the equivalent common-mode voltage is maintained at constant, i.e., $v_{cm,eq} = v_{1n}$.

The experimental test of ground leakage current is conducted using a 100 nF capacitor connected in between the negative terminal of the dc source and the ground to emulate the parasitic capacitances. The results are shown in Fig. 21(b). Under the nominal operating power, the measured peak value of the ground leakage current is not zero, but below 20 mA. Despite that, the common-ground structure of the proposed

MLI demonstrates the feasibility in applications requiring a low ground leakage current [39], [40].

F. Discussion on the Experimental Test

With the aforementioned attractive features experimentally verified though, the demerit of large charging current preserved from the SC-based MLIs needs to be paid attention to. The experimental results are obtained with the prototype operating within its rated power of 1000 W, under which, the measured peak switch current is about 20 A. The peak switch current of the proposed inverter, therefore, is two times larger than the input current, which may prevent its applications at a higher power level if without proper suppression of the capacitive charging current. Note that such a capacitive charging current exists in other SC-based MLIs reported in the literature, and a general solution is to use large capacitance to maintain a low voltage ripple. The large capacitance installed, however, increases the volume of the overall system and challenges a compact design. Therefore, the proposed inverter topology still has room for improvement and the investigations of peak capacitive charging current can add additional values to such type of topologies. Despite that, many recently developed SC-based MLIs have demonstrated their viability in PV systems. In addition to those MLIs compared in Table III, a supplementary file illustrating more applications of such type of topologies is included.

VI. CONCLUSION

A novel single-phase MLI is proposed based on a switched-capacitor network capable of stepping-up the output voltage with a voltage gain of 4. It only uses nine switches and three diodes to achieve a nine-level operation, yielding a low switch-per-level ratio. The operating states of the proposed inverter under a multicarrier PWM scheme are described. The theoretical analysis shows that the voltages across the switches and diodes are all lower than the maximum of the output voltage, avoiding the use of high-voltage semiconductor devices. This subsequently reduces the overall conduction and switching losses. All the mentioned features have been addressed through comparisons with the selected prior-art SC-based boost MLIs with their pros and cons discussed. The feasibility of the proposed inverter is verified by experimental tests on a 1-kVA inverter prototype. Additionally, the proposed MLI can be applied to the three-phase systems for achieving higher line-to-line output voltages. The proposed inverter, therefore, provides an innovative solution with improvements to a wide range of applications such as renewable generation systems, where boost-type dc-ac power conversion with a high voltage gain, low voltage stresses while maintaining a low switch count, and using a single dc source is expected.

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