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Safe Operating Area of DC-link Film Capacitors

Shuai Liu, Zhan Shen, *Member, IEEE*, and Huai Wang, *Senior Member, IEEE*

Abstract—This letter proposes a Safe Operating Area (SOA) concept for film capacitors in DC-link applications. The SOA is presented by capacitor voltage and ripple current, considering the impact of ambient temperature, degradation, and parameter variance. The theoretical derivations and proof-of-concept experimental verifications are given.

Index Terms—Safe Operating Area (SOA); Film capacitor; DC-link

I. INTRODUCTION

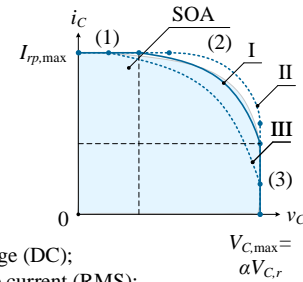
Film capacitors are widely used in DC-links for applications either with high ripple currents or kV-level voltage stresses. These applications are usually reliability- and availability-critical, such as wind turbine converters, traction inverters, and electric vehicle inverters. The safe operation of the DC-link film capacitors is essential to fulfill the intended functions of these power electronic converters. The common failure mechanisms of film capacitors are discussed in [1]: 1) dielectric breakdown due to excessive voltage; 2) thermal breakdown due to excessive ambient temperature, ripple current, leakage current, or Equivalent Series Resistance (ESR); and 3) parameter shifts due to long-term degradation under electro-thermal stresses and humidity. The above three types of failure mechanisms correlate with each other. Even though the limits in terms of voltage, current, and temperature are given in capacitor data-sheets and applications notes [2, 3], they do not provide sufficient information to guide the sizing of film capacitors for specific applications. This is because: 1) the limits are given at individual operating points; and 2) the limits do not consider parameter variations due to degradation and tolerance. For a population of properly designed products, failure may occur only for a small fraction of them which experience severe conditions and have a different set of parameters from the rated ones. It demands a more comprehensive way to present the operation limits which can guide the selection of proper film capacitors for specific DC-link applications.

Safe Operating Area (SOA) is a concept used for power semiconductor devices [4–6]. It is presented by voltage, current, and current pulse duration, considering the limits of voltage, current, and temperature. The proposed SOA concept for film capacitors is inspired by that for power semiconductors, nevertheless, with the following distinctive features: 1) ripple current pulse is not included for DC-link applications, as these capacitors usually have significantly larger thermal

time constants compared to that of power semiconductor devices; 2) it correlates the impact of ambient temperature, degradation, and component parameter variations (i.e., in terms of confidence intervals); and 3) voltage- and temperature-dependent leakage current are considered in the thermal limits.

The letter is organized as below: Section II presents the SOA concept for film capacitors in DC-link applications. Section III shows how to derive the boundaries of the SOA. Section IV discusses a case study of film capacitors rated at 1.25 kV / 645 μ F and the experimental results, followed by the conclusions.

II. PROPOSED SOA CONCEPT FOR DC-LINK FILM CAPACITORS



v_C : operating voltage (DC);
 i_C : operating ripple current (RMS);
 $V_{C,max}$: maximum DC voltage;
 $V_{C,r}$: rated DC voltage;
 α : scale factor of the limit DC voltage to $V_{C,r}$;
 $I_{rp,max}$: maximum ripple current (RMS, defined by data-sheets);
 (1)(2)(3): different regions divided according to equation (3);
 I, II, III: boundaries under different ambient temperatures T_{a1} , T_{a2} , and T_{a3}
 ($T_{a2} < T_{a1} < T_{a3}$).

Fig. 1. Proposed SOA for DC-link film capacitors without considering degradation and confidence interval.

A. Baseline

As shown in Fig. 1, the SOA boundaries include three regions: Region (1) is limited by the maximum ripple current ($I_{rp,max}$, current limit); Region (2) is limited by the hotspot temperature raise induced by power loss (thermal limit); Region (3) is limited by the maximum DC voltage ($V_{C,max}$, voltage limit). The electrical specifications are usually provided in capacitor data-sheets, as illustrated in Table I.

B. Boundaries with environmental stresses

The SOA boundary changes with the variation of environmental stresses. For example, ambient temperature T_a has a critical impact on Region (2). As shown in Fig. 1, curves I, II, and III refer to those conditions at different ambient temperatures, respectively, i.e. T_{a1} , T_{a2} , and T_{a3} ,

Shuai Liu, Zhan Shen and Huai Wang are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: sli@et.aau.dk, zhs@et.aau.dk, and hwa@et.aau.dk). Corresponding author: Zhan Shen.

TABLE I
EXAMPLE SPECIFICATIONS OF COMMERCIAL DC FILM CAPACITORS

C_r [μF]	$V_{C,r}$ [V]	$V_{C,max}$ [V]	$I_{rp,max}$ [A]	$T_{a,op}$ [°C]	$R_s@50\text{Hz}$ [mΩ]	R_{TH} [K/W] (ambient to hotspot)	Reference
645	1250	1875	80	-40 ~ +85	1.5	2.3	customized sample
660	1320	1980	100	-55 ~ +85	1.4	2	[7]
700	1500	2250	93	-40 ~ +85	1.9	1.8	[8]
640	1300	—	78	-45 ~ +85	2.2	1.5	[9]
140	1100	1350	43.5	-40 ~ +85	2	—	[3]
260	900	—	140	-40 ~ +105	1.17	2.1	[10]

C_r : rated capacitance; $V_{C,r}$: rated DC voltage; $V_{C,max}$: maximum DC voltage (non-recurrent surge voltage); $I_{rp,max}$: maximum ripple current (RMS); $T_{a,op}$: ambient temperature for normal operation; R_s : series resistance caused by contacts; R_{TH} : thermal resistance.

where $T_{a2} < T_{a1} < T_{a3}$. The change of SOA is to keep the hotspot temperature staying within a limit, which will be analyzed in Section III. Moreover, as discussed in Section III later, the insulation resistance (R_p) is also temperature-dependent [11].

C. Boundaries with parameter tolerances

Parameter tolerances exist due to the variances in materials and manufacturing—for example, the tolerances in capacitance, ESR, and R_p . The obtained voltage stress and thermal stress of a population of capacitors vary due to these tolerances. Fig. 2 introduces a confidence interval of the SOA by the gray shaded area. For example, a 90% confidence interval implies that the SOA is within the interval with a 90% probability. In other words, there is 5% probability that the actual SOA is smaller than the lower boundary and 5% probability that it is larger than the upper boundary.

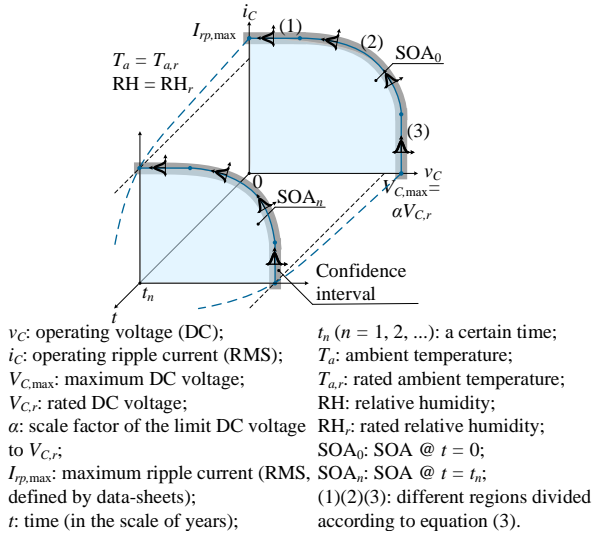


Fig. 2. Proposed SOA for DC-link film capacitors considering degradation and confidence interval.

D. Boundaries with capacitor degradation

The t -axis shown in Fig. 2 represents the operation time of the capacitors of interest. Due to the environmental stresses and operational stresses, such as T_a , Relative Humidity (RH), voltage, and ripple current, the capacitance, ESR, and R_p change with the degradation [1]. The impact of these parameter shifts can be described by an updated SOA along the operation

time, as shown in Fig. 2. In practical applications, capacitors need to be sized according to the end-of-life parameters. Therefore, the SOA when capacitors approaching the end-of-life needs to be considered.

III. DERIVATION OF SAFE OPERATING AREA FOR DC-LINK FILM CAPACITORS

The derivation of the SOA boundary is based on the following equations:

$$T_h = T_a + R_{TH} \times P_{loss} \quad (1)$$

$$\begin{aligned} P_{loss} &= i_C^2 \times R_s + i_{lk}^2 \times R_p \\ &= i_C^2 \times R_s + \frac{v_C^2}{R_p} \end{aligned} \quad (2)$$

where T_h is the hotspot temperature, T_a is the ambient temperature, R_{TH} is the thermal resistance, P_{loss} is the power loss, i_C is the RMS value of the ripple current, i_{lk} is the leakage current, v_C is the applied DC voltage, R_s is the series resistance due to contacts (leads, sprayed metal and film metallization [2, 11]), and R_p is the insulation resistance. R_s and i_C define the AC power loss, and R_p and i_{lk} or v_C define the DC power loss.

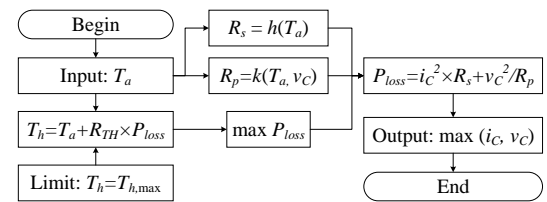


Fig. 3. A flowchart for deriving the SOA boundaries.

Fig. 3 shows the flowchart for deriving the SOA. The limit of the hotspot temperature is temperature which would cause a thermal runaway. R_{TH} can be obtained based on three methods: a) experimental characterizations under the cooling conditions of interest, b) from the respective capacitor supplier, and c) from finite element simulations. Since the letter focuses on deriving the SOA, the details on how to obtain R_{TH} is not included. Therefore, the maximum P_{loss} can be obtained. On the other hand, as R_s and R_p are influenced by T_a , and can be expressed with the functions of T_a (also v_C for R_p), R_s and R_p can be determined for a specific T_a . Then (2) can be used to obtain the maximum operating current and voltage, resulting in the maximum P_{loss} .

For a film capacitor, the SOA boundary can be divided into three regions as follows:

$$\begin{cases} i_C = I_{rp,max}, & 0 < v_C < V_{C,1} \\ i_C^2 \times R_s + \frac{v_C^2}{R_p} = \frac{T_{h,max}-T_a}{R_{TH}}, & V_{C,1} \leq v_C < \alpha V_{C,r} \\ v_C = \alpha V_{C,r}, & \text{others} \end{cases} \quad (3)$$

where $V_{C,1}$ is $\sqrt{(\frac{T_{h,max}-T_a}{R_{TH}} - I_{rp,max}^2 \times R_s) \times R_p}$, R_p can be written as the function of T_a and v_C , i.e. $k(T_a, v_C)$ [2]. The tolerances of R_s , R_p , and R_{TH} can be taken into account by Monte Carlo simulation based on (3). To consider the impact of degradation on the SOA, the updated degradation-dependent parameters need to be substituted in (3) to derive the corresponding SOAs. Similarly, if the impact of cooling condition is of interest, the respective R_{TH} values are applied in (3).

IV. CASE STUDY

This section presents a case study of a 1.25 kV / 645 μ F film capacitor, with specifications listed in Table I.

A. SOA derivations

For Region (1), according to the specification, $I_{rp,max}$ is 80 A. For Region (3), $V_{C,r}$ is 1.25 kV, while the surge voltage is 1.875 kV. Therefore, α is 1.5. For Region (2), experiments are conducted to determine R_p and $T_{h,max}$.

The experiment setup is shown in Fig. 4. The sample capacitors are placed in the chamber, which can maintain a specified T_a . The power supply can provide up to 2 kV DC voltage, 0.1 A DC current, and up to 50 A RMS AC current with controllable frequencies from 50 Hz to 1 kHz. The multimeter is used to measure the leakage current i_{lk} of the samples. The data logger is used to monitor T_h with a thermal sensor integrated inside of the capacitor samples.

1) R_p : To obtain the relation of R_p with T_a and v_C , a series of experiments under different temperatures (65 °C, 75 °C, 85 °C, 95 °C) and voltages (1 kV, 1.1 kV, 1.2 kV, 1.3 kV, 1.4 kV, 1.5 kV, 1.6 kV) are performed. The results are shown in Fig. 5. According to the curve shape, R_p can be expressed as follows:

$$R_p = k(T_a, v_C) = R_{p0} \times a_1^{\frac{T_0-T_a}{a_2}} \times \left(\frac{v_C}{V_0}\right)^{a_3} \quad (4)$$

where T_0 is the reference temperature (e.g., 25 °C), V_0 is the reference DC voltage (e.g., the rated voltage), R_{p0} is the reference insulation resistance measured under T_0 and V_0 , and $a_0 \sim a_3$ are coefficients. Based on the results shown in Fig. 5 and the model in (4), the curve-fitted model is:

$$R_p = 2000 \times 2^{\frac{25-T_a}{7}} \times \left(\frac{v_C}{1.25}\right)^{-3.858} \quad (5)$$

2) $T_{h,max}$: An experiment with two capacitors, sample 1 and sample 2, is performed to determine the rough thermal limit $T_{h,max}$. A relatively critical testing condition under 1.6 kV and T_a of 95 °C is chosen to trigger possible thermal runaway. No ripple current is supplied. Fig. 6 shows the measured hotspot temperature curves of the samples and the

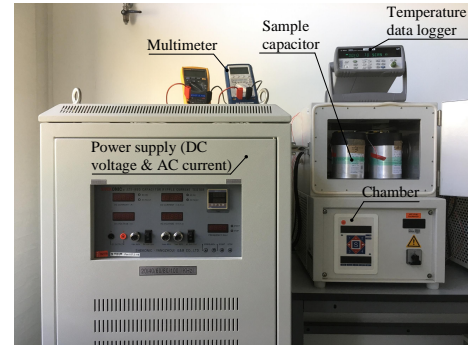


Fig. 4. The experimental setup for the limit testing of capacitor samples.

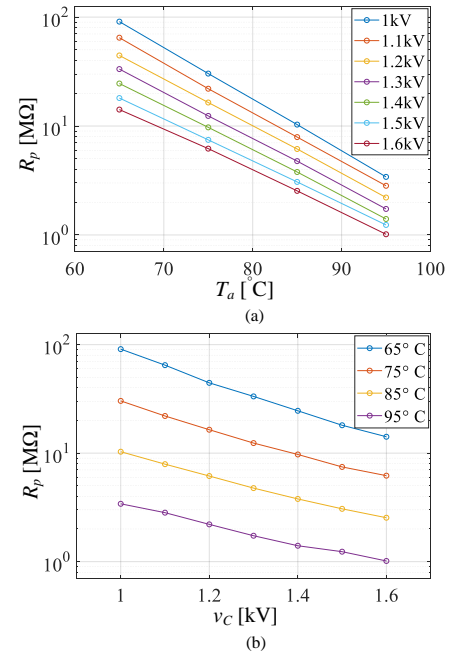


Fig. 5. Measured temperature- and voltage-dependent insulation resistance: (a) R_p vs. T_a ; (b) R_p vs. v_C .

photo of the failed capacitor. At the first 16.4 hours, the hotspot temperature of both samples is 97 °C. After that, the two thermal curves become distinctively increasing. At 18.1 hours of testing, sample 2 reaches a thermal stress level of 122 °C which subsequently induces a thermal runaway. As shown in Fig. 6 (b), the capacitor is melted as the temperature exceeds the dielectric's melting point. At the time of 19.5 hours, the protection of the chamber is triggered. The increase of the hotspot temperature is due to the leakage current increase. The excessive thermal stress leads to a catastrophic failure of sample 2. Sample 1 has not entered into a thermal runaway mode, most likely due to parameter tolerances. According to these initial testing results, it is reasonable to assume the $T_{h,max}$ is 122 °C for the SOA derivation.

Based on the obtained information and (3), the SOA of the capacitor of interest is derived and shown in Fig. 7. It can be noted that the SOA is ultimately defined by Region (1) and Region (2) only when the ambient temperature is above 87 °C.

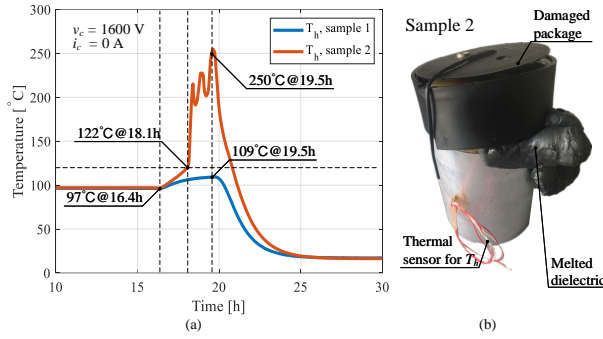


Fig. 6. Experimental testing results of the two capacitor samples: (a) capacitor thermal stresses; and (b) photo of the failed sample with thermal breakdown.

B. Proof-of-concept experimental verifications

Eight additional capacitor samples are tested under four conditions with different DC voltages and AC ripple currents. Samples 3 and 4, 5 and 6, 7 and 8, and 9 and 10 are tested under T_a of 95 °C and 50 Hz ripple current of 10 A, 20 A, 30 A, and 40 A, respectively. The DC voltages are 1550 V, 1540 V, 1530 V, and 1500 V, respectively. The design of these tests aims to verify the Region (2) boundary of the derived SOA. It should be noted that this letter focuses on a proof-of-concept only. More comprehensive experimental verifications under different ambient temperatures, different cooling conditions, and more diverse capacitor samples will be conducted in future research.

Fig. 8 shows the testing results. It should be noted that, different from the test shown in Fig. 6, the testing system is shutdown at a maximum ambient temperature between 125 °C to 150 °C for safety consideration. For the testing condition of $i_C = 10$ A, T_h of sample 3 is relatively steady, while T_h of sample 4 increases fast, and goes up to 125 °C within 3 hours, resulting in the package broken as shown in Fig. 8 (b). The similar results occur in the testing condition of $i_C = 20$ A, T_h of sample 5 is relatively steady, while T_h of sample 6 increases fast, and much faster when it goes up to 125 °C, and also fails in the end. For the testing condition of $i_C = 30$ A, T_h of sample 8 increases to 122 °C within 2 hours. T_h of sample 7 also has a distinct rise rate but less than that of sample 8. For the testing condition of $i_C = 40$ A, T_h of both samples increases fast and reaches the temperature threshold at 6.7 hours. The package of sample 10 breaks up. Sample 9 does not fail as the measured capacitance value after the cooling down has only 0.8% variation compared with the rated one.

The above four testing conditions are selected from the derived SOA curve under the ambient temperature of 95 °C, as shown in Fig. 9. Since failures do occur at the respective testing conditions, the derived SOA is partially verified. Based on the testing of the ten capacitor samples, it can be noted that under the same testing conditions, part of the capacitors reach the thermal runaway modes, while others can still operate safely within their SOAs. Therefore, the experiments also reveal the necessity to consider parameter tolerances. The dashed line shown in Fig. 9 shows an indicative SOA for the capacitors which have not failed in the tests.

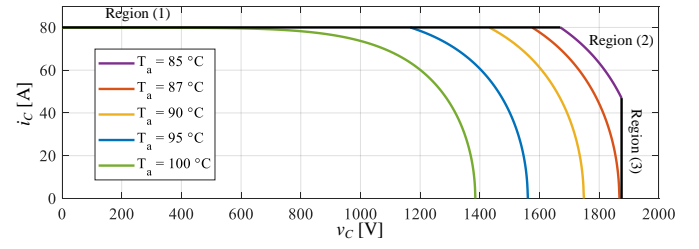


Fig. 7. Derived SOAs under different ambient temperature of the capacitors in the case study.

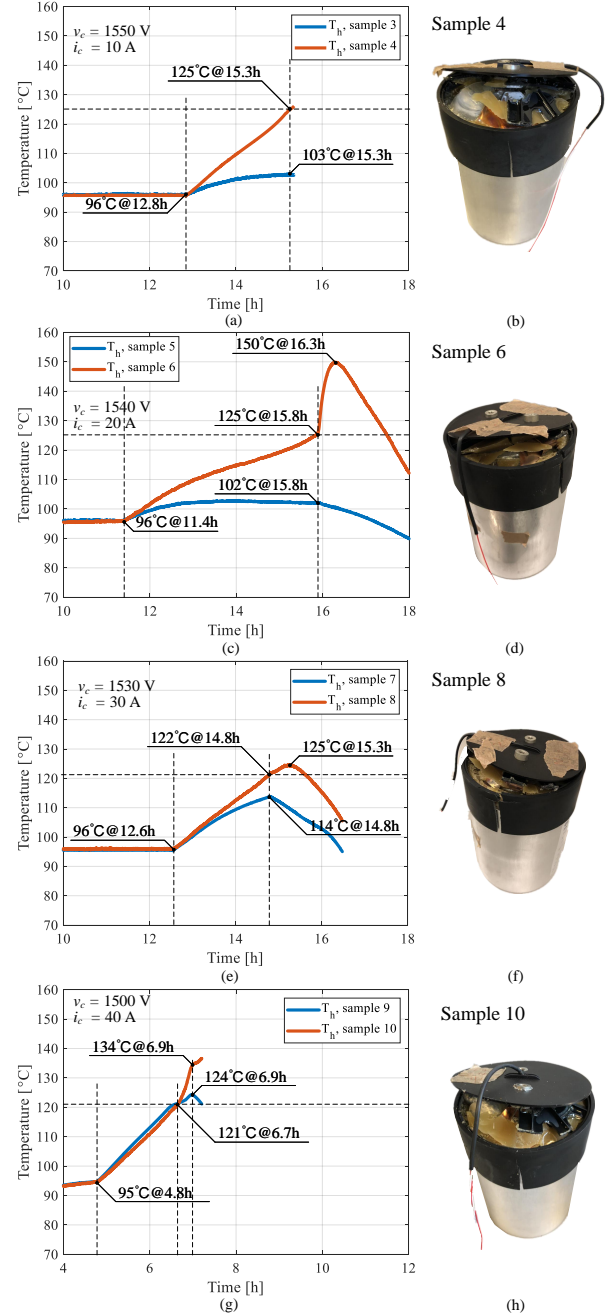


Fig. 8. Experimental testing results of the capacitor samples for SOA boundary verification, thermal stresses and failed samples: (a)(b) $v_C = 1550$ V, $i_C = 10$ A; (c)(d) $v_C = 1540$ V, $i_C = 20$ A; (e)(f) $v_C = 1530$ V, $i_C = 30$ A; and (g)(h) $v_C = 1500$ V, $i_C = 40$ A.

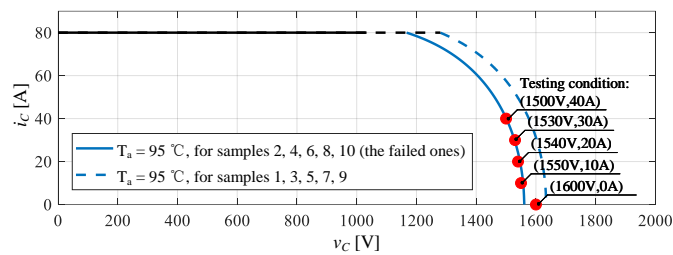


Fig. 9. Operating points of the experimental testing added to the derived SOA shown in Fig. 7 under the ambient temperature of 95 °C.

V. CONCLUSIONS

A Safe Operating Area (SOA) concept is proposed for DC-link film capacitors considering the voltage and ripple current boundaries under different ambient temperature, degradation level, and component variances. It provides more comprehensive operation limits of film capacitors for power electronic converter design and failure investigation. The case study of ten 1.25 kV / 645 μ F capacitors demonstrates the derivations of the SOA boundaries. The experimental results reveal that insulation resistance (i.e., related to leakage current) plays an important role in the thermal stresses under high-voltage and high-temperature conditions. It reveals different SOA boundaries of the ten testing samples due to the component variances (e.g., parameter tolerance). Part of the testing samples fail due to the thermal breakdown as the selected testing conditions are out of their SOA. The other ones maintain safe operation. Future studies will be SOA characterizations under different degradation levels and cooling conditions, with more comprehensive experimental testing. It expects that the proposed SOA concept will enable a better design guideline for sizing of film capacitors in DC-link applications.

REFERENCES

- [1] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters – An overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014.
- [2] TDK, *General technical information: Film capacitors*, 2018. [Online]. Available: <https://www.tdk-electronics.tdk.com/download/530754/480aeb04c789e45ef5bb9681513474ba/pdf-generaltechnicalinformation.pdf>.
- [3] Vishay, *Datasheet: MKP1848 DC-Link, metallized polypropylene film capacitors DC-link capacitor*, 2017. [Online]. Available: <https://www.vishay.com/docs/28164/mkp1848dcl.pdf>.
- [4] C. P. Lee, N. G. Tao, and B. J. F. Lin, "Studies of safe operating area of InGaP/GaAs heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 4, pp. 943–949, 2014.
- [5] Texas Instruments, *TI training: Understanding MOSFET datasheets - safe operating area (SOA)*, 2016. [Online]. Available: <https://training.ti.com/zh-tw/understanding-mosfet-datasheets-safe-operating-area-soa>.
- [6] Toshiba, *Knowledge: What is a safe operating area?* [Online]. Available: https://toshiba.semicon-storage.com/ap-en/semiconductor/knowledge/faq/mosfet_igbt/igbt-008.html.
- [7] TDK, *Datasheet: Film capacitors – Power electronic capacitors, MKP DC*, 2018. [Online]. Available: https://www.tdk-electronics.tdk.com/inf/20/50/ds/MKP_DC_B2568X_ed2.pdf.
- [8] KEMET, *Datasheet: Aluminum can power film capacitors - C44U_M, 600 - 1,800 VDC, for DC link*, 2020. [Online]. Available: <https://www.kemet.com/en/us/capacitors/film/product/C44USGT6300M51K.html>.
- [9] CDE Cornell, *Datasheet: Type 947D polypropylene, high energy density, DC link capacitors*. [Online]. Available: <https://www.cde.com/resources/catalogs/947D.pdf>.

- [10] AVX, *Datasheet: Hybrid vehicles and electric vehicles capacitors - general description*, 2017. [Online]. Available: <https://datasheets.avx.com/AVX-FHC-Series.pdf>.
- [11] Vishay, *General technical information: Film capacitors*, 2017. [Online]. Available: <https://www.vishay.com/docs/26033/gentechinfofilm.pdf>.