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Design for Reliability of SiC-MOSFET-Based 1500-V PV Inverters with Variable Gate Resistance

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***Abstract*—1500-V Photovoltaic (PV) configuration is the standard design in the solar PV industry. Extending the maximum DC voltage from 1000 V to 1500 V can reduce the installation cost of the entire power plant. However, it may affect the reliability of the corresponding 1500-V PV inverters, due to the increased loading stresses, i.e., voltage stress and thermal loading of power devices. In this context, this paper proposes a solution to the reliability enhancement of SiC-MOSFET-based 1500-V PV inverters with variable gate resistance. This solution offers a possibility to adaptively adjust the switching speed to make a compromise between the switching power loss and voltage overshoot during commutation, thus enhancing the reliability. The evaluation results based on the mission profile of a 125-kW 1500-V PV system installed in Denmark indicate that the PV inverter with the proposed design, i.e., variable gate resistance, can improve reliability performance compared to the fixed gate resistance solution while ensuring a safer operating voltage margin.**

***Index Terms*—Photovoltaic (PV) inverters, SiC-MOSFET, gate driver, lifetime, reliability.**

I. Introduction

More grid-connected PV systems are expected to be installed in the future and they will soon share a major part of the renewable energy generation [1]. Several studies have shown that increasing the DC voltage is an effective way to reduce the installation cost of PV power plants, hence further improving their competitiveness [2]–[5]. Currently, the mainstream DC voltage of large-scale PV plants has been increasing from 600 V or 1000 V to 1500 V, which is the maximum voltage limit in low-voltage grids according to the IEC standards [6]. There have been increasing discussions on higher DC voltages for PV systems to directly integrate into medium-voltage grids [7]. The increased voltage requires careful considerations in the design and control of PV inverters [8]–[10], which are the key to achieve the power conversion efficiently and reliably.

Single-stage energy conversion based on two-level inverter is a typical system configuration of PV systems with lower PV-string voltages, e.g., 1000-V. It offers a cost-effective solution due to the reduced weight, size, and cost [3]. Nevertheless, the PV inverter based on two-level topology may not be a suitable candidate to accommodate the 1500-V technology. This is mainly due to the high power losses and increased filtering efforts as well as the voltage de-rating of the 1700-V IGBT power module to avoid an increase in the failure rate due to cosmic rays [11], [12]. On the other hand, the advances in power semiconductor technologies bring more opportunities to improve the performance of PV systems. Silicon-Carbide (SiC) devices offer lower power losses, faster switching capability, higher voltage blocking capability, and lower failure rates caused by cosmic radiation [13]–[15]. Thus, the use of the 1700-V SiC power devices, as illustrated in Fig. 1, can potentially enable the two-level inverter to be widely adapted in 1500-V PV systems. The corresponding SiC devices/modules and inverters for 1500-V PV applications are already available on the market [16], [17].

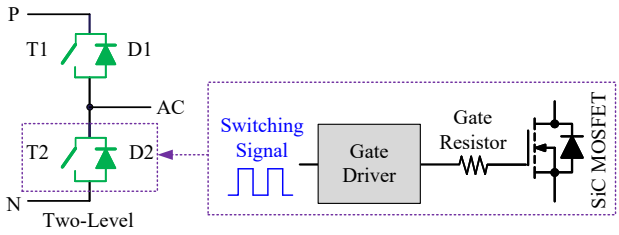

Fig. 1. Two-level inverter topology based on SiC power devices.

However, for 1500-V PV applications, the two-level topology with 1700-V SiC modules still has a limited voltage blocking margin, especially considering the voltage overshoot during the switching transients of a SiC MOSFET. This is primarily due to its high switching speed (i.e., large di/dt) and the stray inductance in the commutation loops, which could be higher than 100 nH for two-level inverter layouts [18]. During the cold days in winter, the voltage at the Maximum Power Point (MPP) of PV strings can reach 80-85% of the open-circuit voltage (i.e., 1500 V), which is approximately 1300 V or even higher [12] depending on the mission profiles of the PV system site, i.e., solar irradiance and ambient temperature. In this case, only a 400-V voltage overshoot is permissible to keep the power devices within their safe operating area in terms of voltage ratings.

To address this challenge, the switching speed of SiC MOSFETs should be reduced, e.g., by using a large gate resistor in practice. However, doing so will affect the semiconductor efficiency and reliability, as discussed in [19]. It is preferable to limit the voltage overshoot, while minimizing the switching losses. This can be achieved by using active

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TABLE I
PV INVERTER MAIN SPECIFICATIONS.

Nominal power P_{nom}	125 kW
Power factor $\cos(\varphi)$	1.0
Grid line-to-line RMS voltage V_{LL}	600 V
Grid frequency f_{g}	50 Hz
Switching frequency f_{sw}	8 kHz
Heatsink thermal impedance $R_{\text{th(s-a)}}$	0.088 K/W per module

gate driving technologies [18], [20], [21], which can adjust the gate resistance dynamically during every single switching transient. Notably, due to the fast switching speed of SiC MOSFETs, the implementation of active gate drivers is, however, challenging, which limits its practical applications. For the considered PV inverter in Fig. 1, a variable-resistance gate driver thus proposed, which adjusts the gate resistance with slower dynamic following the mission profiles (i.e., the PV voltage variations) rather than every switching transient. Accordingly, the proposed method is easier to implement in comparison with the state-of-the-art solutions, being a cost-effective way to improve the reliability performance of PV systems. In light of the above, the impact of switching speed on the reliability of SiC-MOSFET-based 1500-V PV inverters is first analyzed in this paper. The analysis is carried out through a case study on a 125-kW two-level PV inverter employing 1700-V SiC power modules [22]. Subsequently, a variable-resistance gate driver is proposed and designed for the 1500-V two-level PV inverter system. The results indicate that, compared to the fixed-resistance gate driver, the lifetime of the SiC MOSFETs within the PV inverter can be improved by over 70% when using the proposed variable-resistance design.

The rest of this paper is organized as follows. In Section II, the system description is provided, which includes the specifications of the system and its operating conditions (i.e., the mission profiles). Then, the impact of the switching speed on the inverter loading stress is presented in Section III, where a variable-resistance gate driver is proposed for reducing the thermal stress, and thus, enhancing the reliability. A comparative reliability assessment of the PV inverter is carried out considering two scenarios (i.e., with the variable-resistance and the fixed-resistance gate drivers), which is presented in Section IV. Finally, concluding remarks are given in Section V.

II. SYSTEM DESCRIPTION

The general configuration of the considered 1500-V PV system is shown in Fig. 2. Here, a single-stage configuration is adopted, where a 125-kW three-phase two-level inverter based on three 1700-V SiC MOSFET power modules is employed as the power interfacing converter between the PV array and the AC grid. The specifications of the PV inverter and the adopted SiC module are given in Tables I and II, respectively. The heatsink is designed to limit the junction temperature to 125 °C at the rated operation (see Table I) with the ambient temperature T_{a} being 50 °C.

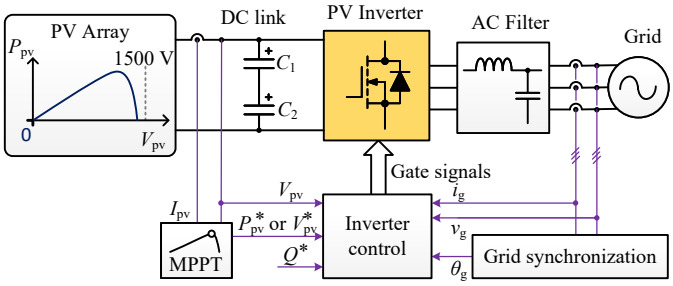

Fig. 2. System configuration and the basic control structure of the 1500-V PV system based on two-level topology and SiC power devices: P_{pv}, V_{pv}, and I_{pv} represent the output power, voltage, and current, respectively; P_{pv}^*, Q^*, and V_{pv}^* denote the control reference of the PV system, i.e., the active power, the reactive power, and the DC-link voltage, respectively; i_{g} , v_{g}, and θ_{g} are the grid current, the grid voltage, and the phase angle of the grid voltage, respectively.

TABLE II
PARAMETERS OF THE SIC MODULE BSM250D17P2E004 [23].

Voltage rating	1700 V
Current rating	250 A
Minimum and maximum gate voltage	-6 V, 22 V
Junction temperature	-40 to 150 °C
Internal gate resistance	1.4 Ω
Stray inductance	13 nH
Diode type	SiC-SBD[1]

[1] Schottky barrier diode.

In addition, in order to evaluate the inverter lifetime under real operating conditions, a one-year mission profile recorded in Denmark with a sampling rate of 1 min/sample is used in this paper [24], which is shown in Fig. 3. The PV array configuration and the specifications of the adopted PV panel are summarized in Table III, where the PV array size is designed to match the inverter ratings under the Denmark mission profile.

As shown in Fig. 2, a Maximum Power Point Tracking (MPPT) operation is considered to obtain the operating conditions (e.g., power and DC-link voltage) of the PV inverter. This is normally achieved by the control of the PV inverter, which operates at the MPP of the PV array and then delivers the maximum available PV power to the AC grid. With these operational conditions, the impact of variable-resistance gate driver on the inverter reliability is analyzed in the following sections.

III. PROPOSED VARIABLE GATE-RESISTANCE DESIGN

The junction temperature of power devices rises above the ambient temperature when power losses, i.e., conduction and switching losses, are generated during operation, which is the origin of thermal-related wear-out failure. Generally, the power losses not only depend on the operating conditions (e.g., voltage, current, and switching frequency) but also the gate-driving parameters (e.g., the external gate resistance) [26]. It is expected to reduce the external gate resistance and increase the gate current in order to achieve high speed switching (less switching losses). However, accelerating the switching

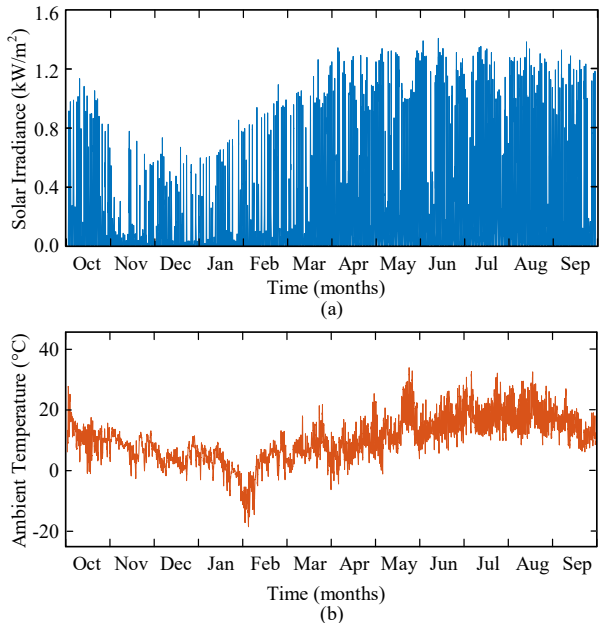

Fig. 3. Yearly mission profiles for the 1500-V PV inverter installed in Denmark: (a) solar irradiance and (b) ambient temperature.

TABLE III
PV ARRAY CONFIGURATION AND SPECIFICATIONS [25].

PV array configuration	
PV panel type	JKM380M-72-V
Number in series / parallel	28 / 12
PV panel specifications[1]	
Maximum power P_{max}	380 W
Maximum power voltage V_{mp}	40.5 V
Maximum power current I_{mp}	9.39 A
Open-circuit voltage V_{oc}	48.9 V
Short-circuit current I_{sc}	9.75 A
Temperature coefficient of V_{oc}	-0.37 %/°C
Temperature coefficient of I_{sc}	0.048 %/°C

[1]Under the Standard Test Condition (STC).

would increase the voltage overshoot, which may destroy the devices and cause EMI issues. Consequently, an appropriate gate resistance design requires careful consideration on the tradeoff between power losses and voltage overshoot.

A. Gate Resistance Impact on Power Losses

In this section, the impact of the SiC MOSFET switching speed on the PV inverter loading (power losses) is analyzed. Power losses, which are composed of conduction and switching losses, induce the thermal loading of the power devices. The forward voltage drop V_{DS} during conduction and the turn-on/-off energy E_{sw}, i.e., E_{on} and E_{off}, during switching, respectively, contribute to the power losses. Fig. 4 shows the variation of the voltage drop V_{DS} and switching energy E_{sw} of the MOSFET in the selected SiC MOSFET module under different drain currents I_D. In addition, the switching behaviors of both the MOSFET and the diode within the

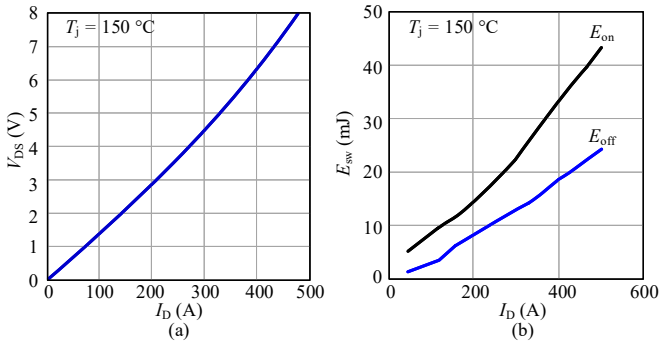

Fig. 4. Voltage drop V_{DS} and switching energy E_{sw} of the MOSFET in the selected SiC module under different drain currents I_D, when the junction temperature T_j is 150 °C (E_{on} and E_{off} represent the switching energy during the turn-on and -off transients): (a) voltage drop and (b) switching energy.

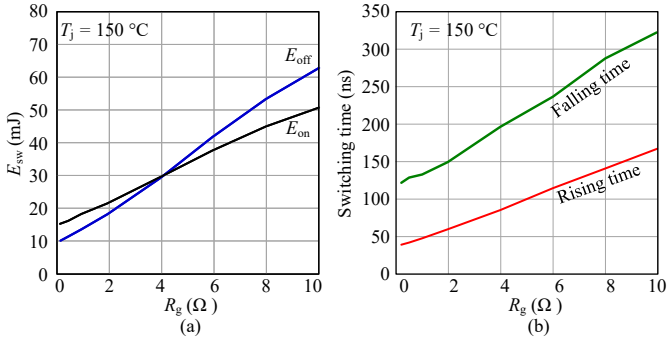

Fig. 5. Switching energy E_{sw} and switching time of the MOSFET in the selected SiC module under various gate resistances R_g, when the junction temperature T_j is 150 °C: (a) switching energy and (b) switching time.

SiC MOSFET module are also affected by the gate resistor. Thus, the value of the gate resistance should be properly designed. The relationship between the gate resistor, switching speed, and switching energy is illustrated in Fig. 5, where a smaller gate resistance (i.e., a fast switching speed) results in lower switching energy losses. Nevertheless, for 1500-V PV applications, the two-level topology with 1700-V devices has a limited voltage blocking margin. As a consequence, its switching speed (dv/dt and di/dt) should be slowed down by using a larger resistor to reduce the switching overshoot due to the stray inductance in the commutation loops. This, however, negatively affects the thermal performance of the PV inverter because of the increased switching losses, as shown in Fig. 6, where the thermal loading of the SiC MOSFET rises drastically with the increase of the gate resistance.

B. Gate Resistance Impact on Voltage Overshoot

To further explain the switching voltage overshoot issue, a detailed switching overvoltage analysis is performed in simulations considering a total stray inductance of 100 nH within the commutation loop. Fig. 7 depicts the schematic representation of the simulation model with all the stray inductances. Since the SiC MOSFET module has a junction barrier Schottky diode instead of using its own body diode, the reverse recovery problems such as current and voltage overshoots during turn-on transients can be effectively suppressed [27]. Thus, only

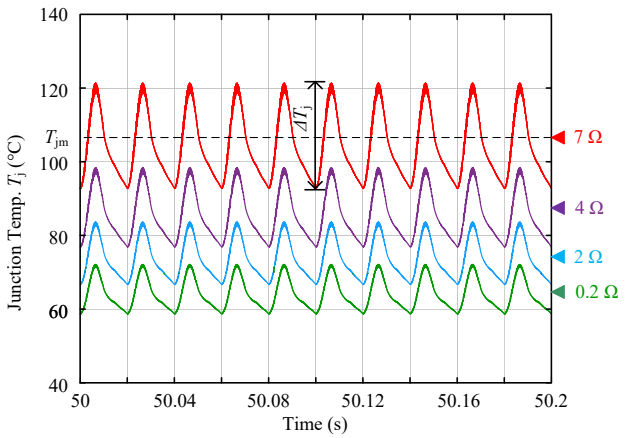

Fig. 6. Thermal loading of the SiC MOSFETs in the considered inverter under the rated operation condition (see Table I) and various gate resistance R_g, where T_{jm} and ΔT_j are the mean value and the cycle amplitude of the junction temperature, respectively.

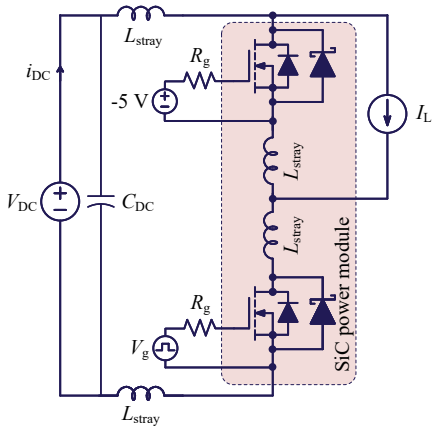

Fig. 7. Schematic representation of the simulation model for the SiC MOSFET module with all the stray inductances: L_{stray} – stray inductance; i_{DC} – DC-link current; I_L – load current; V_{DC} – DC-link voltage; R_g – gate resistor.

the turn-off transients are analyzed. Fig. 8 presents the turn-off transients of the lower MOSFET with different gate resistance values. In the simulation, the DC-link voltage is kept at 1300 V, and the drain current is 250 A with the junction temperature of T_j = 150 °C. It can be observed in Fig. 8 that using a small gate resistance value, i.e., R_g = 0.2 Ω (the minimum permissible external gate resistor in the datasheet), results in large voltage overshoots even exceeding the device voltage rating (i.e., 1700 V). When using higher value of R_g, the voltage overshoots will be reduced. However, the voltage-changing slope becomes smaller, which will result in higher switching losses as aforementioned.

C. Variable Gate Resistance Design

To achieve a high reliability performance, it is expected to attain fast switching transients to reduce switching loss while ensuring a safe voltage overshoot margin. A variable-resistance gate driver, which can dynamically change the gate resistance following the mission profiles, can be a cost-effective solution in this case. Fig. 9 presents the MPP voltage

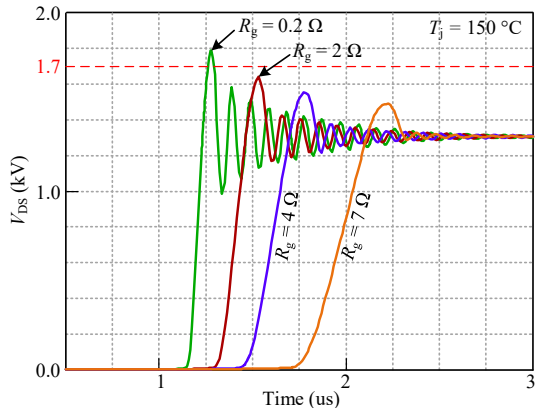

Fig. 8. Turn-off transients of the lower MOSFET in the selected SiC module (see Fig. 7) under various gate resistances R_g, when the junction temperature T_j is 150 °C.

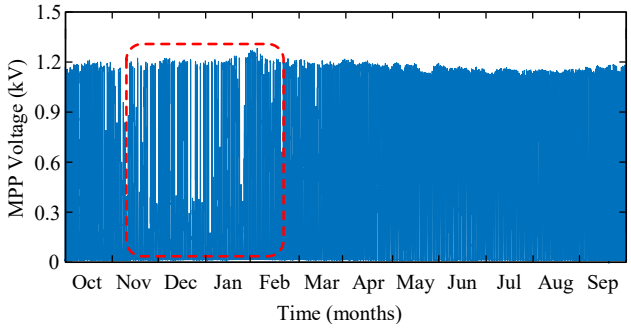

Fig. 9. MPP voltage profile under the one-year Denmark mission profile.

profile during the one-year Denmark mission profile (see Fig. 3). It should be pointed out that the MPP voltage varies from 1000 V to 1200 V during the yearly operation. However, the MPP voltage can reach 1300 V during the cold winter days (the highlighted area in Fig. 9). In addition, considering low-voltage ride-through operations, the PV inverter may need to provide reactive power with the DC-link voltage being the open-circuit voltage of the PV array, which could be as high as 1500 V. Correspondingly, the variable gate resistance is designed in the following considering three available gate resistors R_g.

1) Maximum R_g: The maximum applied gate resistance considers the most severe operating condition in terms of voltage overshoot, i.e., reactive power support at 1500-V DC-link [28], [29]. Fig. 10 presents the turn-off transients of the lower MOSFET with various gate resistance values, where the device current is set to 188 A (1.1 times of the inverter's rated current) and the DC-link voltage is 1500 V. It can be observed from Fig. 10 that small gate resistance, e.g., < 5 Ω, should not be adopted; otherwise, the voltage overshoot would exceed the device rating. Consequently, the maximum gate resistance is determined as 7 Ω to limit the voltage overshoot and avoid significant switching losses.

2) Medium R_g: Regarding the medium gate resistance, the most stressed case during normal operating conditions is considered, i.e., maximum output current under the highest MPP voltage (e.g., 1300 V). Fig. 11 presents how the gate resistance affects the voltage overshoot in such a case, where

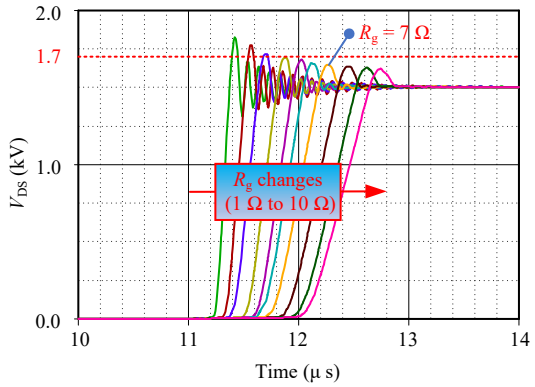

Fig. 10. Turn-off transients of the lower MOSFET in the selected SiC module (see Fig. 7) under various gate resistances R_g, when the DC-link voltage is 1500 V and the load current is 188 A.

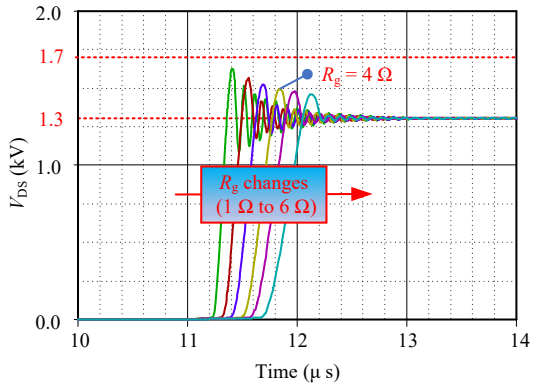

Fig. 11. Turn-off transients of the lower MOSFET in the selected SiC module (see Fig. 7) under various gate resistances R_g, when the DC-link voltage is 1300 V and the load current is 188 A.

several gate resistance could be adopted depending on the expected blocking voltage margin. The medium gate resistance value is considered to be 4 Ω for ensuring a 200-V voltage margin.

3) Minimum R_g: As for the minimum gate resistance, a moderate value should be considered to avoid the high switching ringing [19]. For the case study, the minimum gate resistance value is set to 2 Ω.

To obtain the usable range of the minimum gate resistance for a certain blocking voltage margin, a series of parametric sweeps have been performed, as presented in Fig. 12, where the load current I_L varies from 100 A to 200 A before turning off the MOSFET at 1300-V DC-link. It is indicated in Fig. 12 that, for a 200-V voltage margin, the load current should be lower than 130 A. Fig. 13 indicates the operating zone for each gate resistance. When the DC-link and the output current are lower than a certain level, the minimum R_g can be applied; otherwise, the applied gate resistance should be changed to the medium R_g, e.g., the green triangular area. In case of a high DC-link voltage, e.g., during reactive power support with open-circuit voltage (>1300 V), the maximum R_g is used. Alternatively, the applied gate resistance can be simply determined according to the variation of the DC-link voltage. According to the previous switching overshoot analysis, the applied R_g and the corresponding DC-link voltage V_{DC} can

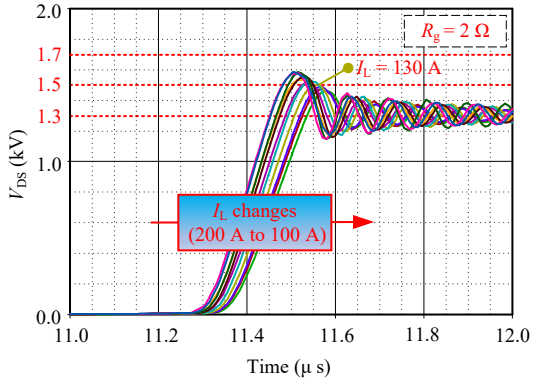

Fig. 12. Turn-off transients of the lower MOSFET in the selected SiC module (see Fig. 7) under under various load current I_L, when the DC-link voltage is 1300 V and the external gate resistance is 2 Ω.

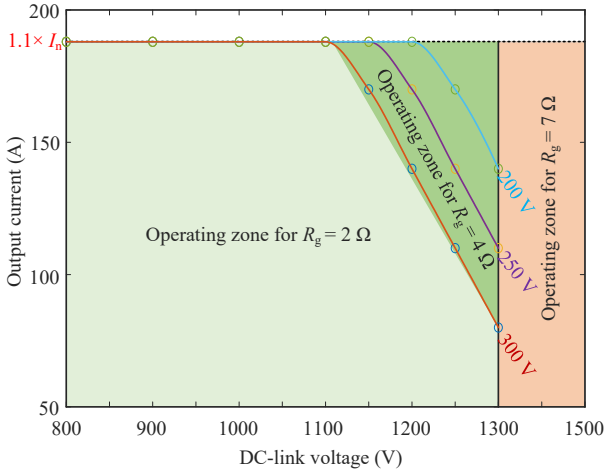

Fig. 13. Operating zone for each gate resistance, where 200 V, 250 V, and 300 V represents the expected blocking voltage margin when R_g = 2 Ω.

be correlated and designed as

$$R_g = \begin{cases} 2\ \Omega, V_{DC} \le 1000\ \text{V} \\ 4\ \Omega, 1000\ \text{V} < V_{DC} \le 1200\ \text{V} \\ 7\ \Omega, V_{DC} > 1200\ \text{V} \end{cases} \quad (1)$$

in which 1000 V and 1200 V are selected as the DC-link thresholds to ensure a sufficient blocking voltage margin.

D. Implementation of the proposed method

The proposed variable-resistance driver consists of three main parts: a signal conditioning unit, two auxiliary gate resistors, and the main gate driver. The overall block diagram of the proposed design is shown in Fig. 14. As it can be seen in it, the pulse width modulation (PWM) signal and the DC-link voltage signal are fed to a signal conditioning unit, which decides the input signals of the variable-resistance gate driver. As a consequence, the SiC MOSFET is driven by the main gate driver through R_{main} when the DC-link voltage is higher than 1200 V, and the effective gate resistance can be reduced to $R_{main} \| R_{aux1}$ or $R_{main} \| R_{aux2}$ in the case of lower DC-link voltages. It should be mentioned that the turn-on and -off gate resistances are assumed to have the same value (e.g.,

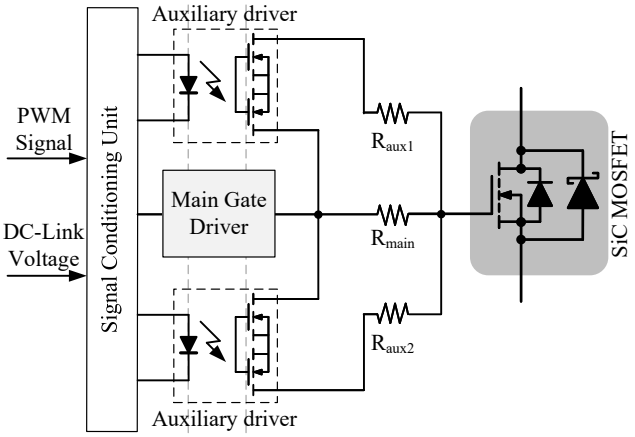

Fig. 14. Circuit diagram of the variable-resistance gate driver: R_{main} – main gate resistors, R_{aux} – auxiliary gate resistors.

$R_{\text{main,on}} = R_{\text{main,off}} = R_{\text{main}}$ in Fig. 14) in this paper for simplicity. In practice, a smaller turn-on gate resistance can be applied in order to further reduce the switching losses.

A hardware prototype employing the considered SiC MOSFET module is built for experimental verification of the proposed gate driver design, as shown in Fig. 15(a). The main gate driving circuits are realized by using the galvanic isolated driver IC UCC21710, which is designed for up to 1700-V SiC MOSFETs by Texas Instruments. This gate driver IC features over 2-kV isolation voltage rating and 10-A peak source/sink current capability. For the auxiliary gate resistors, they are switched by the solid-state relays LCA715 from IXYS for industrial application, featuring 3750-V input-to-output isolation and ultra-low on-resistance for up to 10-A peak current capability. The LCA715 has no moving parts, offering faster, bounce-free switching in a more compact surface mount package, which is well-suited to the variable gate resistance design. The auxiliary gate resistors and the relays are placed on a separate small printed circuit board to avoid affecting the layout of the main gate driver and making a large gate driving loop, as shown in Fig. 15(b).

A double pulse test (DPT) under a 1000-V supply voltage and 250-A load current is performed to validate the proposed design, where a high-voltage passive probe and a current probe based on Rogowski coils are used to measure the drain-source voltage v_{ds} and the drain current i_{d}, respectively. The experimental results are shown in Fig. 16, which are captured with three gate resistor combinations (i.e., R_{main}, $R_{\text{main}} \| R_{\text{aux1}}$, and $R_{\text{main}} \| R_{\text{aux2}}$) controlled by the solid-state relays, i.e., LCA715. It should be pointed out that during the turn-off transient, the switching speed can be increased by enabling the auxiliary gate resistors, thus reducing the switching losses when the voltage stress on the DC-link is low. On the contrary, when the DC-link voltage is high, only the gate resistance on the main gate driver will be applied to reduce the voltage overshoot. The voltage spectrum for the transient waveforms of the drain-source voltage v_{ds} are estimated with Fast Fourier Transform (FFT), as shown in Fig. 17. The resonant frequency 19.2 MHz is the ringing frequency of the turn-off overshoot in Fig. 16, and the magnitude at this point increases with

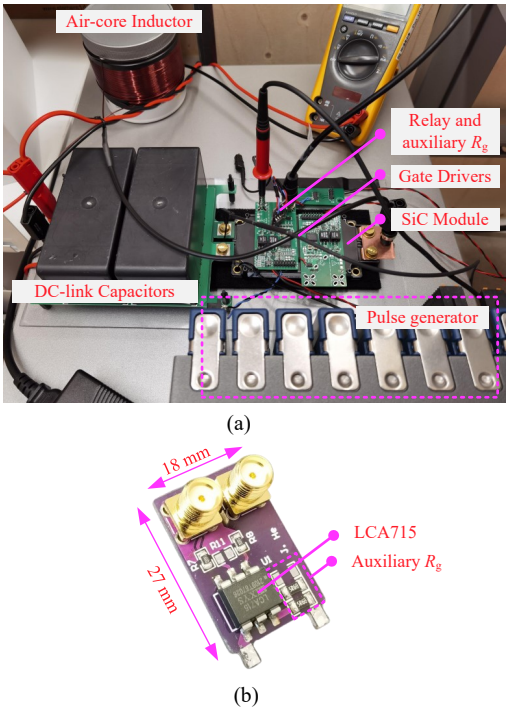

Fig. 15. Prototype for the proposed variable-resistance gate driver: (a) photo of the prototype and (b) the implementation of the auxiliary gate resistors.

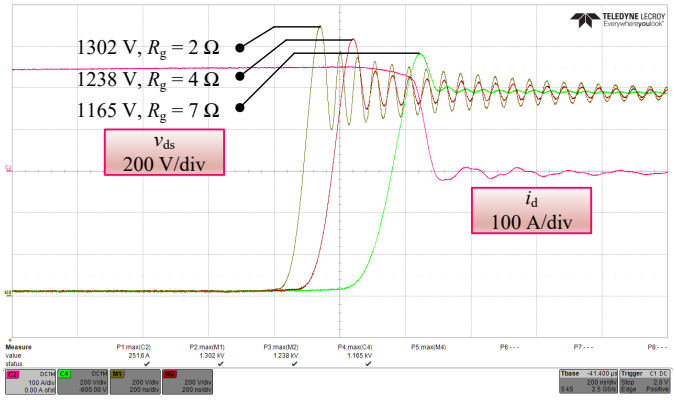

Fig. 16. Turn-off transient waveforms of the drain-source voltage v_{ds} and the drain current i_{d} under different turn-off gate resistance.

the decrease of gate resistance. This is the drawback of the proposed design compared to a fixed one with large gate resistance, i.e., increased filtering efforts for EMI [30], [31].

It should be mentioned that the estimation of the total stray inductance L_{stray} in the commutation loop is critical for modeling the switching process, thus affecting the variable gate resistance design. A robust measurement of L_{stray} can be performed by using the DPT turn-off waveforms, which can be estimated by [32]

$$L_{\text{stray}} = \frac{V_{\text{DM}} - V_{\text{DC}}}{\left| \frac{di_{\text{D}}}{dt} \right|} \tag{2}$$

where V_{DM} denotes the peak drain-source voltage during turn-off, V_{DC} is the DC-link voltage, and di_{D}/dt is the current slope during the initial drain current fall. With the turn-off

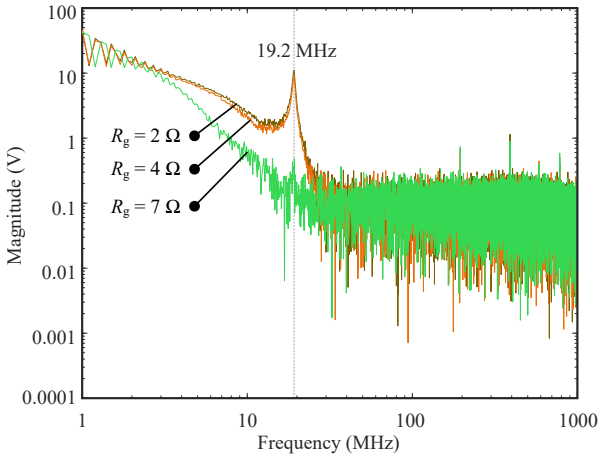

Fig. 17. Voltage spectrum for the transient waveforms of the drain-source voltage v_{ds} under different turn-off gate resistance.

waveforms in Fig. 16, L_{stray} for the realized prototype is estimated to be 90 nH.

The general steps for applying the variable-resistance gate driver on the SiC-MOSFET-based 1500-V PV inverters can be summarized based on the above discussion, which is presented in Fig. 18. Firstly, the stay inductance of the inverter's commutation loop should be estimated experimentally. Then, the gate resistance value for each considered case can be designed. After that, the operating zone for each gate resistance can be determined. Finally, the gate resistance design should be verified experimentally, e.g., by double pulse tests.

IV. Reliability Assessment

In this section, a comparative lifetime evaluation will be performed to analyze the impact of the proposed gate driver design on the lifetime of the 1500-V PV inverter.

Fig. 19 shows the general procedure of the lifetime evaluation. As it can be observed in it, several steps are required to estimate the power device lifetime under certain mission profiles [24]. First, the thermal stress of the power device in the PV inverter should be simulated for a set of operating conditions, in order to obtain look-up tables (LUTs) for the long-term mission profile translation. Then, the thermal loading of the power device can be obtained. Subsequently, a counting algorithm (e.g., rainflow method [33]) can be applied to extract the thermal stress information which can later on be applied to the lifetime model. After that, the lifetime consumption (LC) can be estimated with a specific lifetime model and damage accumulation method. More details regarding the lifetime evaluation have been discussed in [24].

The power loss analysis in Fig. 20 shows that, with the proposed variable gate-resistance design, energy losses can be reduced during operation compared to a fixed gate-resistance design which considers the highest voltage stresses. This energy loss reduction, i.e., over 300 kWh difference per year as shown in Fig. 20, will certainly contribute to a higher reliability performance, which will be analyzed in the following.

After a certain number of power cycles, the SiC MOSFETs tend to fail due to accumulative bond-wire fatigue [34], [35].

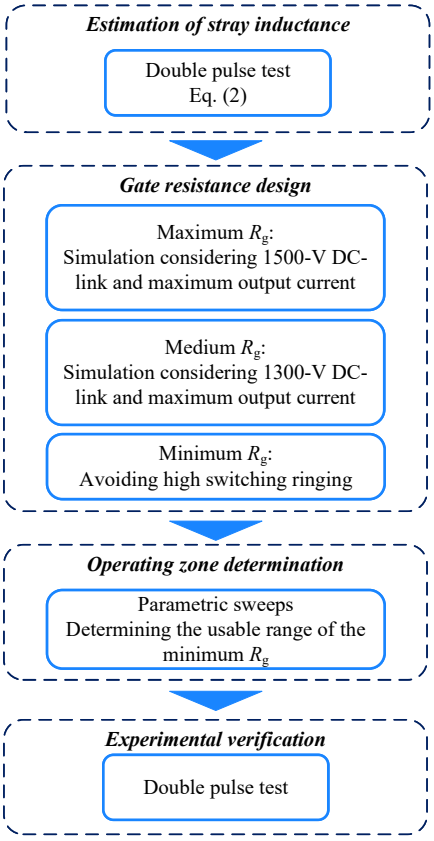

Fig. 18. General steps for applying the proposed variable-resistance gate driver.

In this paper, the lifetime model proposed in [36] is used. It describes the number of cycles to failure N_f under a certain thermal stress (i.e., mean junction temperature T_{jm} and cycle amplitude ΔT_j) as

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C + (t_{on})^{\gamma}}{C+1}\right] \times \exp\left(\frac{E_a}{k_b \times T_{jm}}\right) \quad (3)$$

where the impact of technology fact A, activation energy E_a, bond wire aspect ratio ar, and heating time t_{on} is considered, as summarized in Table IV. More details regarding this lifetime model have been discussed in [36]. Normally, it is assumed that various thermal loading events are independent, and the impact of the damage can be linearly accumulated following the Miner's rule [37]. With that, the LC during operation is then calculated as

$$\text{LC} = \sum_i \frac{n_i}{N_i} \quad (4)$$

in which n_i is the number of temperature cycles under a certain thermal stress, and N_i is the corresponding number of cycles to failure according to the lifetime model given in (3). It is considered as the end of the component life when LC equals to one.

Considering the Denmark mission profile, the above reliability assessment procedure is used to analyze the LC of the

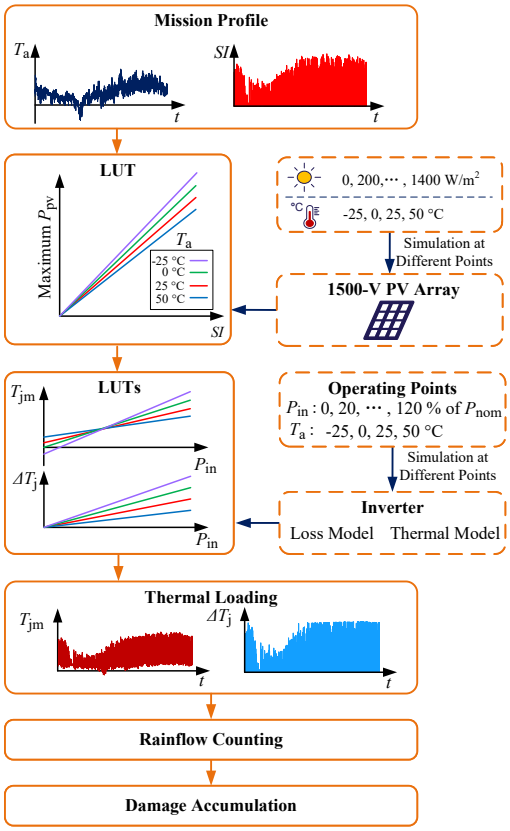

Fig. 19. Lifetime evaluation procedure: T_a – ambient temperature, SI –solar irradiance, P_{pv} – PV output power, P_{in} – inverter input power, LUT – lookup table, T_{jm} – mean junction temperature, ΔT_j – cycle amplitude of junction temperature.

TABLE IV
PARAMETERS OF THE LIFETIME MODEL [36].

Parameter	Value	Test condition
A	3.4368×10^{14}	
α	-4.923	64 K $\leq \Delta T_j \leq$ 113 K
β_1	-9.012×10^{-3}	$0.19 \leq ar \leq 0.42$
β_0	1.942	
C	1.434	
γ	-1.208	0.07 s $\leq t_{on} \leq$ 63 s
E_a	0.06606 eV	32.5 °C $\leq T_j \leq$ 122 °C
k_B	8.6173324×10^{-5} eV/K	

SiC-MOSFET two-level 1500-V PV inverter with a variable-resistance gate driver. For comparison, the LCs of the same PV inverter with various fixed-resistance gate drivers are also estimated. Fig. 21 shows the one-year thermal loadings of the SiC MOSFETs, and Fig. 22 presents the corresponding rainflow counting results. It can be observed in Fig. 21 that the PV inverter with the proposed variable-resistance gate driver experiences much lower thermal stresses than that with a fixed gate resistance value of 7 Ω. When comparing the rainflow counting results, as it can be seen in Fig. 22(a) and (b), the proposed design can reduce the number of thermal cycles with high mean junction temperature T_{jm} and cycle amplitude ΔT_j (the circled area in Fig. 22(b)) in comparison to that with

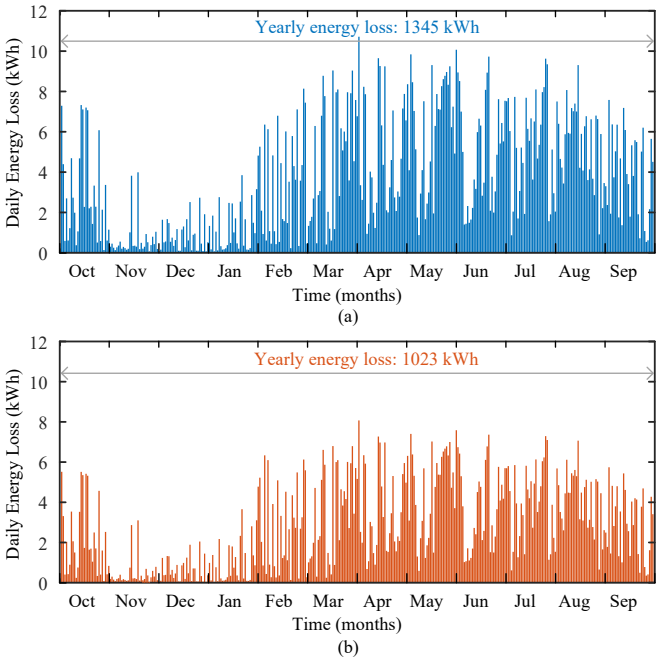

Fig. 20. Daily energy loss under the Denmark mission profile (see Fig. 3): (a) with the fixed gate-resistance design (R_g = 7 Ω) and (b) with the proposed variable gate-resistance design.

TABLE V
LIFETIME CONSUMPTION COMPARISON.

Gate driving methods	LC	LC compared to Case 5
Case 1: variable R_g: 2-7 Ω	0.0071	72.8% lower
Case 2: fixed $R_g = 4$ Ω	0.0070	73.2% lower
Case 3: fixed $R_g = 5$ Ω	0.0134	48.7% lower
Case 4: fixed $R_g = 6$ Ω	0.0198	24.1% lower
Case 5: fixed $R_g = 7$ Ω	0.0261	–

a fixed gate-resistance (the circled area in Fig. 22(a)). Table V presents the comparison of the LCs. It can be seen in Table V that the proposed design can reduce the LC of the SiC MOSFETs by 72.8% compared to the fixed gate resistance case. Moreover, the proposed design achieves a similar lifetime performance as that with a fixed gate resistance value of 4 Ω (i.e., Case 2). The LCs of Case 1 (i.e., the proposed design) and Case 2 are clearly lower than that with a higher fixed gate resistance value. More importantly, compared to Case 2, the proposed design can have a better voltage margin according to the analysis in the previous section.

Table VI further summarizes the comparison of the gate-resistance design in terms of switching losses, voltage overshoot, and LC. As seen in Table VI, with the conventional fixed gate-resistance design, there will be a trade-off between switching losses and voltage overshoot. In contrast, the variable gate-resistance design pushes this trade-off forward and enhances the PV inverter reliability, thus leading to potential reduced cost of PV energy.

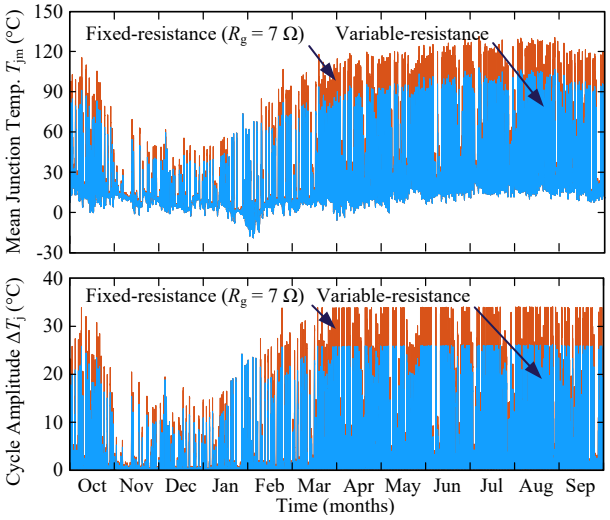

Fig. 21. Thermal loadings (i.e., mean junction temperature T_{jm} and cycle amplitude ΔT_j) of SiC MOSFETs with different gate drivers under the Denmark mission profile (see Fig. 3).

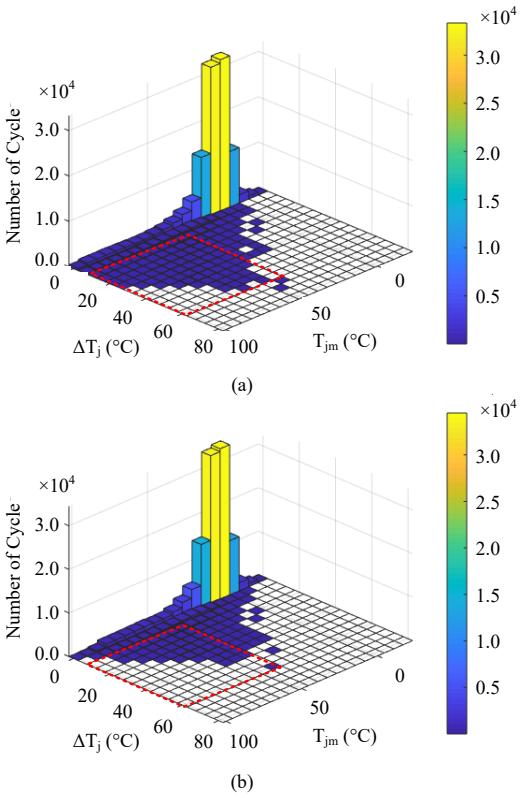

Fig. 22. Rainflow counting results of the thermal loading profile under the Denmark mission profile (see Fig. 3): (a) with the fixed gate-resistance design (R_g = 7 Ω) and (b) with the proposed variable gate-resistance design.

V. Conclusion

In this paper, a method to enhance the reliability of the SiC-MOSFET-based two-level inverter through the design of variable-resistance gate drivers was proposed considering the 1500-V PV application and mission profiles. The proposed variable-resistance gate driver can adjust the gate resistance according to the variation of the DC-link voltage due to the mission profile. By doing so, the switching overshoot due to the stray inductance in the commutation loops can be reduced when the PV array voltage is high, keeping the power devices within their voltage ratings. The proposed design was validated with double pulse tests at 1000-V DC-link and 250-A load current. The corresponding reliability assessment results indicate that the PV inverter with the proposed design has a better lifetime performance than that with fixed-resistance gate drivers, where the gate resistance is typically designed for the highest voltage stresses. It should be mentioned that more EMI filtering efforts may be required for the proposed design when compared to a fixed-type gate driver with relatively larger gate resistance.

TABLE VI
Gate-Resistance Design Comparison.

Gate resistance	Switching losses	Voltage overshoot	LC
Large	High	Low	High
Small	Low	High	Low
Variable	Low	Low	Low

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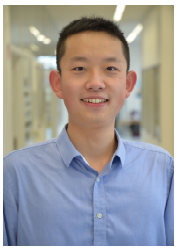

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