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Overview of fault detection approaches for grid connected photovoltaic inverters

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ABSTRACT

Over the past few years, the power electronic converters have gained significant attraction among researchers, especially as an interface between distributed generation (DG) systems and the grid. Hence, it is imperative to establish a path for enhancing the operation of power electronic converters, and improve their reliability. Further, it is identified that for a solar photovoltaic (PV) inverter the power module construction intricacy and the complex operating conditions may degrade the reliability of these modules, affecting the functional efficiency of the overall grid-connected PV systems (GCPS). These constraints are considered to have a serious impact on the safety and failure cost especially associated with the grid-connected PV inverters (GCPIs). Therefore, it becomes crucial to have a clear understanding on the health monitoring strategies and reliability aspects corresponding to GCPIs. Consequently, it is also necessary to arrange all the information regarding major failure modes and categorize their root-cause analysis specific to GCPIs. In light of the above requirements, this paper contributes to the current research in making the GCPS more robust, efficient and reliable. The review identifies a comprehensive list of various failure modes in the inverter power modules and capacitors, and provides a broad view of their detection and localization approaches available in the literature.

1. Introduction

Recently, renewable energy sources like solar, wind, etc. have witnessed an unprecedented growth in their utilization. They are increasingly preferred over conventional sources of energy due to the demerits and associated with the conventional energy resources including their harmful effects on the environment, their finite and exhausting nature etc. Moreover, with the ever-growing energy demand and global population, it is imperative to ease stress on the traditional power system [1]. Therefore, GCPS has attracted significant attention among researchers [2,3]. These systems have DC to AC converters or inverters as the "core" component since they are responsible for the grid forming, grid feeding, and grid supporting operations of the PV systems [4]. A general structure of a GCPS with two-stage three-phase inverter is shown in Fig. 1. These DC/AC converters not only work as an interface, but they also support the grid during disturbances and irregular operating conditions [5]. These converters are affected by the consistent power cycling and temperature deviations experienced by their power modules, their safety and uninterrupted operation is utmost important [6]. However, since these converters often operate in harsh and extreme conditions, they are subjected to innumerable stresses including thermal, electrical, physical and mechanical stress conditions. The combined influence of these stresses results in early degradation in the components. The IEC 62109 standard defines general requirements for inverter components safety and stress related guidelines [7]. The power switching devices are highly susceptible and vulnerable to surrounding harsh environments leading to their fault events [8]. Other than the power switching devices, capacitors also contribute to the faults in a GCPS. To balance the power between the PV and the grid, DC link capacitors are employed. These DC link capacitors encounter extreme surroundings including high temperature, increased humidity etc. Therefore, there are plethora of evidences to support the necessity to concentrate over efforts and strategies in the direction of fault diagnosis of these devices.

It must be noted that a fault detection and localization (FDL) strategy does not substitute the hardware protection equipment like fuses, inbuilt

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limiters, circuit breakers etc.; rather it demonstrates granular knowledge regarding the health of the converter. This knowledge is helpful to attain information on device condition monitoring (CM), prognosis and further, fault corrective measures [9]. The performance of power switching devices with reference to GCPI can be impacted through the occurrence of fault events like Open Circuit (OC) faults, Short Circuit (SC) fault, gate intermittent misfiring faults, etc. These faults might be severe depending upon their intensity; therefore, it is desired to identify them in an early stage [10]. OC faults do not occur suddenly and they do not affect the device operation in the initial stage; instead they are observed to develop gradually affecting other components in the system severely. Thus, the detection of OC faults is more critical and require greater attention. On the other hand, SC faults occur suddenly causing abrupt large inrush current [11]. Electronic devices usually consist of fuses to stop the spread of SC fault in other components. Various factors are affecting these fault occurrences and these factors are studied and investigated in this work. GCPIs consist of different topologies like H-bridge, modular, flying capacitor multi-level etc. Depending upon these topologies, faults may affect them at various intensities. Therefore, it is important to study these faults at many levels including device level, converter topological level and system level and this work is aligned in the direction focusing on various fault diagnostic approaches [12].

This work provides a brief review on the vulnerable component faults in GCPS and their detection techniques. Various FDL techniques have been designed during the past decade and FDL for GCPI, particularly has been perceived as a research hotspot [13]. Therefore, many advanced FDL techniques can be found in literature and they are still worked upon to get better results. Some of these strategies solely focus on a single fault type [14–17], whereas some can handle multiple kinds of faults [18,19].

As of now, there are a few review articles proposed with discussions on various power switch faults and their detailed root-cause analysis. Few of these focus on the in-depth analysis of the major causes of failures in switches or reviewing the CM and prognostics methods [20–22]. In addition, review on online monitoring to estimate the severity of wear-out in power switch is presented [23]. However, they do not inculcate the fault diagnostics, which is an important parameter for ensuring the reliability. Very few articles have focused on the diagnostics in power electronic converters [24,25]. However, they are not dedicated particularly towards GCPI faults and a fresh and up to date analysis and review is lacking [26–28]. As compared to the previous articles, this review provides comprehensive and contemporary analysis on available FDLs in GCPIs, with in depth study of various faults and discussion on performance parameters. Moreover, various failure modes and FDLs are investigated, discussed and categorized systematically.

The objectives of this review include

- Detection, classification and localization of various component failure modes and their potential causes in a tabular form. This helps in recognizing different fault signatures that can further help with device CM, diagnostics and prognostics.
- Diverse methods of data preparation and feature mining are consolidated and presented consistently and methodically.
- Consolidating available FDLs and systematically categorizing them with the description of their merits and demerits in a tabular manner. Further, reviewing major kinds of presented variants of FDLs to provide a comprehensive analysis.
- Challenges and future prospects of FDLs in GCPIs are elaborated to further improve and encourage upcoming research in this area.

Further sections of the paper are organized as follows: Section II present the failure modes, their potential reasons and fault signatures of switching devices in inverters. Section III discusses the available FDLs and their several variants with their benefits and limitations. Section IV lists the performance parameters associated with the FDLs. Section V provides the conclusion on this review.

2. Types of faults

2.1. Failures in Insulated gate bipolar transistors (IGBTs)

Through a study, it is observed that the PV inverters are the most delicate components and they attribute to nearly 37% of unscheduled maintenance activities [29]. These inverters dominantly comprise of power semiconductor based switching devices. Insulated Gate Bipolar Transistor (IGBT) based power switching devices are mostly utilized for inverters in GCPS [30]. The IGBTs in inverters are exposed to diverse and rigorous working conditions and therefore, they are susceptible to failure conditions [31]. In past few years, physics of failure (PoF) based cause-effect analysis of IGBT failures has been widely applied during the design phase [20]. The manufacturers of IGBT have invested a lot in enhancing device performance so that it can handle harsh operating environment [32]. PoF approach has the potential to estimate and evaluate the potential destruction caused by the loading conditions in the operational and surrounding environment. It has provided improved understanding to analyze the causes of failures in IGBTs and certainly helped in enhancing the overall lifetime of these devices [33]. However, the reliability of IGBTs still remains a concern, especially for safety-sensitive applications. Early failures may occur in IGBT during fabrication, packaging, transportation etc. Once these are taken care,

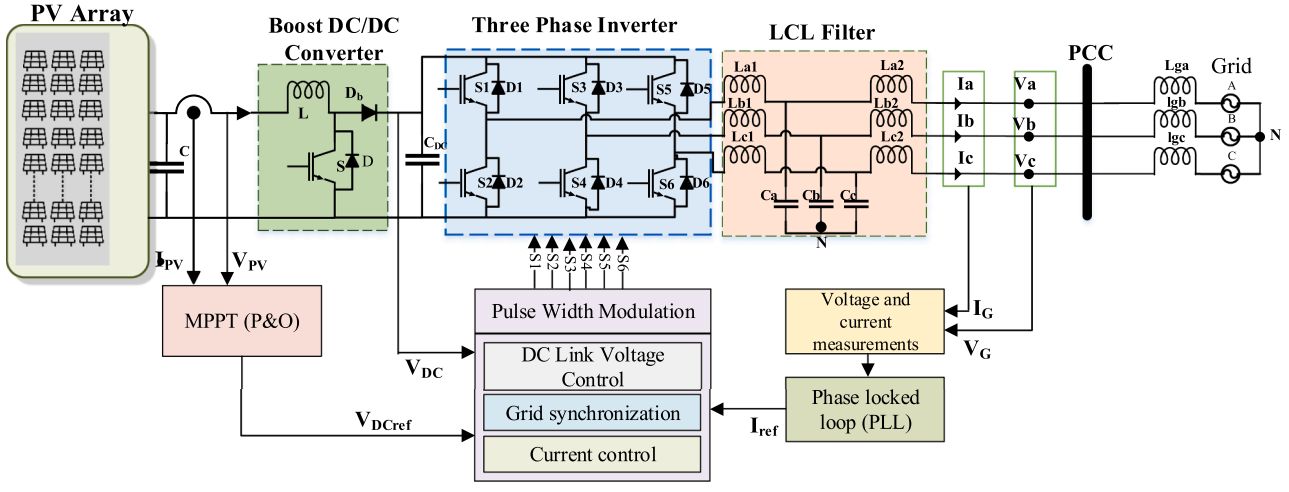


Fig. 1. Three-phase Grid-connected PV system (GCPS).

then there are other external factors, which might reinforce failure in the devices including thermal and electrical breakdown, mechanical factors, fatigue in the device material etc. [34].

An IGBT is fabricated using several material types and these materials form a layer kind of structure [35]. The direct bonded copper (DBC) ceramic substrate is soldered on the copper (Cu) baseplate. It has the Silicon (Si) die or chip bonded on it. The Si die is insulated from the baseplate through DBC substrate. The upper side of the Si die is joined to the aluminum (Al) bond wire. A typical structure of IGBT power module package is shown in Fig. 2. The primary weak-points are the joints and connecting points of different materials. With the application of stress at connection points, the different Coefficient of Thermal Expansions (CTEs) of materials causes the layers to expand and compress at dissimilar rates [36]. The potential failure mechanisms are mainly divided into two categories- wear out and catastrophic failures [37]. Wear-out failures refer to the cumulative damage of the device due to operation for a longer period of time. Whereas, catastrophic failures correspond to the collective damage of the device owing to the thermal, mechanical and electrical overstress events. These mechanisms lead to various kinds of failure modes in the IGBT devices such as OC failure mode, SC failure mode, gate leakage current, increased collector to emitter on state voltage, etc.

2.1.1. *Wear-out failures*

Bond-wire lift-off: Bond-wire failure occurs primarily due to the ageing and fatigue as a result of either continued flexure of wire or repeated stress between bond pad and wire [38]. Owing to the mismatch between CTE of Si and Al, bond wires can be raptured. The difference in their material strain causes stress strain energy loss. This hysteresis energy loss gives rise to temperature swings [22]. These substantially high temperature swings eventually lead to the crack in Al wire [39]. When thermal fatigue further enhances, crack propagates along the sides of wire to the center and bond wire lifts off. This phenomena causes rise in the on-state resistance of the switching device and may further result in OC of the device [40].

Bond-wire heel crack: This particular failure may be triggered by long endurance tests or the thermomechanical processes [41]. Due to sustained temperature cycles, the bond-wire is subjected to flexure fatigue causing change in the heel bending angle [39]. When ohmic self-heating is dominantly observed, it may experience heel crack.

Solder joints: Solder fatigue is one of the most common wear-out failure. Solder layers connect – 1) baseplate and the substrate, 2) substrate and Si chip. Solder film between the ceramic substrate and the baseplate is the most vulnerable to failures. Here, the CTE mismatch is found to be the worst and it has high temperature deviations [42]. The continuous thermomechanical stresses result in the formation of voids and cracks in the solder layers [43]. Consequently, the effective area accessible for heat loss reduces leading to rise in the module thermal resistance [44]. This further results in increase in the device junction temperature. The rise in temperature may cause acute localized heating; further possibly leading to catastrophic burnout [45].

Die-attach degradation and delamination: Die-attach joins the semiconductor die with the substrate. Owing to the sustained thermo-mechanical loading and CTE mismatch, the die delamination may occur leading to die parting from the die-attach [46,47]. It may result in enhanced thermal resistance, causing reduction in the heat-dissipating capability of the die-attach, eventually leading to die-attach degradation [48]. This causes higher junction temperature, which further may result in secondary breakdown [49]. The research is going on to find the solution for better material characteristics such that it is able to withstand high thermal, mechanical and electrical loading.

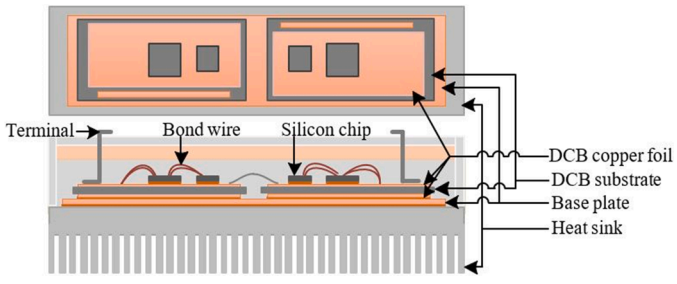


Fig. 2. Structure of IGBT module.

Aluminum reconstruction: The metallization for semiconductor die or chip is usually Aluminum [50]. Because of the difference between the CTEs of Si die and Al metallization, compressive and tensile stresses are applied on the thin metallization layer [21]. Temperature cycling gives rise to periodic thermomechanical loading and eventually, these stresses lead to metallization degradation [51]. With prolonged degradation, formation of hillocks take place and this whole phenomena is termed as Al reconstruction [52]. If the substrate material is direct bonded aluminum (DBA), then metallization degradation may be aggravated before the stipulated time. It may result in surge in the metallization layer resistance.

Substrate crack: The substrate is responsible for internally insulating the Si die from the Cu baseplate. Substrate fracture is one of the most detrimental failure mechanisms in IGBTs [53,54]. Due to the power cycling and continuous thermo-electrical stress, the ceramic in the substrate may crack [55]. These cracks formed are principally stealthy since they eventually lead to weakened insulation strength of ceramic. Further, this can dramatically induce leakage path within the module affecting its partial discharge properties.

Corrosion: The metallic components of the module may be affected by galvanic corrosion processes. It is difficult to identify the exact cause of the corrosion since several mechanisms correspond to induce failure [56]. The moisture may ingress within the module due to either some damages or discontinuities within the module [57]. In general, IGBT encounters many kinds of contaminant origins like periodic power cycling, different metals and alloys, mechanical and thermal loading etc. Corrosion of Al bond wire and bond pad may occur due to moisture penetration within the package [39]. When Al reacts with moisture, it forms hardly soluble Aluminum Hydroxide film, passivating its surface. This process raises the on-state resistance of the power semiconductor.

Electrochemical migration: Generally, die attaches have silver in the form of either alloy solder with tin or sintered paste [58]. If the environment contains corrosive contaminants or humidity, silver and other metals present low solubility. They migrate from anode to cathode in the presence of electric field, establishing electrochemical migration [21, 59]. The die passivation degradation caused by electrochemical migration results in steady loss in voltage blocking ability and further, it may lead to voltage breakdown. In bond wires, electro-migration may occur due to high current densities, causing higher resistance [60]. This may eventually lead to creating voids and hot-spots.

Ionic contamination: Impact ionization may cause hot electrons damaging the gate-oxide when the acquired energy becomes higher than the lattice potential barrier [55]. This causes deviation in the intended device characteristics affecting the collector-emitter saturation current, gate leakage current, threshold voltage, transconductance [22,61]. This shift in the device characteristics eventually results in severely damaging the operation of the device.

Time-dependent dielectric breakdown (TDDB): Dielectric breakdown can be observed over a period of time through TDDB process [21]. High electric fields and high temperature gradients may degrade the gate-oxide layer due to TDDB. With the application of high electric fields over time, the semiconductor Si-Si bonds in the dielectric are weakened and broken down with increased stress, creating path for electrons to flow through insulating gate [62]. This mechanism may eventually lead to gate current leakage.

2.1.2. Catastrophic failures

Latch up: IGBTs consist of parasitic elements in the power package like thyristors, Bipolar Junction Transistors (BJTs) etc. These thyristors require the current to be higher than a specific latching current value to turn on and once they turn on, they don't need the gate current for continuous conduction [63]. Latch-up can be manifested in the form of either static or dynamic process or is basically defined by the process in which the collector current is no longer controlled by gate causing inevitable damage to IGBT [64]. The activation of parasitic transistor may trigger latch-up failure in the device leading to an abrupt collector-emitter voltage collapse. If the latch-up is not identified in time, it may result in thermal runaway, eventually leading to gradual burnout of the device.

Bond-wire melting: Bond-wire melting may occur owing to electrical and thermal overstress events. Bond wires are surrounded by Si gel or epoxy molding compound depending upon press pack or module package [65]. Since they both are bad heat conductors, dissipation of heat produced becomes difficult. Eventually, the temperature rise is observed and melting of bond wires takes place if proper cooling measures are not taken [66]. This may create an OC fault in the device.

Avalanche breakdown: An uncommon short-circuit failure can be realized during turn-off transition in IGBTs. It may manifest in the form of avalanche breakdown [67]. It appears when collector-emitter voltage surpasses the breakdown voltage, particularly under repeated voltage spikes [68]. At this point, impact ionization occurs activating positive feedback mechanism, which enhances the collector current [69]. The collector current keeps increasing until the failure of device. Therefore, it is important to limit the collector-emitter voltage during transition process.

Electrostatic discharge (ESD): Latent damage due to ESD may pose a serious threat to the functionality of IGBT devices [70]. It has the ability to gradually puncture the gate oxide making it a concealed failure initially such that the device work satisfactorily for a period of time and fails abruptly [71]. ESD is responsible for gate shorting due to application of very high voltage at gate in the absence of any protection. To ensure proper reliability, it is important to identify the latent degradation caused by ESD.

Secondary breakdown: Due to high current stresses, the space charge density at the collector-base interconnection may increase leading to decline in breakdown voltage [72]. This further causes increase in the current density. This stays till the increased current density area falls to the minimum acceptable stable current. This process results in temperature increase such that it may cause local thermal breakdown [73]. This whole process is termed as secondary breakdown. It is one of the major catastrophic failures reported in the IGBT switching devices. The various faults discussed above, their potential causes, potential failure modes, failure location etc. are listed in Fig. 3.

2.1.3. Impact of failure on power module operation

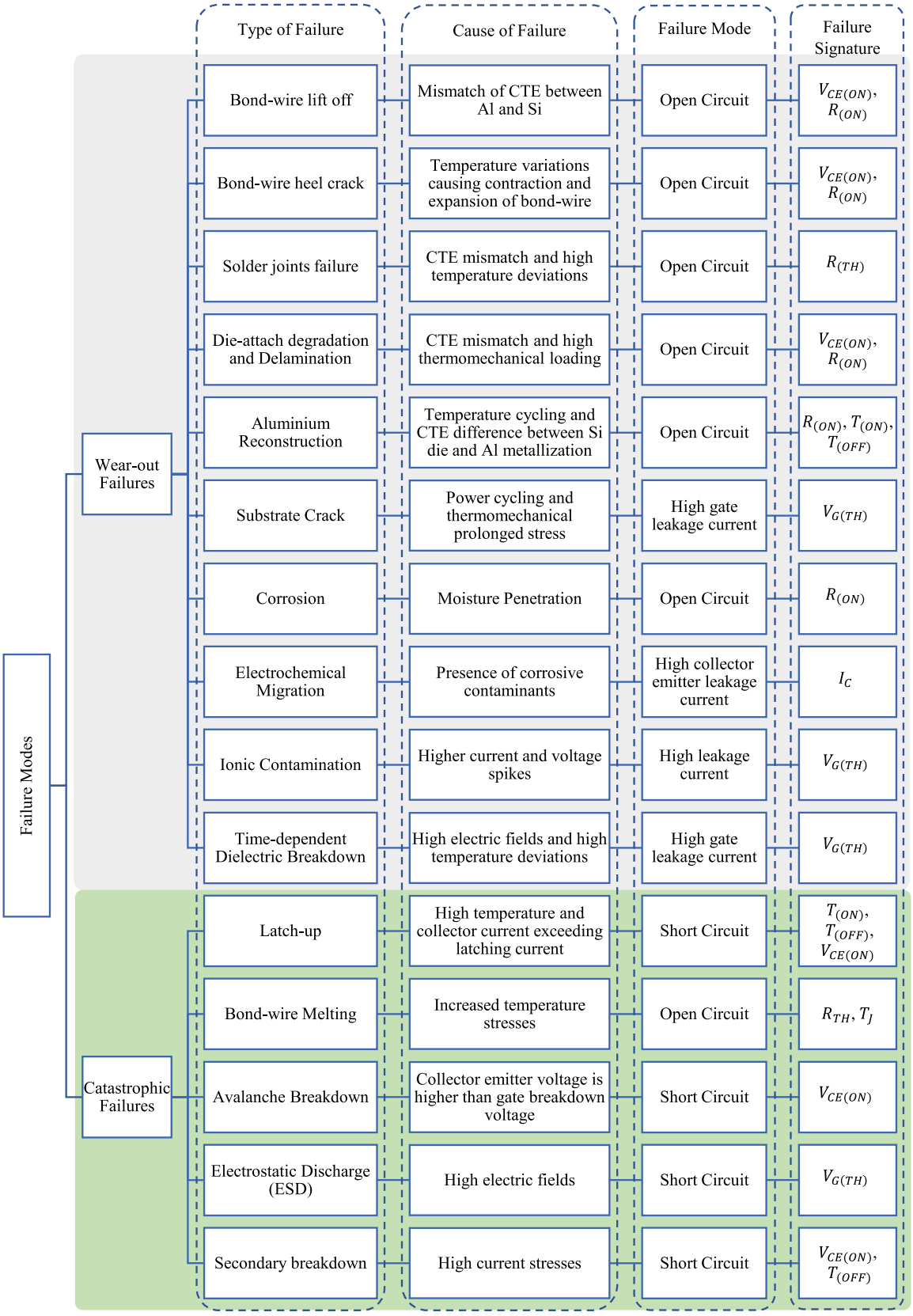
The device parameters that provide the indication of fault event are referred to as fault signatures [74]. Direct monitoring of the device parameters can be performed using dedicated embedded sensors. They may also help to analyze the level of degradation caused by a particular fault. For instance, strain gauges may be utilized for mechanical stress measurement and electric resistance measurement can be performed to detect failure like bond-wire lift off. Other device parameters, which can be employed as fault signatures include threshold gate voltage ($V_{G(TH)}$), on-state collector-emitter voltage ($V_{CE(ON)}$),on-state resistance ($R_{(ON)}$), collector current (I_C), internal thermal resistance ($R_{(TH)}$), junction temperature (T_J), device turn-on time ($T_{(ON)}$) and turn-off time ($T_{(OFF)}$) etc. [43]. It is observed that the decrease of 8-25% in $V_{CE(ON)}$ indicates die-attach degradation [20]. Similarly, an increase of 3% in $V_{CE(ON)}$ indicates bond-wire fault. These parameters cause changes in the device characteristics during turn-on or turn-off. These changes can also be captured for device CM.

To illustrate the impact of faults on the trends and performance on power modules, simulations were conducted for various stress levels caused due to increased heat exchange. To measure the characteristics of the power switches under the influence of various faults and operating conditions, a monitoring and measurement unit (MMU) is designed as shown in Fig. 4. The design process modifies the diver circuit of the power switch by adding selector switches, and data processing tools to efficiently measure the characteristics. Further, to protect the MMU from failure due to high voltage and current thresholds, few protection elements are also used in the design process. The protection circuit consists of a diode, Zener diode, and a current limiting resistor connected across the inverting and noninverting inputs. The antiparallel arrangement of the Zener diode and the diode across the power switch clamps the off-state voltage, whereas the embedded resistor limits the current through the off-state of the Zener diode. In addition to the protection circuit, the MMU is operated with two current sources, a low current source of 100 mA and a high current source of 50 A. The low current source is operated while sensing the temperature sensitive electrical parameters, whereas the high current source is operated for providing high current pulses to perform the monitoring process. To facilitate the uninterrupted monitoring process during the operation of the converter, a double pole change over (DPCO) switch is used in the MMU circuit. The details related to the operation switching sequence and operating process of MMU are provided in [75].

The details of IGBT SGP15N60 power modules used for performing these tests are shown in Table 1. The tests were performed in PLECS/MATLAB simulation environment. The online Temperature Sensitive Electrical Parameters (TSEPs) were investigated by conducting electro-thermal simulations with an IGBT pulse tester circuit [75]. TSEPs refer to the fault signatures discussed above; which are monitored to analyze the module characteristics with variation of temperature [76]. Here, the supplied voltage is set to 1200V DC, and an inductive load of 400 μH was simulated to achieve DC current levels for an IGBT pulse test. This inductor size is commonly used for pulse testing of high voltage IGBTs. The top IGBT's gate emitter is shorted so that it is always off, and used for an antiparallel diode operation which can create an inverse recovery effect [77]. The IGBT under test was supplied from an ideal $-10V$ to $+15V$ switching voltage source at $1kHz$, which is typical for high-power applications. Besides, an external gate resistor of 3.9Ω for turn on and 6.2Ω for turn off between the IGBT gate terminal and the ideal pulse voltage generator. Fig. 5 shows the temperature-dependencies of $V_{GE(th)}$, $I_{C(sat)}$, dI_C/dt and $t_{d(on)}$ during the IGBT turn on phase. To emulate the impact of thermal stress, temperatures from $25°C$ to $150°C$ are configured with the power modules. From the results it is identified that, apart from the collector current saturation, all the other TSEPs have approximately linear behavior with the temperature change. But the collector current exhibited an approximately exponential variation for the increase in temperature during the turn on phase.

Further, the gate-emitter threshold voltage, and turn on delay characteristics showed falling values with change in the temperature. However, the collector saturation current, and the collector current slope indicated that the values are rising with change in the temperature. Further, the impact of thermal stress on the power module between the turn on and turn off phase are shown in Fig. 6.

During this transition phase between the turn on and turn off process, the IGBT allows the measurement of only two TSEPs, the collector emitter saturation voltage during the device turn on state, and the collector saturation current during the device turn off state. The results in Fig. 6 (a) indicate that the collector emitter saturation voltage has a linear relation with temperature with a tail off at higher temperatures. Further, the collector saturation current which is measured during the IGBT blocking state shows an exponential rise with the increasing temperature as shown in Fig. 6 (b). This is due to the acute generation and movement of charge carriers during the temperature increase process. Lastly, the impact of thermal stress on the power module during its



$V_{CE(ON)}$- on-state collector-emitter voltage, $R_{(ON)}$- on-state resistance, $V_{G(TH)}$- threshold gate voltage, I_C- collector current, $R_{(TH)}$- internal thermal resistance, T_J- junction temperature, $T_{(ON)}$-device turn-on time and $T_{(OFF)}$- turn-off time

Fig. 3. Failure modes and their potential causes for IGBT.

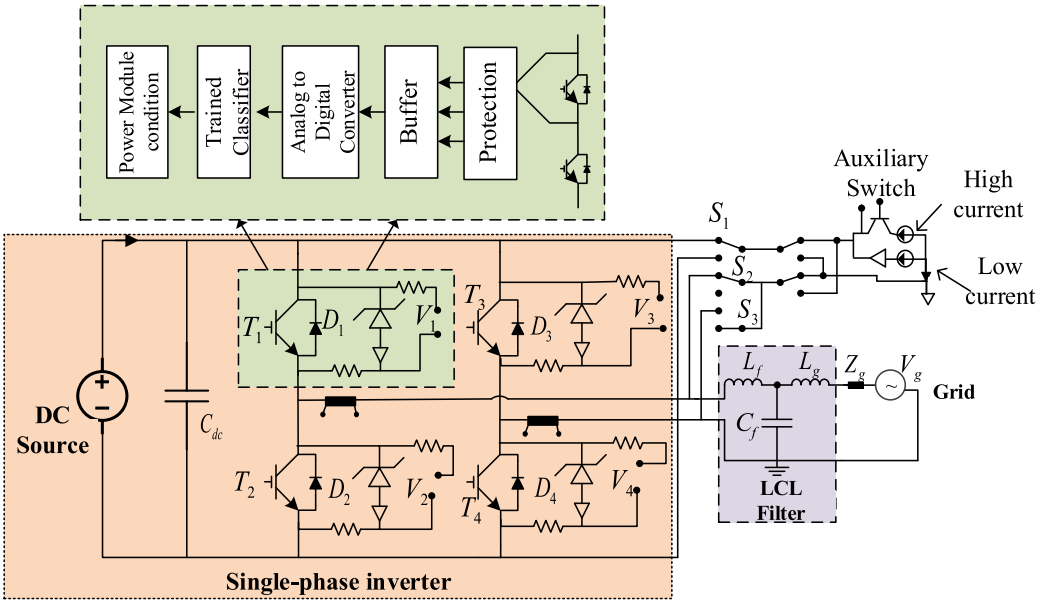


Fig. 4. The designed schematic for MMU to measure power module characteristics.

Table 1
Single phase grid connected system simulation parameters for generating the normal and faulty operation data.

Parameter		Value
DC link voltage		400 V
Infineon (IGBT SGP15N60) [78]	Maximum Power Dissipation	139 W
	Maximum Collector-Emitter Voltage	600 V
	Collector-Emitter saturation Voltage	2.3 V
	Maximum Collector Current	31 A
	Thermal resistance, junction to case	$0.9^0 C/W$
	Thermal resistance, junction to ambient	$62 - 40^0 C/W$
Microsemi (Diode APT15D60BG) [79]	Maximum D.C. Reverse Voltage, Peak Repetitive Reverse Voltage, and Working Peak Reverse Voltage	600 V
	Maximum Average Forward Current	15 A
	RMS Forward Current	32 A
	Non-Repetitive Forward Surge Current	110 A
	Junction-to-Case Thermal Resistance	$1.35\ ^\circ C/W$
	Junction-to-Ambient Thermal Resistance	$40\ ^\circ C/W$

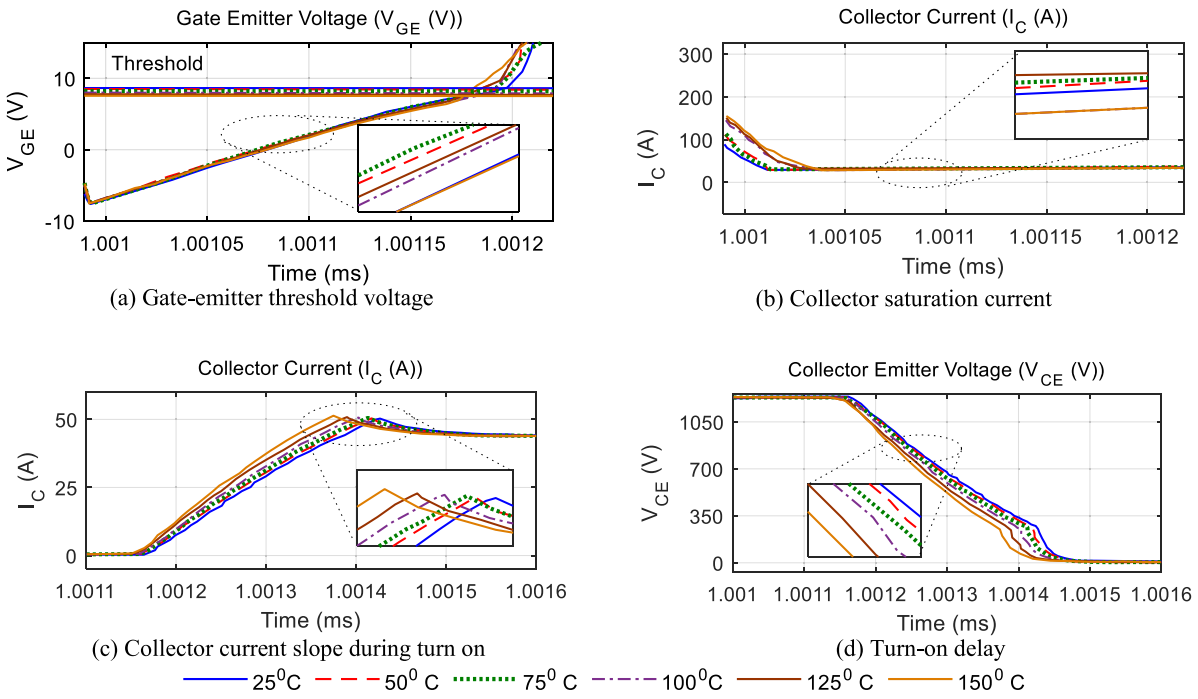
turn off stage are shown in Fig. 7.

During the turn off stage, six different TSEPS can be identified i.e., the collector-emitter voltage slope, the collector current slope, Collector current tail, turn off delay, and the characteristics of gate-emitter miller plateau voltage. The results indicated that the collector emitter voltage slope has a negative linear relation with the temperature, whereas the collector current slope indicated that the values are rising with change in the temperature. In Fig. 7(c), the collector current tail indicates the slow fall of the collector current during the end of the turn off process. This TSEP increases with temperature and its magnitude is mostly dependent on the maximum voltage across the power module. Further, the turnoff delay indicates the time taken by the trigger condition for the falling edge of the gate emitter voltage and its action in the real time. This is mostly affected by the collector current tail, and has high positive temperature coefficient as shown in Fig. 7 (d). In Fig. 7 (e), the miller plateau indicates both the voltage level and the duration for the gate emitter voltage during the turn off phase. This characteristic is registered when the voltage sample is triggered after the turn off process of the power module. It indicates the change in gate emitter voltage gradient which is identified to have an irregular variation for the change in temperature. This is due to the dramatic changes in the gate emitter voltage slope after the turn off phase.

2.1.4. *Impact of failure on inverter output*

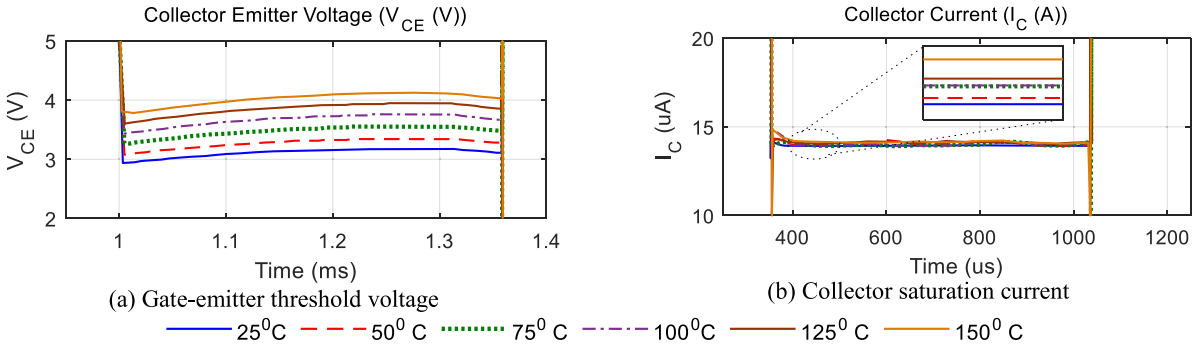
To assess the impact of wear out failures on the operation of the power module in an inverter, a single-phase grid connected inverter operating with a DC link voltage of 400 V is simulated in the MATLAB/PLECS environment. The details of the power module components used in the development of inverter are given in Table 1. The simulated faults include the impact of bond wire degradation of the IGBT and diode in the individual half bridge module of the inverter. The impact of these faults is identified at the inverter terminal voltage and current in order to identify the impact of wear out on the system operation.

Fig. 8 (a) shows the impact of bond wire lift off in the IGBT of a power module operating with the single-phase grid connected system. The inverter terminal voltage experiences a gradual change during the bond-wire lift-off, whereas the current flow varies irregularly for each cycle. In Fig. 8 (b) the impact of bond-wire lift-off in the power diode of the half bridge module operating with the single-phase grid connected system is shown. The inverter terminal voltage increases gradually and has a peak voltage of 3000 V which will damage the power module. Further, the current flow varies irregularly for each cycle and has increased by 10 times due to the high inrush. In Fig. 8 (c), the impact of simultaneous bond wire lift-off failure in parallel arranged IGBTs of a single-phase inverter is identified at the terminal voltage and current of the inverter. Here, it is identified that the impact is similar to the fault impact caused due to a single IGBT bond wire lift-off fault, but there is a large transient in the terminal voltage for each cycle, whereas the peaks of the terminal current are clipped. Similarly, the impact of simultaneous bond wire lift-off in diagonally arranged IGBTs of a single-phase inverter is shown in Fig. 8 (d). The impact of this fault is identified as a half wave operation and the corresponding voltage and current indicate the same. Further, the impact of simultaneous bond wire lift-off in parallel and diagonally arranged diodes of a single-phase inverter is shown in Fig. 8 (e) and (f) respectively. Through these faults the terminal voltage and current characteristics experience a large magnitude with an irregular off set which results in the failure of power module and shut down of the inverter.



(a) Gate-emitter threshold voltage (b) Collector saturation current (c) Collector current slope during turn on (d) Turn-on delay

Fig. 5. Temperature sensitive electrical parameter variation during IGBT turn on under different thermal stresses.



(a) Gate-emitter threshold voltage (b) Collector saturation current

Fig. 6. Temperature sensitive electrical parameter variation between IGBT turn on and turn off under different thermal stresses.

2.2. *Failure in capacitors*

Capacitors are widely employed in GCPS as DC link capacitors, capacitors in DC/DC converter for two stage applications, and capacitors in filters. These are the most susceptible to failure components in GCPS after power switching devices [80]. Therefore, investigations are being carried out to improve and enhance the capacitor technology with optimal manufacturing and design solutions including progressive dielectric materials [81]. The equivalent lumped circuit of electrolytic capacitor comprises of a capacitor in series with inductor and resistor [82]. The increase in equivalent series resistor (ESR) component is mostly considered as a fault indicator [83]. Other than that, decrease in capacitor value is a strong indicator of fault event. In addition, current ripple (I_C), voltage ripple (V_C) and temperature (T) can be considered as critical stressors [84]. These both fault indicators may also be adopted as parameter for predictive maintenance and CM. In general, capacitors are available in three types – Al electrolytic capacitors, multi-layer ceramic capacitors (MLC), and metallized polypropylene film (MPPF) capacitors. For instance, electrolytic capacitors are widely adopted due to low cost and high energy density [85]. However, they consist of drawbacks like short life, low ripple current, vulnerability to temperature deviations, etc. [86]. MLC capacitors have benefits like broader frequency range, small size and greater operating temperatures [87]. However, they possess shortcomings including mechanical sensitivity, and increased cost [88]. MPPF capacitors comprise of advantages including low cost, ability to withstand ripple current, better filter bandwidth, unique self-healing property and longer life [89]. Though they still have the disadvantage of large volume; the design process requires finding the capacitor, which possess characteristics consistent with the specific application. These capacitors may have different values depending upon operating conditions, temperature, frequency, current and voltage stress etc. These factors must be taken into account for failure analysis of capacitors. Generally, the failure modes of the capacitor are categorized as early failure, and wear out failures. Each of these have their own merits and demerits. The capacitor failures along with various capacitor health indicators are detailed in Fig. 9.

Fig. 10 reflects these failures in the form of a bathtub curve where the failure rate function is indicating the infancy at the beginning of the components, and wear out at the end of the component life. The Early failures in capacitors may be observed owing to the manufacturing

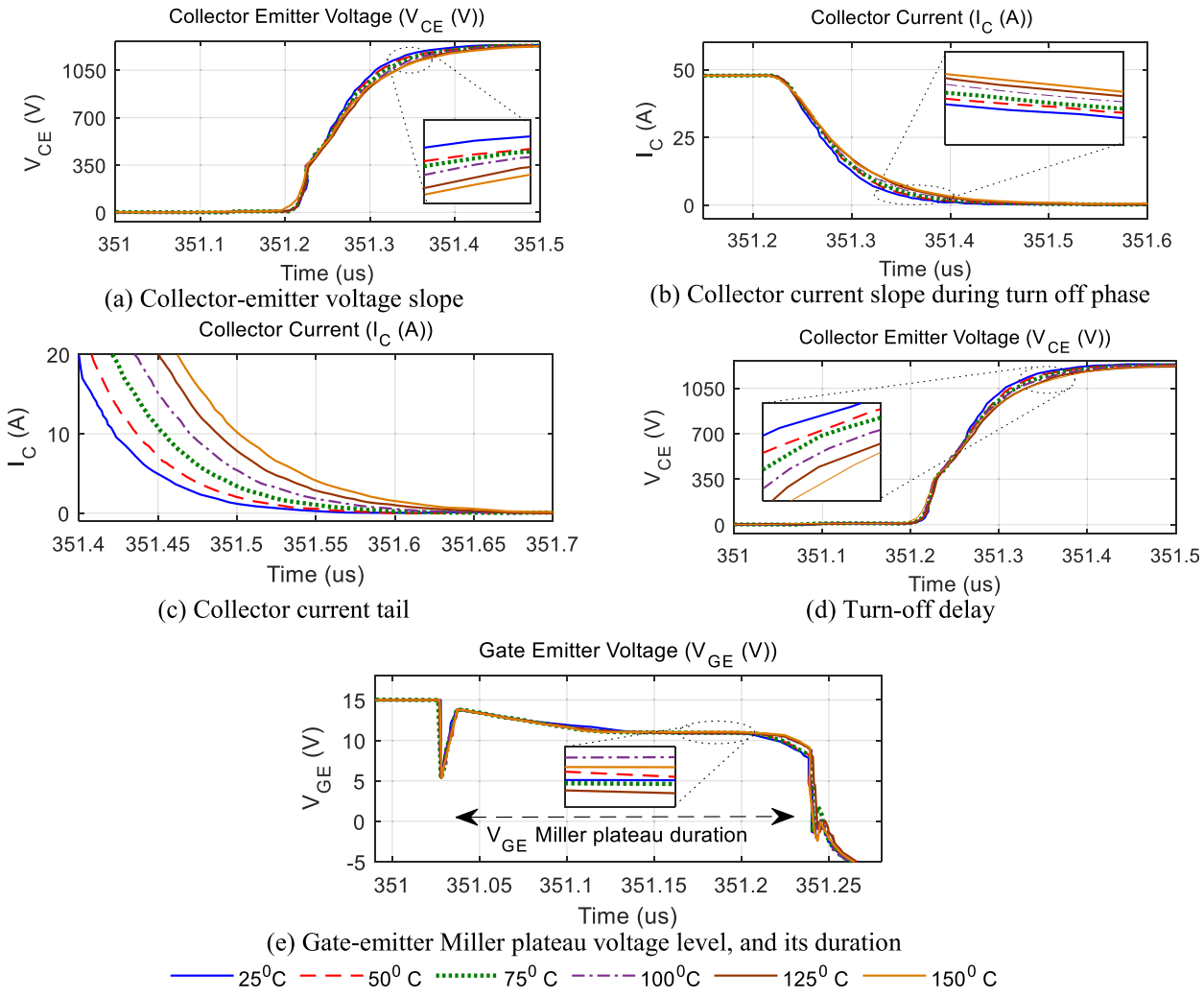


Fig. 7. Temperature sensitive electrical parameter variation during IGBT turn off phase under different thermal stresses.

defects. In addition, most of the failures are caused by wear-out owing to ageing and catastrophic failures occur owing to exceeding stress events [90]. The major wear out failure cause is electrolyte evaporation, which is enhanced due to temperature increase and ripple currents [91]. This results in increase in ESR and further, decrease in capacitor value (C).

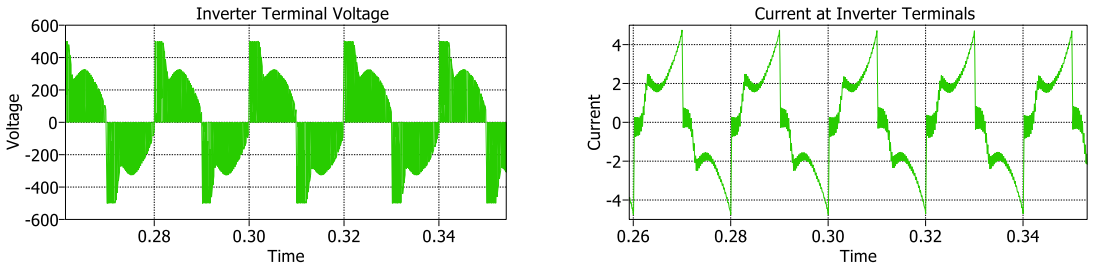
Some standards have identified increase in ESR, which leads to double its value as a potential capacitor failure indicator. In addition, decrease in C value by 20% also indicates capacitor failure [83]. In case of MPPF capacitor, ESR may not be taken as a relevant fault identifier since they inherently consist of low ESR. Therefore, for MPPF capacitors, C is the main fault indicator.

2.2.1. Impact of failure on capacitor

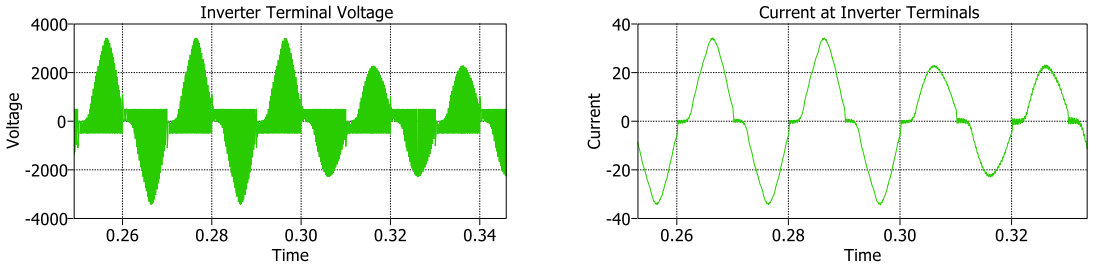
To identify the impact of failure mechanisms on the capacitor operation and its degradation, the equivalent series resistance (ESR) of an electrolytic capacitor is identified against the temperature and frequency. For an increasing frequency in Fig. 11(a), it is identified that the ESR decreases due to dipole relaxation time in the dielectric oxide. Similarly, the ESR decreases for the increasing temperature due to the decreasing electrolyte viscosity which allows for greater ion mobility in the capacitor.

3. Solar PV profile and its effect on inverter reliability

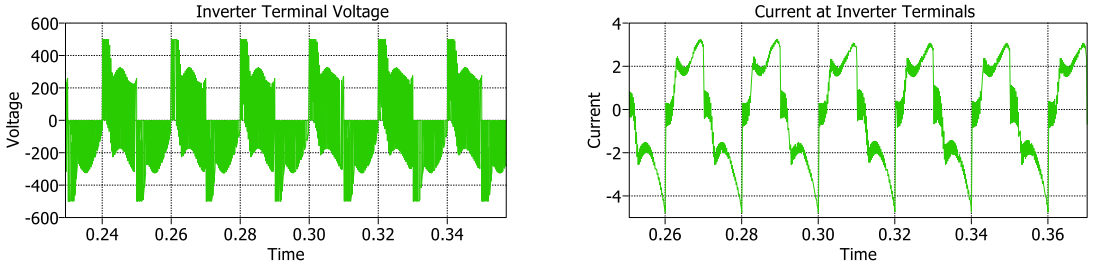
DG systems utilize numerous power generation sources including PV, wind turbines, batteries etc. They help in the required power conversion employing power electronics converters. However, for grid-integration, they need to be connected to the inverter and power sources like wind turbine may require an additional AC to DC conversion stage. Unlike wind generators, PV arrays provide DC output and thus, can be directly joined to the input of an inverter. This helps in reducing the total cost of the system. The operating conditions of PV including the ambient temperature and irradiance are referred to as the major constituents of mission profile. It is concluded from the research that the solar PV profile or mission profile strongly affects the life of power electronic converters including inverters [92]. The overall system reliability is also affected by the solar PV profile. Some studies suggest that, mission profile is an essential factor to be considered at the converter design stage since the irradiance and temperature depend on the installation location. The mission profile vary depending on the site and therefore, converter reliability is also impacted. Hence, it is important to address this perspective at the design stage. This concept is termed as “Design for Reliability (DfR) approach” and the general process is described in Fig. 12. After the last stage, i.e. the reliability prediction stage, the predicted outcomes are included in the design stage and further, if required, the process continues until an optimal design is finalized. Adopting DfR has become a challenge as the converter’s lifetime relies highly on the climatic conditions of the location [93]. It can be understood from the fact that if the converter is designed for cold weather conditions, it is highly likely that it may not be suitable for hot weather conditions and the set reliability target cannot be achieved. Moreover, it is not desirable in the DfR approach since it will lead to high initial cost,



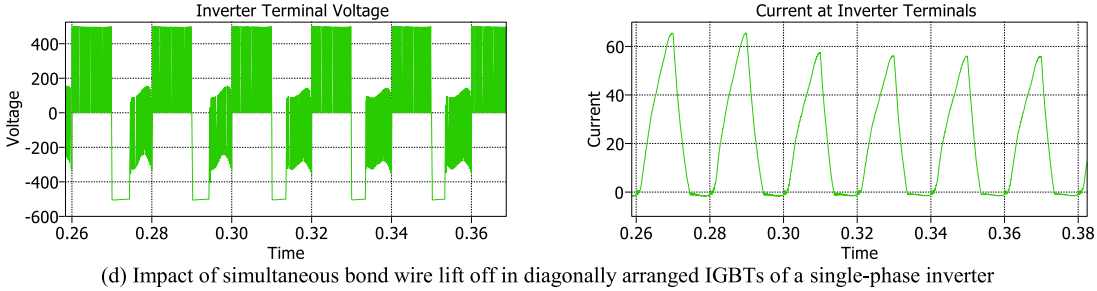
(a) Impact of bond wire lift off in IGBT of a half bridge power module



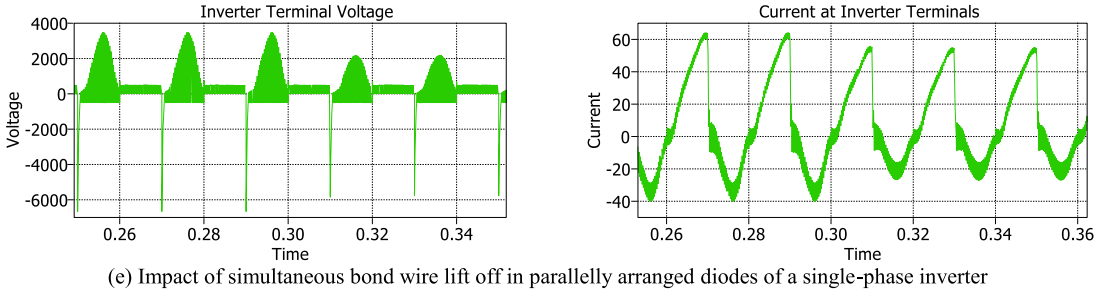
(b) Impact of bond wire lift off in power diode of a half bridge power module



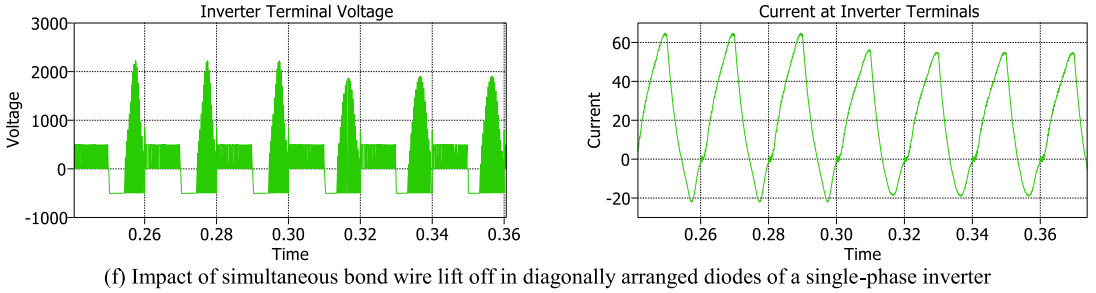
(c) Impact of simultaneous bond wire lift off in parallelly arranged IGBTs of a single-phase inverter



(d) Impact of simultaneous bond wire lift off in diagonally arranged IGBTs of a single-phase inverter

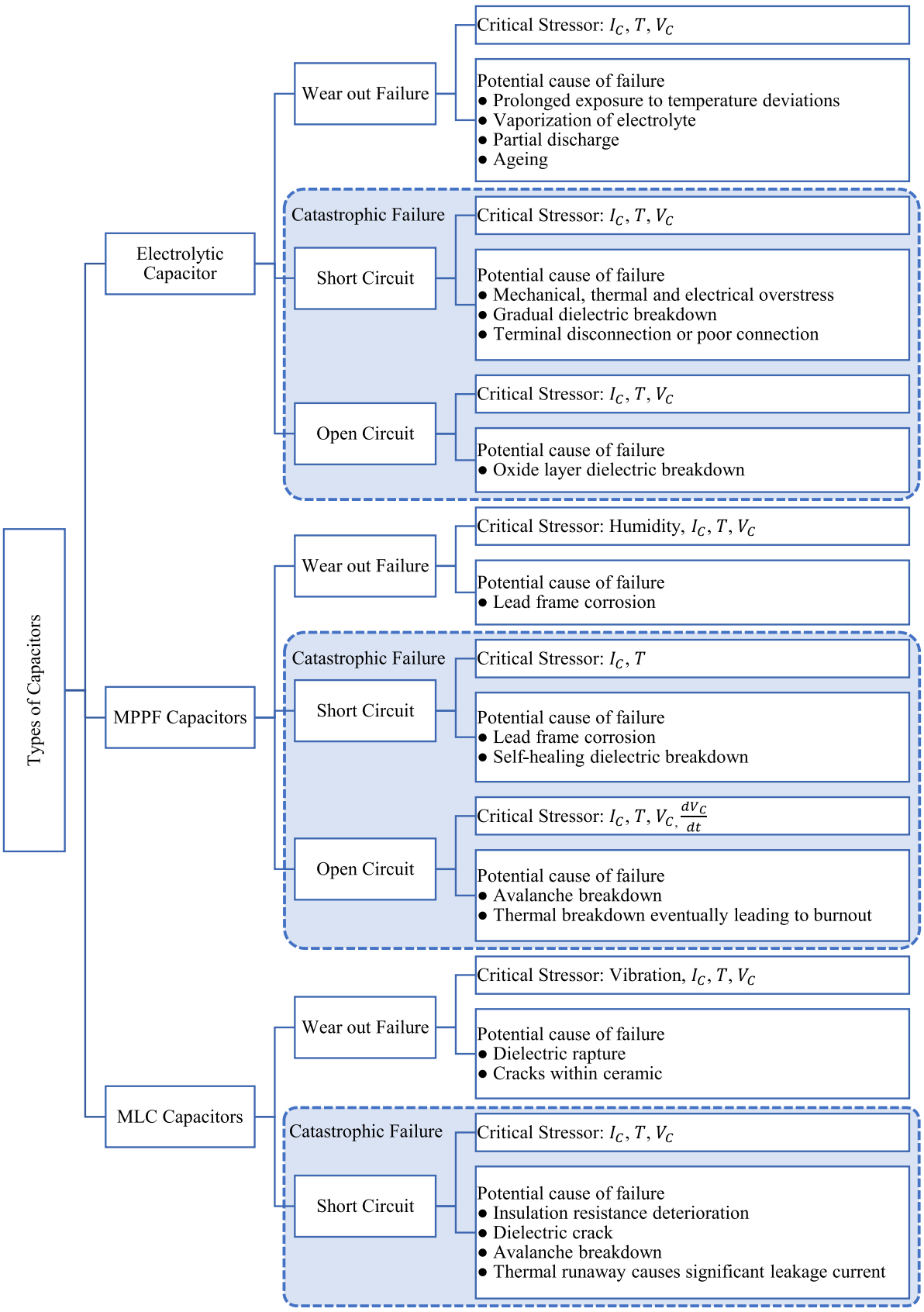


(e) Impact of simultaneous bond wire lift off in parallelly arranged diodes of a single-phase inverter



(f) Impact of simultaneous bond wire lift off in diagonally arranged diodes of a single-phase inverter

Fig. 8. Inverter terminal voltage and current during power module faults.



V_C- Capacitor voltage stress, I_C - capacitor ripple current, T -Ambient temperature

Fig. 9. Potential causes and critical stressors of capacitor failure.

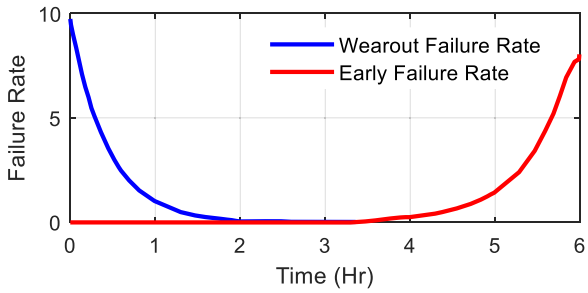


Fig. 10. Bathtub curve of the failure rate function for capacitor.

and maintenance cost. Component level reliability can also be analysed for components highly contributing to the increased failure rate [94]. The investigations reveal that semiconductor devices are the highest failure contributing devices, followed by the capacitor [95]. The thermal factor is also a major contributor to an increased failure rate leading to reduced converter life, which necessitates the significance of effective heat-management strategies. In addition, the inverter control techniques may also impact the converter lifetime and reliability. It is known that the inverter loading depends on the power generation by the PV arrays. Therefore, variation in the mission profile can cause thermal fluctuations in the GCPIs. Further, to improve the overall reliability and lifetime of GCPIs, proper control strategy should be adopted with consideration to the mission profile.

The impact of mission profile with reference to different converter topologies, on the overall reliability is investigated [96]. The general block diagram for the presented technique is shown in Fig. 13. It majorly

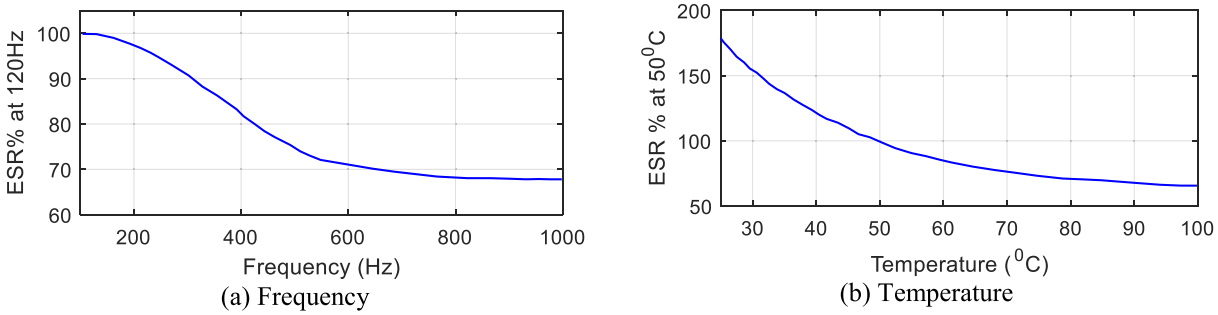


Fig. 11. ESR of a dielectric capacitor (a) frequency and temperature (b).

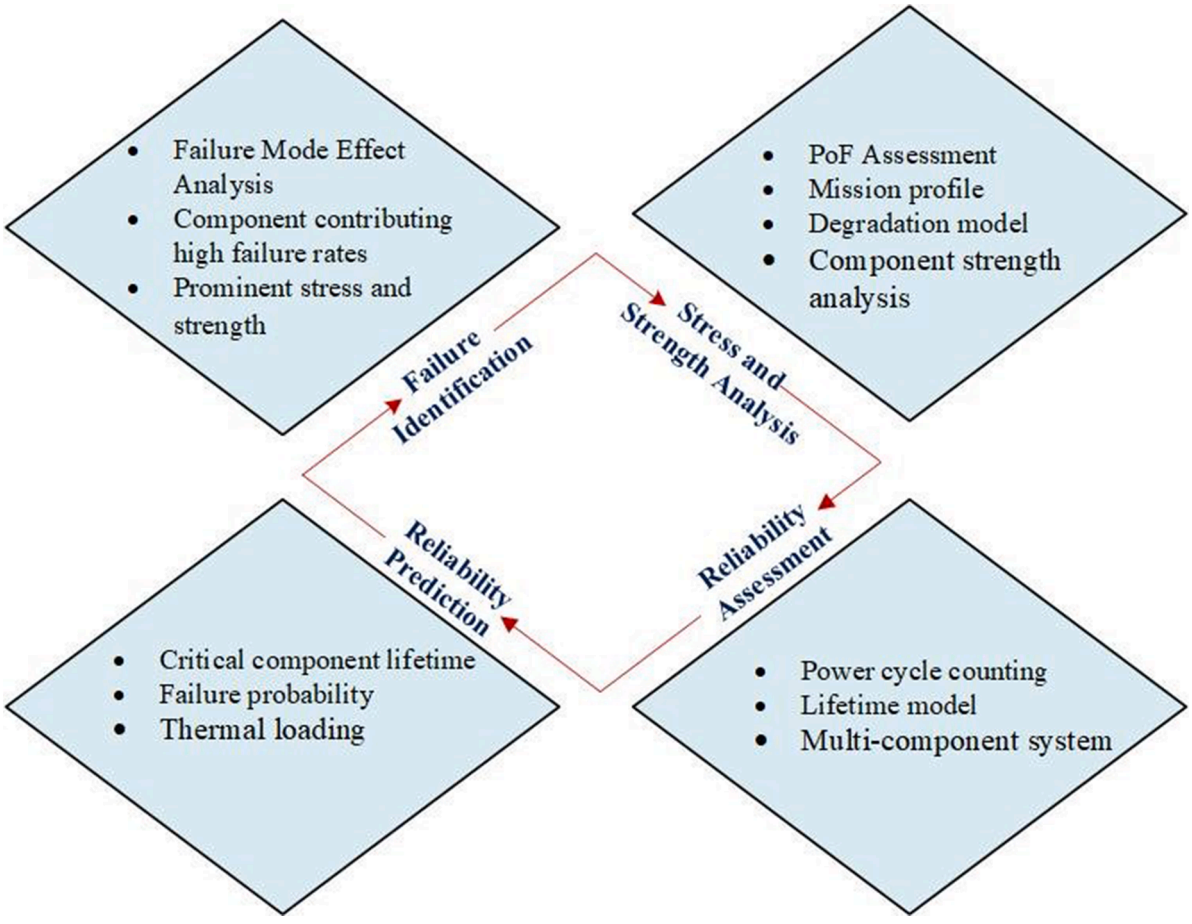


Fig. 12. A general block diagram of design for reliability (DfR) approach.

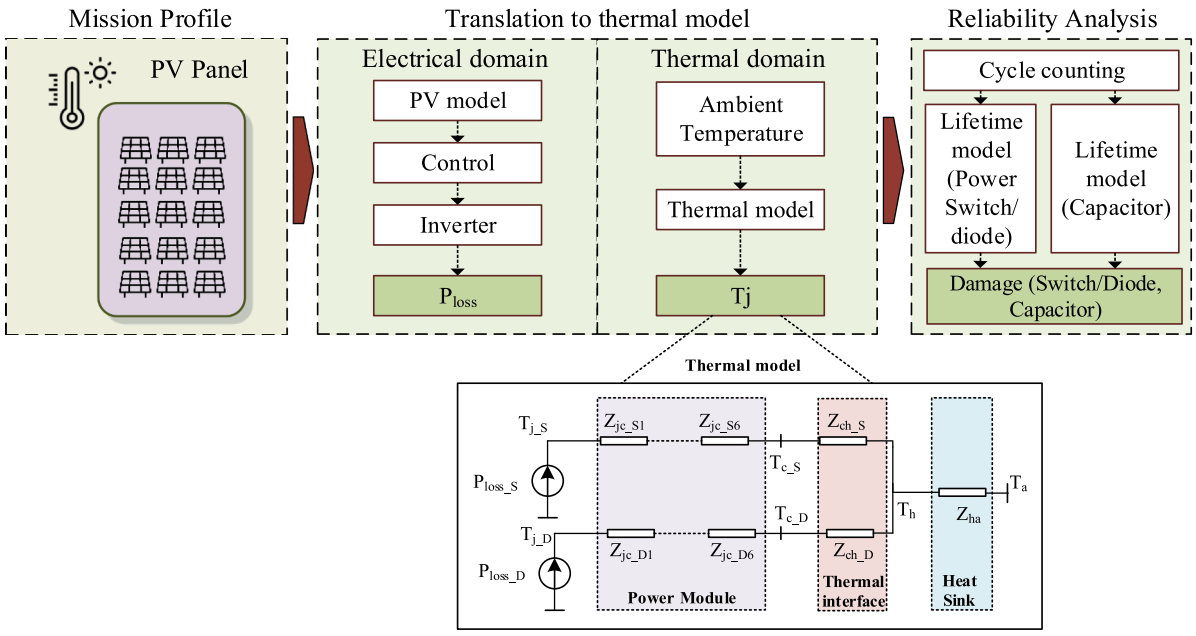


Fig. 13. General structure for reliability analysis using mission profile.

focuses on the two most vulnerable component failures, i.e. switching devices and capacitor failures. To quantify the damage to the devices, mission profile (solar PV irradiance and surrounding temperature) for one year at two different sites is captured. After that, thermal stresses on both the devices are obtained by electrothermal analysis, which can convert electrical stress to thermal stress through a suitable electro-thermal model. Further, the switching device junction temperature and capacitor temperature can be determined and can be compiled in look-up tables. Firstly, the accumulated damage and the lifetime of capacitor can be calculated based on the capacitor lifetime model. The obtained data can be utilized to identify the Weibull-based unreliability function. Thereafter, for switching devices like IGBT and diode, Monte-Carlo simulation is adopted to determine the failure density function and their lifetime. Consequently, the reliability function of both the switching devices can be quantified using the Weibull distribution. Overall converter reliability is found out considering the reliability functions related with capacitor, diode and IGBT in series. A similar approach is applied for DC/DC converter system based reliability assessment [97,98]. Furthermore, to enhance the life of converter up to 7.5 years, an additional 1 kW converter is assessed [97]. Consequently, the lifetime of converter is increased by applying the relevant information obtained from the mission profile based prediction. Whereas, in [98], system level reliability analysis is carried out for DC microgrids considering the semiconductor device and capacitor failures. The thermal stress caused by PV power is shared between the fuel cell converters and battery. It is concluded from the analysis that the PV converter has failure probability of almost double to ten times of other components in the system.

In practice, owing to the comparatively less cost of PV modules, PV array oversizing is a general method to lower the cost of solar energy. It helps in increasing total energy production under weak solar irradiance. However, loading of inverters in the system is increased affecting the overall inverter lifetime and reliability. Further, it may lead to increased cost owing to the increased inverter maintenance. An evaluation of the impact of PV array sizing over the PV inverter lifetime and reliability is presented [99]. Two installation sites are considered in Arizona and Denmark, taking the critical components like power switching devices and capacitors. For the case of Denmark, the normal solar irradiance experienced is low and therefore, a definite design margin with respect to reliability is essential. Three steps are executed to evaluate the inverter lifetime – mission profile conversion to thermal loading, interpreting the thermal cycling and lifetime modelling. Reliability analysis at component level is investigated utilizing the Monte-Carlo simulation and further, system level reliability is evaluated.

A residential PV-Battery Energy Storage System (BESS) is investigated for converter reliability considering mission profile along with the impact due to battery sizing and functionality [100]. For a PV-BESS, the overall reliability and availability of the system is affected by the battery parameters including power rating, capacity, charging and discharging processes. Along with taking the battery operation impact into account, a self-consumption strategy is utilized for optimum PV power distribution. As the battery charges, it results in reduction in the inverter loading, since loading is characterized by the difference between the PV power production and battery power, leading to improved reliability. However, during the battery discharge, the inverter reliability is affected in a negative manner. Based on the mission profile and battery operation, short term (1 day) and long term (1 year) reliability analysis is carried out. It is concluded that with battery integrated into the system, the accumulated damage is decreased by 11% over a year of operation causing improved system reliability.

It is estimated the cost incurred for inverter failure in GCPS is approximately 59% of the overall system cost [8]. Thus, the lifetime estimation of GCPI plays an important role in the analysis of operational cost as well as the DfR. To provide a more convincing approach for high accuracy in lifetime estimation of GCPI, PV panel degradation has been taken into account [101]. Two installation sites are considered, one is related with cold weather conditions and other is related with hot weather conditions. Along with the mission profile, PV degradation plays an important role in determining the lifetime of GCPI. Monte-Carlo simulation is performed for reliability analysis. The holistic approach taking mission profile, site weather conditions and PV panel degradation provides highly accurate lifetime prediction of GCPIs. The results show that in hot climate conditions, PV degrades at a fast rate and therefore, inverter life is greatly affected.

While many researchers have worked upon the converter lifetime prediction considering the mission profiles, the contribution of generated profile data resolution in accurate lifetime prediction remains unexplored. An investigation regarding different resolutions of mission profile data for modular multilevel converter (MMC) reliability evaluation is performed [102]. High data resolution may lead to increased

accuracy in converter lifetime estimation. However, more efforts have to be invested in proper data acquisition, analysis and storage. After considering one year mission profile data, power loss profile is obtained according to the observed power fluctuations. Then, obtained power losses are translated to thermal profile, where a proper thermal model is determined. After applying rainflow power cycle counting, monte-carlo simulation is executed for an appropriate converter lifetime estimation.

Mission profile can also be employed to estimate real-time life consumption, which can be useful in building a health management tool [103]. PoF analysis manifesting the electrothermal model is utilized to determine true life consumption of power modules. The model combined with the module temperature data uses online counting technique for accurate life assessment of power modules. The counting technique is based on modified real-time rainflow counting method. The obtained model coupled with the real mission profiles is adopted to deliver advance warning regarding fault events. Hence, it provides valuable information that can be helpful to meet reliability requirements at the design phase.

Another work based on reliability prediction of a push-pull converter considering the critical components, i.e. transistor, diode and capacitor, is presented [104]. It compares the MIL HDBK 217 procedure with the IEC62380 prediction procedure, which considers the impact of mission profile. This work aims to identify the elements most susceptible to failures observing temperature as a major influence factor. Moreover, corrective actions can be suggested based on the observed results. Different prototypes are built with different ratings of switches and further, testing is done. Mission profile data is produced through the measurement of both ambient temperature and solar irradiance. The analysis suggests that not only temperature, thermal cycles also largely contribute towards increased failure rate. The IEC62380 is able to provide better results and reliability estimations as compared to the MH 217 procedure.

4. Fault detection and localization (FDL) Techniques

The electrical and thermomechanical overloading may make the inverter switches susceptible to failures inducing unanticipated downtime in the system. Therefore, reliability becomes a great concern for optimum operation of grid connected PV systems [105]. To enhance the availability, flexibility and sustainability, the system is required to undergo various maintenance actions incorporating fault diagnosis, CM, prognosis/Remaining useful life (RUL) estimation etc. [106]. System behavior is analyzed for parameter identification and anomaly detection. Based on this system behavior, the information obtained can be utilized for real-time or online health monitoring (OHM) [107]. To ensure improved reliability, FDL techniques are employed in grid connected PV systems. FDL techniques accomplishes two important tasks-firstly, it detects whether fault has occurred or not, secondly, it identifies and classifies the type and location of fault. Another advantage of having FDL mechanism is that it aids in making the system fault tolerant. They can be implemented through either model based or model-free approaches.

4.1. Model based FDL techniques

Model based schemes have become appealing FDL since they don't need additional sensors or other measurement hardware units making the system cost efficient. They generally require residual generation and utilize the analytical and mathematical information related to the system. This analytical modelling is established on the deep understanding of the physical properties of the model. It is important to develop accurate model since inconsistent and inaccurate model may lead to false results. The residue refers to the difference between the actual value and estimated value. The mathematical relationship developed due to residue is extracted for anomaly detection [24].

The residue being very small represents no fault conditions and

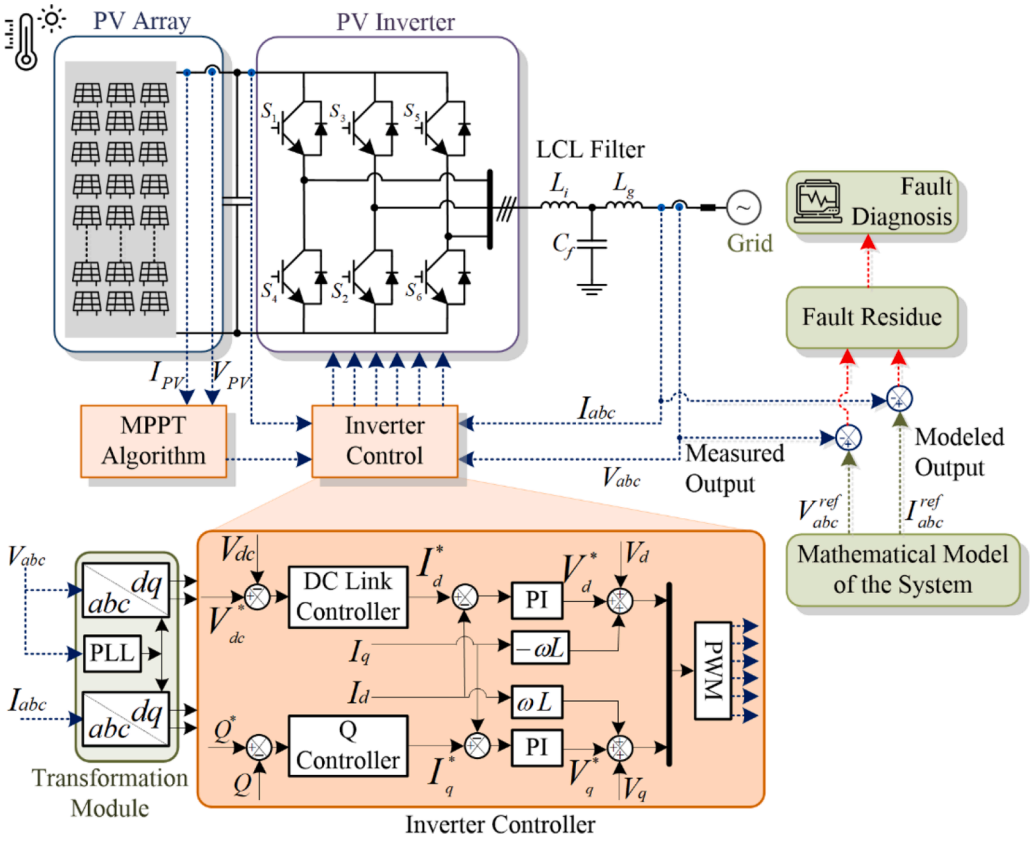


Fig. 14. A typical model based FDL approach.

greater residue indicates the presence of fault. A general model-based FDL process is presented in Fig. 14. Different approaches can be employed for residual generation including parity equations, parameter estimations, state observers etc. [14]. Depending upon the type of modelling procedure employed, the residue can be either scalar or vector quantity. A model based FDL approach is developed for nanogrid based application [14]. The converter is modelled utilizing a combination of linear state space model and a continuous-time switching signal representing the active mode of the system. The dynamics of controlled and uncontrolled switches are utilized for obtaining the switching signal. The converter is modelled for different switch fault conditions and state space representation is acquired for all the possible modes. In case of fault conditions, the product of time varying scalar component and time-invariant vector component, is added to the original state space dynamics. For error residue calculation, linear state estimation is utilized. The FDL consists of taking L2-inner product of the available fault signatures and state estimator.

A switching function model based OC fault diagnostic technique for three-phase voltage source inverters (VSI) is proposed [15]. It does not utilize sensors for measurement; rather a simple hardware unit is used for measurement of signals for fault diagnosis. Firstly, switching function based tables are created for collector-emitter voltages of lower IGBTs. Then, based on the information obtained, the detection circuit utilizes photocoupler for diagnosis, logic gate circuit, and time-delay circuit of rising edges.

A finite set MBPC (Model based predictive control) based fault detection technique for OC fault detection in flying capacitor inverter. It utilizes the switching functions to detect the fault and take corrective action [108]. To begin with, a mathematical model is developed for 3 phase flying capacitor inverter for all the switch fault possibilities. Since, it consists of 12 switches, the switching functions for all the possible scenarios are identified. A 13th current vector is identified for no fault scenario. An estimation is made for different instants and through utilizing a cost function, an optimal state is selected. With the update in the given instant, the measured current vector is attained. It is then compared with the estimated 13 current vectors and corresponding to the proximity to one of the vectors, fault is detected.

A model-based fault detection and isolation (FDI) technique is presented for grid connected inverter with output LC filter [109]. An input-affine differential equation is developed for representing the model of inverter. The model equations are computed for both healthy and OC fault conditions for switches and sensors. A fault signature table is developed based on the model equations. Further, a relationship between the fault events and fault signature is identified using residual generator. Based on the residue calculation and experimental results obtained, this technique is able to localize switch and sensor faults.

A parallel open-circuit fault diagnosis method (POFDM) for cascaded full-bridge neutral-point clamped inverters (CFNPCIs) is proposed [110]. It involves utilization of model predictive control (MPC) since it provides fast dynamic response and can handle multiple control objectives. The control objectives include capacitor voltage balancing and output current tracking. For that, a system predictive model is constructed, which corresponds to the calculation of switching variables for all the available switching states and computation of respective cost functions. Then, optimal switching state is selected based on the minimization of cost function to trigger IGBTs. The change in the capacitor voltages and output currents and corresponding switching states is analyzed to detect the OC fault in any switch.

Another model based OC fault detection and isolation technique for switching devices in NPC converter for PV application is developed [111]. A bank of sliding-mode observer incorporating proportional–integral (PI) control is proposed to predict the fault event. It consists of an additive model approach to better predict the OC fault occurrence. By taking all the fault profiles under consideration, it utilizes directional residual evaluation such that both single and multiple device faults can be diagnosed. Experimental observations validate the robustness of the proposed approach to noise, parameter uncertainty or disturbances in the system.

A robust fault diagnostic scheme for VSI in induction motor drive application is proposed [112]. The technique consists of taking non-linear dynamics of the system into consideration with observed based approach. A bank of PI observers is adopted along with the utilization of stator current and mechanical velocity measurements.

The dq frame residuals are constructed with the aim of isolating the defected switches. These residuals have a major advantage that they are insensitive to disturbances and load changes. The experiments are conducted using the proposed approach with varying frequency and load conditions and are found to perform satisfactorily with a less fault detection time. The literature review discussed above regarding model based approaches is summarized in Table 2.

4.2. Model-free FDL Techniques

Model-free fault detection techniques have become promising diagnostic methods mainly because of associated low-cost and independence from knowledge regarding the system behavior and dynamics. Fundamentally, it incorporates the utilization of huge potential of artificial intelligence (AI) in deriving the relation between the given input and output details [113]. Initially, they were used for applications like healthcare, education, finance, transportation etc. Recently, AI based approaches have attracted significant research in the area of power systems and renewable energy [107]. Over the years, AI based fault diagnostic techniques have proved to be more efficient and robust providing better performance and accuracy. The AI based fault diagnosis methods can be understood through a branch of AI popularly known as machine learning [114]. Machine learning is based on utilizing the ability of algorithms to emulate human learning with gradual progression making it more accurate [107,115]. These machine learning based approaches can be further categorized into supervised learning, semi-supervised learning, and unsupervised learning methods. Since AI based techniques work on large amounts of data, the first step towards FDL is data cleaning and preprocessing and second step consists of feature extraction. Further, in the next step, the acquired features are used for training using machine learning data-driven approaches.

Data preprocessing and feature extraction: The machine learning based FDL consists of acquiring the relevant data with respect to appropriate parameter identification [116]. To begin with, the parameter identification refers to identifying which system parameter is getting affected by the fault conditions. Then, the next step consists of monitoring and acquiring the data pertaining to it. The obtained data is usually in raw form. Therefore, proper data cleaning and preprocessing is essential before proceeding towards the feature mining process [117]. It consists of removal of outliers and noise in the data, estimation of density to explore the data distribution, clustering of data in their respective similarity groups, projection of high-dimensional data into low-dimensional data to aid in reducing the number of features, etc. [118]. Proper data preprocessing is important in order to derive improved and better performance for FDL.

After the data preprocessing, it is essential to identify and extract relevant features for next step in FDL. When a fault occurs in GCPS, it affects the system characteristics in a particular way that may be detected using feature mining. This process helps in finding out the appropriate pattern in the acquired fault data. Feature extraction in a particular application might provide higher dimensional feature-set, which may lead to more computational efforts and time. Therefore, different approaches have been proposed to compress the feature-set into more computationally efficient and significant feature-set collection. Various feature extraction methods have been proposed in literature including time-domain methods, frequency-domain methods and time-frequency domain methods.

Table 2
Summary of model-based approach as per literature review.

Ref.	Inverter Topology	Fault types	Fault Signature	Detection time	Advantages	Disadvantages
[14]	3-phase H-bridge	Switch OC	I_O	3.45ms	Ø Good generalization capability Ø Flexible modeling of converter Ø No extra hardware is required	Ø Can only tackle OC faults Ø Precise parameter estimation is difficult
[15]	VSI	Switch OC	V_{CE}	–	Ø No extra sensor is required Ø Simple, low cost and less complex Ø Detection time is less	Ø Cannot be generalized Ø Only handles switch and phase open faults
[108]	Flying capacitor MLI	Switch OC	I_O	49ms	Ø Online diagnosis is easier Ø Does not require additional calculations	Ø Computationally intensive Ø Determination of parameters is not unique
[109]	3-phase H-bridge	Switch OC	I_O,V_O	0.4ms	Ø Residual convergence is faster Ø Not affected by disturbance or islanding Ø Does not depend upon balanced grid conditions	Ø Generalization capability is poor Ø Difficult to detect transient and intermittent faults
[110]	Cascaded NPC	Single, multiple OC faults	I_O,V_T	1.4ms	Ø Fast dynamic response Ø Can handle multiple faults simultaneously Ø Less complex and does not require extra sensors	Ø Computationally intensive Ø Demands accurate modeling Ø Uncertainties may be difficult to incorporate
[111]	NPC	Single, multiple OC faults	I_O, V_O	<16ms	Ø Ability to diagnose multiple faults Ø Insensitive to noise and parameter variation	Ø Meeting stability requirement is not certain Ø Poor generalization capability
[112]	VSI	SC, OC, misfiring faults	I_O	20ms	Ø Fast response Ø Optimal error convergence Ø Independent of operating conditions Ø Insensitive to disturbances	Ø Precise residual estimation may be difficult Ø Uncertainties may be difficult to incorporate

I_O - Output current or grid current, V_O - Output voltage or grid voltage, V_T – Voltage at inverter terminals, V_{CE} - Voltage between the collector and emitter terminals

Table 3
Description of time-domain and frequency-domain features.

	Feature Name	Description	Formula of Feature
Time-domain features	Mean	Mean provides the average value of the given signal.	$\mu = \frac{1}{n}\sum_{i=1}^{n} S_i$
	RMS	RMS measures the root mean square value of the given signal. It increases as the fault gradually develops.	$RMS = \sqrt{\frac{1}{n}\sum_{i=1}^{n} S_i^2}$
	Variance	It quantifies the dispersion of a signal around its mean value.	$Var = \frac{1}{n}\sum_{i=1}^{n}(S_i-\mu)^2$
	Standard Deviation	Standard deviation measures the closeness of the given data point to the mean value.	$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(S_i-\mu)^2}$
	Skewness	Skewness measures the asymmetric behavior of the fault signal.	$S_K = \frac{\frac{1}{n}\sum_{i=0}^{n}(S_i-\mu)^3}{\left(\frac{1}{n}\sum_{i=0}^{n}(S_i-\mu)^2\right)^3}$
	Kurtosis	It describes the shape of the signal. Kurtosis quantifies the "tailedness" of the signal.	$K = \frac{\frac{1}{n}\sum_{i=0}^{n}(S_i-\mu)^4}{\left(\sqrt{\frac{1}{n}\sum_{i=0}^{n}(S_i-\mu)^2}\right)^4}$
	Entropy	Entropy determines the degree of "uncertainty" in the given signal.	$H = -\sum_{i=1}^{n} p(S_i)\log_{10} p(S_i)$
Frequency domain features	Energy	Energy of a signal determines the strength it possess.	$E = \int_{-\infty}^{\infty} \lvert S_i(t)\rvert^2 dt$
	Power	It determines the strength of the signal over a particular time.	$P = \lim_{n\to\infty}\frac{1}{2T}\int_{-T}^{T} \lvert S_i(t)\rvert^2\, dt$
	Mean Frequency	It represents the average frequency of the power spectrum.	$MF = \frac{\sum_{i=1}^{n} f_i P_i}{\sum_{i=1}^{n} P_i}$
	Power Spectral Density (PSD)	It determines the power distribution of a signal (in frequency domain).	$PSD = \lim_{T\to\infty}\frac{1}{T}\int_{-\infty}^{\infty}\left[\int_{-\infty}^{\infty} S_{i_T}(t-\tau)\, S_{i_T}(t)\, dt\right] e^{-i2\pi f\tau} d\tau$
	Signal to Noise Ratio (SNR)	It distinguishes the desired signal from the noise and disturbance (represented in decibels).	$SNR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right)$
	Spectral Skewness (SS)	It quantifies the symmetry around the spectral centroid (μ_f).	$SS = \frac{\sum_{i=b_1}^{b_2}(f_i-\mu_f)^3 s_i}{(\mu_s)^3\sum_{i=b_1}^{b_2} s_i}$ $\left[\begin{array}{c} f_i \to Frequency\ belonging\ to\ bin\ i \\ s_i \to Spectral\ value\ at\ bin\ i \\ \mu_s \to Spectral\ spread \\ b_1, b_2 \to Band\ edges \end{array}\right]$
	Spectral Kurtosis (SK)	It determines the flatness of a spectrum around its centroid.	$SK = \frac{\sum_{i=b_1}^{b_2}(f_i-\mu_f)^4 s_i}{(\mu_s)^4\sum_{i=b_1}^{b_2} s_i}$

- Time-domain methods consist of applying statistical methods to the time-series representation of signal under consideration. The signal is first segmented into shorter time-series windows depending upon overlap consideration and various statistics are then applied to those windows. These features include finding peak, mean, root-mean square (RMS) values, variance, standard deviation, skewness, kurtosis, entropy, etc. [114].
- Frequency domain methods initially consist of transformation of time domain signals into frequency domain signals [119]. This can be performed through techniques like Fourier transform (FT), Fast Fourier transform (FFT), etc. The transformation in frequency domain makes the mathematical analysis easier. Various frequency domain features can be calculated including power spectral density (PSD), energy, peak frequency, mean power, signal to noise ratio (SNR), spectral kurtosis, spectral skewness, spectral entropy, Shannon entropy etc. [120]. Various time domain and frequency domain features are included in Table 3.
- Time-frequency domain methods are very common for the analysis of non-stationary signals. They require the conversion of one-dimensional time-domain signal to two-dimensional time-frequency representation [121]. This conversion is made through various methods like wavelet transform (WT) [122], short-time Fourier transform (STFT) [123], Hilbert-Huang transform (HHT) [124], Wigner-Ville distribution (WVD) [125], etc.

Anomaly detection and FDL: Once data preprocessing and feature mining are conducted successfully, it is essential to work upon anomaly detection. Anomaly detection consists of analyzing the data to identify any abnormal patterns [126]. It helps in pointing out when the signal or parameter under consideration surpasses the defined system characteristics. Furthermore, with anomaly detection, FDL can identify and pinpoint the type and area of fault [127]. Machine learning based FDL process block diagram is shown in Fig. 15. Numerous machine learning based and other AI based FDL techniques have been proposed in literature.

Supervised learning based FDL: In supervised learning algorithms, the training data in the labeled form act as a teacher or supervisor. The labeled data consist of inputs and their respective outputs. With the correct available data, the machine learns the behavioral patterns to predict the output. Principally, it finds the relationship or mapping function with the associated input and output data [128]. Various supervised learning based FDLs have been utilized for GCPS applications. They are detailed in Table 4 with their advantages and disadvantages.

Artificial Neural Network (ANN) refers to a method under supervised learning, which is inspired from the structure of human brain. It incorporates a neural network similar to the biological neuron network and tries to imitate human brain in terms of learning. ANN based FDL for multilevel H-bridge inverter is presented [16]. The parameter under consideration for anomaly detection is voltage at inverter terminals. Many features like signal power, energy etc. are extracted using discrete wavelet transform (DWT). These features are then fed as input to the ANN having input, output and one hidden layer for fault localization. The classification accuracy is found to be 99.9%. Another Feed Forward Back Propagation Neural Network (FFBPNN) is utilized for fault detection in a three-phase voltage source inverter (VSI) switch faults [17]. The faults considered are single switch and double switch OC fault scenarios for different load and frequency variations. Here, the fault parameter is the normalized stator currents through park's vector transform (PVT). The real-time simulation results help in understanding the effectiveness of the technique. Another approach based on fault feature mining through FFT and FDL using ANN is proposed for Cascaded H-Bridge Multilevel Inverter [129]. It consists of offline training in MATLAB and then transfer of complete system parameters on LabVIEW based real time system. Multilayer perceptron network (MLPN) based FDL approach has been implemented using DFT and FFT combined feature mining for multi-level inverter FDL [18].

Supervised learning based fault diagnosis in diode clamped multilevel inverter using probabilistic neural network (PNN) [19] is developed. DWT is employed for feature extraction through Daubechies order 4 (db4) mother wavelet. The overall classification accuracy is quantified

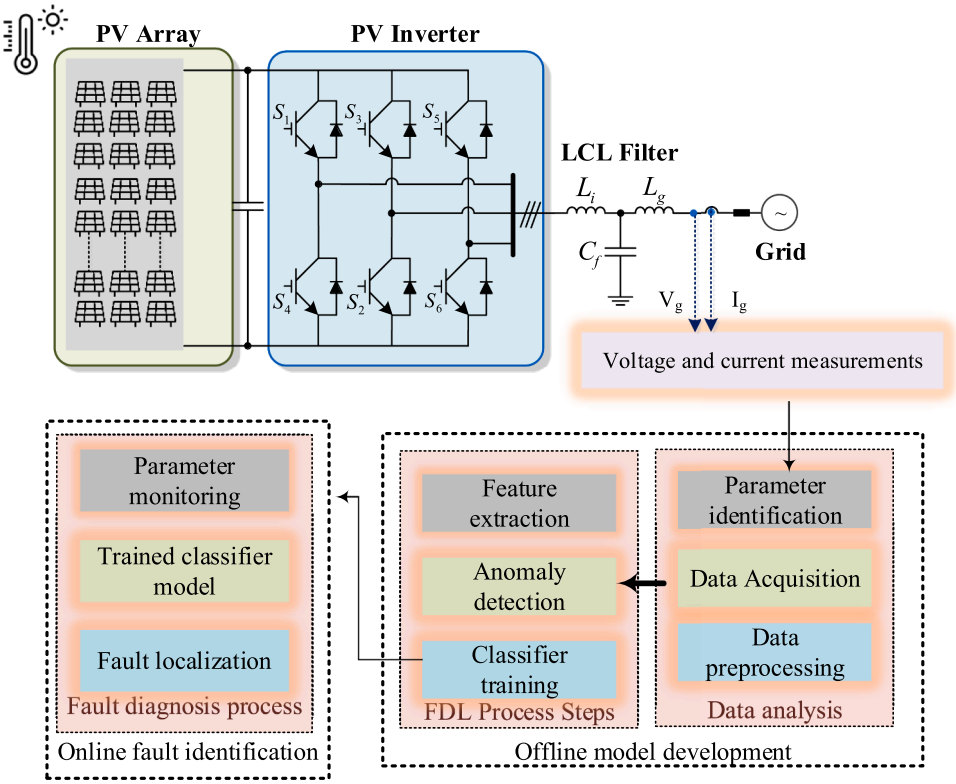


Fig. 15. Block diagram for a machine learning based FDL.

Table 4
Details of supervised learning based approaches.

Supervised learning Approach	Advantages	Disadvantages
Artificial Neural Network (ANN) [16–19,129, 114]	Ø Simple network structure Ø Robust to noise in data Ø Can handle more than one task	Ø Computationally intensive Ø Sensitive to dimensionality of data Ø Network structure is based on trial and error
K-nearest neighbor (KNN) ([130])	Ø Easy to implement Ø Able to adapt to new data Ø Suitable for multi-class classification	Ø Computational complexity Ø Optimal value for "k" is difficult to decide Ø Sensitive to noise in data
Decision Trees ([131])	Ø Consists of simple structure Ø Predicts clear outstanding results Ø Outcome is not affected by noise or outliers presence.	Ø Large and complex trees may suffer from overfitting Ø With some dominant classes, tree may provide biased decision.
Random Forest (RF) [132–134]	Ø Less vulnerable to overfitting Ø Able to tackle missing values Ø Less impacted by noise in data	Ø Difficult to adapt to new data Ø Training time is higher Ø Computational complexity
Bayesian Networks [135,136]	Ø Optimal utilization of features Ø Generalization ability is good Ø Can be applied to reason in both forward and backward directions	Ø Construction of network is difficult. Ø Requires high computational efforts Ø Poor performance with high dimensional data
SVM (Support Vector Machine) [118,137–140]	Ø Can handle high dimensional data Ø Can work with non-linear data using kernel Ø Memory efficient Ø Strong generalization capability	Ø Vulnerable to noise in data Ø Training time is higher Ø Challenging to interpret the results Ø Difficult to visualize the effect of hyper-parameters

as 99% for the proposed FDL. An ANN based FDL employing DWT based fault feature mining for grid connected PV inverters is proposed [114], which incorporates thermal overstress and wear out failures in IGBTs using MATLAB/PLECS integration. This work develops two classifiers, which are able to work in both component failure and degradation conditions. The accuracy in component degradation mode is observed to be 94.2% and in component failure mode, it is 97.4%. The detection time in both the cases is 0.02 seconds.

K-nearest neighbor (KNN) algorithm works upon the principle of association with the closely available data points. It classifies the data by utilizing the proximity information with other data incorporating formulas like Euclidean distance. A KNN based fault diagnostic technique for grid side faults is presented [130]. For feature mining, DWT is employed for approximate coefficients collection from the output voltage and current signals and further, standard deviation is calculated. The obtained features are input to KNN for training. Various fault modes are considered under load variations and overall, it is found to have satisfactory performance.

One of the most common supervised learning-based approach is ***Decision Trees***. It consists of a tree-like upside decision structure having root at the top splitting into numerous braches below the root. The point where the branch stops further splitting into more branches is the final decision made by the tree regarding the outcome. Decision trees have been utilized for FDL in various applications. A decision tree based FDL is developed to classify different inverter faults for induction motor drive application [131]. Since selection of root is essential for optimum results, Quinlan's information theory is employed for root selection. The input of decision tree is the time-domain inverter current output obtained through the hall sensors. Relevant features are extracted to feed as input to the decision tree and various attributes of decision trees can be represented through these features. To build and analyze the appropriate decision tree, proper training and testing data collection are important. Experimental results dictate 100% training and testing accuracy in case of 10 class decision tree and 100% training and 96.4% testing accuracy for 22 class decision tree.

Random Forest (RF) is another supervised learning-based algorithm, which works upon the combination of decision trees. Various decision trees, uncorrelated, are collected together to form a forest kind structure and make accurate estimations. An OC fault diagnostic technique for Neutral-point clamped (NPC) inverter is proposed [132]. It adopts Concordia transform to process the fault variables in *dq* reference frame. The acquired features are provided to the RF based classifier for training purpose. The results obtained are compared with other data driven techniques and it is found to have better performance in terms of classification accuracy that was observed to be 97.27%. Another RF based switch FDL for GCPS is proposed [133]. Firstly, the acquired fault data is preprocessed through interval reduced kernel Principal Component Analysis (IRKPCA) based model. It helps in dimensionality reduction and selecting the best performing features, then selected features are fed to RF based classifier. The results are further evaluated using various diagnostic metrics. A reduced kernel RF based FDL is implemented for GCPS involving inverter switch faults [134]. It employs two classifiers having the Euclidean distance based reduced kernel RF and K-means clustering based reduced kernel RF for respective dimensionality reduction and useful feature selection. Since, training data is reduced, it becomes computationally efficient and further, it is found to have better performance as visible from the results.

Bayesian Networks are also a category under supervised learning and are considered as quite popular in the area of probabilistic information representation. They are characterized through directed acyclic graph and they come under probabilistic graphical model utilizing Bayesian implication to quantify probability computations. The objective is to consider conditional dependence through conducting inference on the given variables. Bayesian network consists of edges and nodes, where each edge refers to a conditional dependency; whereas each node represents a unique variable. Recently, they have been demonstrated for FDL applications in power electronic converters. A data driven FDL technique for three-phase inverter based on Bayesian network is implemented [135]. It comprises of acquiring output line-to-line voltage information for various fault modes including no fault condition. Further, different relevant features are extracted through FFT and dimensionality reduction takes place with the help of principal component analysis. Thereafter, Bayesian network consisting of fault and fault symptom layers, is utilized for FDL. These layers comprise of fault and fault symptom nodes for inverter switch faults. Both normal and faulty states are represented by these nodes corresponding to their respective harmonic magnitudes obtained through PCA. Parameter learning of Bayesian networks in employed through maximum likelihood estimation (MLE) approach. After Bayesian networks are modelled with optimum parameters, pearl's belief propagation is adopted for probabilistic inference with test data for final FDL outcome. Another prognostic scheme for IGBTs to predict RUL is proposed combining the failure mode information with the algorithm of probability reasoning under Bayesian network [136]. Online measurements of device temperature are collected and employed as the loading profile to obtain the simulations. The strain caused due to overloading and other reasons to the device as a function of temperature is incorporated to construct response surface equation. This equation helps in identifying the lifetime model of IGBT and further, helps in predicting the RUL with the help of conditional probability information made available through Bayesian network.

One of the popular supervised learning algorithms is ***Support Vector Machine (SVM)***. It is based on creating a hyperplane, which constructs the boundary between the data objects belonging to the same class [141]. An SVM based FDL for three-phase PWM inverter is presented [137]. To begin with, the output currents are normalized and then, multi

resolution analysis (MRA) based DWT is employed for feature mining. Further, the features attained are fed to the SVM classifier, which works by constructing optimized boundary for OC switch fault diagnosis. An FDL based on PCA-SVM is implemented for cascade H-bridge multilevel grid-tied PV inverter [138]. After the selection of fault signature, the corresponding data is pre-processed utilizing FFT analysis. The FDL method operates on removing the noise from the data and further feature reduction through PCA. Overall the fault classification accuracy is found to be more than 98%. Another hybrid SVM based FDL for three phase inverter faults is proposed [139], employing discrete orthogonal wavelet transform (DOWT) for feature extraction. It consists of a multi-classes classification strategy utilizing 1 versus rest (1-v-r) approach. A new Huffman tree structure is further employed to enhance accuracy of SVM classifier. The correctness of the proposed FDL was observed to be 99.6%. A tri-class SVM is proposed for OC FDL in inverter fed motor drive [118]. It obtains the fault features through applying recursive wavelet transform to the respective fault signature. Further obtained coefficients and their energy are given as input to two different SVM classifiers. Their results are compared and evaluated with the classification performance metrics. An incipient fault diagnostic technique based on SVM for inverter fed induction motor drive is presented [140]. It consists of signal processing based on mean current vector approach. Time-domain features like skewness, kurtosis etc. are computed and fed to SVM classifier. Further metaheuristic method based data training is carried out and promising results are obtained. The classifier is presented to have accuracy of 94.82% for the provided data. Hence, a general machine learning based approach follows steps as shown by the block diagram in Fig. 16.

Unsupervised learning based FDL: Unlike supervised learning, unsupervised learning is independent of a supervisor or labeled datasets and functions upon exploring data to find hidden patterns or association among data points. It is widely utilized for clustering and data compression tasks.

An unsupervised learning based OC fault diagnosis for three phase inverter switches is proposed [142]. It utilizes the normalized values of DC current for finding the relevant fault features and employs Auto-adaptive and Dynamical Clustering (AUDyC) algorithm for further processing with unlabeled data. It performs similarity verification, adaptation and evaluation to obtain labels for the given fault data. Overall it is able to work as a satisfactory fault diagnostic technique. A fast clustering and Gaussian mixture model based fault prognostic technique for grid-tied PV inverter is presented [143]. Firstly, real time system data is attained incorporating output voltage, current, power, temperature of IGBT switches etc. The collected feature data is compressed to a low dimensional feature set employing t-distributed

Table 5
Advantages and disadvantages of unsupervised learning based methods.

Unsupervised learning Approach	Advantages	Disadvantages
Auto-adaptive and Dynamical Clustering (AUDyC) ([142])	Ø Able to find hidden patterns in data Ø Easier to obtain unlabeled data Ø Data preprocessing is simple and effortless	Ø Uncertain outcomes Ø Vulnerable to outliers
Fast clustering and Gaussian mixture model [143]	Ø Fast clustering makes the distribution of classes easier Ø Less complex as compared to others	Ø Analysis of results is difficult Ø Results may vary considerably in the presence of new data points

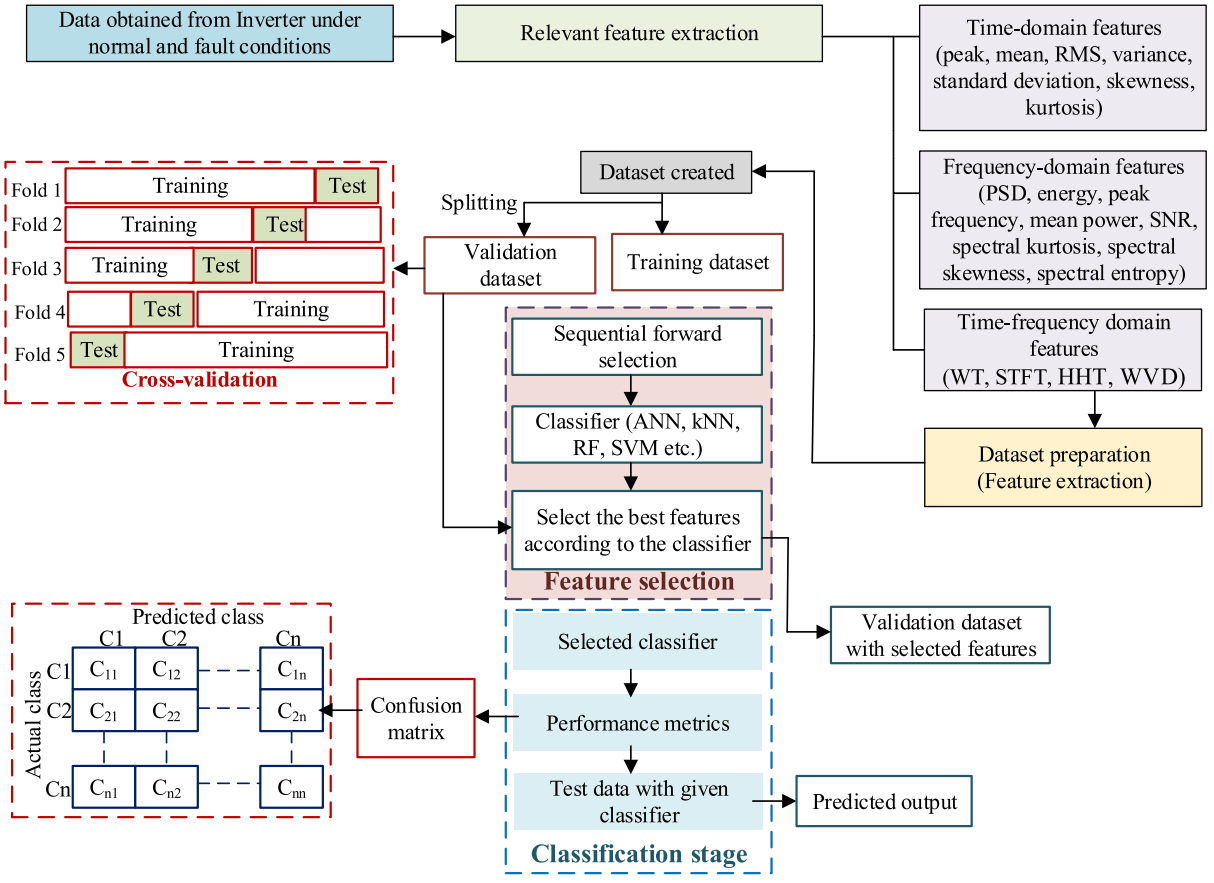


Fig. 16. General steps followed by a machine learning technique.

stochastic neighbor embedding (t-SNE). Then, similar data is clustered together using fast clustering and for evaluating fault prognostics, Gaussian mixture model is utilized. The features of unsupervised learning based methods are discussed in Table 5.

Semi-supervised learning (SSL) based FDL: Semi-supervised learning is based on mix of labeled and unlabeled data. It has advantages of both supervised and unsupervised learning. Furthermore, its full potential has not been explored yet for GCPS applications.

A real time fault diagnostic technique based on active semi-supervised fuzzy clustering for multiphase multilevel NPC Converters is developed [144]. Firstly, existence of fault is identified using self-recurrent wavelet neural network (SRWNN). Fault indicators for five phases are computed with adaptive learning rate formulation. Then, semi-supervised fuzzy clustering approach is implemented for fault localization and isolation with pairwise constraints. The technique is able to localize the fault within 500microseconds of its occurrence. Another approach based on the contribution of kNN and decision tree utilizing majorly unlabeled and remaining labeled data is proposed for three-phase faults [145]. After gathering the required fault data, DWT is adopted for feature vector representation and harmony search algorithm (HAS) is utilized for finding the appropriate mother wavelet and decomposition level. Once proper feature vectors are acquired, two test-systems are developed with different ratios of labeled and unlabeled data. These are then compared along with graph-based SSL utilizing same fault data. The results obtained provide adequate information regarding the significant improved accuracy of the presented technique based on ten-fold cross validation. The comparison among the SSL based FDL approaches discussed here is detailed in Table 6.

Deep Learning: It is an advanced subfield of machine learning, which inculcates deeper neural networks than the conventional ANNs and therefore, it is more efficient and accurate than conventional machine learning techniques. As compared with the machine learning based FDL, it is independent of feature mining steps [13]. It consists of powerful inherent feature extraction capability, typically applied to unstructured data, making it a promising technology for FDL in GCPS.

Deep learning has many branches including convolutional neural networks (CNNs), recurrent neural networks (RNNs), Boltzmann machines, deep belief network (DBN) etc. Among these CNNs are considered to be the most powerful tool since they are independent of tedious manual feature extraction process, providing them an edge over conventional machine learning techniques [146]. The typical implementation of CNN in a GCPS for FDL is shown in Fig. 17. They typically consist of many convolutional and pooling layers stacked over one another followed by fully connected layer having softmax layer containing the final classification output, as shown in Fig. 17. An improved CNN-GAP (global average pooling) scheme is implemented for inverter FDL [121]. Inverter output data is acquired in raw time-series form, which is typically in one-dimensional (1D) form. This 1D data is fed to the CNN-GAP structure. At the input layer, it constitutes two dimensional (2D) feature maps with convolutional and pooling layer architecture. It has an additional GAP layer at the end, which compresses and transforms the dimension of the given output. The FDL decision is provided in the final layer, i.e. softmax layer. The results demonstrate a reduction in training time by 15% as compared to the traditional CNN. Another 1D CNN based OC FDL for three-phase inverter is proposed [147]. The advantage of this approach is that it directly takes 1D time-domain inverter current signal as input omitting the 2D conversion into images. The automatic feature extraction capability in the initial layers and all convolutional and pooling layer outputs as 1D vectors. Compared to MLP and Stacked Denoising Auto Encoder (SDAE) methods for the same application, the proposed 1D CNN is found to have better accuracy and less computational effort. The implementation of these techniques as per the literature review is summarized in Table 7.

Table 6
Comparison of SSL based FDL techniques.

SSL Approach	Advantages	Disadvantages
Fuzzy clustering [144]	Ø Contains both labeled and unlabeled data Ø Provides better results as compared to k-means clustering Ø Flexible as belonging of data points to different clusters is easier to attain	Ø Computationally complex Ø Takes more time compared to k-means clustering Ø Difficult to interpret the final outcome
Co-training of eager and lazy learner [145]	Ø Provides better accuracy compared to graph based SSL Ø Real-time implementation provides consistent outcomes	Ø Fitness parameter selection for HSA is critical Ø Computationally intensive

4.3. Other FDL techniques

Fuzzy logic: Fuzzy logic is another category under AI based technique, which is a rule-based approach and is meant to handle system uncertainties. It takes values that are not completely true/false, low/high or 0/1; rather it can function over some intermediate values as well. It consists of taking input as crisp values, then they are converted to corresponding fuzzy values through applying membership functions. Further, fuzzy rule-set is applied to them to provide inference in fuzzy form. Consequently, defuzzification of the output takes place and finally, we get a corresponding crisp output as can be viewed from Fig. 18. Fig. 18 shows the implementation of fuzzy logic based FDL in case of inverter switch faults.

A fuzzy logic based OC fault diagnostic scheme is developed for PWM-VSI induction motor drive [148]. It consists of using the inverter current as fault parameter and analyzing Concordia transformed current patterns. The proposed method then applies the fuzzy rule based technique to identify the changes in the current pattern. The experiment with the fuzzy based fault diagnostic approach manifest that it is particularly feasible in the real-time applications. Another fuzzy logic based intelligent fault diagnostic approach for solar inverter is presented [127]. Firstly, the output current and voltage signals are acquired and then RMS and average values are calculated. Thereafter, they are input to fuzzy logic based fault detector and a correlation based analysis is done. It then declares the faulty area and the intensity of the fault.

Combination of two different AI techniques: Other FDL schemes also include the combination of two different AI based methods. For instance, fuzzy logic is applied with neural networks making Fuzzy Neural Network (FNN) having better performance than their individual performances for control applications. However, their scope for FDL in solar inverters is yet to be explored. Similarly, another improved hybrid version called Adaptive Neuro-fuzzy Inference System (ANFIS) is implemented for fault diagnosis in capacitors, PV panels and rectifier based systems [149].

Comparison based: These techniques are based on comparing the measured fault parameters with their specified threshold reference values. The fault can be identified through the analysis of the error generated between the measured and reference values, as described in Fig. 19. An OC fault diagnostic technique based on comparison approach is proposed for three phase inverter [150]. It incorporates different fault signatures like inverter pole voltage, system line voltage, etc. and then, these are analyzed and compared. The threshold limits for error generated are identified and then, these are compared with the actual error generated and corresponding fault is identified.

Hybrid FDL: These techniques consist of a combination of model based and model-free approaches. A combination of model based and ANN approach is implemented for three phase inverter open switch FDL [151]. Different OC fault conditions and corresponding voltages and currents are modelled. Further, for offline training, the signals are segmented with one-third overlap ratio and statistical features are extracted like mean, standard deviation, etc. These features are fed to

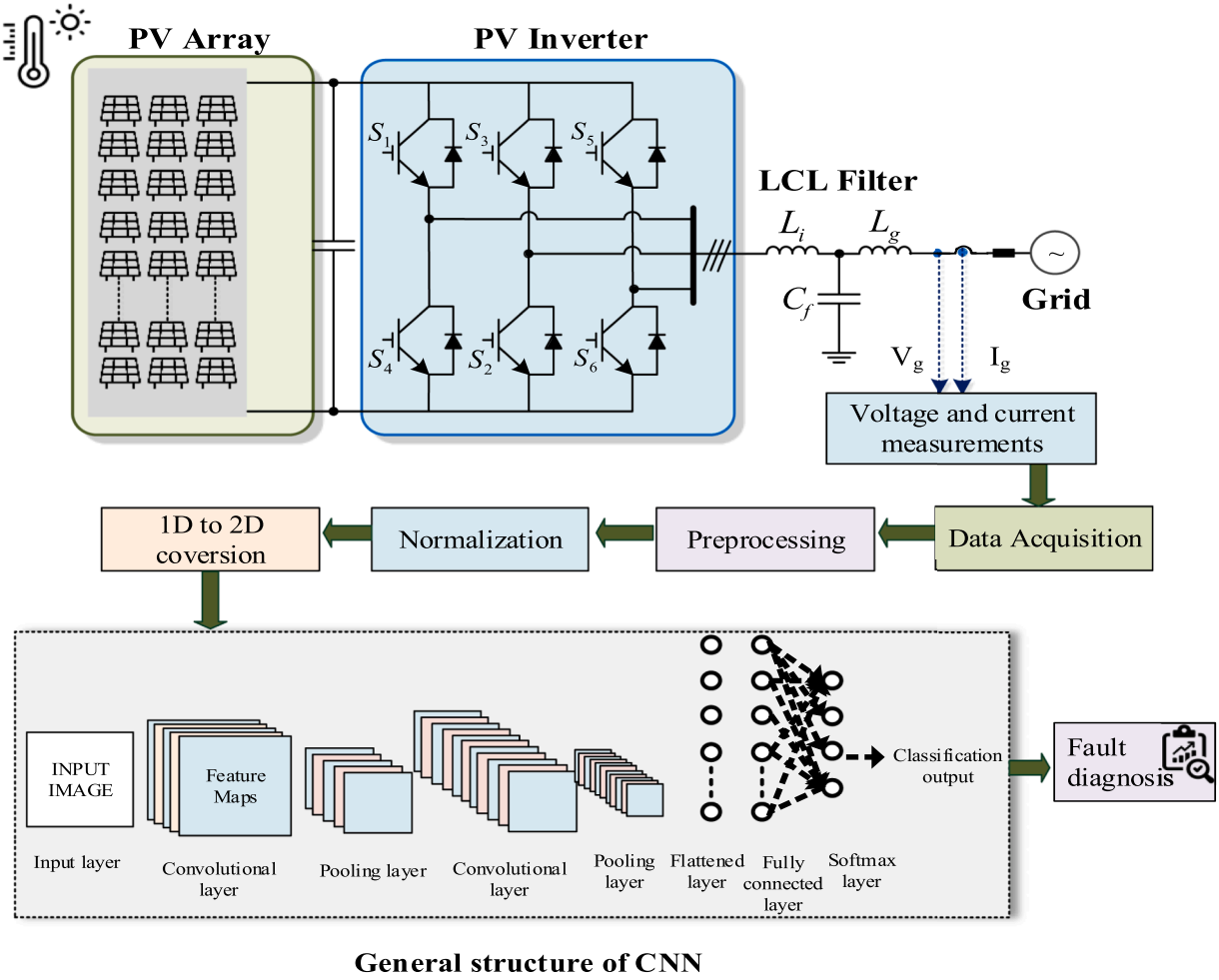


Fig. 17. CNN implementation as FDL technique along with its general structure.

multi-class neural network for FDL. In conclusion, individual classification accuracy and overall accuracy are evaluated.

4.4. Condition monitoring and FDL in capacitors

Typically CM based techniques are utilized for capacitors so as to enhance the reliable operation of the system [152]. Capacitor deterioration in LCL filter leads to increase in total harmonic distortion (THD) on grid side. A capacitance estimation and replacement technique for LCL filter is proposed [153]. It focuses on analyzing the change in response corresponding to 80% C value from its original value. It is observed that capacitor degradation results in drop in overall power factor and moves the resonant frequency towards switching frequency, which further leads to adverse effects in the system. Therefore, the proposal is to replace the capacitor before its failure impacts the whole system reliability. Since, ESR is not a valid failure indicator for MPPF capacitors, capacitance estimation is a better approach for their CM. And to further improve the C value estimation, a quasi-online novel CM approach for DC link capacitor is presented [154]. It incorporates LC resonance purposely when the system is non-functional. This leads to production of capacitor resonance current, which is the condition variable and is assessed to determine the health of capacitor. It is a simple and low cost approach since it employs already installed current sensors for measurement of current. The time-varying capacitor current is analyzed and for curve fitting, multivariate non-linear regression is utilized. After a number of iterations and corrections, the presented algorithm is able to converge to the optimal values. Experimental results manifest high accuracy of the above proposed algorithm.

Another online non-invasive CM technique based on parameter estimation is proposed for Boost converter capacitor [155]. It consists of capacitor estimation during the online operation using polynomial fitting for parameter estimation and then, applying it offline to find ESR value, thereby providing more reliable solution. The condition variables referred are the input current and output voltage of the Boost converter as a function of capacitance. To eradicate the switching noise, data acquired near to switching is ignored and polynomial fitting is done using least mean squares algorithm (LMS). An online impedance spectroscopy technique is developed for capacitor health estimation in power electronics drive. To begin with, it derives a capacitor model to investigate the health and performance of DC bus capacitors. The current through the capacitor and AC component of capacitor voltage are measured and further, their FFT is computed to quantize the frequency spectra. Eventually, the ESR is estimated through the extraction of spectral lines nearest to twice the line frequency. Another ESR estimation based failure diagnosis and prediction for Al electrolytic capacitors is proposed [86]. It also involves deducing life of capacitor based on analytical equations relating electrolyte volume with the ambient temperature and eventually, curve fitting.

A capacitor health monitoring based technique is implemented for buck DC/DC converter using printed circuit board Rogowski coil (PCBRC) as a cost effective method [156]. The PCBRC is employed to capture the derivative of current flow in capacitor. It is observed to quantize the lifetime of the capacitor through the calculation of ESR. Overall, it is cost effective and serves the purpose to determine the lifetime of the capacitor. There are specific limitations on temperature by the electrolyte based on the material resistance and vibration range

Table 7
Summary of model-free FDL techniques.

Fault Type	Inverter topology	FDL approach	Fault signature	Signal processing technique	Feature extraction method	Detection time	Detection accuracy
Switch OC	Cascaded H-bridge MLI [16]	ANN	V_O, I_O	DWT (dB10)	Frequency domain	–	99.9%
	VSI [17]	ANN	I_S	DWT (dB3)	Frequency domain	15.47 ms	–
	Cascaded H-bridge MLI [129]	ANN	V_O	Fourier transform	Frequency domain	10 ms	~100%
	3-phase VSI [131]	Decision Tree	I_O	–	Time-domain	–	96.4%
	NPC inverter [132]	RF	I_O	–	Time-domain	–	97.27%
	3-phase H-bridge inverter [133]	RF	V_O, I_O	–	Time-domain	–	–
	3-phase H-bridge inverter [134]	RF	V_O	–	Time-domain	–	~100%
	3-phase H-bridge inverter [137]	SVM	I_O	DWT (dB2)	Frequency domain	–	–
	H-bridge MLI [138]	SVM	V_O	–	Time-domain	–	99.95%
	3-phase H-bridge inverter [118]	SVM	I_O	DWT	Frequency domain	–	95.6%, 93.3%
	3-phase H-bridge inverter [142]	Clustering	I_O	–	Time-domain	0.0226 s	–
	NPC MLI [144]	Clustering	I_S	Wavelet multiresolution analysis	Frequency-domain	500 μs	–
	3-phase H-bridge inverter [121]	CNN	V_O	–	Automatic feature extraction	–	99.95%
	3-phase H-bridge inverter [147]	CNN	I_O	FFT	Frequency domain	–	99.21%
Switch OC & SC faults	Cascaded H-bridge MLI [18]	ANN	I_O	FFT	Frequency domain	–	97.5%
	Diode clamped MLI [19]	ANN	V_O	DWT (dB4)	Frequency domain	–	99.8%
Other faults	Single-phase H-bridge inverter [114]	ANN	V_T	DWT	Frequency domain	0.02 s	97.4%
	3-phase H-bridge inverter [130]	kNN	V_O, I_O	DWT (dB3)	Frequency domain	–	~100%
	3-phase H-bridge inverter [135]	Bayesian Network	V_O	FFT	Frequency domain	–	98.99%
	3-phase VSI [139]	SVM	V_O	DOWT	Frequency domain	–	99.6%
	3-phase H-bridge inverter [140]	SVM	I_O	–	Time-domain	–	94.82%

Other faults – multiple switch faults, diode faults, three-phase faults, degradation faults, I_S- Stator current, I_O- Output current or grid current, V_O- Output voltage or grid voltage, V_T – Voltage at inverter terminals

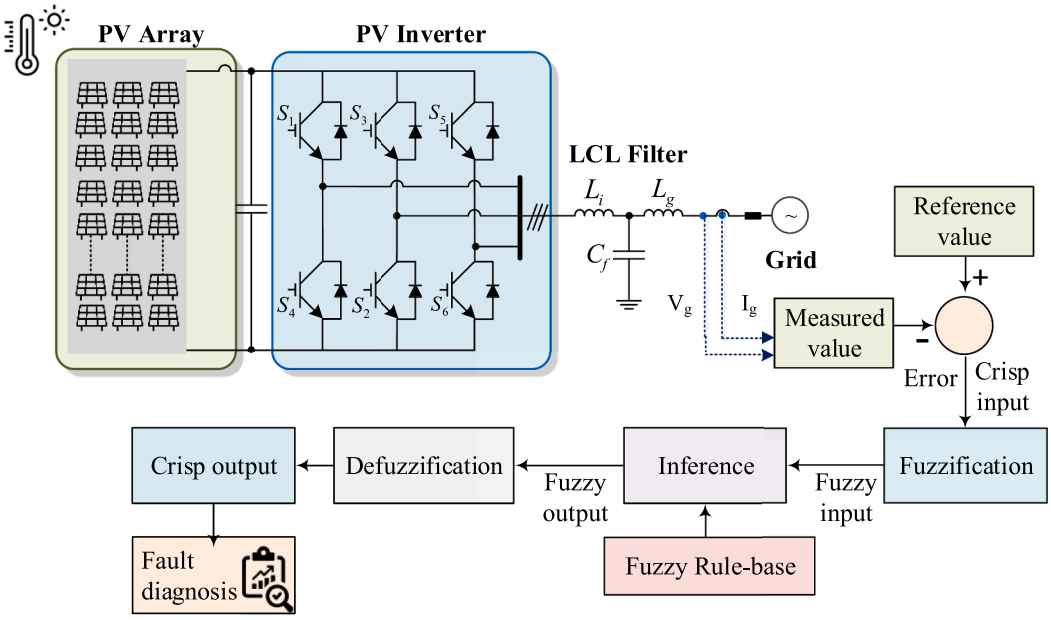


Fig. 18. Block diagram of fuzzy based FDL approach.

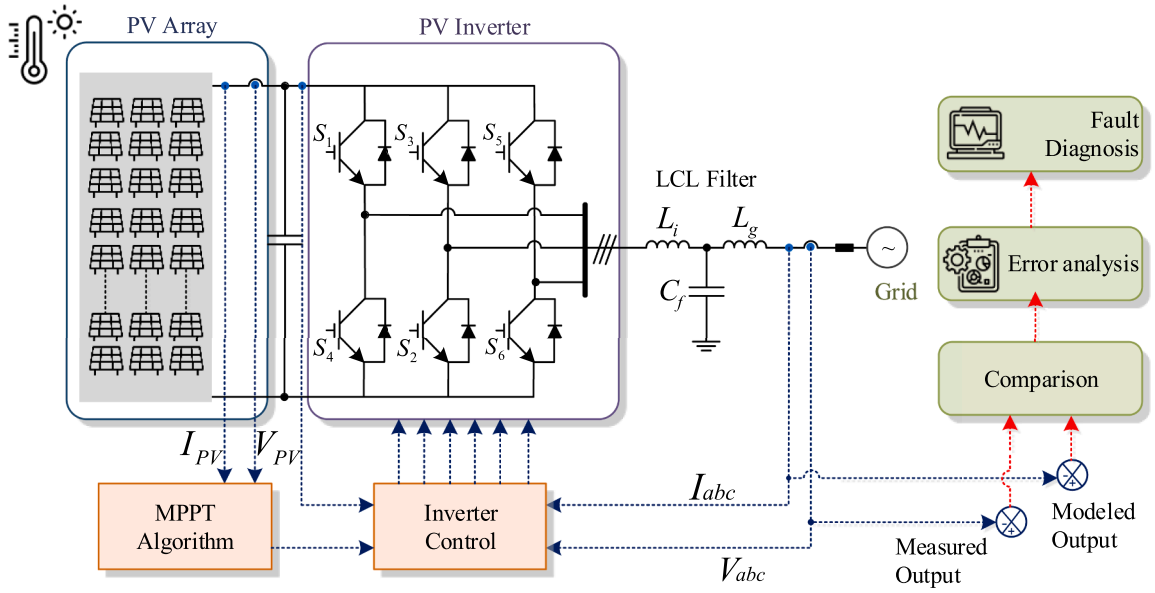


Fig. 19. . Structure for a comparison based FDL.

[157]. The operating temperature has a definitive effect on the ESR and C values and this effect is quantized through the mathematical equations. The estimated ESR and C values at a particular temperature are compared with the reference values at that temperature. The obtained ratios are observed and if they exceed the corresponding values for the reference, then it is a clear indication that now the capacitor is no longer healthy. Overall, experimental results present the effectiveness of the proposed technique with an estimation accuracy of 6%. A novel genetic algorithm (GA) based capacitor ESR estimation and remaining time to failure evaluation is proposed [158]. It incorporates theoretical calculation realizing current through capacitor involving low-frequency and high frequency components, as well as the THD of the source current. The GA based model described through frequency independent parameters, is able to consider the capacitor behavior when subjected to large temperature and frequency ranges. Owing to this model, impact of skin effect causing ESR increase at high frequencies is considered. Ultimately, the ESR value and remaining time to failure is determined utilizing the output ripple voltage measurement. An ANN based capacitance estimation technique for DC link capacitors for the application of three-phase motor drive systems is proposed [159]. The system configuration consists of applying diverse conditions to the DC link capacitor. It further comprises of designing capacitor printed circuit board (PCB) to be connected in parallel to the already existing DC link capacitor. The PCB is divided into 9 capacitor individual steps and each capacitor step is added every time to assess different capacitor values. This work presents thorough analysis on the factors impacting the capacitance estimation. There are two ANNs compared in this work, ANN1 consists of capacitance estimation via providing input to ANN as output current and DC link voltage ripple. On the other hand, ANN2 incorporates the effect of DC link voltage harmonics for predicting C value. After applying simulations and experiments, it is observed that ANN2, i.e. the effect of DC link voltage harmonics validates the effectiveness of the approach and is able to predict the C value with lowest estimation error.

An online condition monitoring utilizing MPPF capacitance estimation technique for fault tolerant aerospace drive is proposed [90]. It employs already existing current and voltage sensors, which are there for control and protection reasons. The novelty of this technique lies in utilizing the condition monitoring in real-time aerospace drive applications. The system configuration consists of having additional DC link capacitors for fault tolerant operation. Furthermore, it has the advantage of not injecting any external signals for capacitor data collection purposes, hence, data can be acquired smoothly for longer time. Based on this data and calculation of current signal integral, change in time and voltages, capacitance can be predicted. The technique is validated through practical implementation providing encouraging results.

Another real-time electrolytic capacitor condition monitoring technique is proposed. The technique comprises determining the ESR changes and C value changes in real-time [160]. It utilizes parameter variation law based on temperature to identify ageing algorithm and calculate remaining time to failure. Furthermore, Kalman filter provides capacitor voltage and current and their assessment may aid the subsequent calculations for ESR and C values. Overall, this low cost technique works well for electrolytic capacitor health estimation. The condition monitoring and FDL techniques for capacitors discussed above are detailed in Table 8.

4.5. *Challenges and Future scope*

Overall, from the discussed analysis, it can be inferred that model-free/AI-based FDLs are better in terms of quantifying the performance parameters. In addition, AI based techniques provide superior detection and localization abilities as compared to model-based techniques. However, a bottleneck in the direction of AI is that there are very few real-time implementations of AI based techniques. Therefore, there is a need to look into the real-time implementation prospects of AI, which will provide deeper understanding about their exceptional and outstanding performance. However, that would not be easy since creating fault data in real-time is an enormous task. Consequently, it becomes a major challenge to identify the potential of AI for FDL

Table 8
Detailed analysis of condition monitoring and FDL in capacitors.

Type	Capacitor considered	Approach (C/ESR)	Description	Accuracy	Advantages	Disadvantages
Online	MPPF [153]	C	The capacitance change to 80% of its value indicates failure of capacitor and is determined through change in resonant frequency.	–	Ø Does not require additional sensors for measurement Ø Simple and low cost implementation	Ø Applies to only specific application
	MPPF and electrolytic capacitors [155]	C and ESR	Parameter estimation through the available capacitor voltage and current measurements employing polynomial fitting. Least mean square (LMS) algorithm is used for polynomial fitting.	C-<1.4% ESR- 1.8%	Ø Simple, flexible and low cost Ø No additional hardware is required Ø Highly accurate	Ø Cannot be generalized for other applications
	Electrolytic capacitor [86]	ESR	Parameter identification algorithm based on capacitor equivalent model utilizing least squares approach for ESR estimation.	6%	Ø Simple and low cost	Ø Requires accurate capacitor modeling
	Electrolytic capacitor [156]	ESR	Capacitor current is monitored through PCBRC and lifetime is estimated based on ESR calculation.	–	Ø Cost effective solution Ø At high frequencies, it has linear response	Ø Requires additional hardware Ø Specific temperature limitations
	Electrolytic capacitor [157]	C and ESR	C and ESR values are predicted using STFT at both low and high frequencies.	~6%	Ø Simple and fast technique Ø Generalization capability is good	Ø Demands additional efforts
	Electrolytic capacitor [159]	C	ANN is adopted for C value estimation in both time and frequency domain.	1.3%, 1.2%	Ø Simple and easy implementation Ø Does not require additional hardware	Ø Precise network parameters are difficult to determine
	MPPF [90]	C	It involves calculating C value in online process through utilizing presented sensors for capacitor voltage and current measurements.	1-5%	Ø No extra sensors are needed Ø Does not depend upon the operating conditions	Ø Relies too much on the accuracy of sensors Ø Sensitive to noise at high frequencies
	Electrolytic capacitor [160]	ESR and C	Temperature based parameter variation law is employed along with Kalman filter to predict ESR and C values.	ESR- 5%C-10%	Ø No extra sensors are needed Ø Insensitive to disturbances	Ø Computationally intensive
Quasi-online	MPPF [154]	C	It utilizes intentionally inducing LC resonance through controlling IGBTs in a quasi-online process.	1%	Ø No need of additional hardware Ø Time-dependent multi-parameters determination	Ø Determination of multiple parameters may make it a complex process
Offline	Electrolytic capacitor [158]	ESR	Involves identification of capacitor parameters through GA.	–	Ø Takes large temperature range into account Ø ESR increase at high frequencies is taken into account	Ø Convergence might be slow Ø Computationally intensive

applications in GCPS in real-time or online scenario. The validation of AI based FDLs should be justified through their comparison with other conventional methods utilizing varying metrics including cost analysis, complexity assessment, accuracy, embedded capability, robustness etc. In addition, there is limited work done on the fusion of model-based and AI based FDLs.

For delivering extraordinary performance in terms of robustness and reliability, the integration of model-based and AI based FDLs can be explored on a broader level. Therefore, it demands further investigation. For future prospects, reinforcement learning can be considered to have great potential in terms of providing highly accurate results for FDL applications [161]. It is different from machine learning techniques described above since it does not rely upon the training data; rather it learns through an action strategy that operates to earn maximum reward. Principally, it is a dynamic programming method and works to achieve the specified goal using trial and error approach. It has been employed for maximum power point (MPP) tracking using the PV array [162], grid frequency regulation [163], grid voltage regulation [164] etc., however it has not been applied to the fault diagnosis applications as of now. Deep learning based FDLs are considered to deliver higher efficiency, accuracy and fast results. However, they demand versatile and large datasets, which can be computationally intensive. Thus, it is desired for future prospects to analyze and explore how computationally less data can be employed such that it does not affect the actual behavior of deep learning based FDLs.

For the future efficient power conversion applications, Gallium Nitride (GaN) power devices are a promising technology. They have astounding performance as compared to the traditional devices since they are wide bandgap devices (with bandgap of 3.2 eV) having high breakdown field (3.3 MV/cm). Moreover, they have high electron mobility (2000 cm2/Vs). These advantages make them suitable for high voltage and high power applications with increased thermal stability even at high temperatures, providing cooling advantages and improved reliability. However, there are still a few barriers in a wide implementation of these devices in power converter applications including cost, reproducibility and yield. In addition, novel packaging methods and high volume GaN substrate technology may help in future dominance of these devices.

5. Performance parameters of fault detection techniques

In order to assess the state and health of a power electronic converter comprising of semiconductor switching devices, it is imperative to incorporate a fault diagnostic mechanism. This mechanism involves assessing the failure mechanisms and their operation modes. It helps in identifying the vulnerabilities of devices, understand the root-causes of failures and applying the understanding to make it more efficient and robust. The mechanism also involves working on FDL, which further comprise of two major functions – 1) discover the existence of fault and, 2) locating the fault and detecting the nature of fault. The FDLs, which perform the two functions meticulously are considered and reviewed in this paper. Further, they are categorized into different groups and are analyzed accordingly. Owing to the investigations from these FDLs, there are some performance parameters, which can be analyzed to assess the performance and robustness of any FDL.

5.1. Criticality analysis

The criticality analysis is a vital metric to determine the severity of the switching device failure [165]. The objective of such analysis is observing the risk analysis and to optimize resource usage to further address reliability concerns. It is based on analyzing the failure and ranking the particular failure mode depending upon its intensity, frequency and detectability. These three categories are ranked separately and further, multiplied to quantify a risk priority number (RPN). More value of RPN indicates a major failure, which needs to be handled on priority [166]. This helps in taking corrective measures to lessen the effect of any risky and dangerous failure. Once preventive measures are taken, RPN should be updated again and reanalysis should take place.

The intensity or severity (S) is ascertained by the design engineer or the assembly process engineer based on the distinctive failure behavior. It also involves tracking down the root cause of failure and based on the description, evaluating the necessary remedial actions to be taken. Second parameter is the frequency or occurrence (O) of the failure. Frequency of failure may depend on many factors including the surrounding environment and operating conditions, temperature conditions etc. The cause of failure provides important insight on the occurrence and this occurrence may be quantified through the probability (O-Rate) at the process step. The next parameter for determination is detectability (D) of a failure. The detectability is characterized by the ability to predict the failure before its occurrence. Based on the assessment, the control action, i.e. either preventive (P) or detection (D) is decided.

5.2. Detection time

Finding the existence of fault in itself not a heavy task and can be performed with minimal efforts. However, locating the specific faulty component and classifying the nature of fault, after detecting fault, is a burdensome task and requires considerable efforts. Therefore, it is important to measure the ability of the given FDL to identify and classify the faulty component efficiently and in a minimal time. Hence, fault detection time is a dominant performance parameter. From Fig. 20, it is observed that model-based techniques provide detection time varying from 0.4 ms to 49 ms, whereas AI-based techniques have variation from 0.5 to 20 ms. Overall, it can be concluded that in general, AI-based techniques are fast and are able to identify the fault in comparatively less time. As shown in the figure, a model-based FDL has lowest detection time 0.4 ms, however it is specific to a particular application and explicit faults. Nonetheless, there is no such disadvantage associated with the model-free FDL approaches.

5.3. Classification accuracy

In general, it is not easy to quantify how accurate an FDL is working. However, for advanced FDLs like machine learning based techniques applied offline, accuracy of any FDL can be calculated statistically. For offline machine learning based binary classification models, outcome is true positive (TP) when it correctly predicts the positive class and outcome is false positive (FP) when it wrongly predicts the positive class. Likewise, outcome is true negative (TN) when classifier correctly predicts the negative class and false negative (FN), when it wrongly predicts the negative class [167]. To evaluate the classification model, accuracy can be expressed

$$Classification\ accuracy = \frac{Number\ of\ true\ predictions}{Total\ number\ of\ predictions}$$

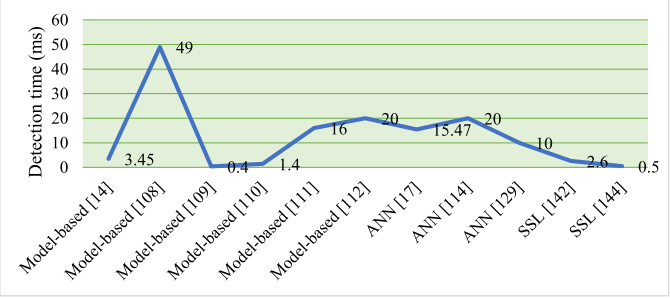


Fig. 20. Comparison between different FDL techniques based on fault detection time.

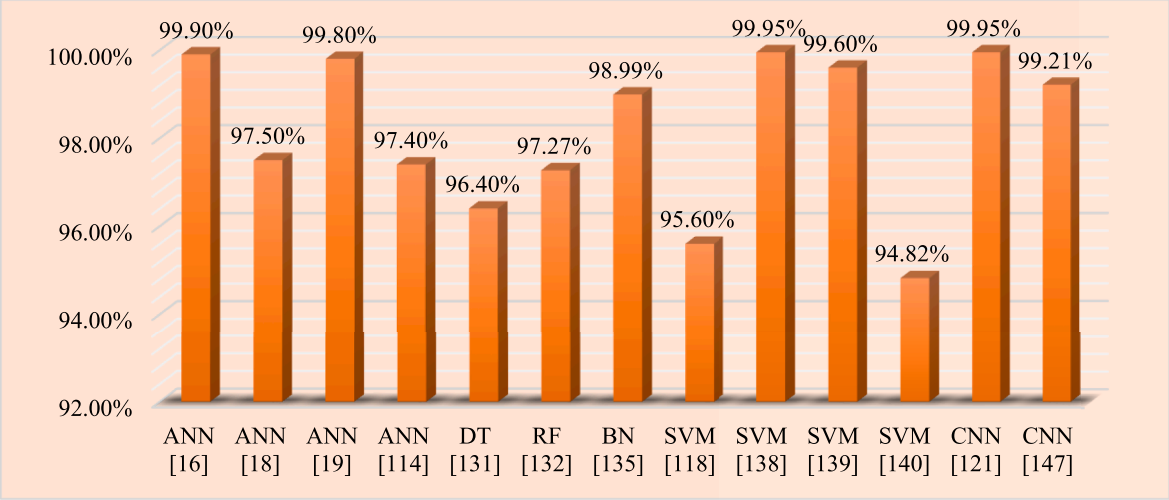


Fig. 21. Comparison between different AI-based FDL techniques based on classification accuracy.

$$Classification\ accuracy = \frac{TP + TN}{TP + TN + FP + FN}$$

Above expression applies to binary or two-class classification problems. For multi-class classification models, above expression can be applied by considering them as a group of many binary classification models. Here, positive and negative change corresponding to the actual label of the given data point. So for a single class, there is only one true positive and multiple true negatives.

The classification accuracy discussed in this paper for various literature works is quantified in Fig. 21. The x-axis represents the FDL techniques with their references and y-axis corresponds to the fault classification accuracy. The chart shown is specific to machine learning-based techniques as per the formula given above. The variation in classification accuracy is found to be from 94.82% to ~100%. The obtained classification metrics depend on many factors including the nature of faults, intensity of faults, acquired data, network parameters etc. It is observed that ANN-based approaches and deep learning-based approaches are highly accurate. However, they have their own merits and demerits and hence, a trade-off has to be made and proper FDL must be chosen depending upon the requirement of the considered applications.

5.4. Area under the curve (AUC)

One of the evaluation measures for machine learning based classification techniques is receiver operating characteristics (ROC). Fundamentally, ROC is a probability curve consisting of a graph between true positive rate (TPR) and false positive rate (FPR). The TPR and FPR are also diagnostic metrics usually represented through sensitivity/recall and specificity respectively. Sensitivity is defined as the ability to predict TP and similarly specificity is the ability to predict TN. Thus, TPR and FPR can be expressed as

$$TPR = Sensitivity \Big/ Recall = \frac{TP}{TP + FN}$$

$$FPR = 1 - Specificity = \frac{FP}{FP + TN}$$

When an ROC curve is plotted, y-axis is TPR and x-axis is FPR. The Area under ROC (AUC) defines the capability of a classification model to differentiate between multiple classes. For higher accuracy, AUC should be high; the closer AUC is to 1, the more accurate is the model. This can be understood through the ROC presented in Fig. 22 with AUC as 1,

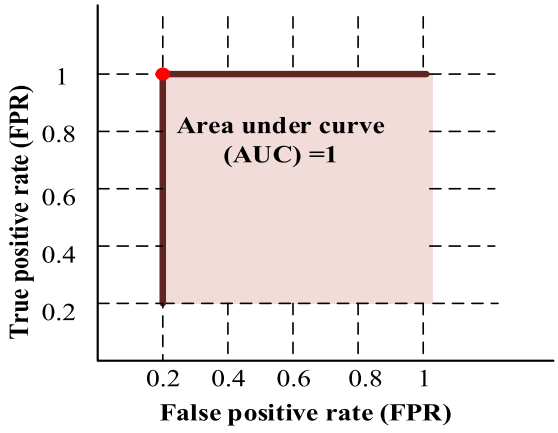


Fig. 22. ROC curve with area under the curve (AUC) as 1.

which indicates a very high accurate model (~100% accurate) [168]. Once the efficiency and robustness of an FDL using offline model is established, it is essential to determine the capability of the particular FDL technique to determine and verify the real time effectiveness. Various FDLs proposed in literature provide online or real-time validation using experiments as discussed in this paper. However, the generalization of the real-time aspect for other FDL applications is yet to be verified and there is lack of information with regards to failure cost analysis. There is a high scope of advancements in the field of fault diagnosis especially in case of GCPS applications. For future aspects, it is also recommended for incorporating performance parameters listed in this paper and thorough analysis on reliability and cost-effectiveness is also required.

6. Conclusion

This paper presents a review regarding the power modules faults, capacitor failures, and their root-cause analysis in GCPS. The root cause analysis including segregation of failure in appropriate categories for both switching devices and capacitors is investigated and detailed. Various FDL techniques for inverter and CM for capacitor faults are discussed meticulously and systematically. After an exhaustive study, it is established that majority of literature in the field of FDL methods consist of AI based techniques and most of them are particularly based

on supervised learning. Besides, it is identified that the unsupervised, semi-supervised, and reinforcement learning based FDL methods need further exploration and evaluation. The observations indicated that, all of the available approaches provide effective fault detection and subsequent protection of the converter. However, their relatively slow response time renders them inefficient in preventing the system from going into failure once the fault occurs. Further, techniques that are integrated into the inverter control unit cannot achieve fast fault detection, identify the fault type or the switch fault location within the desired time. In addition to the above, the appropriate FDL categories for both power modules and capacitors, with their utilization, merits, limitations, and other interpretations are compared thoroughly. From the challenges, it is observed that to improve the efficiency, and reliability of the power converters it is necessary to improve the performance of the fault classification techniques under noisy conditions. The future work is further motivated to include the inductance estimation in current emulators as a part of new fault detection approaches and improve the efficiency under high power operation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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