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A Double-PLLs-Based Impedance Reshaping Method for Extending Stability Range of Grid-Following Inverter Under Weak Grid

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***Abstract*- Conventional vector current control (VCC) scheme has been widely used in grid-connected inverter systems. However, it suffers from severe power limitation issues under weak grids. This paper reveals that the coupling effect between the power delivery and the voltage at the point of common coupling (PCC) causes the static power limit, which only depends on physical parameters of the system. When the stability of the control scheme is considered, negative resistance characteristics of the phase-locked loop (PLL) mainly result in the small-signal stability limit, which is called the dynamic power limit in this paper. Because the small-signal stability limit can be improved by using different control methods, it attracts lots of research attention. In this paper, a simplified *d-q* small-signal impedance model is introduced to show the destabilizing factors. Then, an initial small-signal impedance reshaping method is proposed to counteract the major destabilizing factor caused by the PLL. Based on the initial impedance reshaping method, an improved control scheme is proposed. Through exhaustive mathematical analysis, it is proved that the dynamic power limit can be extended almost to the static power limit by using this proposed method. Finally, simulation and experimental results verify the effectiveness of the proposed method.[1]**

***Index Terms*— grid-following inverter, vector current control, weak grid, small-signal stability range, impedance reshaping**

I. INTRODUCTION

In the past decades, due to the foreseen exhaustion of conventional fossil-based energies and their climate impact, many global efforts have been devoted to developing renewable energy sources, such as solar photovoltaic (PV) and wind [1]. Moreover, uneven distributions of solar and wind resources lead to their power plants usually being deployed in remote areas [2]. As a result, the power grid connected to renewable energy generation system is weaker than the conventional power grid due to the larger impedance of long-distance power transmission lines and the smaller short-circuit ratio (SCR) [3], [4]. At present, one of the main problems of the weak grid system is that the power transfer capability is limited because the larger transferred active power leads to the larger voltage drop on the transmission line. It finally causes severe voltage deviation at the point of common coupling (PCC) and some instability issues [5].

In fact, two aspects should be considered for such power limitation issues. When the mathematical model of the system is established based on the steady-state algebraic equations, the power limit only depends on the parameters of grid impedance. This power limit is named as "static power limit" in [6]. When the mathematical model of the system is established based on the dynamic differential equations, the control stability is considered. The small-signal stability boundary of the system can be estimated according to stability criteria in control theory, which depends on the specific control scheme. This small-signal stability boundary is called "dynamic power limit" in this paper. Because the static power limit is constant for an existing system and it is higher than the dynamic power limit, the main idea is to optimize the control scheme to extend the stability boundary and increase the dynamic power limit. Therefore, how to enlarge the stability range becomes a hot topic [7].

Although some researchers focus on the power synchronization based grid-forming control methods to enlarge the stability range [8], [9], the conventional phase-locked loop (PLL) based grid-following vector current control (VCC) method is still a mainstream method in real wind and PV generation systems at present. It attracts significant research attentions to revealing the instability mechanism and enhancing the stability of the system under weak grid conditions [10]-[16].

To study the instability mechanism of the grid-following inverter system, some scholars ignore the outer control loops and only take into account the inner control loops [17], while other scholars ignore the inner control loops and only consider the outer control loops [18]. However, to have more accurate stability analysis results, all the control loops should be considered. Recently, literature [19] introduces the bandwidth interactions of all control loops, but only two parameters are analyzed each time so that the overall relationship of the four

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parameters (namely the bandwidths of the current control loop, the PLL, the power control loop, and the AC voltage control loop) is still unclear.

Due to the complexity of the multiple-input multiple-output (MIMO) grid-following control system, it is difficult to directly observe the root cause of the instability issues. Proper simplification is necessary to highlight the main influential factors. In this paper, assuming that the inner current control loops are fast enough, a simplified *d*-*q* small-signal impedance model is firstly introduced, which highlights the influence of the PLL and the outer control loops. It clearly shows that there is an equivalent negative resistance on the *q*-*q* channel introduced by the PLL, which is a major destabilizing factor [20]-[22]. Besides, there are an equivalent negative inductance on the *q*-*d* channel introduced by the AC voltage loop and an equivalent negative resistance on the *d*-*q* channel introduced by the active power loop and the PLL, which may cause the coupling effect and instability [23]. Relatively, they are the secondary destabilizing factors. To extend the stability range as much as possible, both the major and secondary factors should be considered. According to the simplified *d*-*q* small-signal model, it is known that reducing the bandwidth of the AC voltage control loop can weaken the destabilizing factor on the *q*-*d* channel. And reducing the bandwidth of the active power control loop can weaken the destabilizing factor on the *d*-*q* channel. Similarly, reducing the bandwidth of the PLL can weaken the destabilizing factors on both *d*-*q* and *q*-*q* channels. Therefore, reducing the bandwidth is a simple solution to enhance the small-signal stability of the system [20]. However, when considering the dynamic performance of the PLL, its bandwidth cannot be designed too low [24]-[28]. For example, a higher PLL bandwidth is beneficial for the low voltage ride through (LVRT) [27], [28]. Thus, this solution needs a trade-off between system stability and dynamic performance.

To address the above problem, an alternative solution can be used, which is reshaping the converter output impedance via an additional supplementary control. This interesting idea is proposed by Alawasa *et al.* [24], where a band-pass filter is used. However, it is reported in [21] that this band-pass filter method cannot fully address the low-frequency instability issue caused by the PLL. Then, two impedance reshaping methods by adding the impedance controller on the *q*-*q* channel are proposed in [21] and [22]. However, the detailed stability boundary extensions of these two methods are not clear. Besides, the negative resistance on the *d*-*q* channel caused by the PLL is not addressed in [21] and [22]. It may exacerbate the coupling effect between the *d*-axis and *q*-axis, which may also cause instability. To solve the coupling effect, another SISO impedance reshaping method based on the symmetrical PLL is proposed in [23]. However, the symmetrical PLL uses a constant voltage magnitude reference, which may cause some control errors when the grid voltage magnitude is varying. Differently, this paper proposes an impedance reshaping method based on the classical PLL, and both negative resistances on *d*-*q* and *q*-*q* channels caused by the PLL are compensated. Moreover, the encountered integral problem during the impedance reshaping process is also a big hurdle to overcome, which is solved by using an auxiliary PLL without affecting the fundamental current control performance. Thus, the proposed improved control scheme based on the double PLLs is also suitable for the grid frequency variation, which can improve the system robustness under weak grid conditions. Furthermore, this paper introduces a standard small-signal stability evaluation method by comparing the dynamic power limit and the static power limit. According to this stability evaluation method, it is known that the stability range can be almost extended to the static power limit by using the proposed method.

Overall, the main contributions of this paper can be summarized as follows. 1) A stability boundary estimation method is introduced to quantitatively analyze the dynamic power limit of the system. 2) A standard small-signal stability evaluation method by comparing the dynamic power limit and the static power limit is introduced to evaluate the performance of control methods. 3) A simplified *d*-*q* small-signal impedance model is introduced to show the impact of different control loop bandwidths on stability. 4) An initial impedance reshaping method based on MIMO small-signal model is proposed to solve the destabilizing factors caused by the PLL on both *d*-*q* and *q*-*q* channels. To overcome the encountered integral problem during the impedance reshaping process, a double-PLLs-based improved control scheme is proposed, which is suitable for the grid frequency variation. This proposed method can extend the stability range almost to the static power limit even when the PLL bandwidth is high.

The rest of this paper is organized as follows. Section II introduces the study system and the classical VCC structure. Then the static power limit of the grid-connected inverter is investigated. Section III introduces a stability analysis method to estimate the stability boundary of the system. After that, a simplified model is introduced to highlight the destabilizing factors. Section IV introduces two basic ideas to enhance stability. Then, an initial small-signal impedance reshaping method and its final implementation method are proposed. In Section V, simulation and experimental results are given to verify the effectiveness of the proposed methods. Finally, this paper is concluded in Section VI.

II. Static Power Limit of Grid-connected Inverter

The schematic diagram of the classical VCC grid-following inverter system is presented in Fig. 1. A very weak grid condition with SCR=1 is used for all analyses in this paper. In Fig. 1, $V_g\angle\theta_g$ is the grid voltage, $V_o\angle\theta_o$ is the output voltage at the PCC, and $V_c\angle\theta_c$ is the converter voltage. R_g and L_g are Thevenin's equivalent grid resistance and inductance. Because the AC grid in this paper is considered as an infinite grid, the grid angular frequency ω is constant and equal to its nominal value ω_N. C_f is the output filter capacitance. L_f and R_f are the output filter inductance and resistance. In order to avoid low-frequency passive resonances on the AC side, the value of C_f should be very small. The control section shown in Fig. 1 includes a *d*-axis inner current control loop, a *q*-axis inner current control loop, an outer active power control loop, an

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outer AC voltage amplitude control loop, and a PLL. The control section is performed in the rotating *d-q* frame, which is synchronized to the voltage phase angle at the PCC obtained by the PLL. The AC voltage reference is 1 per unit (pu), which means $|V_o|=|V_g|$ in the steady-state.

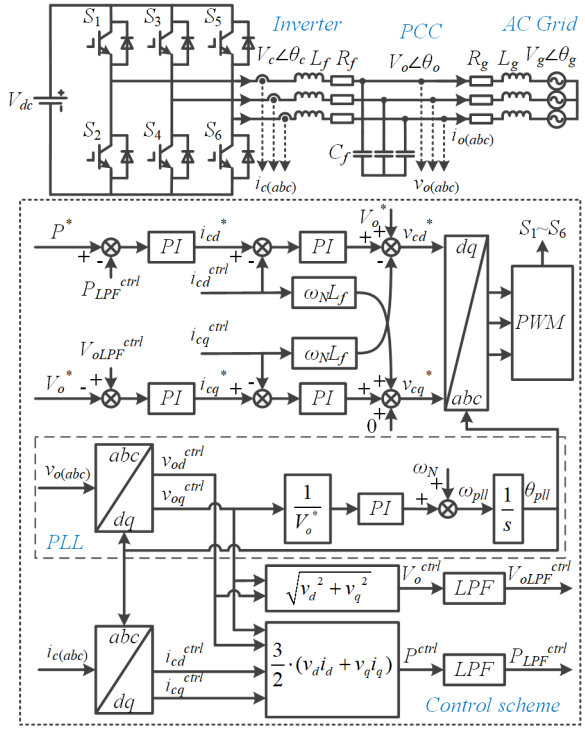

Fig. 1. Schematic diagram of classical VCC grid-following inverter system.

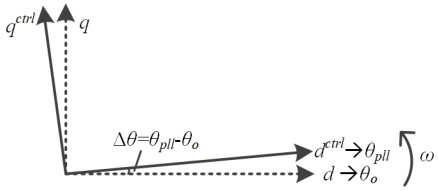

Fig. 2. Schematic diagram of the voltage-orientated *d-q* frames.

When considering the small-signal perturbation, there are two *d-q* frames [17], [20], namely the grid *d-q* frame and the control *d-q* frame, as shown in Fig. 2. The grid *d-q* frame is oriented to the phase angle of the PCC voltage θ_o, but θ_o is unknown. The PLL is used to estimate θ_o, and it outputs an angle θ_{pll}. Thus, the angle θ_{pll} can be used for control and the *d-q* control frame is oriented to θ_{pll}. However, there is a small error $\Delta\theta$ between θ_o and θ_{pll} in the dynamic state, namely $\theta_{pll} = \theta_o + \Delta\theta$. Thus, θ_o can be considered as the steady-state operating point of θ_{pll}, and $\Delta\theta$ can be considered as the small-signal perturbation. This concept is very important to derive the small-signal model in Section III. In the following sections, the superscript '*ctrl*' denotes the control frame variables. At first, the static power limit of the grid-connected inverter is analyzed as follows.

Ideally, the steady-state equivalent circuit of the grid-connected inverter system is shown in Fig. 3, and the voltage vector diagram at the *d-q* frame is shown in Fig.4. $V_o\angle 0$ is the PCC voltage at the *d-q* frame. $V_g\angle\varphi_g$ is the grid voltage at the *d-q* frame. The static power limit of the grid-connected inverter can be calculated based on the steady-state circuit.

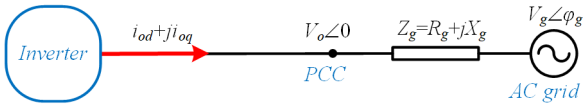

Fig. 3. Steady-state equivalent circuit of the grid-following inverter system.

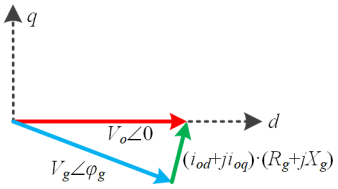

Fig. 4. Steady-state voltage vector diagram at the *d-q* frame.

According to the steady-state relationships of variables shown in Fig. 3 and Fig. 4, the steady-state expressions of the circuit are derived as (1).

$$\begin{cases} v_{od} - v_{gd} = R_g i_{od} - \omega L_g i_{oq} \\ v_{oq} - v_{gq} = R_g i_{oq} + \omega L_g i_{od} \end{cases} \tag{1}$$

Take "$v_{od}=V_o=V_g$, $v_{oq}=0$" and "$v_{gd}^2+v_{gq}^2=V_g^2$", then (1) is derived as (2).

$$(X_g^2 + R_g^2)(i_{od}^2 + i_{oq}^2) + 2V_g(X_g i_{oq} - R_g i_{od}) = 0 \tag{2}$$

The stiffness of the grid at the PCC can be described by the SCR, which is expressed as (3).

$$SCR = \frac{S_{SC}}{S_N} = \frac{3/2 \cdot V_g^2 / |Z_g|}{3/2 \cdot V_{pcc(rated)} \cdot I_{inv(rated)}} \tag{3}$$

where S_{SC} is the short-circuit apparent power of the grid at the PCC, S_N is the total rated apparent power of inverters, V_g is the amplitude of the grid voltage (phase to ground), $V_{pcc(rated)}$ and $I_{inv(rated)}$ are the amplitude of the rated PCC voltage (phase to ground) and rated inverter current.

Generally, the rated PCC voltage should be equal to the grid voltage, namely "$V_{pcc(rated)} = V_g$", and the rated current $I_{inv(rated)}$ is the same as the maximum inverter current $I_{o(max)}$, which is determined by hardware. Thus, $|Z_g|$ can be represented by the SCR, which is expressed as (4).

$$\sqrt{R_g^2 + X_g^2} = |Z_g| = \frac{V_g}{I_{o(max)} \cdot SCR} \tag{4}$$

Then, R_g and X_g can be derived as (5).

$$\begin{cases} X_g = \dfrac{V_g}{I_{o(max)} \cdot SCR} \cdot \dfrac{1}{\sqrt{(R_g / X_g)^2 + 1}} \\ R_g = \dfrac{V_g}{I_{o(max)} \cdot SCR} \cdot \dfrac{(R_g / X_g)}{\sqrt{(R_g / X_g)^2 + 1}} \end{cases} \tag{5}$$

Substituting (5) into (2), the pu value expression of i_{od} and i_{oq} can be derived as (6).

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$$i_{oq(pu)}{}^2+[\frac{2\cdot SCR}{\sqrt{(R_g/X_g)^2+1}}]\cdot i_{oq(pu)} +[i_{od(pu)}{}^2-\frac{2\cdot SCR\cdot(R_g/X_g)}{\sqrt{(R_g/X_g)^2+1}}\cdot i_{od(pu)}]=0 \quad (6)$$

Considering (6) as a quadratic equation of $i_{oq(pu)}$, thus only when (7) is satisfied, equation (6) has solutions.

$$\Delta=\frac{4\cdot SCR^2}{(R_g/X_g)^2+1}+\frac{8\cdot SCR\cdot R_g/X_g}{\sqrt{(R_g/X_g)^2+1}}\cdot i_{od(pu)}-4i_{od(pu)}{}^2\geq 0 \quad (7)$$

According to (7), the maximum value of $i_{od(pu)}$ can be calculated, as shown in (8). Because the PCC voltage is considered as a constant, the pu value of the current i_{od} is equal to the pu value of the active power P. Hence, the maximum power $P_{(pu)max}$ can also be represented by (8). Since the power at the PCC cannot be higher than $P_{(pu)max}$, $P_{(pu)max}$ is the static power limit of the grid-connected inverter [6].

$$P_{(pu)max}=i_{od(pu)max}=SCR\cdot[\frac{(R_g/X_g)}{\sqrt{(R_g/X_g)^2+1}}+1] \quad (8)$$

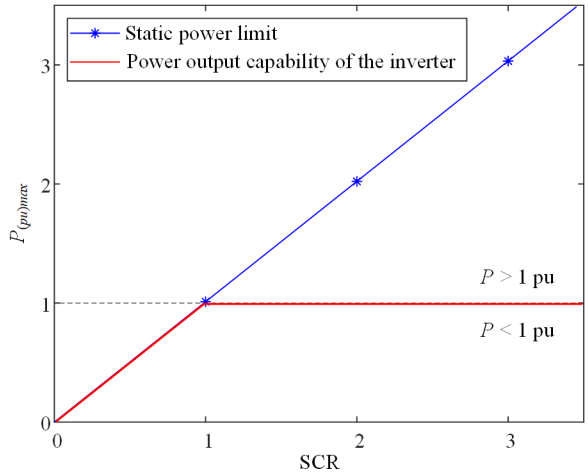

Fig. 5. Relationship between static power limit and SCR when $R_g/X_g = 0.01$.

According to (8), it can be seen that the static power limit $P_{(pu)max}$ is proportional to the SCR if the ratio R_g/X_g is given. Considering the grid impedance is usually inductive, the ratio $R_g/X_g = 0.01$ is used as an example for analysis in this paper. Thus, the relationship between the static power limit and the SCR is shown in Fig. 5. Notably, the ratio R_g/X_g can also be other values, such as 0.1 [15], 0.3 [20], etc, which depends on the power transmission systems in different cases. The analyses for other values of R_g/X_g are similar to the analysis for 0.01. Since the ratio R_g/X_g is not the study focus in this paper, the analyses for other values are omitted.

As shown in Fig. 5, the relationship of the static power limit $P_{(pu)max}$ and the SCR is linear. Generally, the rated power of the inverter is no more than 1 pu [29], so the power output capability of the inverter can be represented by the red line in Fig. 5. It can be seen that for a stronger grid, the static power limit is higher than 1 pu. Thus, it hardly ever influences the power output capability of the inverter. However, for a weaker grid (especially SCR≤1), the power output capability of the inverter is limited by the static power limit [30]. This is due to the coupling effect of the power delivery and the voltage at the PCC caused by the grid impedance. Moreover, when the dynamic power limit related to the small-signal stability is considered, the situation is even worse, which will be analyzed in the next section.

III. Small-Signal Stability Boundary Estimation

To analyze the stability of the nonlinear system introduced in Section II, the small-signal model is an effective tool. The system can be linearized by adding a small-signal perturbation near a steady-state operating point [20]. Then, it is convenient to use the linear analysis method to study stability issues. In this section, the subscript '$_0$' denotes a steady-state operating point. The symbol 'Δ' denotes a small-signal perturbation.

A. Small-signal stability boundary estimation

The detailed derivation of the small-signal expressions are omitted in this paper, because they have been presented in [31]. The small-signal control structure of the classical grid-following control system can be described in Fig. 6. The transfer function matrices are represented in (9).

$$\begin{cases}
\mathbf{B_{Lg}}=\begin{bmatrix} sL_g+R_g & -\omega L_g \\ \omega L_g & sL_g+R_g \end{bmatrix},\mathbf{B_{Cf}}=\begin{bmatrix} sC_f & -\omega C_f \\ \omega C_f & sC_f \end{bmatrix},\\
\mathbf{B_{Lf}}=\begin{bmatrix} sL_f+R_f & -\omega L_f \\ \omega L_f & sL_f+R_f \end{bmatrix},\mathbf{B_{decpl}}=\begin{bmatrix} 0 & -\omega L_f \\ \omega L_f & 0 \end{bmatrix},\\
\mathbf{B_{PI\text{-}PV}}=\begin{bmatrix} G_{pi_P} & 0 \\ 0 & -G_{pi_V} \end{bmatrix},\mathbf{B_{PI\text{-}I}}=\begin{bmatrix} G_{pi_I} & 0 \\ 0 & G_{pi_I} \end{bmatrix},\\
\mathbf{B_{LPF}}=\begin{bmatrix} G_{LPF} & 0 \\ 0 & G_{LPF} \end{bmatrix},\mathbf{B_{pll\text{-}Vc}}=\begin{bmatrix} 0 & -v_{cq0}/V_o\cdot G_{pll} \\ 0 & v_{cd0}/V_o\cdot G_{pll} \end{bmatrix},\\
\mathbf{B_v}=\begin{bmatrix} 3/2\cdot V_o & 0 \\ 0 & 0 \end{bmatrix},\mathbf{B_{pll\text{-}Ic}}=\begin{bmatrix} 0 & -i_{cq0}/V_o\cdot G_{pll} \\ 0 & i_{cd0}/V_o\cdot G_{pll} \end{bmatrix},\\
\mathbf{B_i}=\begin{bmatrix} 3/2\cdot i_{cd0} & 3/2\cdot i_{cq0} \\ 1 & 0 \end{bmatrix},\mathbf{B_{pll\text{-}Vo}}=\begin{bmatrix} 0 & 0 \\ 0 & G_{pll} \end{bmatrix}
\end{cases} \quad (9)$$

where $G_{pi\_P} = K_{p\_P}+K_{i\_P}/s$, $G_{pi\_V} = K_{p\_V}+K_{i\_V}/s$, $G_{pi\_I} = K_{p\_I}+K_{i\_I}/s$, and $G_{LPF} = \omega_{LPF}/(s+\omega_{LPF})$.

As shown in Fig. 6, the small-signal grid-following control system can be represented by a Norton-Thevenin equivalent model. The whole system can be divided into two parts. The converter-side part is represented by a current source with an output admittance $\mathbf{Y}(s)$, while the grid-side part is modeled by a voltage source in series with an impedance $\mathbf{Z_g}(s)$. This leads to (10) for the converter output current. Thus, $\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)$ can be used for stability analysis [19].

$$\mathbf{\Delta i_{cdq}}=[\mathbf{\Delta i_{sdq}}-\mathbf{Y}(s)\cdot\mathbf{\Delta v_{gdq}}]\cdot\frac{1}{\mathbf{I}+\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)} \quad (10)$$

Based on the control structure in Fig. 6, considering $\mathbf{\Delta i_{cdq}}$ as input and $\mathbf{\Delta v_{odq}}$ as output for the grid-side subsystem, the equivalent impedance $\mathbf{Z_g}(s)$ can be derived as (11). When the capacitance C_f is very small, $\mathbf{B_{Cf}}$ in (11) can be ignored.

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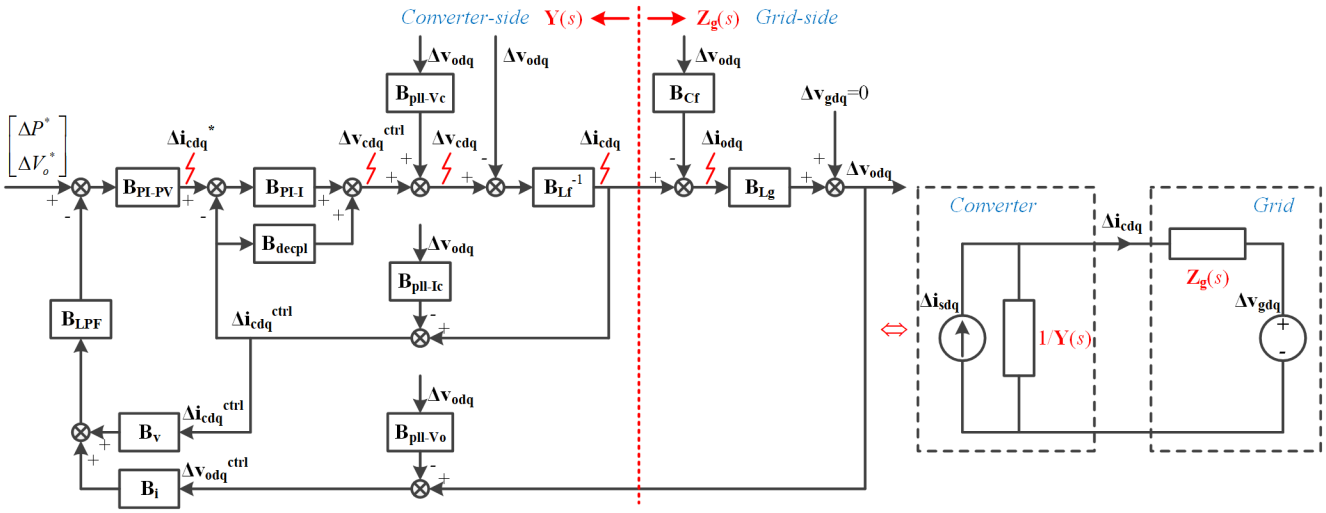

Fig. 6. Small-signal control structure and equivalent impedance circuit of the classical grid-following inverter system.

$$\mathbf{Z}_g(s) = (\mathbf{B}_{Lg}^{-1} + \mathbf{B}_{Cf})^{-1} \approx \mathbf{B}_{Lg} \tag{11}$$

Similarly, considering $\mathbf{\Delta v_{odq}}$ as input and $\mathbf{-\Delta i_{cdq}}$ as output for the converter-side subsystem, the equivalent admittance $\mathbf{Y}(s)$ can be derived as (12).

$$\begin{aligned}\mathbf{Y}(s) = &[\mathbf{B}_{Lf} + \mathbf{B}_{PI\text{-}I} - \mathbf{B}_{decpl} + \mathbf{B}_{PI\text{-}I}\mathbf{B}_{PI\text{-}PV}\mathbf{B}_{LPF}\mathbf{B}_v]^{-1} \cdot \\ &[\mathbf{I} - (\mathbf{B}_{PI\text{-}I} - \mathbf{B}_{decpl} + \mathbf{B}_{PI\text{-}I}\mathbf{B}_{PI\text{-}PV}\mathbf{B}_{LPF}\mathbf{B}_v)\cdot\mathbf{B}_{pll\text{-}Ic} \\ &-\mathbf{B}_{pll\text{-}Vc} + \mathbf{B}_{PI\text{-}I}\mathbf{B}_{PI\text{-}PV}\mathbf{B}_{LPF}\mathbf{B}_i \cdot (\mathbf{I} - \mathbf{B}_{pll\text{-}Vo})]\end{aligned} \tag{12}$$

Take $G_{pi\_I} = \omega_i L_f + \omega_i R_f/s$ for the current control loops, $G_{pi\_P} = \omega_p \cdot 1/(1.5V_o) \cdot (1/\omega_{LPF} + 1/s)$ for the power control loop and $G_{pi\_V} = \omega_v \cdot I_{max}/V_o \cdot (1/\omega_{LPF} + 1/s)$ for the voltage amplitude control loop. Then, (12) can be derived as (13). The parameter ω_i is the designed bandwidth of the current loop, ω_p is the designed bandwidth of the power loop, and ω_v is the designed bandwidth of the AC voltage loop.

Notably, G_{pll} in (13) is the closed-loop transfer function of the small-signal model of the PLL, which is a second-order system. The parameters ζ and ω_n in the G_{pll} are the damping ratio and natural angular frequency of this second-order system. Although the actual bandwidth of the PLL is hard to know, it is approximately equal to the bandwidth of the G_{pll} [28], which is proportional to ω_n if ζ is given. It is reported in [28] that when considering the requirement of the LVRT, a typical range of the PLL bandwidth is 20~40 Hz for renewable energy conversion systems. In following sections, several PLL bandwidths from 0.8 Hz ($\zeta = 1$, $\omega_n = 2$ rad/s) to 80 Hz ($\zeta = 1$, $\omega_n = 200$ rad/s) will be analyzed and compared.

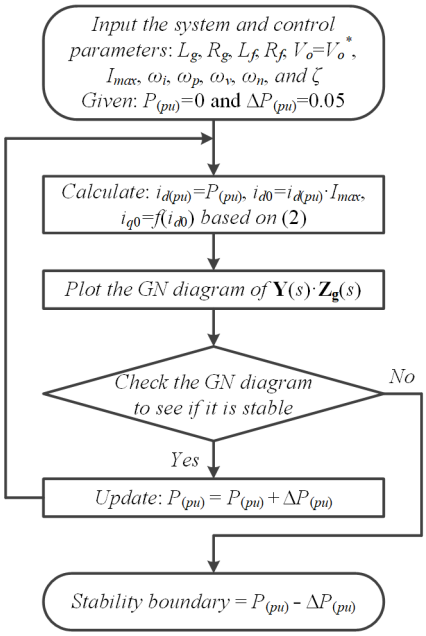

Fig. 7. Flow chart of finding the stability boundary of the system.

$$\mathbf{Y}(s) = \begin{bmatrix} \dfrac{\dfrac{1}{sL_f + R_f}\cdot\dfrac{s}{s+\omega_i} + \dfrac{i_{cd0}}{V_o}\cdot\dfrac{\omega_p}{s}\cdot\dfrac{\omega_i}{s+\omega_i}}{1 + \dfrac{\omega_p}{s}\cdot\dfrac{\omega_i}{s+\omega_i}} & \dfrac{\dfrac{i_{cq0}}{V_o}\cdot\dfrac{[(sL_f+R_f)\omega_i + sR_f]\cdot G_{pll}}{(sL_f+R_f)(s+\omega_i)} + \dfrac{i_{cq0}}{V_o}\cdot\dfrac{\omega_p}{s}\cdot\dfrac{\omega_i}{s+\omega_i}}{1 + \dfrac{\omega_p}{s}\cdot\dfrac{\omega_i}{s+\omega_i}} \\ \dfrac{-I_{max}}{V_o}\cdot\dfrac{\omega_v}{s}\cdot\dfrac{\omega_i}{s+\omega_i} & \dfrac{(1-G_{pll})}{sL_f+R_f}\cdot\dfrac{s}{s+\omega_i} - \dfrac{i_{cd0}}{V_o}\cdot\dfrac{[(sL_f+R_f)\omega_i + sR_f]\cdot G_{pll}}{(sL_f+R_f)(s+\omega_i)} \end{bmatrix} \tag{13}$$

where $G_{pll} = (2\zeta\omega_n s + \omega_n^2)/(s^2 + 2\zeta\omega_n s + \omega_n^2)$.

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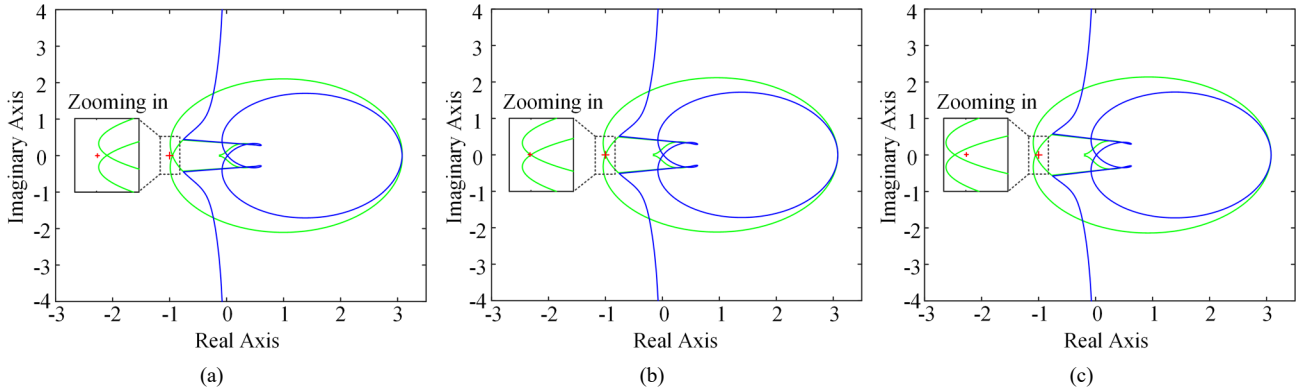

Fig. 8. Generalized Nyquist diagrams of $\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)$ with SCR=1. (a) $P_{(pu)}$ = 0.5. (b) $P_{(pu)}$ = 0.55. (c) $P_{(pu)}$ = 0.6.

TABLE I
PARAMETERS OF GRID-CONNECTED SYSTEM

	Parameters	Values
V_g	Grid phase voltage, peak value	50 V (1 pu)
f_g	Grid frequency	50 Hz (1 pu)
P_n	Rated active power (3 phase)	800 W (1 pu)
S_n	Rated apparent power (3 phase)	800 VA (1 pu)
I_{max}	Rated current, peak value	10.7 A (1 pu)
V_{dc}	Input DC voltage	600 V
f_{sw}	Switching frequency	10 kHz
L_f	Output filter inductance	5 mH (0.33 pu)
R_f	Output filter resistance	16 mΩ
C_f	Output filter capacitance	10 μF (0.015 pu)
SCR	Short-circuit ratio	1
R_g/X_g	R/X ratio of grid impedance	0.01
L_g	Grid inductance	15 mH (1 pu)
R_g	Grid resistance	48 mΩ (0.01 pu)

TABLE II
PARAMETERS OF CONTROL LOOPS

	Parameters	Values
V_o^*	Reference value of the output voltage	50 V (1 pu)
ω_i	Designed bandwidth of the inner current loops	1000 rad/s
ω_v	Designed bandwidth of the AC voltage loop	50 rad/s
ω_p	Designed bandwidth of the active power loop	10 rad/s
ω_{LPF}	Cut-off angular frequency of the LPFs	200 rad/s
ζ	Damping ratio of the PLL	1
ω_n	Natural angular frequency of the PLL	200 rad/s

Given a steady-state operating point and parameters of the control loops, a frequency-domain matrix $\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)$ is determined. Then, the generalized Nyquist (GN) diagrams can be plotted to analyze the stability of the system. Thus, given different steady-state operating points, the stability boundary can be found accordingly. The flow chart of finding the stability boundary is shown in Fig. 7.

The parameters of the system and the control loops are shown in Table I and Table II respectively. As shown in Fig. 7, the following steps can be used to find the stability boundary of the system. Step 1: Input all system and control parameters. Give initial value $P_{(pu)}$=0 and the step length $\Delta P_{(pu)}$=0.05. Step 2: Calculate the steady-state values i_{d0} and i_{q0}. Step 3: Plot the GN diagram of $\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)$ according to (11) and (13). Step 4: Check the GN diagram to see if the system is stable. If it is stable, increase a step length for $P_{(pu)}$ and return to Step 1. If not, the stability boundary can be found, which is $P_{(pu)}$-$\Delta P_{(pu)}$.

When the SCR is 1, given different steady-state operating points, the generalized Nyquist diagrams of the matrix $\mathbf{Y}(s)\cdot\mathbf{Z_g}(s)$ are plotted in Fig. 8 (a), (b), and (c) respectively. It can be seen that the point (-1, j0) is outside the generalized Nyquist envelope curves in Fig. 8(a), which means that the system is stable when active power is 0.5 pu. However, the point (-1, j0) is inside the generalized Nyquist envelope curves in Fig. 8(c), which means that the system is unstable when the active power is 0.6 pu. Therefore, the critical stable point is between 0.5 pu and 0.6 pu. As shown in Fig. 8(b), when the point (-1, j0) is on the generalized Nyquist envelope curves, the stability boundary is found, which is 0.55 pu. By using the same method, the stability boundary of the system with SCR=2 can also be found, which is 1.65 pu. Similarly, the stability boundary of the system with SCR=3 is 2.75 pu.

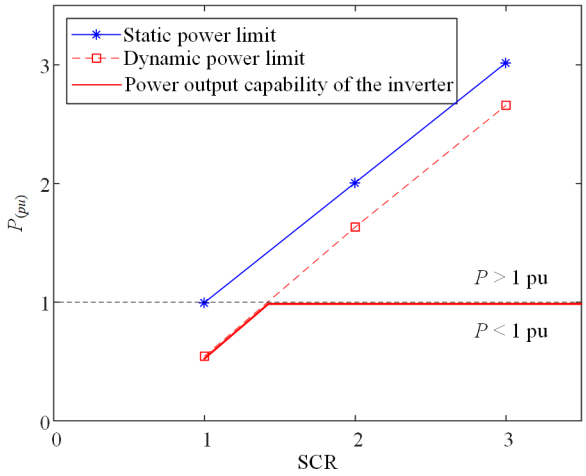

Fig. 9. Relationship between the dynamic power limit and the SCR.

According to the stability analysis results above, the relationship between the dynamic power limit (stability boundary) and the SCR is shown in Fig. 9, where the static power limit is added for comparison. It can be seen that the dynamic power limit is lower than the static power limit. Thus, the power output capability of the inverter is limited by the dynamic power limit that is related to the control scheme. It is notable that although the stability analysis results in Fig. 9 are

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based on the parameters of an 800 W inverter in Table I, the stability analysis results of other power level inverters are basically same as Fig. 9, because the power shown in Fig. 9 is in pu value. Besides, the case of parameters mismatch is not considered in this paper. Then, the destabilizing factors of the system will be analyzed in the next subsection.

B. Simplified model for observing the destabilizing factors

To have a deeper insight into the instability mechanism of this complicated MIMO system, proper assumptions and simplifications are necessary to do. Assume the bandwidth of inner current control loop is infinite (namely $\omega_i \approx +\infty$ and $\omega_i/(s+\omega_i) \approx 1$) and the filter resistance is ignored ($R_f \approx 0$), then (13) can be simplified as (14).

$$\mathbf{Y}(s) \approx \begin{bmatrix} \dfrac{(1-G_p)}{sL_f+\omega_i L_f}+\dfrac{G_p}{R_d} & \dfrac{G_p+(1-G_p)\cdot G_{pll}}{-R_q} \\ \dfrac{\omega_v}{-sX_m} & \dfrac{(1-G_{pll})}{sL_f+\omega_i L_f}+\dfrac{G_{pll}}{-R_d} \end{bmatrix} \tag{14}$$

where $G_p = \omega_p/(s+\omega_p)$, $R_d = V_o/i_{cd0} > 0$, $R_q = V_o/(-i_{cq0}) > 0$, $X_m = V_o/I_{max} > 0$.

Although it is still hard to see the destabilizing factors in (14), the earlier study experience tells that lower bandwidths of the PLL, the active power loop, and the AC voltage loop are beneficial for stability. Therefore, assume $\omega_n = 0$, $\omega_p = 0$, and $\omega_v = 0$, then (14) is derived as (15).

$$\mathbf{Y}_{\mathbf{ideal}}(s) = \begin{bmatrix} \dfrac{1}{sL_f+\omega_i L_f} & 0 \\ 0 & \dfrac{1}{sL_f+\omega_i L_f} \end{bmatrix} \tag{15}$$

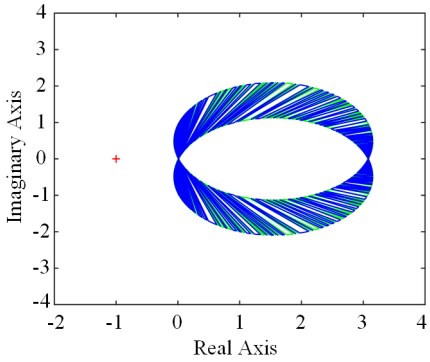

Fig. 10. Generalized Nyquist diagram of $\mathbf{Y}_{\mathbf{ideal}}(s)\cdot\mathbf{Z}_{\mathbf{g}}(s)$ with SCR=1.

The Generalized Nyquist diagram of matrix $\mathbf{Y}_{\mathbf{ideal}}(s)\cdot\mathbf{Z}_{\mathbf{g}}(s)$ are plotted in Fig. 10. It can be seen that the stability performance of this ideal case is very good because it has much stability margin. Besides, the matrix $\mathbf{Y}_{\mathbf{ideal}}(s)$ is not influenced by the steady-state operating points, which means it is a global stable system. So if the admittance matrix $\mathbf{Y}(s)$ in (14) can be modified like $\mathbf{Y}_{\mathbf{ideal}}(s)$ in (15), the stability range must be enlarged a lot. This is the basic idea for the following sections in this paper.

Comparing (14) with (15), it can be seen that there is a negative resistance term $G_{pll}/(-R_d)$ on the *q-q* channel. As i_{cd0} increases, G_{pll}/R_d increases, which will aggravate the influence of the negative resistance. As ω_n decreases, G_{pll}/R_d decreases, which will weaken the influence of the negative resistance. In addition, there is a negative resistance $[(1-G_p)G_{pll}+G_p]/(-R_q)$ on the *d-q* channel. As ω_n and ω_p decrease, $[(1-G_p)G_{pll}+G_p]/R_q$ decreases, which will weaken the influence of the negative resistance. Moreover, there is a negative inductance $\omega_v/(-sX_m)$ on the *q-d* channel. As ω_v decreases, $\omega_v/(sX_m)$ decreases, which will weaken the influence of the negative inductance.

Therefore, to weaken the influence of the *d-q* negative resistance, ω_p should be designed to be very small [18], [19], such as 5~20 rad/s. To weaken the influence of the *q-d* negative inductance, ω_v should be designed to be very small but larger than ω_p [18], [19], such as 20~50 rad/s. Similarly, reducing the PLL bandwidth can weaken the influence of the *q-q* and *d-q* negative resistances. However, if the PLL bandwidth is designed too low, the dynamic performance of the PLL will be worsened a lot, which is difficult to meet the requirement of the LVRT [27], [28]. Thus, this solution needs a trade-off between the system stability and the dynamic performance. To overcome this problem, an alternative solution by reshaping the converter output impedance is a good choice [21], [24].

IV. Stability Enhancement Methods

A. Reducing the bandwidth of the PLL

As aforementioned, reducing the PLL bandwidth by reducing ω_n can weaken the influence of the negative resistances caused by the PLL. The relationship of the dynamic power limits and the SCR with different PLL bandwidths are shown in Fig. 11. It can be seen that as the PLL bandwidth (proportional to ω_n) decreases, the dynamic power limit increases. When $\omega_n = 2$ rad/s, the dynamic power limit is very close to the static power limit. So the power output capability of the inverter can be improved in this way.

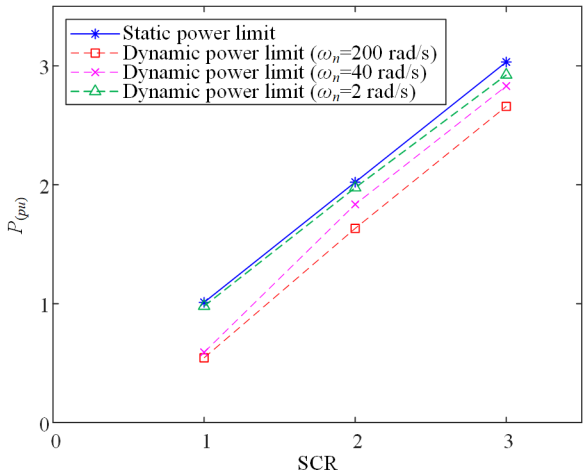

Fig. 11. Relationship of the dynamic power limits and the SCR with different PLL bandwidths.

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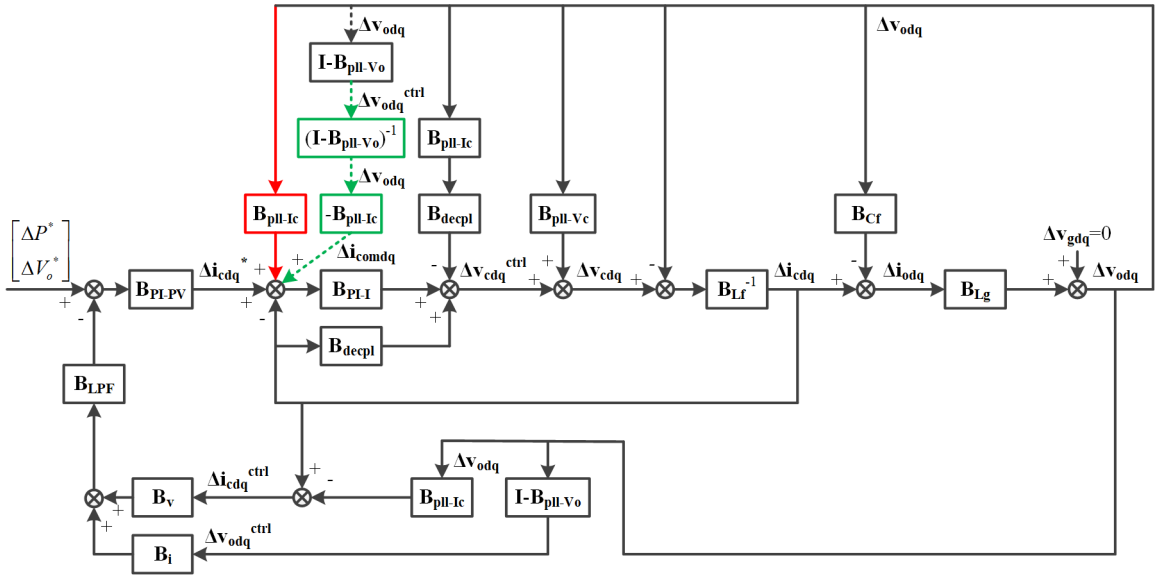

Fig. 12. Small-signal control structure with expected reshaped impedance.

B. Proposed impedance reshaping method

Although reducing PLL bandwidth can enhance the stability, the dynamic performance of the PLL is worsened. Aiming at this problem, an initial impedance reshaping method is proposed in this paper, which will be introduced in this subsection.

The small-signal control structure in Fig. 6 can also be represented by the equivalent control structure in Fig. 12. The positive feedback caused by the PLL can be observed, which is marked in red in Fig. 12. Moreover, it can be seen from the matrix $\mathbf{B}_{\text{pll-Ic}}$ in (9), both the *d-q* and *q-q* elements are positive ($i_{cd0}>0$ and $i_{cq0}<0$ for the inductive grid impedance [29]), so both the positive feedback on *d-q* and *q-q* channels caused by $\mathbf{B}_{\text{pll-Ic}}$ in Fig. 12 should be counteracted.

To counteract the positive feedback in the control loop, additional negative feedback is expected to be added, which is marked by the dotted line in Fig. 12. To implement this idea in the control scheme, some actual situations should be considered. Because the voltage v_{odq}^{ctrl} can be measured rather than v_{odq}, the added transfer function is modified from the voltage $\mathbf{\Delta v_{odq}^{ctrl}}$ as input to the compensating current $\mathbf{\Delta i_{comdq}}$ as output, which is marked in green in Fig. 12. The equation of compensating current $\mathbf{\Delta i_{comdq}}$ is given by (16).

$$\begin{bmatrix}\Delta i_{comd}\\ \Delta i_{comq}\end{bmatrix}=-\mathbf{B}_{\text{pll-Ic}}\cdot(\mathbf{I}-\mathbf{B}_{\text{pll-Vo}})^{-1}\cdot\begin{bmatrix}\Delta v_{od}^{\ ctrl}\\ \Delta v_{oq}^{\ ctrl}\end{bmatrix} \tag{16}$$

Substituting (9) into (16), it is derived as (17).

$$\begin{bmatrix}\Delta i_{comd}\\ \Delta i_{comq}\end{bmatrix}=\begin{bmatrix}i_{cq0}\cdot\dfrac{\Delta v_{oq}^{\ ctrl}}{V_o}\cdot\dfrac{G_{pll}}{1-G_{pll}}\\ -i_{cd0}\cdot\dfrac{\Delta v_{oq}^{\ ctrl}}{V_o}\cdot\dfrac{G_{pll}}{1-G_{pll}}\end{bmatrix} \tag{17}$$

Substituting G_{pll} into (17), it is derived as (18).

$$\begin{bmatrix}\Delta i_{comd}\\ \Delta i_{comq}\end{bmatrix}=\frac{\Delta v_{oq}^{\ ctrl}}{V_o}\cdot\left(K_{p\_pll}+\frac{K_{i\_pll}}{s}\right)\cdot\frac{1}{s}\cdot\begin{bmatrix}i_{cq0}\\ -i_{cd0}\end{bmatrix} \tag{18}$$

C. Proposed initial improved control scheme

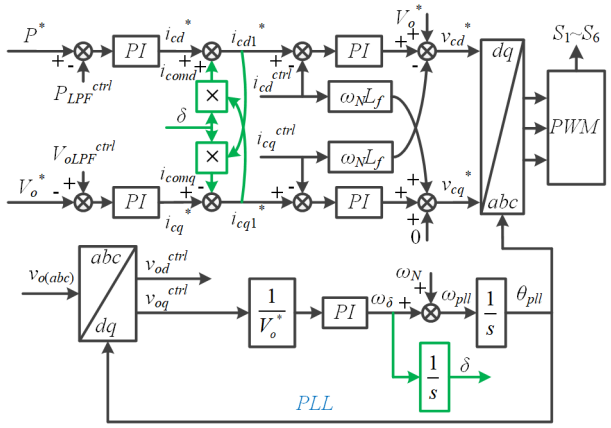

Fig. 13. Proposed initial improved control scheme.

Although an initial impedance reshaping method can be found based on the small-signal model in Fig. 12, it needs to be redesigned for implementation in the control scheme. In Fig. 13, the current reference values in the control scheme are used to represent the steady-state value i_{cd0} and i_{cq0} in (18). Thus, according to the small-signal equation (18), an initial improved control scheme is presented in Fig. 13. The main difference between the proposed control scheme and the classical control scheme is marked in green in Fig. 13. An integral term and two current compensation terms i_{comd} and i_{comq} are added, so that the current reference is modified from $i_{cdq}^{\ *}$ to $i_{cdq1}^{\ *}$.

The small-signal model is established again to analyze the stability of the proposed improved control scheme. Thus, the original simplified admittance matrix $\mathbf{Y}(s)$ in (14) is reshaped as $\mathbf{Y_r}(s)$ in (19). The new variable δ_0 in (19) represents the steady-state value of the variable δ.

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$$\mathbf{Y}_\mathbf{r}(s) \approx \begin{bmatrix} \dfrac{(1-G_{p(\delta)})}{sL_f+\omega_i L_f}+\dfrac{G_{p(\delta)}}{R_d}+\dfrac{\delta_0 G_{p(\delta)}}{-X_m\cdot\omega_p/\omega_v} & \dfrac{G_{p(\delta)}}{-R_q}+\dfrac{\delta_0^{\,2}(1-G_{p(\delta)})\cdot G_{pll}}{-R_q(1+\delta_0^{\,2})}+\dfrac{\delta_0(1-G_{p(\delta)})\cdot G_{pll}}{R_d(1+\delta_0^{\,2})} \\ \dfrac{(1+\delta_0^{\,2}G_{p(\delta)})\cdot\omega_v}{-sX_m(1+\delta_0^{\,2})}+\dfrac{\delta_0 G_{p(\delta)}}{-R_d}+\dfrac{\delta_0 G_{p(\delta)}}{sL_f+\omega_i L_f} & \dfrac{(1-G_{pll})}{sL_f+\omega_i L_f}+\dfrac{\delta_0[(G_{p(\delta)}-G_{pll})+\delta_0^{\,2}G_{p(\delta)}(1-G_{pll})]}{R_q(1+\delta_0^{\,2})}+\dfrac{\delta_0^{\,2}(1-G_{p(\delta)})\cdot G_{pll}}{-R_d(1+\delta_0^{\,2})} \end{bmatrix} \quad (19)$$

where $G_{p(\delta)} = \omega_{p(\delta)}/(s+\omega_{p(\delta)})$, $\omega_{p(\delta)} = \omega_p/(1+\delta_0^2)$.

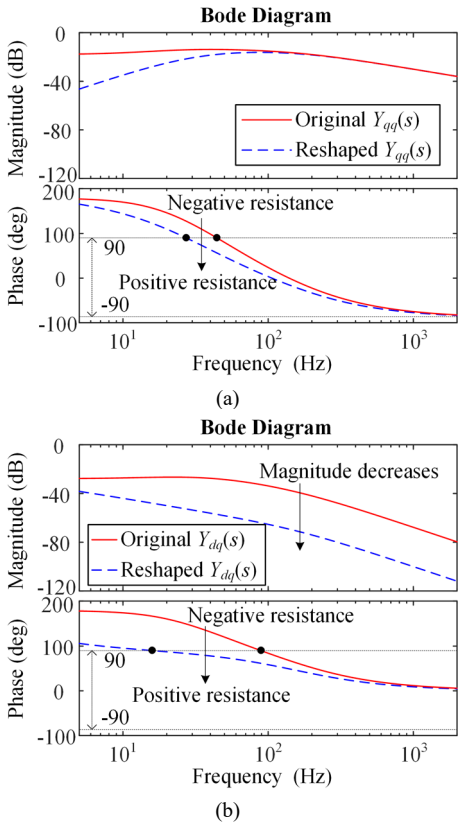

Fig. 14. Impedance characteristics of original and reshaped $Y_{qq}(s)$ and $Y_{dq}(s)$ when SCR = 1 and P = 0.6 pu. (a) $Y_{qq}(s)$. (b) $Y_{dq}(s)$.

By using the parameters in Table I and Table II, the impedance characteristics of the original $Y_{qq}(s)$ and $Y_{dq}(s)$ in (13) and the reshaped $Y_{qq}(s)$ and $Y_{dq}(s)$ are compared in Fig. 14 when the steady-state active power is 0.6 pu. It can be seen that the $Y_{qq}(s)$ is reshaped from the negative resistance characteristic to the positive resistance characteristic within the frequency range [27 Hz, 44 Hz]. Besides, the $Y_{dq}(s)$ is reshaped from the negative resistance characteristic to the positive resistance characteristic within the frequency range [16 Hz, 89 Hz]. Moreover, the magnitude of $Y_{dq}(s)$ is reduced, so the coupling effect between the *d*-axis and *q*-axis can be weakened.

Moreover, to see the effect of the proposed control scheme on stability, the generalized Nyquist criterion is used again. When the SCR is equal to 1, given the active power equal to 0.6 pu and 0.9 pu as the steady-state operating points, the generalized Nyquist curves of matrix $\mathbf{Y_r}(s)\cdot\mathbf{Z_g}(s)$ are plotted in Fig. 15(a) and Fig. 15(b) respectively. Comparing Fig. 15(a) with Fig. 8(c), it can be seen that when the steady-state power is 0.6 pu, the original unstable system is changed to be a stable system by using the proposed method. Furthermore, as seen in Fig. 15(b), the system is still stable when the steady-state power is 0.9 pu. Hence, the stability range is improved a lot by using the proposed method.

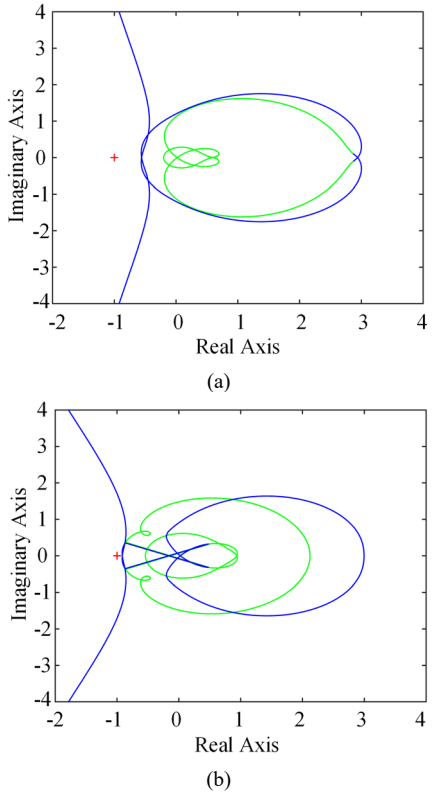

Fig. 15. Generalized Nyquist diagrams of $\mathbf{Y_r}(s)\cdot\mathbf{Z_g}(s)$ with SCR=1. (a) $P_{(pu)}$ = 0.6. (b) $P_{(pu)}$ = 0.9.

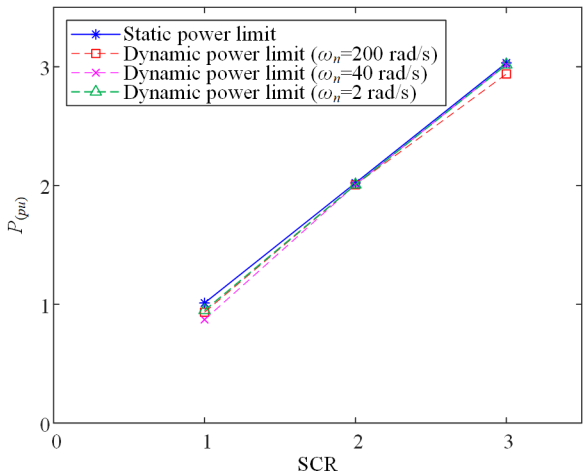

Fig. 16. Relationship of the dynamic power limits and SCR with different PLL bandwidths by using the proposed initial improved control scheme.

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According to the stability analysis results of $\mathbf{Y_r}(s)\cdot\mathbf{Z_g}(s)$ with different parameters, the relationship of the dynamic power limits and the SCR with different PLL bandwidths by using the proposed initial improved control scheme are shown in Fig. 16. It can be seen that the PLL bandwidth (proportional to ω_n) scarcely influences the dynamic power limit. All the dynamic power limits are very close to the static power limit. As a result, the power output capability of the inverter is improved.

Although the proposed initial improved control scheme can extend the stability range of the system, it only works under the ideal condition that the grid angular frequency ω is constant and always equal to its nominal value ω_N. However, this ideal condition is not satisfied in the real world. When ω is not equal to ω_N, ω_{pll} is not equal to ω_N in the steady-state. Thus, ω_δ is not equal to 0 in the steady-state. If ω_δ is larger than 0, the variable δ will continue to increase due to the integrator. Similarly, if ω_δ is smaller than 0, δ will continue to decrease. Finally, the system will be out of control. Hence, this method cannot be used in real applications. To solve this problem, an alternative practical improved control scheme is proposed, which will be introduced in the next subsection.

D. Proposed practical improved control scheme

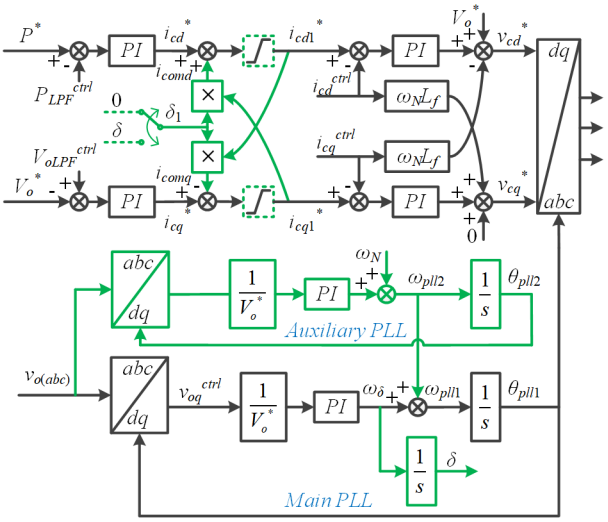

Fig. 17. Proposed practical improved control scheme.

To make the proposed control scheme adaptable to the grid frequency variation, another auxiliary PLL is added to calculate the frequency feedforward term instead of using a constant value. Thus, the proposed practical improved control scheme is shown in Fig. 17. The main purpose to add an auxiliary PLL is to make the frequency feedforward term equal to grid angular frequency ω in the steady-state (namely, $\omega_{pll2}=\omega$). Thus, in the steady-state, $\omega_{pll1}=\omega=\omega_{pll2}$ and $\omega_\delta=0$, so that δ is a constant. Therefore, the auxiliary PLL bandwidth should be much smaller than the main PLL bandwidth so that ω_{n2} of the auxiliary PLL should be designed much smaller than ω_{n1} of the main PLL, such as $1/10\cdot\omega_{n1}$.

Notably, the current compensation terms i_{comd} and i_{comq} should be disabled in the initial start-up process to avoid wrong compensation. Thus, the variable δ_1 is given 0 in the initial start-up process. When the initial start-up process is finished and the converter is ready to receive the power reference, the current compensation terms can be enabled. Namely, the switch of δ_1 can be changed from 0 to δ. Moreover, because the current reference is modified from i_{cdq}^* to i_{cdq1}^* by using the proposed control method, two new current limiters are also added in Fig. 17 for overcurrent protection.

It is worth mentioning that this proposed method is just an improved scheme based on the conventional VCC scheme with PLL shown in Fig. 1 so that it is possible to be applied in any grid-following converters. Namely, it is suitable for the PV inverter [5], the back-to-back converter in the wind energy conversion systems [18], the back-to-back converter in high voltage direct current (HVDC) transmission systems [32], etc. Moreover, although this paper mainly focuses on the power outer loop control, the proposed method is also suitable for the dc voltage outer loop control introduced in [18] and [32].

V. Simulation and Experimental Verification

A. Simulation verification of the stability ranges

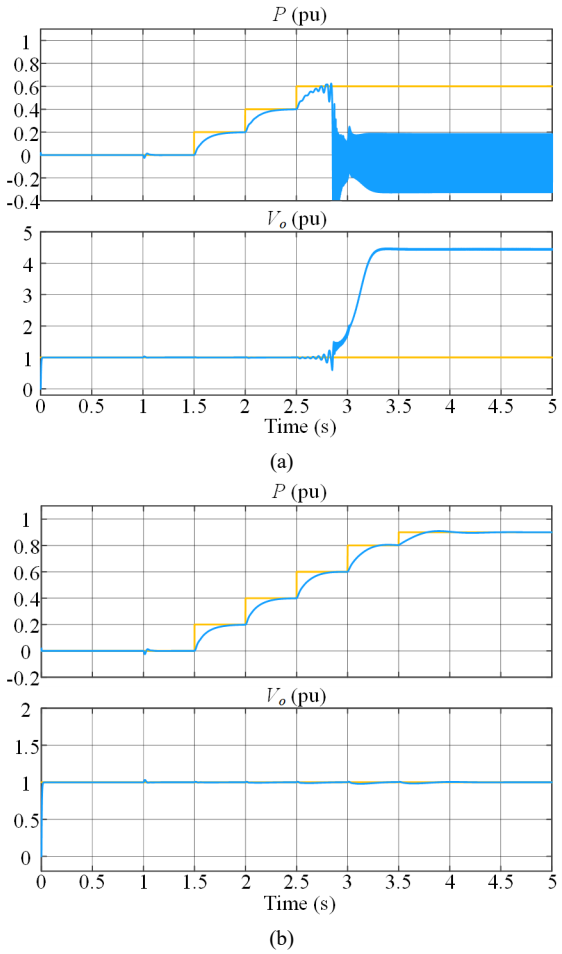

Fig. 18. Simulation results of grid-connected inverter with SCR=1. (a) 0~0.6 pu power reference by using the classical control scheme. (b) 0~0.9 pu power reference by using the proposed practical control scheme.

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In order to verify the effectiveness of the analysis above, a time-domain simulation model of a grid-connected inverter is built in Matlab/Simulink. To avoid the influence of high-frequency harmonics, the average model of the inverter is used. The system and control parameters are shown in Table I and Table II, which are the same as the parameters used in small-signal stability analysis. The simulation results of the classical grid-following control scheme and the proposed practical improved control scheme are shown in Fig. 18(a) and Fig. 18(b) respectively. Moreover, the control parameters of the double PLLs are shown in Table III.

TABLE III
PARAMETERS OF DOUBLE PLL

	Parameters	Values
ζ_1	Damping ratio of the main PLL	1
ω_{n1}	Natural angular frequency of the main PLL	200 rad/s
ζ_2	Damping ratio of the auxiliary PLL	1
ω_{n2}	Natural angular frequency of the auxiliary PLL	20 rad/s

As seen in Fig. 18(a), by using the classical control scheme, when the power reference is close to 0.6 pu, the PCC voltage starts to oscillate. Then, both the PCC voltage and the active power are out of control. However, as seen in Fig. 18(b), by using the proposed improved control scheme, the PCC voltage is controlled as 1 pu and the active power follows the power reference. The system is still stable when the power reference reaches 0.9 pu. These simulation results are consistent with the stability analysis in Fig. 8(c) and Fig. 15(b). It is worth mentioning that if the power reference is given 1 pu, the system will also become unstable even using proposed control scheme. The unstable result is similar to Fig. 18(a). This is because the power reference is higher than the dynamic power limit (stability boundary) shown in Fig. 16. Hence, to avoid this phenomenon happens, the power reference should be lower than the stability boundary and some stability margin should be reserved for reliable operation.

B. Simulation verification of the dynamic performance

In order to verify the PLL bandwidth is proportional to the natural angular frequency ω_n when ζ is constant, simulation results of frequency step responses with different ω_n are shown in Fig. 19. The damping ratio ζ is given as 1. It can be seen that when the grid frequency is changed from 50 Hz to 50.5 Hz, the step responses of different ω_n are different. When ω_n is equal to 200 rad/s, the step response of the PLL is fast. As ω_n decreases, the step response of the PLL becomes slower. Therefore, the bandwidth of the PLL is proportional to ω_n approximately.

Moreover, according to the analysis results in Fig. 11 and Fig. 16, it is known that both reducing the PLL bandwidth and using the proposed improved control scheme can enhance the stability. However, the dynamic response is slow by using a lower PLL bandwidth. To prove that the proposed control scheme does not slow down the frequency dynamic response, simulation results of two control schemes are compared in Fig. 20, where the same natural angular frequency ω_n is used for two control schemes. Fig. 20(a) shows the simulation results of the classical control scheme, while Fig. 20(b) shows the results of the proposed practical improved control scheme. It can be seen that when the grid frequency is changed from 50 Hz to 50.5 Hz, the rise time t_r of the classical control scheme in Fig. 20(a) is basically same as the rise time t_{r1} of the proposed control scheme in Fig. 20(b). Besides, the rise times of two control schemes with different PLL bandwidths are listed in Table IV for comparison. It can be seen that when using the same natural angular frequency ω_n, the rise times of two control schemes are in the same time level.

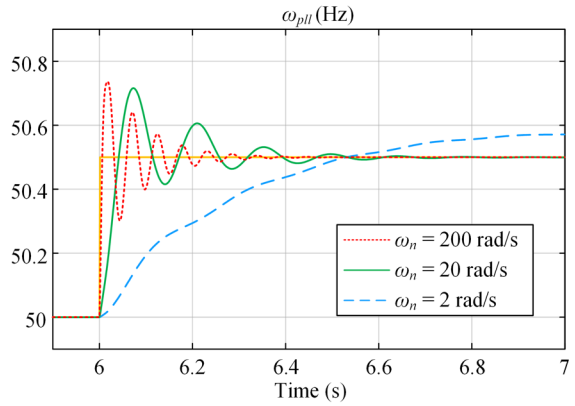

Fig. 19. Simulation results of frequency step responses with different ω_n of the classical PLL.

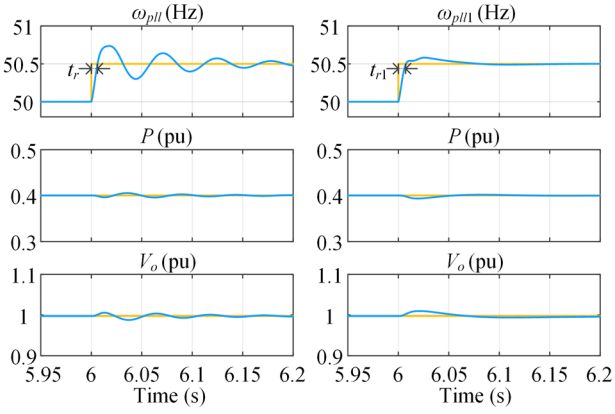

Fig. 20. Simulation results of frequency step responses by using two control schemes with ω_n = 200 rad/s. (a) Classical control scheme. (b) Proposed control scheme.

TABLE IV
RISE TIME OF FREQUENCY STEP RESPONSE

Values of ω_n	Rise time t_r	Rise time t_{r1}
200 rad/s	6.2 ms	7.3 ms
20 rad/s	42 ms	55 ms
2 rad/s	530 ms	535 ms

C. Simulation analysis of PCC voltage harmonics

In order to check the impact of the proposed method on the voltage harmonics, the switching model of the inverter is used in simulations. The simulation results of the PCC voltages and the grid currents by using two control schemes are shown in Fig. 21, where the steady-state power is 0.9 pu. Based on the

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analysis in Fig. 9, it is known that the conventional control scheme is unstable when the power is 0.9 pu and the SCR is equal to 1. Hence, SCR = 2 is used to evaluate the harmonic levels. It can be seen in Fig. 21 that the PCC voltage $v_{o(abc)}$ includes a certain level of harmonics. The THDs of the PCC voltages in Fig. 21 are 11.57% and 10.67% respectively, which are higher than the standards and unacceptable.

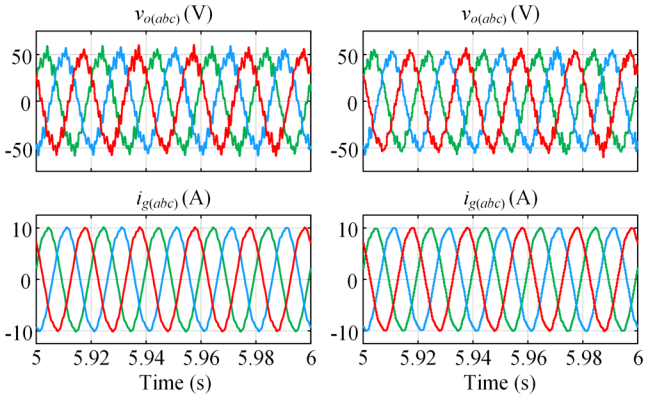

Fig. 21. Simulation results of the PCC voltages and grid currents by using two control schemes with SCR = 2. (a) Classical control scheme. (b) Proposed control scheme.

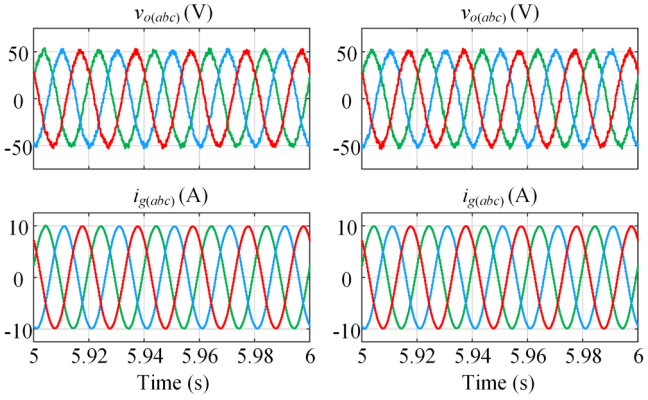

Fig. 22. Simulation results of the PCC voltages and grid currents by using two control schemes with SCR = 2 and ω_i = 5000 rad/s. (a) Classical control scheme. (b) Proposed control scheme.

According to IEEE Standard 519-2014 [33], the THD of the PCC voltage should be smaller than 8% (5%) in the low (medium) voltage application that the PCC bus voltage is lower than 69 kV [34]. To reduce the harmonics, suitable optimization for the inverter parameters is necessary. When the current control loop bandwidth ω_i is increased to 5000 rad/s, the simulation results of the PCC voltages and the grid currents by using two control schemes are shown in Fig. 22. The FFT analysis results of the PCC voltages in Fig. 22 are shown in Fig. 23. It can be seen that the THDs of the PCC voltages for both control schemes are smaller than 5%, which can meet the THD standards of low and medium voltage application.

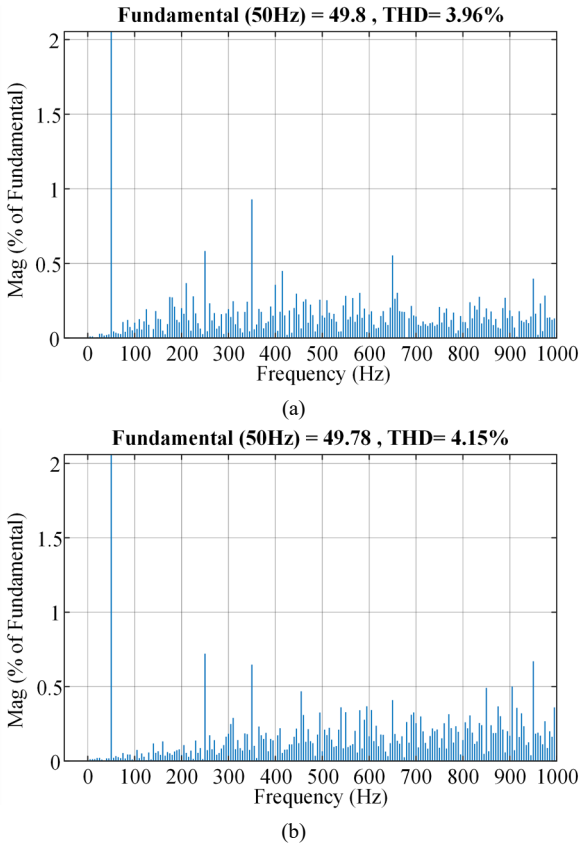

Fig. 23. FFT analysis results of the PCC voltages by using two control schemes with SCR = 2 and ω_i = 5000 rad/s. (a) Classical control scheme. (b) Proposed control scheme.

D. Experimental verification of the stability ranges

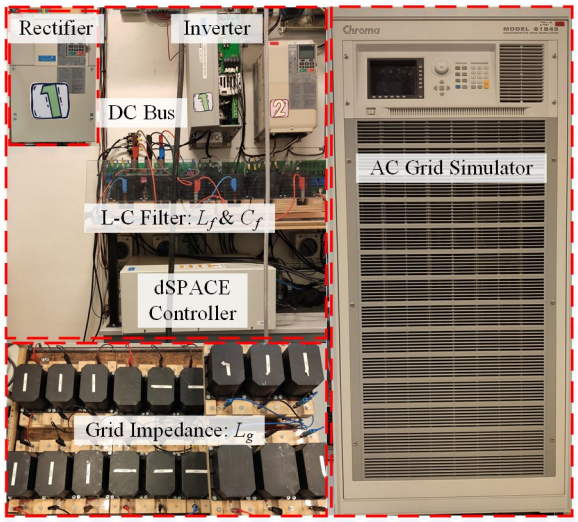

Fig. 24. View of experimental setup based on a dSPACE control system.

As shown in Fig. 24, the experimental setup is also built to verify the effectiveness of the proposed practical control scheme. The circuit and control parameters in experiments are the same as the parameters shown in Table I, Table II, and Table III, where the grid voltage amplitude is intentionally

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reduced to create a very weak grid condition (SCR=1). The weak grid is realized by connecting inductors (L_g) with a grid simulator Chroma 61845. The grid-connected inverter is implemented by using the Danfoss FC103P11KT11, and the control algorithms are implemented by using the dSPACE1007. The experimental results of the classical grid-following control scheme and the proposed practical control scheme are shown in Fig. 25(a) and Fig. 25(b) respectively.

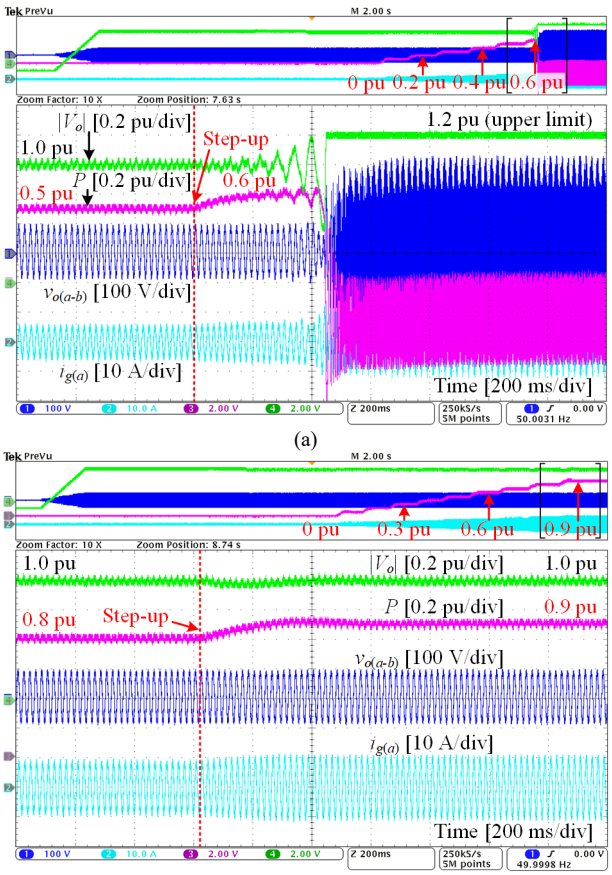

Fig. 25. Experimental waveforms of grid-connected inverter with SCR=1. (a) 0~0.6 pu power reference by using classical control scheme. (b) 0~0.9 pu power reference by using proposed practical control scheme. (CH1: phase to phase voltage at the PCC; CH2: grid phase current; CH3: active power, 160W/div; CH4: PCC voltage amplitude, 10V/div)

As seen in Fig. 25(a), by using the classical control scheme, when the power reference is close to 0.6 pu, the PCC voltage starts to oscillate. Then, the system becomes unstable. However, as seen in Fig. 25(b), the PCC voltage is controlled constantly and the active power follows the power reference. The system is still stable when the power reference reaches 0.9 pu. These experimental results agree well with the simulation results in Fig. 18(a) and Fig. 18(b).

VI. Conclusion

In this paper, a simplified *d-q* small-signal impedance model is derived to show the destabilizing factors of the classical grid-following control system. Based on the simplified model, it can be observed that the negative resistance caused by the PLL is a major destabilizing factor. Relatively, the negative inductance and resistance caused by the outer control loops are secondary destabilizing factors. To weaken the destabilizing factors caused by the outer loops, the bandwidths of the outer loops are designed low. To weaken the destabilizing factors caused by the PLL, two methods are introduced. One is simply reducing the PLL bandwidth. The other is reshaping the converter output impedance. Compared with the reducing bandwidth method, the impedance reshaping method does not worsen the dynamic performance of the PLL. Because both the major destabilizing factor caused by the PLL and the secondary destabilizing factors caused by the outer control loops are addressed in this paper, the stability range can be almost extended to the static power limit of the grid-connected inverter. Finally, simulation and experimental results have verified the effectiveness of the proposed method.

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