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A Temperature-Dependent dV_{CE}/dt model for Field-Stop IGBT at Turn-off Transient

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***Abstract*—In this paper, an analytical model is proposed to model collector-emitter voltage rising slope (dV_{CE}/dt) of field-stop (FS) IGBT during turn-off transient. Thanks to TCAD simulation, the internal physics of the FS IGBT during V_{CE} rise transient is investigated. Based on the improved understanding of the V_{CE} rise transient, an analytical solution of the excess carrier distribution in the N-base region and FS layer is derived. An analytical model for dV_{CE}/dt of FS IGBT is also proposed. The temperature dependency of various silicon material and device parameters are included in the model. In the end, the double-pulse tests are performed on 650V/40A and 1200V/40A FS IGBTs. The test results are compared with the analytical predictions and good agreement is obtained.**

***Index Terms*—field-stop (FS) IGBT, collector-emitter voltage rising slope, IGBT modeling, turn-off transient.**

I. Introduction

The recent development of power conversion technology requires the power switches to operate under high switching frequency while maintaining a low on-state voltage drop. To achieve the goal, the field-stop insulated gate bipolar transistors (FS IGBTs) are proposed [1], [2]. With a thin and lightly doped FS layer utilized, the FS IGBTs can achieve a better trade-off relationship between the on-state voltage drop and switching loss than the conventional punch-through (PT) IGBTs and non-punch-through (NPT) IGBTs [1]. After commercial roll-out, the FS IGBTs quickly become a mainstay among the mass IGBT market and are widely used in power conversion applications.

When the FS IGBTs turn off under clamped inductive load conditions, a high dV_{CE}/dt is applied on their collector-emitter. The dV_{CE}/dt acts as an intrinsic source to generate the common mode electromagnetic interference (EMI) [3]. The generated common mode EMI noise can give rise to very severe electromagnetic compatibility (EMC) problems for the power electronic systems [3]–[5]. Moreover, the steep dV_{CE}/dt can capacitively couple into the gate through the gate-collector stray capacitances, which induces a displacement current. The displacement current generates a voltage on gate loop impedance, which drive the gate to increase [6], [7]. When the dV_{CE}/dt is high enough, the gate voltage can surpass the threshold voltage and causes unwanted false turn-on. This false triggering turn-on can cause shoot-through faults [8]. Recently, the dV_{CE}/dt is found to be a good junction temperature indicator [9], [10]. Many studies are proposed to use dV_{CE}/dt to monitor the junction temperature of IGBT during converter operation [9], [10]. Last but not least, the dV_{CE}/dt is also a very critical parameter for the power loss estimation. Therefore, an accurate model of the dV_{CE}/dt for FS IGBT is highly required to optimize the performance of power converter.

Unfortunately, the dV_{CE}/dt modeling of IGBT at turn-off transient did not receive proper attention it deserves, only a few papers are proposed to discuss this topic. In [11], a simple dV_{CE}/dt model is proposed for NPT IGBT. The model can only make a very rough estimation on dV_{CE}/dt of NPT IGBT at turn-off transient. In [12], [13], an analytical expression is used to describe of dV_{CE}/dt of IGBT at turn-off transient. The dV_{CE}/dt model is widely used for power loss calculation [14]–[16] for FS IGBT. Based upon the initial steady-state minority carrier distribution, an analytical dV_{CE}/dt model of FS IGBT at turn-off transient is proposed in [10]. The model is utilized for power loss modelling [17] and junction temperature monitoring [9] of FS IGBT.

Looking into the previous studies presented above, the two models proposed in [12], [13] and in [10] are widely used for the dV_{CE}/dt modeling of FS IGBT. The model proposed in [12], [13] considers the IGBT as a unipolar device. The excess carrier dynamics in the N-base of in the FS IGBT is not included in the model. This can give rise to huge error in the prediction. With the impact of junction temperature, internal device operation, and external gate circuit on the dV_{CE}/dt included, a closed-form expression of dV_{CE}/dt is proposed in [10] for FS IGBT. However, the proposed FS IGBT model has a few major drawbacks. Firstly, the model directly uses the Hefner PT IGBT model [18] to model the FS IGBT and low-level injection is assumed on the FS layer. Since the FS layer is optimized to be thin and lightly doped, the excess carrier in the FS layer can surpass FS layer doping concentration and high-level injection assumption is required [19]–[23]. Secondly, the model assumes excess carrier in N-base linearly distributed in N-base, which is not accurate and can give rise errors on the prediction. Last but not least, some physical operations at turn-off transient, like the dependency of V_{ce} on the MOS transconductance, the MOS-side hole current reduction and displacement currents generated by the depletion region extension, are not considered in the model.

The goal of this paper is to derive an analytical model to describe the dV_{CE}/dt of the FS IGBTs during the turn-off transient. Thanks to the TCAD simulation, the physic of the FS IGBTs during the turn-off transient is analyzed in section II, which clarify the basic assumptions to simplify the dV_{CE}/dt

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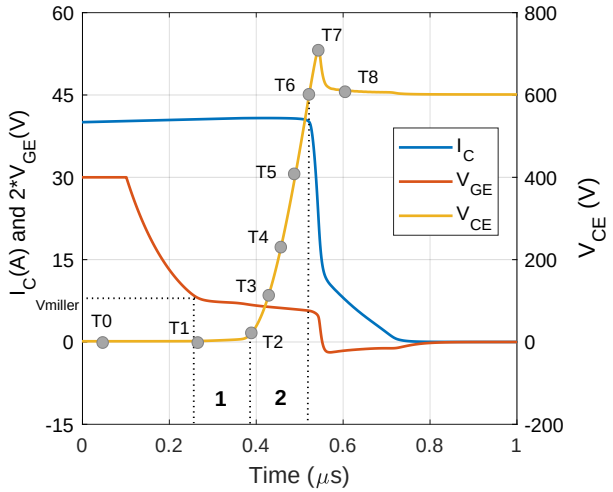
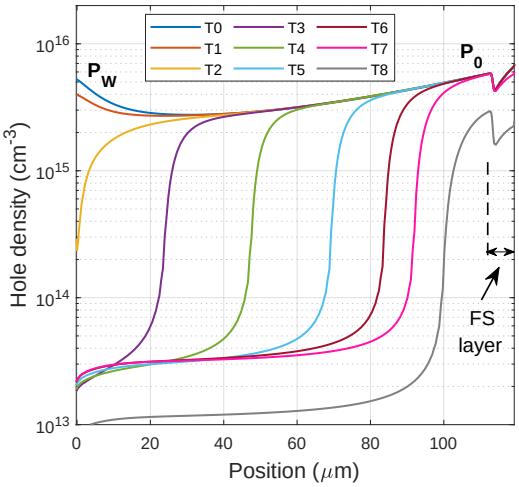


(a)



(b)

Fig. 1. TCAD simulation during clamped inductive turn-off transient of FS IGBT: (a)Simulated turn-off waveforms with the definition of time $T_0 - T_8$ and phases 1-2 of turn-off transient; (b) Simulated hole density profiles in the N-base at time $T_0 - T_8$.

modeling. Based on the assumptions, the excess carrier density in N-base and FS layer is derived in section III. In section IV, a temperature-dependent dV_{CE}/dt model of the FS IGBTs is proposed. In section V, double pulse tests are performed to validate the proposed model.

II. Improved Understanding on V_{CE} Rise Transient of FS IGBT

In order to model the dV_{CE}/dt at turn-off transient, it is necessary to have an overview on the V_{CE} rise process. To achieve this, the TCAD simulation is used to investigate the excess carrier dynamics in the N-base. Fig. 1a shows TCAD simulated clamped inductive turn-off waveforms of FS IGBT. The excess carrier density in N-base at time $T_0 - T_8$ (defined in Fig. 1a) are presented in Fig. 1b. The FS IGBT operates under the static on-state and off-state at T_0 and T_8, respectively. From T_1 to T_7, the IGBT operates at turn-off transient. Fig. 2 shows the structure of FS IGBT utilized, which defines the cell width L, intercell width l_m, N-base width W_B and FS layer width W_H. Based on the TCAD simulation results, the physical operations of the FS IGBT during the V_{CE} rise transient are discussed in this section.

A. V_{CE} Rise Process at clamped inductive Turn-off transient

As shown in Fig. 1a, the V_{CE} rise transient can be divided into two phases. The physical operations of the FS IGBT at phases 1 and 2 are described as follows:

Phase 1) Phase 1 initiates when V_{GE} achieves its Miller voltage V_{Miller} that is just sufficient to support the I_c. In this phase, the MOS channel of the IGBT starts to work in saturation region. Due to the reduction of V_{GE}, the MOS electron current decreases. The corresponding hole current induced by ambipolar transportation also reduces. To maintain a constant I_c, the V_{CE} rises to generate displacement current I_{disp} on the collector-emitter stray capacitance C_{CE} and displacement current I_{CG} on the gate-collector stray capacitance C_{GC}, as

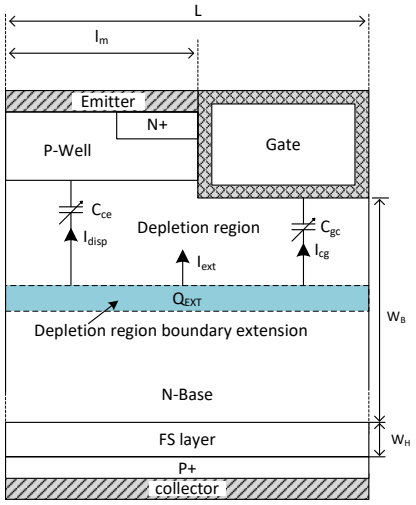


Fig. 2. Schematic structure of FS IGBT with definitions of the current components generated during the turn-off transient.

shown in Fig. 2. In this phase, the depletion region is not formed, as shown in Fig. 1b at time T_1. The stray capacitances C_{CE} and C_{GC} are very large, which give rise to a small dV_{CE}/dt in this phase.

Phase 2) When the V_{CE} increases to tens of volts, the depletion region starts to form in the N-base and the phase 2 starts, as shown in Fig. 1b at time T_2. In this phase, the stray capacitances C_{CE} and C_{GC} greatly decrease, which give rise to the abrupt increase in V_{CE}. The V_{CE} rising induces the extension of depletion region, as shown in Fig. 1b at time $T_2 - T_7$. The depletion region extension extracts excess charge in the N-base, which generates charge extraction current I_{ext}, as shown in Fig. 2. The sum of the I_{ext}, I_{disp} and I_{CG} supports I_c to remain constant in this phase.

During the phase 1 and phase 2, the dV_{CE}/dt induces collector-gate displacement current I_{CG} in the stray capacitance C_{GC}. As shown in Fig. 3, the I_{CG} flows to the gate

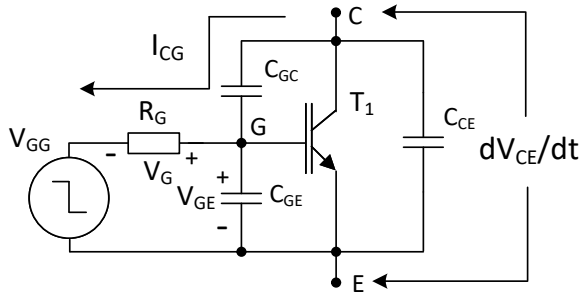


Fig. 3. The gate negative feedback during turn-off transient.

circuit, which generates a voltage V_G on the gate resistor. The V_G support the gate voltage V_{GE}, which greatly reduce the gate turn-off speed. As a result, the MOS channel current reduction greatly slows down, which in return induces a lower dV_{CE}/dt. As a result, a negative feedback action is achieved, which has a significant impact on the dV_{CE}/dt during the turn-off transient.

B. Pivotal current components for the dV_{CE}/dt modeling

During phases 1 and 2, the MOS-side electron and hole current reduces. To maintain a constant I_c, the V_{CE} is forced to rise so that various current components can be generated to compensate for the MOS-side current reduction. Therefore, it is necessary to identify pivotal current components for dV_{CE}/dt modeling, which are discussed as follows.

1) The displacement current I_{CG} on the stray capacitance C_{GC}: As shown in Fig. 3, the displacement current I_{CG} induces negative feedback action, which has significant impact on the dV_{CE}/dt. The displacement current I_{CG} is thereby very critical for the dV_{CE}/dt modeling.

2) The charge extraction current I_{ext}: During phase 2, the charge extraction current I_{ext} can be very large due to the high-level injection in the N-base. Therefore, the charge extraction current I_{ext} is very critical for the dV_{CE}/dt modeling in the phase 2.

3) The displacement current I_{disp} on the stray capacitance C_{CE}: During the turn-off transient, the dV_{CE}/dt induces displacement current on the stray capacitance C_{CE}, which greatly compensate the MOS-side current reduction. Therefore, the impact of I_{disp} on the dV_{CE}/dt should be considered.

C. Basic Assumptions

In order to simplify the dV_{CE}/dt modeling, few basic assumptions are made, which are presented as follows:

1) The collector current I_c remains constant during the phase 1 and 2: During the phases 1 and 2, the high-side freewheeling diode cannot conduct forward current. I_c thereby slightly reduces due to the displacement current generated by the dV/dt applied on the freewheeling diode, as shown in Fig. 1a. The tiny reduction of I_c is typically neglected in the IGBT turn-off modelling [10], [11], [24], [25]. The I_c can thereby assume to be constant.

2) The profile of excess carrier density in the undepleted N-base and FS layer at turn-off transient is the same as

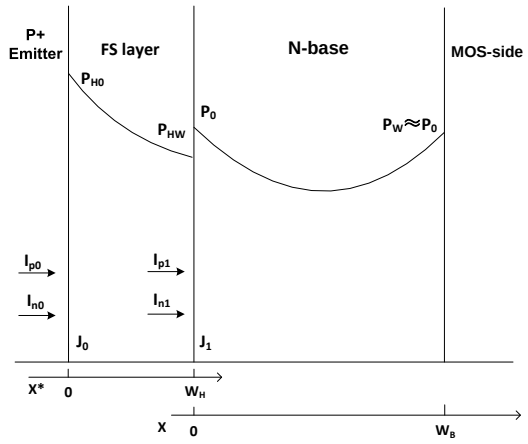


Fig. 4. Coordinate diagram of FS IGBT under on-state with boundary condition definition.

that under on-state: Due to the high excess carrier lifetime, the excess carrier density in the undepleted N-base remains constant during the voltage rising transient [10]. As shown in Fig. 1b, the profile of hole density in the undepleted N-base and FS layer at time $T_1 - T_7$ (turn-off transient) is almost identical to that at time T_0 (on-state). Therefore, the profile of excess carrier density under on-state is utilized in the dV_{CE}/dt modeling.

3) The excess carrier densities at the two ends of the N-base are approximately identical under on-state: Nowadays, the technologies like trench gate [26] and carrier storage layer [27] are widely utilized in the FS IGBT. These technologies greatly enhance the MOS-side excess carrier density P_W to a level very close to excess carrier density P_0 at the anode nn+ junction, as shown in Fig. 1b. Therefore, the excess carrier densities at two ends of the N-base are assumed to be identical in this study.

4) The FS layer is under high-level injection conditions: During turn-off transient, the excess carrier density in the FS layer approaches or exceeds the doping concentration of FS layer [19], [20]. Therefore, high-level injection condition should be assumed for the FS layer [19]–[22].

III. Static on-state Modeling

In this section, excess carrier density under static on-state is derived, which will be utilized for the dV_{CE}/dt modeling based on assumption 2 proposed in the previous section. Fig. 4 shows the coordinate diagram of FS IGBT under on-state. J_0 is the junction between the P+ emitter and the FS layer. J_1 is the junction between the FS layer and N-base. I_{n0} and I_{p0} are the electron and hole current at J_0. I_{n1} and I_{p1} are the electron and hole current at J_1. Under on-state, the excess carrier distribution in the N-base is governed by ambipolar diffusion equation (ADE) [28]:

$$D\frac{\partial^2 p(x)}{\partial x^2} = \frac{p(x)}{\tau} \tag{1}$$

where τ is the carrier lifetime in the N-base. $p(x)$ is the excess carrier density in N-base. D is the ambipolar diffusion

coefficient, which can be expressed as:

$$D = \frac{2D_nD_p}{D_p + D_n} \tag{2}$$

where D_p and D_n are the hole and electron diffusion coefficients, respectively.

The solution of the ADE (1) is :

$$p(x) = \frac{P_W \cdot sinh\left(\frac{x}{L}\right) + P_0 \cdot sinh\left(\frac{W_B - x}{L}\right)}{sinh\left(\frac{W_B}{L}\right)} \tag{3}$$

where W_B is the N-base width. P_0 and P_W are the excess carrier density at $x = 0$ and $x = W_B$, as shown in Fig. 4. $L = \sqrt{D\tau}$ is the diffusion length.

Based on assumption 3 proposed in section II, $P_W \approx P_0$ is assumed. The equation (3) is thereby simplified as:

$$p(x) = P_0\frac{sinh\left(\frac{x}{L}\right) + sinh\left(\frac{W_B - x}{L}\right)}{sinh\left(\frac{W_B}{L}\right)} \tag{4}$$

With the equation (4) utilized, the electron current I_{n1} at $x = 0$ is obtained:

$$\begin{aligned} I_{n1} &= \frac{bI_c}{1+b} + qAD\frac{\partial p(x)}{\partial x}\bigg|_{x=0} \\ &= \frac{bI_c}{1+b} - \frac{qADP_0}{L}tanh\left(\frac{W_B}{2L}\right) \end{aligned} \tag{5}$$

Where q is electronic charge. b is the ratio of electron mobility μ_n and hole mobility μ_p. A is the active die area.

With high-level injection assumed in the FS layer, the excess carrier density $\delta p(x^*)$ in the FS layer is governed by ADE:

$$D\frac{\partial^2 \delta p}{\partial x^{*2}} = \frac{\delta p(x^*)}{\tau_H} \tag{6}$$

where τ_H is the lifetime of excess carrier in the FS layer.

In the FS layer, a linear distribution of $\delta p(x^*)$ is assumed for initial estimation of the $\delta p(x^*)$. $\delta p(x^*)$ can thereby be expressed as:

$$\delta p(x^*) = P_{H0} - \frac{P_{H0} - P_{HW}}{W_H}x^* \tag{7}$$

where W_H is the width of FS layer. As shown in Fig. 4, P_{H0} and P_{HW} are the excess carrier density at $x^* = 0$ and $x^* = W_H$, respectively.

Substituting (7) into (6), integrating the two side of the equation twice. Utilizing the boundary conditions $p(0) = P_{H0}$ and $p(W_H) = P_{HW}$, the excess carrier distribution in FS layer can be obtained [20]:

$$\begin{aligned} \delta p(x^*, t) = &\left[P_{H0} - \frac{P_{H0} - P_{HW}}{W_H}x^*\right] + \frac{1}{L_H^2}\left[\frac{P_{H0}}{2}x^{*2} - \frac{x^{*3}}{6}\right. \\ &\left.\times\frac{(P_{H0} - P_{HW})}{W_H} - \frac{(2P_{H0}W_H + P_{HW}W_H)}{6}x^*\right] \end{aligned} \tag{8}$$

where $L_H = \sqrt{D\tau_H}$ is the diffusion length in the FS layer.

With high-level injection assumed in the FS layer, the hole and electron current can be expressed as [29]:

$$I_p = \frac{I_c}{1+b} - qAD\frac{dp}{dx} \tag{9}$$

$$I_n = \frac{bI_c}{1+b} + qAD\frac{dp}{dx} \tag{10}$$

Substituting (8) into (9) and (10) with $x^* = 0$ and $x^* = W_H$, the hole current I_{p0} at $x^* = 0$ and electron current I_{n1} at $x^* = W_H$ can be obtained:

$$I_{p0} = \frac{I_c}{1+b} + qAD\left[\frac{P_{H0} - P_{HW}}{W_H} + \frac{W_H}{6L_H^2}(2P_{H0} + P_{HW})\right] \tag{11}$$

$$I_{n1} = \frac{bI_c}{1+b} - qAD\left[\frac{P_{H0} - P_{HW}}{W_H} - \frac{W_H}{6L_H^2}(P_{H0} + 2P_{HW})\right] \tag{12}$$

Using quasi-equilibrium simplification at the J_1 junction, (13) can be obtained [20].

$$P_0^2 = (N_H + P_{HW})P_{HW} \tag{13}$$

In the FS layer, the excess carrier density is close to the FS layer doping concentration [19]–[22]. $P_{HW} \approx N_H$ is thereby assumed in this study. The (13) is further simplified to (14).

$$P_0^2 = (N_H + P_{HW})P_{HW} \approx 2N_HP_{HW} \tag{14}$$

The electron current I_{n0} at the J_0 junction is [30]:

$$I_{no} = qAh_pN_HP_{H0} \tag{15}$$

where h_p is hole recombination coefficient in emitter.

Combining (11) and (15), the P_{H0} can be obtained:

$$P_{H0} = \frac{\frac{bI_c}{1+b} + qAD\left(\frac{P_{HW}}{W_H} - \frac{W_HP_{HW}}{6L_H^2}\right)}{qA\left(\frac{D}{W_H} + \frac{W_H}{3\tau_H}\right) + qAh_pN_H} \tag{16}$$

Substituting (16) to the (12), the electron current I_{n1} can be obtained:

$$I_{n1} = K_1\frac{3bI_c}{2(1+b)} + qAK_2P_{HW} \tag{17}$$

where K_1 and K_2 are

$$K_1 = \frac{W_H^2 + 2N_HW_Hh_p\tau_H}{3D\tau_H + W_H^2 + 3N_HW_Hh_p\tau_H} \tag{18}$$

$$K_2 = \frac{W_H^3 + 12D\tau_H(W_H + N_H\tau_Hh_p) + 4N_HW_H^2h_p\tau_H}{4\tau_H(3D\tau_H + W_H^2 + 3N_HW_Hh_p\tau_H)} \tag{19}$$

Combining the equations (5) , (13) and (17), the carrier density P_0 can be obtained by:

$$P_0 = \sqrt{K^2 + \frac{bI_cN_H(2 - 3K_1)}{qAK_2(1+b)}} - K \tag{20}$$

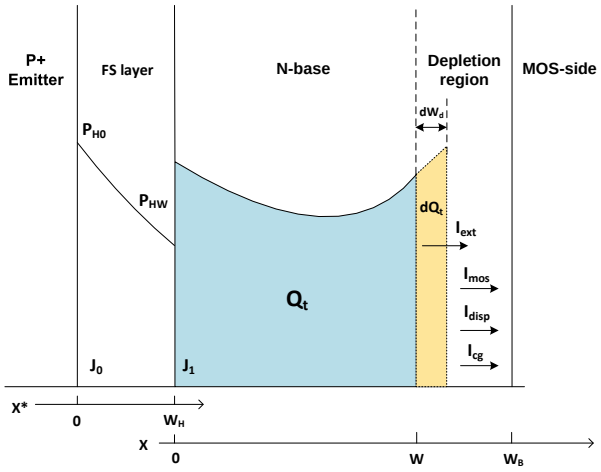


Fig. 5. Coordinate diagram of FS IGBT at turn-off transient with boundary condition definition.

where K is

$$K = \frac{N_H D}{LK_2} tanh\left(\frac{W_B}{2L}\right) \tag{21}$$

IV. Temperature-Dependent dV_{CE}/dt Modeling at Turn-off Transient for FS IGBT

A. dV_{CE}/dt Modeling of the FS-IGBT

Fig. 5 shows the current components in the depletion region of FS IGBT at turn-off transient. During the turn-off transient, the collector current I_C is supported by I_{mos}, I_{ext}, I_{disp} and I_{CG}, as shown in Fig. 5. I_{mos} is the MOS electron current. I_{ext} is the charge extraction current. I_{disp} is the collector-emitter displacement current. I_{CG} is the collector-gate displacement current. The equation (22) can thereby be obtained.

$$\begin{aligned} I_C &= I_{ext} + I_{mos} + I_{disp} + I_{CG} \\ &= I_{ext} + I_{mos(on)} + \Delta I_{mos} + I_{disp} + I_{CG} \end{aligned} \tag{22}$$

where $I_{mos(on)}$ is the MOS current under on-state condition. ΔI_{mos} is the MOS current reduction during the turn-off transient.

The collector-emitter displacement current I_{disp} is given by [31]:

$$I_{disp} = C_{CE} \frac{dV_{CE}}{dt} \tag{23}$$

C_{CE} is the collector-emitter depletion capacitance, which is obtained by [31]:

$$C_{CE} = \frac{\epsilon_{si} A(1 - a_i)}{W_d} \tag{24}$$

where ϵ_{si} is the dielectric coefficient of silicon. a_i is the area factor. With cell width L and intercell width l_m defined in Fig. 2, a_i is expressed as:

$$a_i = \frac{(L - l_m)}{L} \tag{25}$$

W_d is the depletion region width, which is given by [30]:

$$W_d = \sqrt{\frac{2\epsilon_{si} V_{CE}}{qN'_B}} \tag{26}$$

Where N'_B is the effective doping concentration, which can be expressed as:

$$N'_B = N_B + \frac{I_C}{qAv_{p,sat}(1+b)} \tag{27}$$

where $bI_C/qAv_{p,sat}(1+b)$ is the free holes injected in the depletion region. $v_{p,sat}$ is the saturated drift velocity of hole.

The collector-gate displacement current I_{CG} is [31]:

$$I_{CG} = C_{GC} \frac{dV_{CE}}{dt} \tag{28}$$

C_{GC} is the gate-collector depletion capacitance, which is obtained by [31]:

$$C_{GC} = \frac{\epsilon_{si} A a_i}{W_d} \tag{29}$$

With the equation (4) utilized, the total excess charge Q_t in the N-base is obtained:

$$Q_t = qA \int_0^W p(x)dx = 2qAP_0 L \cdot tanh\left(\frac{W}{2L}\right) \tag{30}$$

where $W = W_B - W_d$ is undepleted N-base width.

As shown in Fig. 5, the extraction of Q_t is used to support the charge extraction current I_{ext}. Therefore, I_{ext} is equal to the decay rate of the Q_t:

$$I_{ext} = -\frac{dQ_t}{dt} = \frac{AP_0\epsilon_{si}}{N'_B W_d} sech^2\left(\frac{W}{2L}\right)\frac{dV_{CE}}{dt} = C_{ext}\frac{dV_{CE}}{dt} \tag{31}$$

where C_{ext} is equivalent capacitance for the N-base charge extraction. C_{ext} is given by:

$$C_{ext} = \frac{AP_0\epsilon_{si}}{N'_B W_d} sech^2\left(\frac{W}{2L}\right) \tag{32}$$

The on-state MOS current $I_{mos(on)}$ can be approximately obtained by [31]:

$$I_{mos(on)} \approx \frac{bI_C}{1+b} \tag{33}$$

The MOS current reduction ΔI_{mos} is given by [32]:

$$\Delta I_{mos} = G_m(V_{GE} - V_{miller}) \tag{34}$$

G_m is the equivalent transconductance of the stray MOSFET when $V_{GE} = V_{miller}$. V_{miller} is Miller voltage, which is expressed as:

$$V_{miller} = \sqrt{\frac{2I_{mos(on)}}{K_p}} + V_{th} \tag{35}$$

G_m can be expressed as:

$$G_m = \left.\frac{dI_{mos\_m}}{dV_{GS}}\right|_{V_{GE}=V_{miller}} \tag{36}$$

Noting that the MOS current I_{mos} is expressed as [33]:

$$I_{mos} = \frac{K_p}{2}(V_{GS} - V_{th})^2(1 + \lambda V_{CE}) \tag{37}$$

where K_p is the MOS transconductance coefficient. V_{th} is the threshold voltage. λ is the MOS short channel coefficient.

Combing the equations (36) and (37) with $V_{GE} = V_{miller}$, The G_m can be obtained by:

TABLE I
EQUATIONS FOR TEMPERATURE-DEPENDENT PARAMETERS

Parameter	Temperature-dependent equation
V_{th}	$V_{th} = V_{th0} - 9 \times 10^{-3}(T_J - 300)$ [36]
K_p	$K_p = K_{p0}(300/T_J)^{0.8}$ [36]
τ	$\tau = \tau_0(T_J/300)^{1.5}$ [36]
τ_H	$\tau_H = \tau_{H0}(T_J/300)^{1.5}$ [36]
h_p	$h_p = h_{p0}(300/T_J)^{2.5}$ [35]
μ_n	$\mu_n = 1417 \times (300/T_J)^{2.5}$ [34]
μ_p	$\mu_p = 470.5 \times (300/T_J)^{2.2}$ [34]
$v_{p,sat}$	$v_{p,sat} = 8.36 \times 10^6(T_J/300)^{0.52}$ [37]

$$G_m = K_p(V_{miller} - V_{th})(1 + \lambda V_{CE}) \tag{38}$$

To include the gate feedback action presented in Fig. 3, the gate circuit equation (39) is included.

$$V_{gg(off)} = V_{GE} - I_{CG}R_g \tag{39}$$

Combining the equations (22), (23), (28), (31), (33), (34), and (39), the dV_{CE}/dt can be expressed as

$$\frac{dV_{CE}}{dt} = \frac{G_m(V_{miller} - V_{gg(off)}) + \dfrac{I_C}{1+b}}{C_{ext} + C_{CE} + C_{GC}(1 + G_m R_G)} \tag{40}$$

In the numerator, the term $G_m(V_{miller} - V_{gg(off)})$ denotes the gate driving force. $V_{miller} - V_{gg(off)}$ is the voltage bias on the gate during the V_{CE} rise transient. The term $I_C/(1+b)$ denotes the MOS-side hole current reduction.

In the denominator, the term C_{ext} relates to charge extraction in the N-base, which generate the current I_{ext}. The terms C_{CE} and C_{GC} denote their corresponding displacement currents I_{disp} and I_{CG}. The term $C_{GC}G_mR_G$ is related to the negative feedback presented in Fig. 3.

B. Temperature-dependent parameters of FS IGBT

To include the impact of junction temperature T_J on the dV_{CE}/dt, the temperature sensitivity of the silicon material properties and device parameters should be considered. Table I summarize all the temperature-dependent parameters and their temperature dependency equations. The equations which describe μ_n and μ_p are proposed [34]. The governing equations for τ, τ_H, h_p, K_p and V_{th} are presented in [35], [36]. The expression of $v_{p,sat}$ is proposed in [37]. In Table I, the V_{th0}, K_{p0}, τ_0, τ_{H0} and h_{p0} are the corresponding parameters measured at 300K. The accuracy of the temperature-dependent models are validated in [34], [35], [35], [36].

C. Parameter Extraction

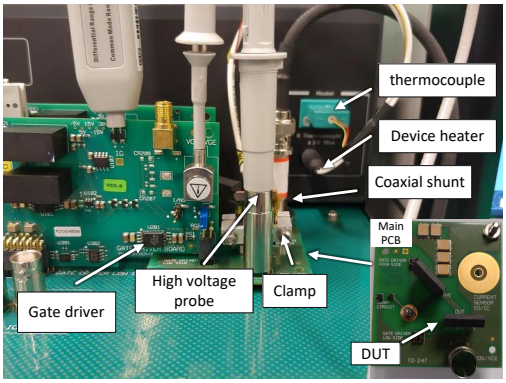
Table II shows the parameter of the proposed IGBT model. The die area A is obtained by direct measurement. The a_i can be extracted by C-V curves [38]. The V_{th0}, K_{p0}, λ is extracted from I-V characteristic curves [39].The τ_0, τ_{H0} and h_{p0} can be extracted based on the proposed in [38], [40]. The N_H, W_H, W_B and N_B can be obtained by the methods proposed in [31], [39]. The parameters of two devices under test are summarized in Table II.

TABLE II
THE PARAMETERS OF IGBT MODEL

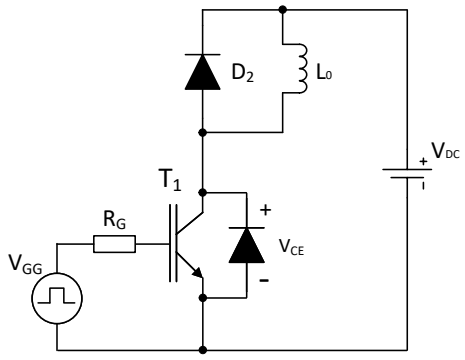
Parameters	IKW40N65ET7	IKW40N120CS6
A(cm^2)	0.2	0.4
$V_{th0}(V)$	5.3	5.55
$K_{p0}(A \cdot V^{-2})$	4.6	5.6
$\lambda(V^{-1})$	0.0025	0.001
a_i	0.38	0.6
$W_B(\mu m)$	60	110
$N_B(cm^{-3})$	1×10^{14}	1×10^{14}
$W_H(\mu m)$	5	5
$N_H(cm^{-3})$	9×9^{15}	1×10^{16}
$\tau_0(S)$	0.8	1.3
$\tau_{H0}(S)$	0.2	0.1
$h_{p0}(cm^4 \cdot S^{-1})$	1×10^{-14}	1×10^{-14}

V. EXPERIMENTAL VALIDATION

To validate the model, a 650V/40A FS IGBT IKW40N65ET7 and 1200V/40A FS IGBT IKW40N120CS6 are utilized in this study. The V_{CE} waveforms of the devices under test (DUTs) are obtained by double-pulse test. The



(a)



(b)

Fig. 6. Double-pulse test setup. (a) Test fixture. (b) Equivalent schematic circuit.

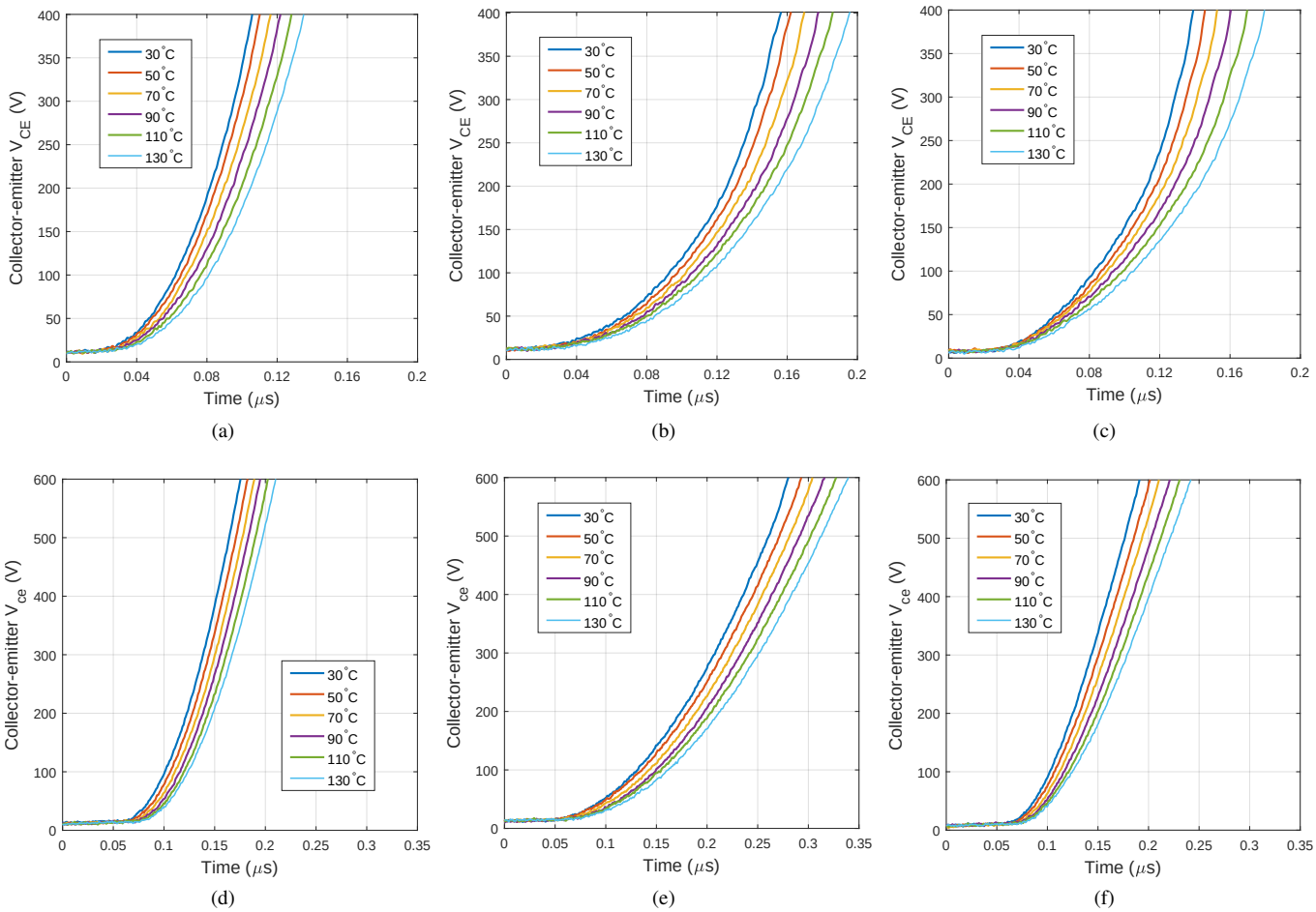


Fig. 7. Experimental turn-off waveforms of V_{CE}. (a) IKW40N65ET7 with $I_L = 30A$ and $R_G = 10\Omega$. (b) IKW40N65ET7 with $I_L = 30A$ and $R_G = 30\Omega$. (c) IKW40N65ET7 with $I_L = 10A$ and $R_G = 10\Omega$. (d) IKW40N120CS6 with $I_L = 30A$ and $R_G = 10\Omega$. (e) IKW40N120CS6 with $I_L = 30A$ and $R_G = 30\Omega$. (f) IKW40N120CS6 with $I_L = 10A$ and $R_G = 10\Omega$.

test is performed with various junction temperatures, gate resistors and load currents utilized.

A. Double-pulse Test

The double-pulse test fixture and its corresponding schematic circuit are shown in Fig. 6. In the test circuit, T_1 at the low-side is the DUT. D_2 is high-side freewheeling diode with part number UJ3D1250K. $L_0 = 330\mu H$ is the load inductor. R_G is the gate resistance. V_{DC} is the DC-bus voltage. V_{gg} is the gate driver, which switches with 15V/0V.

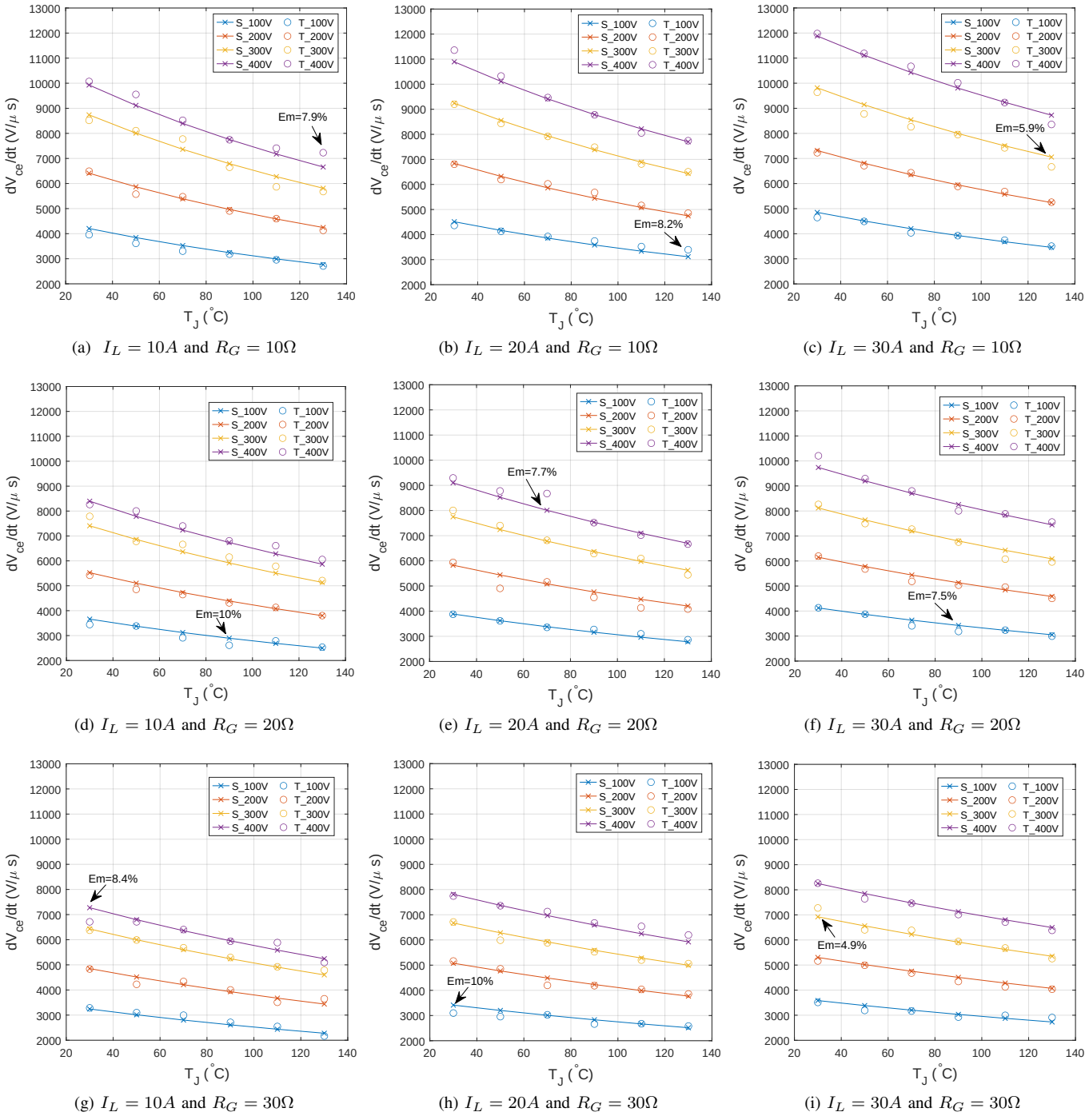
To heat up the DUT, a device heater is attached to the DUT by a clamp. A K-type thermocouple is integrated into the device heater, which can monitor the junction temperature of the DUT. The double-pulse test performs when the desired junction temperature is achieved. The V_{CE} waveforms are measured by a high-voltage probe. The I_C waveforms are measured by a coaxial shunt resistor.

The experimental turn-off waveforms of V_{CE} using IKW40N65ET7 and IKW40N120CS6 are presented in Fig. 7. The V_{CE} waveforms are measured at six different junction temperatures ranges from 30°C to 130°C. It can be noticed that the dV_{CE}/dt significantly decreases when the junction temperature increases. When the I_L increases from 10A to 30A, the dV_{CE}/dt significantly increases. The dV_{CE}/dt greatly decreases when the R_G increase from 10Ω to 30Ω.

In this study, the dV_{CE}/dt are extracted when V_{CE} is 100V, 200V, 300V and 400V. The extracted dV_{CE}/dt at various load currents, gate resistors and junction temperatures are compared with the value derived by (40) to validate the proposed analytical model.

B. Comparison of Experimental and Analytical Derived dV_{CE}/dt

Fig. 8 and Fig. 9 compare the experimental and analytical derived dV_{CE}/dt of the IKW40N65ET7 and IKW40N120CS6 with various junction temperatures (30°C, 50°C, 70°C, 90°C, 110°C and 130°C), load currents (10A, 20A and 30A) and gate resistors (10Ω, 20Ω and 30Ω). For the turn-off waveforms of IKW40N65ET7, the dV_{CE}/dt is extracted when V_{CE} equals to 100V, 200V, 300V and 400V, as shown in Fig. 8. For the turn-off waveforms of IKW40N120CS6, the dV_{CE}/dt is extracted when V_{CE} equals to 150V, 300V, 450V and 600V, as shown in Fig. 9. The analytical derived dV_{CE}/dt is marked in solid line and are labelled as S_n, where n is 100V, 200V,



(a) $I_L = 10A$ and $R_G = 10\Omega$ (b) $I_L = 20A$ and $R_G = 10\Omega$ (c) $I_L = 30A$ and $R_G = 10\Omega$

(d) $I_L = 10A$ and $R_G = 20\Omega$ (e) $I_L = 20A$ and $R_G = 20\Omega$ (f) $I_L = 30A$ and $R_G = 20\Omega$

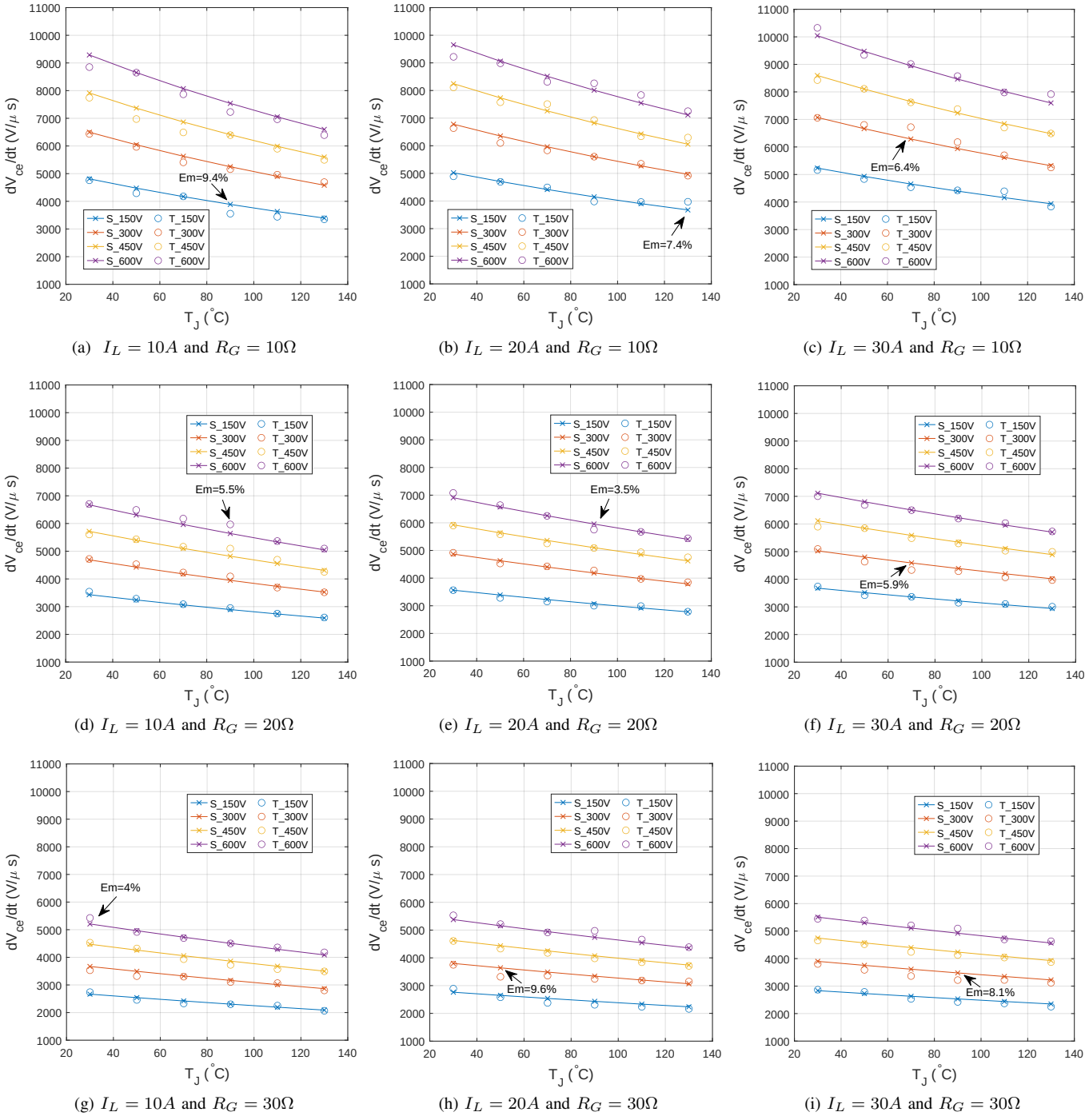
(g) $I_L = 10A$ and $R_G = 30\Omega$ (h) $I_L = 20A$ and $R_G = 30\Omega$ (i) $I_L = 30A$ and $R_G = 30\Omega$

Fig. 8. Comparison of experimental (T_n) and analytical derived (S_n) dV_{CE}/dt of IKW40N65ET7 for various junction temperature and V_{CE} values when (a) $I_L = 10A$ and $R_G = 10\Omega$, (b) $I_L = 20A$ and $R_G = 10\Omega$, (c) $I_L = 30A$ and $R_G = 10\Omega$, (d) $I_L = 10A$ and $R_G = 20\Omega$, (e) $I_L = 20A$ and $R_G = 20\Omega$, (f) $I_L = 30A$ and $R_G = 20\Omega$, (g) $I_L = 10A$ and $R_G = 30\Omega$, (h) $I_L = 20A$ and $R_G = 30\Omega$, (i) $I_L = 30A$ and $R_G = 30\Omega$.

300V and 400V for IKW40N65ET7 and is 150V, 300V, 450V and 600V IKW40N120CS6. The experimental dV_{CE}/dt is marked in dot and are illustrated as T_n.

With the increase of V_{CE}, the equivalent transconductance G_m increases while the depletion capacitances C_{CE} and C_{GC} decreases. This gives rise to the increased dV_{CE}/dt, as shown in Fig. 8. In the proposed model, the impacts of V_{CE} on the transconductance G_m is included in (37). (26) reflect the influence of V_{CE} on the depletion capacitances C_{CE} and C_{GC}. The analytical derived dV_{CE}/dt thereby agree with the test results with various V_{CE}, as shown in Fig. 8 and Fig. 9.

As shown in Fig. 8 and Fig. 9, dV_{CE}/dt reduces with the increase of junction temperature T_J. The reduction of dV_{CE}/dt is due to the increased charge extraction capacitance C_{ext} and reduced transconductance G_m. As shown in Table I, the impact of T_J on C_{ext} is considered by the temperature-dependent models of τ, τ_H, h_p, μ_n and μ_p. The influence of T_J on G_m is considered by the temperature-dependent models



(a) $I_L = 10A$ and $R_G = 10\Omega$ (b) $I_L = 20A$ and $R_G = 10\Omega$ (c) $I_L = 30A$ and $R_G = 10\Omega$

(d) $I_L = 10A$ and $R_G = 20\Omega$ (e) $I_L = 20A$ and $R_G = 20\Omega$ (f) $I_L = 30A$ and $R_G = 20\Omega$

(g) $I_L = 10A$ and $R_G = 30\Omega$ (h) $I_L = 20A$ and $R_G = 30\Omega$ (i) $I_L = 30A$ and $R_G = 30\Omega$

Fig. 9. Comparison of experimental (T_n) and analytical derived (S_n) dV_{CE}/dt of IKW40N120CS6 for various junction temperature and V_{CE} values when (a) $I_L = 10A$ and $R_G = 10\Omega$, (b) $I_L = 20A$ and $R_G = 10\Omega$, (c) $I_L = 30A$ and $R_G = 10\Omega$, (d) $I_L = 10A$ and $R_G = 20\Omega$, (e) $I_L = 20A$ and $R_G = 20\Omega$, (f) $I_L = 30A$ and $R_G = 20\Omega$, (g) $I_L = 10A$ and $R_G = 30\Omega$, (h) $I_L = 20A$ and $R_G = 30\Omega$, (i) $I_L = 30A$ and $R_G = 30\Omega$.

of K_p and V_{th}. With these temperature-dependent models included, the analytical derived dV_{CE}/dt accurately captures the impact of T_J on the experimental dV_{CE}/dt, as shown in Fig. 8 and Fig. 9.

The gate resistor R_G affects the dV_{CE}/dt due to the $C_{GC}dV_{CE}/dt$ induced gate negative feedback action, as shown in Fig. 3. With the increase of R_G, stronger negative feedback action is achieved, the dV_{CE}/dt thereby reduces, as shown in Fig. 8 and Fig. 9. Since the gate negative feedback is included in the equation (39), the analytical derived dV_{CE}/dt matches with the experimental results when the resistors with 10Ω, 20Ω and 30Ω are utilized as R_G.

As shown in Fig. 8 and Fig. 9, with the increase of load current I_L, the dV_{CE}/dt becomes larger. The I_L has significant impact on the transconductance G_m, charge extraction capacitance C_{ext} and MOS-side hole current, which affect the dV_{CE}/dt. In this model, the influence of I_L on G_m and C_{ext} are included in the equations (35) and (20), respectively. In

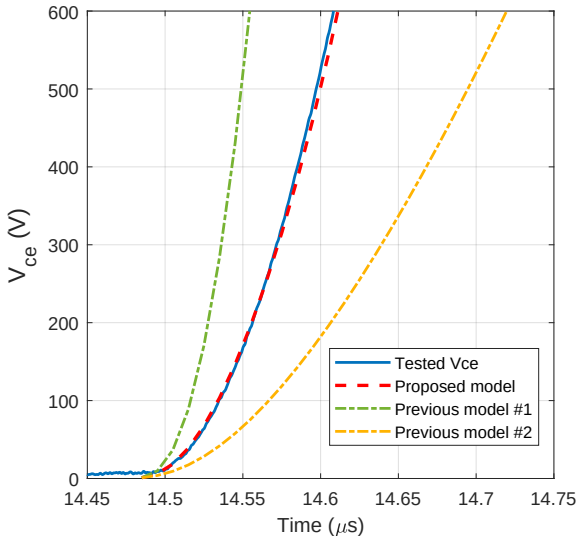


Fig. 10. Comparison between previous and proposed dV_{CE}/dt model of IKW40N120CS6 at turn-off transient with $I_L = 20A$, $R_G = 10\Omega$ and $T_J = 30°C$.

equation (40), the term $I_C/(1+b)$ reflects the MOS-side hole current reduction. As a result, the analytical derived dV_{CE}/dt agree with the experimental data when 10A, 20A and 30A of I_L are utilized.

In Figs. 8 and 9, the maximum relative error Em between the analytical derived and experimental is calculated for each test conditions. The Em is up to 10% IKW40N65ET7 and up to 9.6% for IKW40N120CS6. In this paper, it is assumed that I_c is constant and profile of excess carrier density is unchanged during the turn-off transient. These assumptions simplified the device physical and make the analytical dV_{ce}/dt modelling feasible. However, the simplifications also gives rise to the errors presented in Figs. 8 and 9.

C. Comparison of the proposed and previous dV_{CE}/dt models

In this subsection, the proposed model is compared with the model presented in [12], [13] and [10]. Fig. 10 shows the V_{CE} waveforms calculated by the proposed and previous dV_{CE}/dt models. The model given in [12], [13] is indicated as model # 1 and the model proposed in [10] is marked as model # 2.

It can be noticed that the proposed model can provide a far more accurate prediction. The dV_{CE}/dt calculated by the model # 1 is much steeper than the test results. This is mainly because the model considers the IGBT as a unipolar device and the excess carrier extraction in the N-base is neglected. As a result, the model greatly overestimates the dV_{CE}/dt. In model # 2, the PT IGBT model proposed in [18] is directly used for FS IGBT modeling. The low-level injection is thereby assumed on the FS layer, which causes the overestimation of the excess carrier in the N-base. As a result, the dV_{CE}/dt is greatly underestimated by the model # 2, as shown in Fig. 10. The lack of considering some device characteristics like the dependency of V_{ce} on MOS transconductance, the MOS-side hole current reduction and displacement currents generated by the depletion region extension also contribute to the error of model # 2.

VI. Conclusion

This paper presents an analytical model on the temperature-dependent dV_{CE}/dt at the turn-off transient of FS IGBT. During the turn-off transient, the MOS-side electron and hole current reduces. This forces the V_{CE} to rise, which generates the charge extraction current I_{ext}, collector-emitter displacement currents I_{disp} and collector-gate displacement I_{CG} to compensate the MOS-side current reduction. The I_{CG} also induced gate negative feedback action, which has a significant impact on the dV_{CE}/dt.

To provide accurate prediction on the dV_{CE}/dt, all these pivotal current components I_{ext}, I_{disp}, I_{CG} and the gate negative feedback are included. The temperature dependency of various silicon material properties and device parameters are also considered to capture the impact of the junction temperature on the dV_{CE}/dt. The good agreement of the experimental data and analytically derived results validate the accuracy of the proposed dV_{CE}/dt model for FS IGBT. The comparison between the previous and proposed dV_{CE}/dt models demonstrates that the proposed model can provide a more accurate prediction than the previous models.

The proposed model can be used for EMI modeling of FS IGBT-based power converters. With dV_{CE}/dt utilized as a junction temperature indicator, the model can also be used for junction temperature detection of the FS IGBT.

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